H-532

OPERATION AND MAINTENANCE MANUAL

FOR

SFR-59-1A UNDERFREQUENCY RELAY

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HATHAWAY INSTRUMENTS INC.

5250 EAST EVANS AVENUE DENVER, COLORADO 80222

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1. PURPOSE AND APPLICATION

The SFR-59-1A is used in load shedding applications to trip at the critical underfrequency setting.

This relay finds application where trip frequency settings must be accurately maintained within ±.02Hz and/or where very short trip delay intervals are required. Such accuracy is required to assure coordinated settings between relays of interconnected utilities. Unique inhibit features enable secure operations at very short trip delay settings. Secure operation is provided even in the presence of arcing noise, ac transfer, severe undervoltage conditions, loss of the power supply or loss of the signal input. Also, holding coils are provided to assure trip coil current until the associated circuit breaker operates.

2. OPERATING CHARACTERISTICS

The SFR-59-1A is designed to provide reliable repeatable indications of an underfrequency condition. The device has an electromechanical relay output which may be used to trip a power circuit breaker.

Because of the special inhibit circuits, the relay will not trip due to loss of signal, loss of voltage or an internal power supply failure.

Special precautions have been taken to insure that the relay will not false trip due to noise. These precautions include careful control of the internal wiring and component placement as well as a test program which ensures that every relay will pass the noise specifications.

3. SPECIFICATIONS

Underfrequency Accuracy	0.018Hz on 60Hz base.
Time Delay Accuracy	±1 cycle.
Surge Withstand Capability	The SWC test wave is an oscillatory wave, nominal frequency 1.5MHz. (1.0 to 1.5MHz range), 2.5kV (-0 +20%) crest value of the first half cycle peak, envelope decaying to 50% of the crest value of the first peak in 10 micro-seconds from the start of the wave. Source impedance of the surge generator used to produce the test wave to be 150 ohms. The test wave to be applied to a test specimen at a repetitive rate of not less than 50 tests per second for a period of at least 2.0 seconds. The test wave is applied between all inputs and the case; between each input and all other inputs. This is a differential and a common mode test. Each test is applied consecutively for two seconds. The relay must not operate at two cycles delay.
Signal Loss Test	The relay will not operate at two cycles delay when the signal is removed, regardless of the rate.
Power Loss Test	The relay will not operate at two cycles delay when the power is removed, regardless of rate.

Undervoltage Adjustment	35 to 70V rms.
Target	2A tap 2A must operate, 200ma must release. 0.2A tap 0.2A must operate, 20ma must release.
Output Contacts	Refer to the following table.

Parameter	Amperes AC or DC at 142V DC Max.	
Holding Coil Tap	.2A	2A
Carry for 1 Second	3A	30A
Carry Continuous	.4A	4A
Resistance	1.3Ω	.20Ω
Impedance at 60Hz	1.45Ω	.20Ω
Break (Controlled by Release of Holding Coil)	0.2A	2A

TABLE 1

OUTPUT CONTACT RATINGS

	Any other time-current characteristics may be found from $k=i^2t$.
Underfrequency Range	52 to 59.98Hz.
Frequency Setting Resolution	Better than .02Hz.
Time Delay Resolution	1 cycle.
Temperature	0° to 140°F.

Humidity	0 to 95%.
Isolation	Will withstand a one minute application of 1500V rms, 60Hz between any inputs, and any other input or any input and case.
Features	Output contacts are sealed in. See NOTE.
	Target indications are remembered even if power is lost.
	Flush mounting or panel mounting. Draw out case.
Outside Dimension	16-1/8 x 6-5/8 x 10-1/2 inches.
Weight	25 lbs.
Burden	Less than 2VA.
Power Requirements	125V dc, nominal (90 to 155V range).
Time Delay	Front panel setting PLUS 6 cycles: 1 cycle output relay pull-in time and 5 cycles built-in logic board delay.

NOTE: The seal in feature may be eliminated if desired by removing diode CR214 from the Input Circuit Board.

4. PERFORMANCE TESTING

The following test information applies equally to all SFR-59 models, with the exception of power supplied to the back panel, which differs from model to model. To check out an SFR-59, the test circuit of Figure 1 must be assembled. Also, a Hathaway Frequency Relay Calibrator, FRC-2A, or equivalent, is required as a programmed signal source. The FRC-2A provides an accurate low frequency output of from 40 to 160V rms at 1 ampere. The output frequencies are digitally set according to the desired period, namely Frequency 1 and Frequency 2. Frequency 2 may be programmed to occur at a delayed period of from 1 to 99 cycles. Particular performance tests are outlined in the following text with reference to the test circuit of Figure 1 and setting tables for the FCR-2A and the SFR-59.

A. TEST EQUIPMENT REQUIRED

125V dc power supply at 300ma, Dresser Barnes Model 3-500B or equivalent.
Hathaway Frequency Relay Calibrator (FRC-2A) or equivalent. Connect to pins 3 and 4, SFR-59 back panel.
0-160V Variac. Connect to pins 1 and 2, SFR-59 back panel.
Oscillator, HP 205AG or equivalent with switch. Connect to pins 3 and 4, SFR-59 back panel.
Timer
Unless otherwise stated, the switches shall be set as follows:

Frequency Setting	59.9Hz
Time Delay	2 cycles

Input signal applied to the signal inputs should be 110V rms, 60Hz.
Power supplied to the back panels should be 125V dc ±2%, 48V dc ±2%, or 115V ac ±10% depending on SFR-59 model that is being tested.

B. UNDERFREQUENCY ACCURACY

Assemble the circuit shown in Figure 1 and set the relay to the frequency shown on the accompanying table. The FRC-2A should be adjusted with Period No. 1 set to the untripped frequency as shown in the table. Period No. 2 should be set to the trip frequency. When a transfer is made between

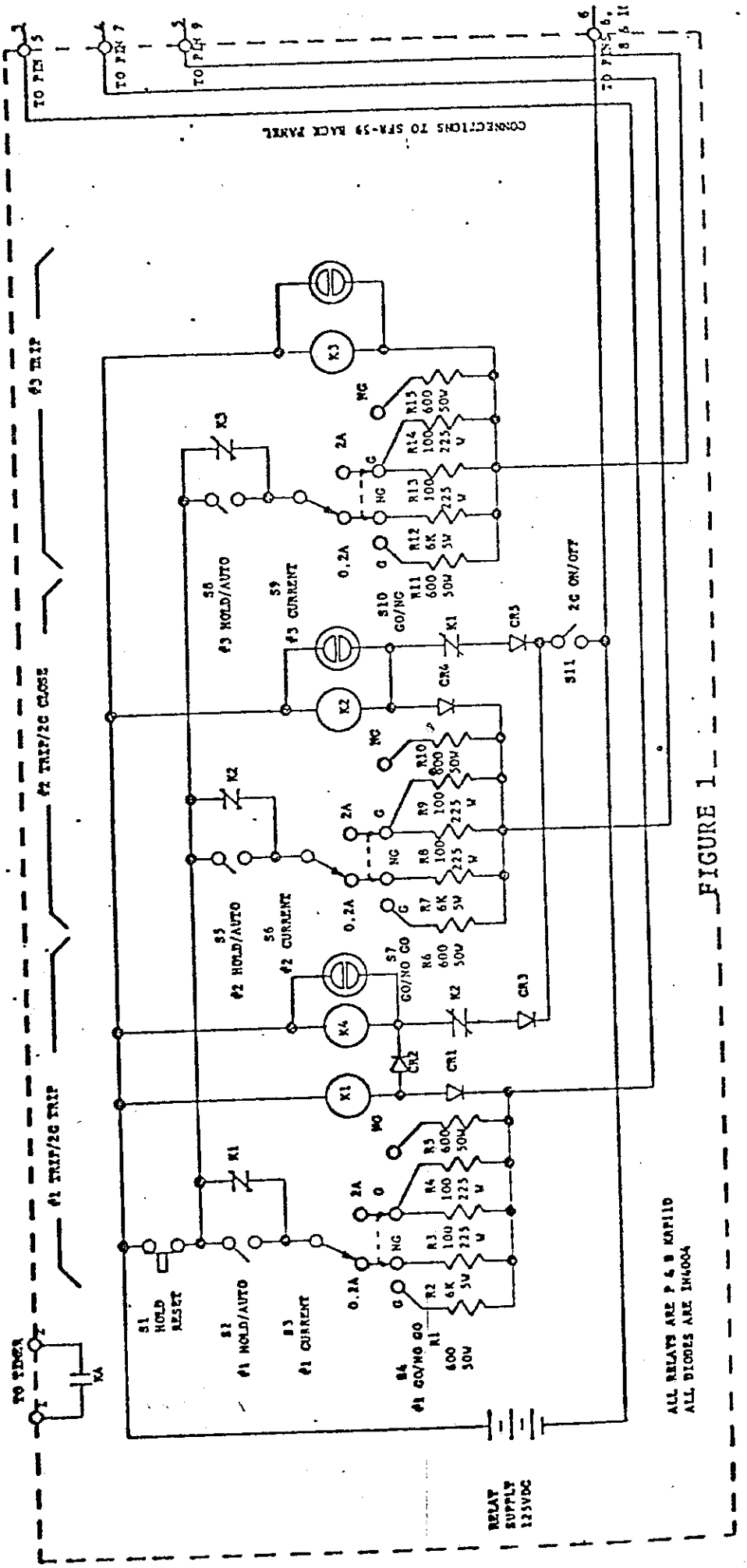


FIGURE 1 TEST CIRCUIT

Period No. 1 and Period No. 2, the SFR-59 should trip and the target light for the appropriate frequency will be energized.

C. TIME DELAY ACCURACY

Assemble the circuit shown in Figure 1. Adjust the time delay switches on the FRC-2A to the time delay shown in the left-hand side of the accompanying table and adjust the relay to the proper value. Adjust Period No. 2 to the value shown under Period No. 2 on the table. Enable Period No. 1. Press the time delay enable switch. FRC-2A should momentarily set to Period No. 2 and then transfer to Period No. 1. The SFR-59 should not trip. Adjust the time delay setting on the FRC-2A to the value shown in the right-hand column on the table. Again, press the delay enable switch. The SFR-59 should now trip. Repeat the procedure to each of the values in the table.

D. UNDERFREQUENCY OUT-OF-RANGE INHIBIT TESTS

Assemble the circuit shown in Figure 1. Close oscillator switch and turn the oscillator amplitude up until the ready light turns on. Adjust the oscillator frequency from 60Hz to 20Hz. The SFR-59 should trip and remain tripped all of the time that the oscillator frequency is below the trip point. Then, as the oscillator is adjusted from this value to 20Hz, the SFR-59 will reset as the trip frequency is approached and remain reset for all values under the trip frequency.

UNDERFREQUENCY ACCURACY

UNTRIPPED	TRIPPED	RELAY SETTING
55.92	55.88	55.9
56.02	55.98	56.0
56.12	56.98	56.1
59.02	58.98	59.00

TIME DELAY ACCURACY

TIME #1	PERIOD 1	PERIOD 2	PERIOD #1	TIME #2	RELAY SETTING
7	60.0	59.8	59.8	9	2
9	60.0	59.8	59.8	11	4
13	60.0	59.8	59.8	15	8
21	60.0	59.8	59.8	23	16
37	60.0	59.8	59.8	39	32

5. INSTALLATION

A. RECEIVING INSPECTION

The SFR-59-1A is carefully tested and inspected at the factory prior to shipment. Before unpacking, inspect the shipment container for visible damage; after unpacking, inspect the equipment for any possible damage incurred during transit. If the unit is damaged, immediately file a claim giving a full damage report to the carrier and notify the nearest Hathaway area representative.

B. MECHANICAL

The SFR-59-1A may be either panel mounted or stud mounted. The required hole patterns and cutouts are shown in drawing no. 7098100.

C. ELECTRICAL

After the relay is mounted, refer to the Wiring Diagram, 7253401, for wiring connections.

6. OPERATING INSTRUCTIONS

Refer to Figure 2 for the location of the controls.

A. FREQUENCY SETTING

CAUTION

DO NOT CHANGE FREQUENCY OR TIME DELAY SETTING WHILE THE RELAY IS IN THE OUTER CASE.

To set the trip frequencies, locate the appropriate switches on the SFR-59-1A. Then, refer to Table 2 and locate the code for the particular frequency to be used. Start with the top switch, set it to either 1 or 0 as determined by the left digit in the table. Continue to set the switches by moving down the panel and across the table.

A 1 or 0 is set by removing the screw and inserting in the appropriate location.

Table 2, Underfrequency Versus Binary Code Settings, is obtained from:

$$F_S = \frac{1}{5FX10^{-6}} - 3072$$

where: F_S is the frequency setting and F is frequency in cycles per second.

The frequency setting, F_S, is then converted to a binary code. Although Table 2 lists frequency settings for every tenth cycle, the frequency can be set to a resolution of 0.02Hz.

B. TIME DELAY SETTING

CAUTION

DO NOT CHANGE FREQUENCY OR TIME DELAY SETTING WHILE THE RELAY IS IN THE OUTER CASE.

The time delay is set in a manner similar to the frequency with a binary code. The numbers are found on the right of the delay screw adjustments. To adjust the delay, set the screws to the "0" or "1" position that corresponds to the binary cycle delay. Then, the cycles of delay will be the sum of the binary digits. Add all of the numbers to obtain the total time delay.

As an example, suppose the desired delay is 15 cycles. The bottom switch would be set to 1, the second and third switch would be 0, the fourth switch would be a 1 and the rest would be 0, thus:

15 cy = 8 cy + 1 cy + fixed 6 cy

C. UNDERVOLTAGE ADJUSTMENT

The undervoltage threshold may be adjusted using the potentiometer on the far right. The level is decreased by turning in a clockwise direction.

D. CURRENT TAP SETTING

To set the current sense tap to the 0.2A setting, place the programming wire in the screw terminal located in the lower right-hand part of the current sense relay. When a 2A setting is desired, put the wire in the lower middle screw terminal.

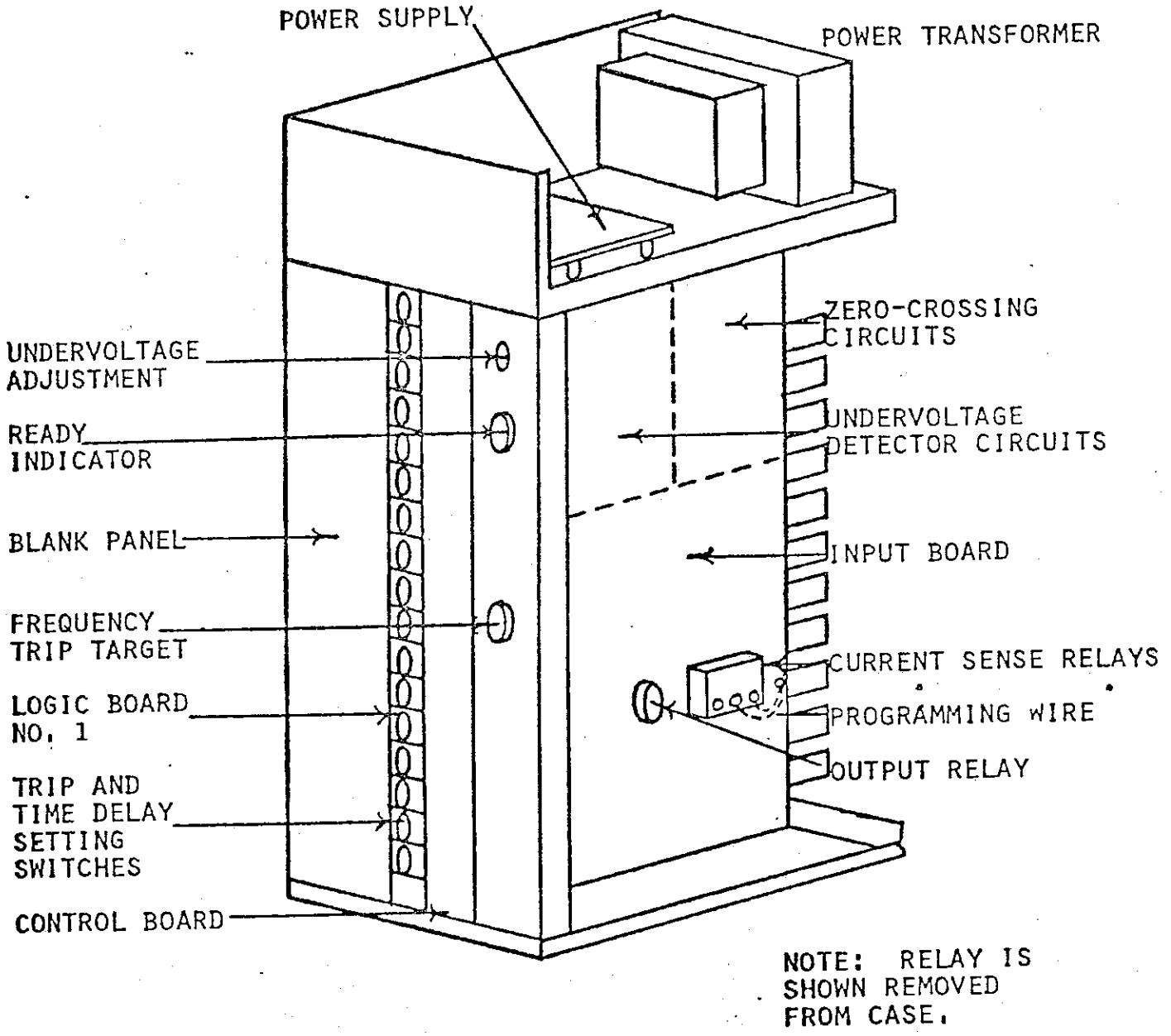


FIGURE 2

SFR-59-1A UNDERFREQUENCY RELAY

TABLE 2

UNDERFREQUENCY

VERSUS

BINARY CODE SETTINGS

FREQUENCY		CODE									
52.	19.231	1	1	0	0	0	0	0	1	1	0
52.1	19.194	1	0	1	1	1	1	1	1	1	1
52.2	19.157	1	0	1	1	1	1	0	1	1	1
52.3	19.120	1	0	1	1	1	1	0	0	0	0
52.4	19.084	1	0	1	1	1	0	1	0	0	1
52.5	19.048	1	0	1	1	1	0	0	0	0	1
52.6	19.011	1	0	1	1	0	1	1	0	1	0
52.7	18.975	1	0	1	1	0	1	0	0	1	1
52.8	18.939	1	0	1	1	0	0	1	0	1	1
52.9	18.904	1	0	1	1	0	0	0	1	0	1
53.	18.868	1	0	1	0	1	1	1	1	0	1
53.1	18.832	1	0	1	0	1	1	0	1	1	0
53.2	18.797	1	0	1	0	1	0	1	1	1	1
53.3	18.762	1	0	1	0	1	0	1	0	0	0
53.4	18.727	1	0	1	0	1	0	0	0	0	1
53.5	18.692	1	0	1	0	0	1	1	0	1	0
53.6	18.657	1	0	1	0	0	1	0	0	1	1
53.7	18.622	1	0	1	0	0	0	1	1	0	0
53.8	18.587	1	0	1	0	0	0	0	1	0	1
53.9	18.553	1	0	0	1	1	1	1	1	1	1

54.	18.519	1	0	0	1	1	1	0	1	1	1
54.1	18.484	1	0	0	1	1	1	0	0	0	1
54.2	18.450	1	0	0	1	1	0	1	0	1	0
54.3	18.416	1	0	0	1	1	0	0	0	1	1
54.4	18.382	1	0	0	1	0	1	1	1	0	0
54.5	18.349	1	0	0	1	0	1	0	1	0	1
54.6	18.315	1	0	0	1	0	0	1	1	1	1
54.7	18.281	1	0	0	1	0	0	1	0	0	0
54.8	18.248	1	0	0	1	0	0	0	0	0	1
54.9	18.215	1	0	0	0	1	1	1	0	1	1
55.	18.182	1	0	0	0	1	1	0	1	0	0
55.1	18.149	1	0	0	0	1	0	1	1	0	1
55.2	18.116	1	0	0	0	1	0	0	1	1	1
55.3	18.083	1	0	0	0	1	0	0	0	0	1
55.4	18.051	1	0	0	0	0	1	1	0	1	0
55.5	18.018	1	0	0	0	0	1	0	0	1	1
55.6	17.986	1	0	0	0	0	0	1	1	0	1
55.7	17.953	1	0	0	0	0	0	0	1	1	1
55.8	17.921	1	0	0	0	0	0	0	0	0	0
55.9	17.889	0	1	1	1	1	1	1	0	0	1
56.	17.857	0	1	1	1	1	1	0	0	1	1
56.1	17.825	0	1	1	1	1	0	1	1	0	1
56.2	17.794	0	1	1	1	1	0	0	1	1	1
56.3	17.762	0	1	1	1	1	0	0	0	0	0

56.4	17.731	0	1	1	1	0	1	1	0	1	0
56.5	17.699	0	1	1	1	0	1	0	0	1	1
56.6	17.668	0	1	1	1	0	0	1	1	0	1
56.7	17.637	0	1	1	1	0	0	0	1	1	1
56.8	17.606	0	1	1	1	0	0	0	0	0	1
56.9	17.575	0	1	1	0	1	1	1	0	1	1
57.	17.544	0	1	1	0	1	1	0	1	0	1
57.1	17.513	0	1	1	0	1	0	1	1	1	1
57.2	17.483	0	1	1	0	1	0	1	0	0	1
57.3	17.452	0	1	1	0	1	0	0	0	1	0
57.4	17.422	0	1	1	0	0	1	1	1	0	0
57.5	17.391	0	1	1	0	0	1	0	1	1	0
57.6	17.361	0	1	1	0	0	1	0	0	0	0
57.7	17.331	0	1	1	0	0	0	1	0	1	0
57.8	17.301	0	1	1	0	0	0	0	1	0	0
57.9	17.271	0	1	0	1	1	1	1	1	1	0
58.	17.241	0	1	0	1	1	1	1	0	0	0
58.1	17.212	0	1	0	1	1	1	0	0	1	0
58.2	17.182	0	1	0	1	1	0	1	1	0	0
58.3	17.153	0	1	0	1	1	0	0	1	1	1
58.4	17.123	0	1	0	1	1	0	0	0	0	1
58.5	17.094	0	1	0	1	0	1	1	0	1	1
58.6	17.065	0	1	0	1	0	1	0	1	0	1
58.7	17.036	0	1	0	1	0	0	1	1	1	1

58.8	17.007	0	1	0	1	0	0	1	0	0	1
58.9	16.978	0	1	0	1	0	0	0	0	1	1
59.	16.949	0	1	0	0	1	1	1	1	0	1
59.1	16.920	0	1	0	0	1	1	1	0	0	0
59.2	16.892	0	1	0	0	1	1	0	0	1	0
59.3	16.863	0	1	0	0	1	0	1	1	0	1
59.4	16.835	0	1	0	0	1	0	0	1	1	1
59.5	16.807	0	1	0	0	1	0	0	0	0	1
59.6	16.779	0	1	0	0	0	1	1	0	1	1
59.7	16.750	0	1	0	0	0	1	0	1	1	0
59.8	16.722	0	1	0	0	0	1	0	0	0	0
59.9	16.694	0	1	0	0	0	0	1	0	1	1

7. CALIBRATION AND ADJUSTMENT

Due to the construction of the SFR-59-1A, no calibration is necessary after the initial adjustment of the relay. However, a periodic 6 month check is desirable to determine if the relay is still operating properly. To perform this test, refer to the section on Performance testing. No adjustments are required on the SFR-59-1A other than the front panel adjustments as listed in the operating instructions. These consist of the undervoltage adjustment, the frequency adjustments and the time delay settings.

8. MAINTENANCE

Due to the construction of the SFR-59-1A, very little maintenance should be required. However, a periodic 6 month check for proper operation of the relay is recommended. This check should be performed as listed in the Calibration and Adjustment section of this manual. At the time of this check, it would be desirable to inspect the contacts of the output relay for degradation and to clean the contacts if necessary. Should trouble be encountered in the routine test, refer to the section on Trouble Isolation.

9. PRINCIPLES OF OPERATION

A. BASIC RELAY

The signal is first applied to the SFR-59-1A through pins 3 and 4 of the input board. The signal is then routed to an undervoltage detector which is shown on the detailed schematic. The function of this device is to disarm the relay whenever the signal voltage is below a sufficient amount to enable the relay to operate properly. The signal is also applied to a zero crossing detector which is shown on the detailed schematic. The purpose of the zero crossing detector is to provide an output pulse on every positive going zero crossing of the input signal. These positive pulses are applied to the logic boards as a reset signal. It is applied through the reset generator which conditions the pulse to a form that is acceptable to the logic.

A 200kHz clock is located on the control board. Also, the clock signal is applied to the logic board. The clock pulses are then counted in a base counter and then the count in the base counter is compared in the gating to a preset count which is set in the switches located on the front of the logic boards. When the count in the counter exceeds the preset amount set in the switches, an output pulse is supplied at the output of the gating. Thus, if the reset signal is applied to the base counter before the counter counts to the preset amount, the input frequency must be higher than the preset frequency. An underfrequency pulse will not occur at the end of the gating. However, if the counter is allowed to count to the comparision point before the reset occurs, the underfrequency pulse will be generated at the output of the gating once a cycle. This pulse is then applied to the time delay counter which acts in a manner similar to the base counter to count the number of underfrequency cycles. Switches are coded to preset the desired number of underfrequency cycles that are necessary to cause the relay to trip. When coincidence occurs between the time delay counter and the preset time delay switches, an output pulse is generated at the output of the time delay gating which then sets the output flip-flop and causes the trip control relay to be energized. When the underfrequency condition disappears, a reset counter is used to reset the output flip-flop and de-energize the trip control relay.

When the trip control relay is energized, a ground is applied through pin 2, through the contacts to pin 1 of the logic board and to pin 23 on the input board. This ground is used to energize the trip output relay K203. However,

if the input signal is lower than the necessary amount to cause the relay to operate properly, the undervoltage contacts located on the input board will not be closed and a ground will not be applied at pin 2 of the logic board number 1. Thus, the output trip relay cannot trip.

When the output relay, K203, is energized, contacts located near pins 5 and 6 are closed. When these output contacts close, current then flows from the external circuitry through input board pin 5, through the K203 contacts, through the current sense trip relay, K202, and out to pin 6 of the input board. When the current exceeds either 0.2 amps or 2 amps, as programmed by the current sense strap, the contact will close on the current sense relay, K202. This contact will then seal in the trip output relay, K203, through diode CR214. At the same time it will cause the underfrequency target memory relay, K204, to be latched. This relay is a magnetic latching relay which will remember its latch condition until the reset switch, S501, is pressed. When this happens, the current will flow through CR217 into the delatch coil of relay K204. When K204 closes, power will be applied to lamp DS201.

Power is applied to the SFR-59-1A through the power supply and is regulated through Q501, resistors R502, R501 and R504. Each of the logic and control boards has an individual regulator to further regulate the voltage.

B. DETAILED SCHEMATIC

1. Zero Crossing Detector

The function of the zero crossing detector is to compare the input signal to zero and when the input signal exceeds zero by a small amount, an output is produced. This circuit operates in the following manner: The input signal is applied through pins 3 and 4, through resistors R204 and R205 to the signal clipping diodes CR204 and CR203. Then, the signal is applied to the zero crossing detector which consists of transistors Q201 and Q204. The output is supplied through transistors Q202 and Q203, which function as an amplifier for transformer T202. The output of transformer T202 is then applied through pins 14 and 15 on the input board to the control board through pins 2 and 3.

2. Reset Generator

The reset generator is located on the control board and has the functions of limiting and shaping the signal to a constant width and amplitude for use as a pulse to reset the base counter. The input signal from the zero crossing detector is first clipped, using diodes CR101 and CR102, to a value which is safe for use with the integrated circuits. Next, the signal is passed through a single shot which consists of IC101; where the signal is formed into a constant-pulse-width and constant-amplitude reset signal. This signal, known as the base counter reset is then applied to the logic cards through control board, pin 5.

3. Clock

The clock oscillator is a 200kHz oscillator which provides the basic timing for the logic boards. It is located on the control board and consists of transistors Q101 and Q102 and crystal Y101. Q103 and its associated circuitry functions as an output amplifier for the oscillator. The signal is passed through IC101 and IC102 to pin 6 of the control board, where it is transmitted to the logic board.

4. Undervoltage Detector

The function of the undervoltage detector is to prevent the SFR-59-1A from tripping in the presence of undervoltage. The input signal is applied to the undervoltage detector from transformer T201. The signal is then rectified by rectifier CR205 and attenuated by the voltage divider consisting of R212, R213 and R214. CR206 clips any unusual voltage surges. The signal then is applied to Q206 which is an emitter follower. The rectified signal is then filtered by R216 and C204 and it is applied through another amplifier, Q207, to a Schmidt trigger consisting of Q208 and Q209. When the input signal is of a sufficient magnitude to switch the Schmidt trigger, the voltage between R218 and Q208 will switch from 12V to approximately 6V. This will turn on transistor Q210 which is a driver amplifier for the undervoltage relay, K201. If transistors Q211 and Q212 are saturated to ground, then the undervoltage relay, K201, will be energized. In order to saturate transistors Q211 and Q212 to ground, the power voltage must be above 11V. If this

is the case, current is passed through R225 to a capacitor C205. When the capacitor C205 charges to approximately 1V, the transistors Q211 and Q212 will be energized. The charging time constant is approximately 200 to 500 milliseconds. If the power supply level should drop below 10V, the voltage change will discharge the capacitor C205 through the diode CR207. This will discharge capacitor C205 within 1 millisecond. Thus, when the relay is initially turned on, approximately 200 milliseconds is required before the SFR-59-1A is on. This time delay enables the logic to be in its correct operating condition. However, if the relay is turned off, it will discharge within 1 millisecond and disarm the relay.

If the input signal drops below the required level as determined by the undervoltage adjustment, potentiometer R213, the capacitor C205 will also be discharged. This is accomplished by the Schmidt trigger, when it recognizes an undervoltage condition through R231 to transistor Q213, which causes it to saturate to the +12V buss. This causes current to flow down through R232 into transistor Q216 which discharges the time relay capacitor C205. The ready lamp, DS204, is energized whenever the undervoltage relay is in a proper condition to cause the relay to trip. Also, the undervoltage relay contacts are routed through input board pin 20 to the logic board where it is connected in series with the output relay, thus, preventing tripping in the event of undervoltage or low power supply conditions.

C. BASIC LOGIC OPERATION

Having followed the generation of the clock signal and of the base counter reset signal, one may now understand the basic operation of the underfrequency relay.

Referring to the schematic, 7265401, one finds the base counter, which is the main frequency sensing circuitry in the relay. The clock input is applied through logic board pin C_L to IC15 where it is amplified and applied to the first flip-flop of the base counter IC1. IC1 through IC6 forms a simple binary counter which counts the number of clock pulses between the base counter reset pulses. The base counter reset pulses are then applied through the logic board pin BCR to IC12 which inverts the signal and amplifies it. The base counter reset is then used to reset the base

counter to zero. Thus, just before being reset, the count in the base counter is an indication of the frequency of the input signal. The count in the counter is then applied to comparison gates IC13 and IC16. From these two integrated circuits, the signal is applied to two gates located in IC11 and finally to IC16 for the final comparison. The function of these comparison gates is to compare the count in the counter with a preset code in switches S1 through S10. In the event that a comparison is generated, the input frequency in the switches S1 through S10. Thus, the pulse that would occur at gate IC1, pin 8, in an indication of an underfrequency condition for one cycle. This signal is then applied through the underfrequency programming jumpers to IC15 and from there to a time delay counter consisting of IC7 through IC9. The time delay counter then counts the number of underfrequency cycles and a comparison is made between the count in the counters and the time delay setting in switches S11 through S16. The comparison is made in the integrated circuit IC14. The output of IC14, pin 8, is a pulse whenever an underfrequency condition has persisted longer than the preset time delay. This output pulse then sets the underfrequency flip-flop, IC11, to a state which will cause the relay driver, Q1, to energize the output relay, K1. This relay is then used to trip the SFR-59-1A.

A reset counter consisting of IC10 is provided to reset the time delay counter when the underfrequency condition returns to normal. The reset counter counts the number of base counter reset pulses which are applied to the logic of the input card. However, if an underfrequency condition exists, a pulse will occur once a cycle out of the mode programming jumper and reset the reset counter. Thus, the reset counter will oscillate between a count of zero and a count of one all of the time an underfrequency condition persists. When the underfrequency condition clears, there will no longer be underfrequency pulses occurring at the reset input of the reset counter and this counter will then be allowed to count to its maximum of three counts. When this maximum is reached, IC12 will sense the full state of the counter and will reset the time delay counter. It will also reset the underfrequency flip-flop and allow K1 to become de-energized.

D. OUTPUT CIRCUITS

The final output circuits for the SFR-59-1A are located on the right side of schematic 7265401. Considering output circuit No. 1, located near the top of the page, pins 5 and 6 are the output contacts. Relay K1 is energized by the trip

condition, closing the output contacts and causing current to flow from pin 5 through the output contacts to the current sensing rleay and out pin 6. When the output current exceeds either 0.2 amps or 2 amps, depending on the output current sense programming, the contacts of the output current sense relay will be energized. This will provide a ground to the cathode of diode CR214 which will seal in the output relay. At the same time, memory relay K204 will be energized. This is a magnetic latching relay which will remember its last condition until the reset switch, S501, is pressed. When the memory relay, K204, is latched, a contact on this relay will close and apply a ground to the target number 1 light, DS201, to turn on the light which indicates the target condition. The light will then remain lit until reset by the switch, S501.

E. DC SUPPLY

There are two main sources of power for the SFR-59-1A shown on schematic 7265401. One of these used in the case of a dc model is an inverter. The other power source is an ac supply. Considering the dc supply first, the input power is supplied to pins 1 and 2 through a filter consisting of L501 and L502 and capacitors C502 and C503. Clipping diodes are provided to clip off any transients which may be on the battery line. Also, diode CR302 is used in the event that the relay should be connected in the reverse direction. The +125V dc is then applied through dropping resistor R505 to zener diode CR314 which acts as a voltage source for a multivibrator used to drive the inverter transistors. The multivibrator consists of Q306 and Q305 and the associated circuitry necessary to make a free-running multivibrator. As soon as the dc signal is applied to the relay, the multivibrator begins to oscillate and switches the dc signal through switching transistors Q301 and Q303. Thus, the input voltage is switched into a square wave of approximately a 100 cycle oscillation. The oscillating voltage is then applied to two main power supplies. Pins 14 and 15 are connected to an isolated supply consisting of rectifier CR201, filter capacitors C206 and C201 and filter resistor R201. The zener diode, CR202, is used to clip any unusual transients which may be passed through the filter. C208 and C207, along with R202 and R203, provide for a balanced supply consisting of a plus and minus voltage with a common point between the two resistors. This voltage is used to power the zero crossing detector. The square wave is also applied through pins 7, 9 and 11 to rectifier diodes CR311 and CR213. Filter capacitors, C307 and C309, are used to

smooth the rectified square wave and regulator transistor Q201 provides a constant 12V dc to supply the rest of the circuitry even though the input voltage may vary. This 12V dc is fed directly to the input board for use in energizing the trip relays. Also, the logic boards and the control board are supplied with power through resistors R501, R502, R503 and R504 to individual regulators located on each of these boards. Considering a typical regulator located on logic board number 1, the power is dropped by the 200 milliamp drain of the logic card to approximately 8V at the input pin of the logic board number 1, pin 1. Zener diode CR2 and regulator transistor Q2, then provide a constant 5V to power the logic on logic board number 1.

F. AC SUPPLY

The entire power supply system, consisting of the individual regulators and the main regulator Q501, is identical in the ac supply to the analogous components in the dc supply. The power is again applied through pins 1 and 2 and filters L501 and L502 and capacitors C503 and C502 to the transformer T501. The circuitry following the transformer is basically a tap changer which automatically adjusts itself to the input signal. This provides a roughly filtered signal across capacitor C402. Transistor Q501 is used to regulate this slightly varying voltage to a constant 12V dc as was done in the case of the dc supply. Transistor Q404, resistor R417 and diode CR401 are identical to the corresponding transistor Q307, resistor R315 and diode CR313 in the dc supply. The ac voltage on pins 8 and 10 is applied through rectifiers CR416 and CR417 which functions as a full wave rectifier to capacitor C401. Thus, a dc voltage is provided which is proportional to the rms value of the ac input. Transistors Q401, Q402 and Q403 function as switching transistors to turn the various SCR's on as the input voltage increases.

Initially, a low turns ratio is required. SCR401 and SCR406 will be energized as the signal is increased above 40V. The switching is accomplished in the following manner: A constant voltage is applied to the cathode of CR420 which acts as a reference voltage. As the power supply voltage increases across each of the voltage divider resistors consisting of R401, R402, R404, R405, R407 and R408, a point will eventually be reached across R407 and R408 where Q403 will be saturated. This will cause current to flow through diodes CR402 and CR414 which will back-bias SCR401 and SCR406, thus turning them off.

The next diodes in the chain, SCR402 and SCR405, will now be energized every cycle. As the voltage continues to increase, a level will be reached where R404 and R405 cause transistor Q402 to become saturated, which turns diodes CR405 and CR412. As the voltage continues to rise, a similar process causes Q401 to turn off SCR403 and SCR404. Thus, at the highest voltages, only the rectifing diodes CR408 and CR409 are being used to supply power to filter capacitor C402. It should be noted that only the SCR connected to the highest tap ratio in the chain which is not being turned off by an appropriate transistor is actually allowed to conduct. As an example, consider SCR401 and SCR402. If SCR401 was energized as the sine wave approached its crest (as soon as SCR401 fired) SCR401 would back-bias SCR402. However, if SCR401 was never allowed to energize, because it was turned off by its diode SCR402, then SCR402 could conduct and it would back-bias SCR403.

10. TROUBLE ISOLATION

To locate any defective section of the SFR-59-1A, refer to the schematic 7265401. Using the wave forms and voltages shown at each of the pin numbers, selectively test each pin until a wave form or voltage is discovered which does not agree with the schematic. This procedure should enable the technician to discover the faulty section of the relay.

A. CLOCK

If the clock oscillator is not oscillating, as determined by locating the appropriate wave form on pin 6 of the control board, then check pin 1 on IC102. The wave form at this point should be very similar to the output. Proceed toward Q101 and test for the appropriate wave form. If the oscillation is not present at the emitter of Q101, test the transistor Q101 with an ohmmeter. If the transistor tests correctly, check for the proper voltage on the collector of Q101. If these conditions are present, the crystal Y101 must be defective.

B. ZERO CROSSING DETECTOR

To locate a problem in the zero crossing detector, first connect an oscilloscope across CR204 and CR203. A half-volt square wave should appear at this point. Next, test the output, pins 3 and 4, of T202. This should be approximately a 20V pulse as shown in the wave form for pins 14 and 15. If this wave form is not present, one of the transistors Q201, Q202, Q203, Q204 or Q205 must be defective. Respectively, test the emitter of Q205 and the junction of R211 and R209 for the +12V and -12V. The tests should be made with respect to the junction of R202 and R203. In these tests, the ready light should be operating properly. If the ready light is not on, Q213 will be applying a short circuit from pins 3 and 4 of T202. Therefore, no output will be obtained.

C. RESET GENERATOR

To test the operation of the reset generator, the proper input should appear at pins 2 and 3. If this is not the case, the problem is in the input board. If the output of pin 5 on the control board is not correct, check to see that the input pulse is clipped between 5V and 0V at the input of IC101, pin 5. If this wave form is not present, diodes CR101 and CR102 are probably defective. If the wave form is present, IC101 is probably defective.

D. UNDERVOLTAGE DETECTOR

To locate problems in the undervoltage detector, first test the input to the base of Q206. If the wave form is not as shown, check the voltage levels on the Schmidt trigger consisting of Q208 and Q209. These voltages are shown for an input voltage of the proper level to turn the light on. If the input voltage is above 6V at the base of Q207, the Schmidt trigger should be in its turned-on condition, and the voltages should be as shown surrounding Q208 and Q209. If the Schmidt trigger is not defective, check the collector of Q210 for the proper voltage. If the proper voltage is found, check the collector of Q211. At this point, the collector should be saturated to ground. If this is not the case, measure the voltage across CR208 which should be 10V. If this is not the case, measure the voltages at Q215, Q216 and Q212. This should enable the defective component to be found. If the voltage at the collector of Q211 is correct, K201 is defective.

E. LOGIC TESTS

Each flip-flop, pins 5 and 9, should produce a square wave of progressively lower frequency. That is, the output of IC1, pin 5, will be half the clock frequency. The output of IC6, pin 9, is tested. However, the outputs of the last flip-flops will not necessarily be symmetrical. The output of these flip-flops can be most conveniently found on the front panel switches. Once all the flip-flops have been determined to be operating correctly, code the input frequency to a trip frequency. Pulses should then appear on the output of IC16, pin 6 and on pins 3 and 6 of IC11. If this is the case, pulses should appear on IC16, pin 8, and they should disappear whenever the input frequency is greater than the trip frequency. If the pulses appear, the relay is operating properly on underfrequency. These pulses should then be applied to the input of the time delay counter, IC7, pin 3. If this is the case, proceed to check the time delay counter in a manner similar to the base counter. Also, check IC14 to see that pulses appear when the frequency is underfrequency. If they do, the trouble with the relay is probably in the underfrequency flip-flop or the output driver. If they do not, the reset counter must be tested.

To test the reset counter for proper operation, code the frequency to a non-trip frequency and check to see that the base counter reset pulses appear on pin 3 of IC10. Also, no pulses should appear on pins 1 and 3 of IC10. The counter

should continue to count in a manner similar to the base counter. For every fourth base counter pulse in, an output pulse should be obtained on pin 8 of IC12 and should be applied to the inputs of each of the flip-flops of the time delay counter. When the input frequency is below the trip frequency, pulses should appear on pins 1 and 13 of IC10 and no output should appear on pin 8 of IC12. If this happens, the reset counter is operating properly.

If the relay fails to pass the underfrequency inhibit test, check the output of IC17. A logic level should appear at the output of IC17, pin 8, for a period of time between approximately 25 milliseconds and the next base counter reset. When this occurs, the output of IC18, pin 9, should go low for this period of time. Also, at IC15, pin 3, the clock pulses should disappear during this period of time. If this is not the case, then either IC17, IC18 or IC15 is defective.

F. OUTPUT CIRCUIT

To determine if the various output and memory relays are operating properly, measure the appropriate wave form and refer to the Principles of Operation for the various sequences. This should locate the defective relay.

G. DC SUPPLY

To check the dc power supply, first determine if the inverter is running as shown by the wave form pin 1 of T501. If the inverter is not running, measure the various voltages as shown on the schematic which should enable the defective component to be located. If the inverter is oscillating, check the wave forms between pins 14 and 15 for power value. If these prove to be correct, check the voltage across R202 and R203. This should locate the defective components in the isolated supply. If the +12 or +5V supplies in the unit are defective, measure the wave form on CR312 and C309. If these wave forms are correct, continue to measure the various wave forms or the various voltages at the emitter of Q501 and to each of the inputs of the logic boards, pin 1. If these voltages all prove to be correct, measure the 5V supply on each of the logic boards and the control board.

H. AC SUPPLY

To determine if the ac power supply is operating properly, first apply 115V ac and measure the output of Q501 on the

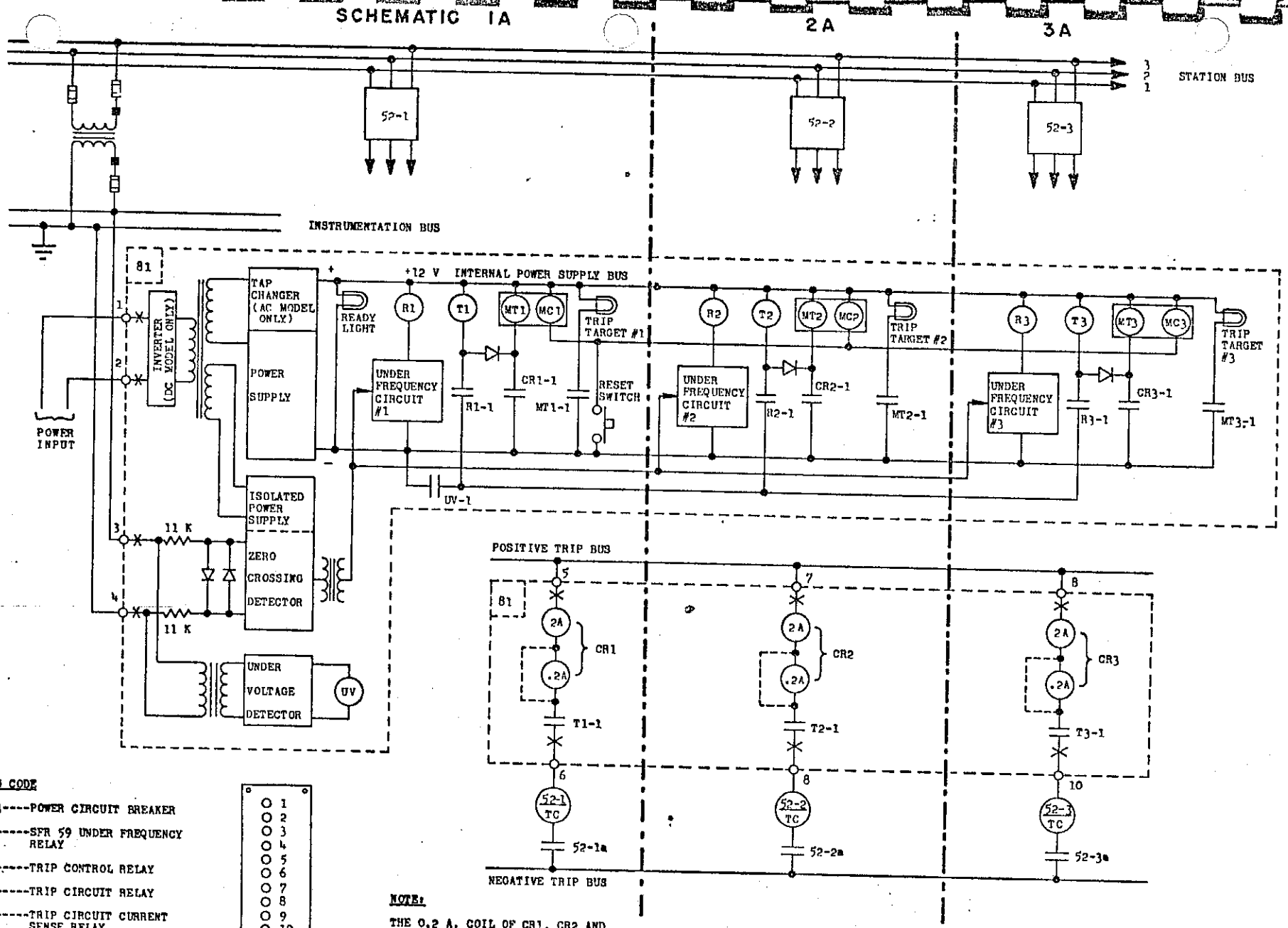
emitter. If this value is 12V, then proceed to determine the trouble as listed under the dc supply trouble shooting procedure for the input to the various logic and control boards. If these values are correct, apply an input voltage of zero and slowly increase to 140V. The value of the voltage across capacitor C402 should change values as shown in the Tap Value Table, Table 3. If one of the tap changes does not occur, the trouble should be in the circuitry associated with the switching transistor listed in the table. Knowing the voltage at which the tap change failed and measuring the appropriate wave forms and voltages as shown on the schematic should enable the defective component to be located.

TAP	INPUT VOLTAGE
1st	75
2nd	100
3rd	115

TABLE 3

TAP VALUES

SCHEMATIC 1A



DEVICE NUMBERING CODE

52-1, 52-2, 52-3----POWER CIRCUIT BREAKER

81----------SFR 59 UNDER FREQUENCY RELAY

R1, R2, R3----------TRIP CONTROL RELAY

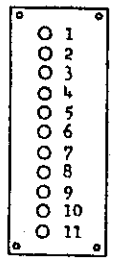
T1, T2, T3----------TRIP CIRCUIT RELAY

CR1, CR2, CR3-------TRIP CIRCUIT CURRENT SENSE RELAY

MT1, MT2, MT3-------TARGET TRIP COIL

MC1, MC2, MC3-------TARGET RESET COIL

UV----------UNDER VOLTAGE INHIBIT RELAY



TERMINAL LOCATION (REAR VIEW)

NOTE:

THE 0.2 A. COIL OF CR1, CR2 AND CR3 IS INTERNALLY SHORTED FOR 2 A. OPERATION.

MT1, MT2 AND MT3 ARE MAGNETICALLY HELD IN A POSITION AS DETERMINED BY THE LAST TARGET COIL THAT WAS ENERGIZED.

LTR	ECO NO	DESCRIPTION	DATE	APPROVED
A	22106	ENG RELEASE	10-27-70	

CONT:
DR BY: TJD
CHK
APPD:
NEXT ASSY
USED ON
SCHEMATIC

HATHAWAY INSTRUMENTS, INC.
DENVER COLORADO 80222

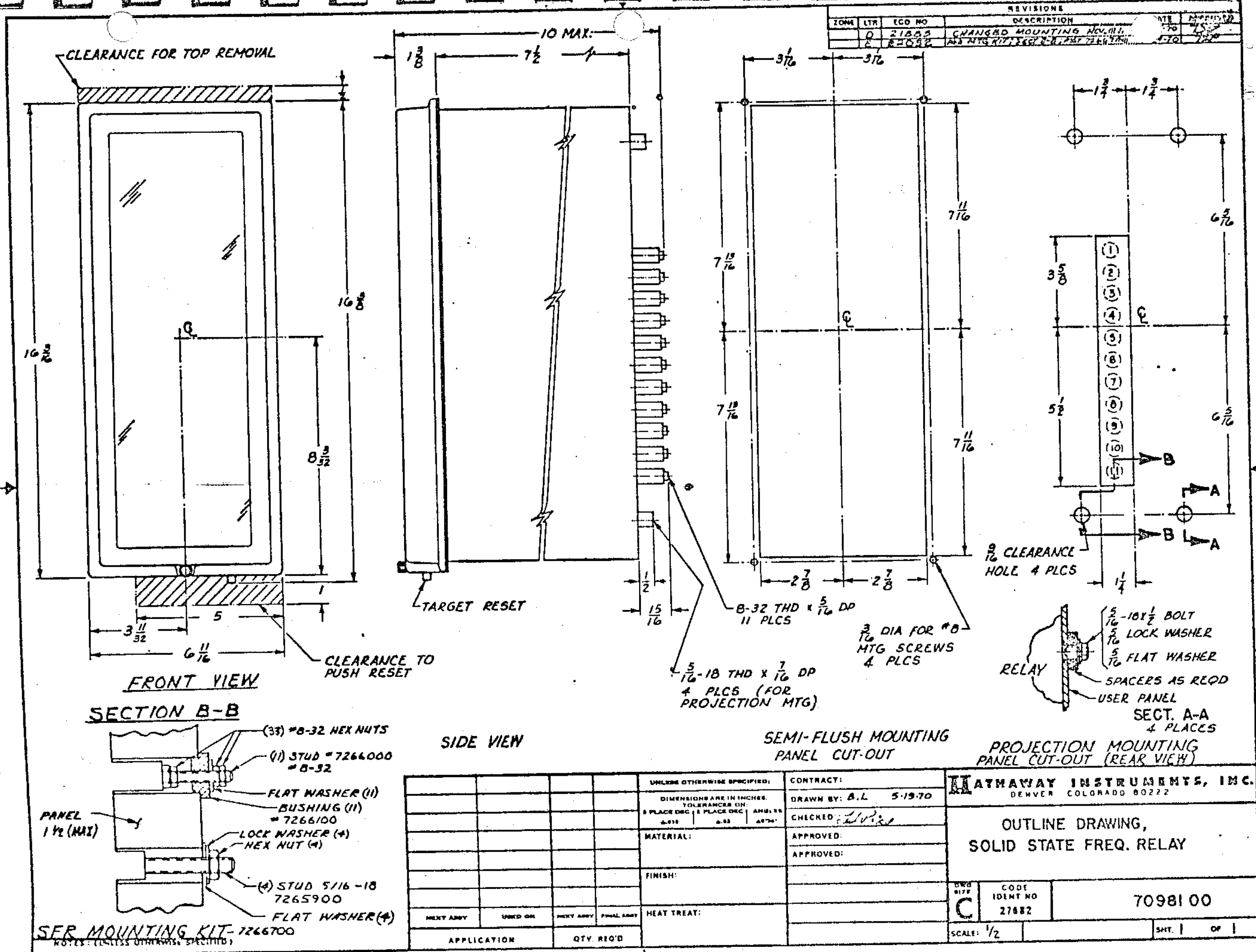
INTERNAL/EXTERNAL WIRING
SFR FREQUENCY RELAY

CODE IDENT NO 27652

7253401

SCALE

SHT OF


REVISIONS
ZONE LTR ECO NO DESCRIPTION DATE APPROVED
D 21885 CHANGED MOUNTING HOLES
E ADD MTG KIT; SECT B-B
CLEARANCE FOR TOP REMOVAL
16 5/16
16 3/8
8 3/32
1
5
3 11/32
6 11/16
CLEARANCE TO PUSH RESET
FRONT VIEW
10 MAX.
1 3/8
7 1/2
TARGET RESET
1/2
15/16
8-32 THD x 5/16 DP 11 PLCS
5/16-18 THD x 7/16 DP 4 PLCS (FOR PROJECTION MTG)
SIDE VIEW
3 1/16
3 1/16
7 11/16
7 11/16
7 13/16
7 13/16
2 7/8
2 7/8
3/16 DIA FOR #8 MTG SCREWS 4 PLCS
SEMI-FLUSH MOUNTING
PANEL CUT-OUT
1 3/4
1 3/4
6 5/16
6 5/16
3 5/8
5 1/2
1 1/4
9/16 CLEARANCE HOLE 4 PLCS
5/16-18 x 1/2 BOLT
5/16 LOCK WASHER
5/16 FLAT WASHER
SPACERS AS REQD
USER PANEL
RELAY
SECT. A-A
4 PLACES
PROJECTION MOUNTING
PANEL CUT-OUT (REAR VIEW)
SECTION B-B
(33) #8-32 HEX NUTS
(11) STUD #7266000 #8-32
FLAT WASHER (11)
BUSHING (11) #7266100
LOCK WASHER (4)
HEX NUT (4)
(4) STUD 5/16-18 7265900
FLAT WASHER (4)
PANEL 1 1/2 (MAX)
SFR MOUNTING KIT-7266700
NOTES: (UNLESS OTHERWISE SPECIFIED)
NEXT ASSY
USED ON
NEXT ASSY
FINAL ASSY
APPLICATION
QTY. REQ'D
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
TOLERANCES ON:
MATERIAL:
FINISH:
HEAT TREAT:
CONTRACT:
DRAWN BY: B.L 5-19-70
CHECKED:
APPROVED:
APPROVED:
HATHAWAY INSTRUMENTS, INC.
DENVER COLORADO 80222
OUTLINE DRAWING,
SOLID STATE FREQ. RELAY
DWG SIZE C
CODE IDENT NO 27882
709800
SCALE: 1/2
SHT. 1 OF 1