INSTRUCTIONS

GEK-6877B

PHASE COMPARISON RELAY

TYPES

SLD42D1
SLD42D2

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

ADDENDUM

TYPE SLD42D1, AND SLD42D2 RELAY

This supplement in addition to the attached booklet comprises the instructions for the SLD421 and 2 relays, which were modified after field installation.

The modifications are discussed below:

1. Filters were added to the positive and negative sequence network outputs to prevent operation on line pickup.

2. A redesigned squaring amplifier card (D22A) with reduced sensitivity to eleiminate operation during network delay.

3. The FDH card (D16H) was modified and the pickup setting increased. This was necessary to avoid operation on charging currents and reduce the possibility of tripping on decaying line currents after external fault clearing.

4. The G4 (D23) was modified to avoid overreach.

5. Modified the transient blocking card (T20) and adjusted pickup time to 35 ms. The avoided blocking on delayed internal fault clearing.

The internal connections for the tap block and logic units are shown in figures 1 and 2 respectively. These supersede those internals illustrated in the attached booklet (fig. 11 and 14). The internals for the printed circuit cards referred above are shown in GEK-7364.

The application section for the modified SLD42D relay is below, and supersedes that application section in the attached book.

APPLICATION

GENERAL

The Type SLD42D phase comparison relays in conjunction with SLYL phase relays are particularly adapted to the protection of transmission lines, where the presence of mutual inductance with split busses or series capacitor compensation makes the application of directional comparison relaying difficult.

The SLD42 relay employs positive and negative sequence excitation. This is accomplished by passing selected phases of the CT secondary current through a positive and then a negative sequence filter. A portion of the single phase output of the positive sequence filter is then vectorially subtracted from the full single phase output of the negative filter to yield a single phase keying quantity that is proportional to:

$$I_k = I_2 - \frac{I_1}{K} \qquad (1)$$

where K can be set for 5, 7, or 10. The phase angle of this quantity is compared with the phase angle of a similarly obtained quantity at the remote end of the line provided that the negative sequence fault detectors FDL, FDH, and the signal magnitude detector FDM operate for either an internal or external fault.

The basic concepts of mixed excitation is to have the negative sequence signal (I_2) dominate the positive seqeunce signal (I_1/K) for all faults, (except three phase faults), hence for all unbalanced faults the phase comparison will essentially be on a negative sequence basis. For three phase faults there will be no negative sequence current (except that which results from unbalances introduced by such things as non-transposition of lines, current transformer saturation, or load unbalance), thus phase comparison will be on a positive sequence basis.

For various faults and fault locations the relative magnitudes of I_1 and I_2 must be known to calculate the quantity I_k. It is important to recognize that neglecting load current I_1 and I_2 in equation (1) will be equal for phase and ground fualts. For double phase to ground faults I_1 will always be greater than I_2 by an amount that depends on the ratio of the system zero sequence to positive sequence impedance. As a result, it is necessary to consider double phase to ground faults as well as single phase to ground faults in the application of the SLD42 relays. Given a fault location, the negative sequence component of current for a phase to phase fault will always be half of the three phase positive sequence fault current, and equal to or greater than the negative sequence component in a double phase to ground fault. Consequently, there is no need to consider phase to phase faults separately.

If the SLD42 relay is applied to long, heavily loaded HV or EHV transmission lines with series capacitor compensation, the influence of load current, shunt capacitance, and series capacitors requires more detailed consideration for optimum reliability than would be necessary for short lines.

LOAD CURRENT

For an internal fault with no load flow the keying signals at the two ends are in phase, and as shown in Fig. 10, the received carrier is in phase with the transmitted carrier. The presence of a substantial load current, which continues to flow through the line during an internal fault, may cause the keying signals at the two ends to be shifted out of phase. Because of the 3 millisecond pickup setting of the integrator timer, tripping is obtained when the phase angle between the keying signals at the two ends of the line is 115^0 or less. Actually the phase angle criterion for determining settings is to restrict the keying signal angular difference to 60^0 or less. This provides a margin of 55^0 to allow for additional phase shift due to factors other than load flow.

I_1 of equation (1) is the superposed sum of the prefault load component and the fault component as determined by Thevenin's theorem. The influence of load current on equation (1) is most readily obtained by evaluating the keying signal, I_{kF}, resulting from fault components of current and comparing it with the keying signal resulting from the load component of I_1, I_{kL}. Equation (1) may be rewritten:

$$I_k = I_2 - \left(\frac{I_{1F} + I_{1L}}{K}\right)$$

$$I_k = \left(I_2 - \frac{I_{1F}}{K}\right) - \frac{I_{1L}}{K}$$

$$I_k = I_{kF} - I_{kL} \qquad (2)$$

Assuming that the positive source impedance is equal to the negative source impedance and the sources at both ends of the line have the same impedance angle, then I_{kF} will have the same phase angle at both terminals but opposite in polarity. It is assumed that I_{kL} may have any phase relationship to I_{kF}; the worst angle is a function of the negative (/positive/) distribution factor, C, as illustrated in Fig. 15.

The optimal value of K is the smallest value that will restrict the phase angle between keying signals on unbalanced faults to 60^0, thereby providing maximum sensitivity on 3 phase faults. The method for selecting the optimal valus of K is covered under CALCULATION OF SETTINGS.

SHUNT CAPACITANCE

The current slowing into the negative sequence shunt capacitance during an external fault will cause the negative sequence currents realized by the two terminals to be of different magnitude. The negative sequence fault detectors FDH and FDL have a difference in setting larger than the negative sequence current flowing in the shunt capacitance. This is to assure that the tripping element FDG is not picked up at one end before the carrier start element FDL is energized at the other.

With the fault keying signal I_{kF} at one terminal larger than it is at the other for an external fault, and with the magnitude of I_{kL} equal to the mean of the two I_{kF} magnitudes, it is possible to produce in phase keying signals, I_k, at the two terminals (provided I_{kF} and I_{kL} are in phase at each end). This could produce an undesired trip for an external fault since in phase keying signals produce a trip output. To overcome this possibility the FDM function, which is operated by I_k, should be set above the maximum value of I_k expected for the above condition to prevent phase comparison from occurring.

The inrush into the shunt capacitance on line energization (particularly with unequal pole closing of the breaker) may limit the setting of FDH which can be safely used.

SERIES CAPACITANCE

The series capacitance may affect the phase comparison indirectly if spurious carrier is generated when the protective gaps flashover. It is anticiapted that these bursts of spurious carrier will be in the range of one millisecond, which could reset the phase comparator timer if allowed to block AND45.

INFORMATION REQUIRED FOR SETTING CALCULATIONS

In order to establish the optimum settings for the SLD42 relay it is necessary to obtain the following system data:

1. Maximum load current present in the line for each system configuration to be considered.
2. Mimimum positive sequence fault current present in each terminal for internal three phase faults near each terminal and the midpoint of the line for each system configuration.
3. Mimimum positive and negative fault current present in each terminal for single line to ground faults near the midpoint of the line and near each terminal for each system configuration.
4. Mimimum positive and negative sequence fault current present in each terminal for double line to ground faults near each of the terminals for each system configuration.
5. The ratio R_0 (ØG) of I_0 for single line to ground faults to $I_{3\emptyset}$ for 3 phase faults at each fault location and each system configuration.

If the information is not available directly in the form required, it can be derived if the fault study provides for each location:

1. The total 3 phase fault current and the distribution factors.
2. The total zero sequence fault current for a single line to ground fault.
3. The maximum load current.

The total negative sequence fault current for a single line to ground fault will equal to I_0, as will the total fault component of the positive sequence current, $I_{1F}(\emptyset G)$.

The ratio $R_0(\emptyset G)$ may be used to obtain the positive and negative sequence components of fault current for double line to ground faults in conjunction with $I_{3\emptyset}$ at the same fault location.

$$I_{1F}(\emptyset\emptyset G) = R_1(\emptyset\emptyset G) \times I_{3\emptyset} = I_{3\emptyset} \times \frac{1 - R_0(\emptyset G)}{2 - 3R_0(\emptyset G)}$$

R_1 (ØØG) can be read directly from Figure 16A.

$$I_2(\emptyset\emptyset G) = R_2(\emptyset\emptyset G) \times I_{3\emptyset} = I_{3\emptyset} \times \frac{1 - 2R_0(\emptyset G)}{2 - 3R_0(\emptyset G)}$$

$R_2(\emptyset\emptyset G)$ can be read directly from Figure 16B.

The distribution of negative and positive sequence components of fault current at terminals X and Y can be obtained by multiplying the total sequence components of fault current by the distribution factors C_X and C_Y.

CALCULATION OF SETTINGS

The installation adjustments of the SLD42 consist of pickup settings of G4, FDH, FDL, FDM and the value of K which determines the relative emphasis on the positive and negative sequence inputs to the keying signals. A sample calculation is made for the system in Figure 17A which is presumed to provide for the protected line the most onerous application from a consideration of load studies and equipment outages. Figure 17B illustrates the tabulation of data for the sample system.

Before calculating $I_2(\emptyset G)_X$ (which is equal to $I_2(\emptyset G) \times C_X$, $R_0(\emptyset G)$ should be evaluated to ascertain if the lowest negative sequence current is associated with single line to ground faults or double line to ground faults. If $R_0(\emptyset G)$ is 0.333 or lower, $I_2(\emptyset G)$ will be equal to or lower than $I_2(\emptyset\emptyset G)$, and $I_2(\emptyset G)$ should be calculated. Conversely, if $R_0(\emptyset G)$ is larger than .333, $I_2(\emptyset\emptyset G)$ will be smaller, and should be calculated.

PICKUP SETTINGS OF FDH AND FDL

The FDL level detector should be set as low as possible without risk of its operating on the maximum expected load unbalance, unless the possibility of continuous keying of the channel is not objectionable. For many applications the minimum FDL pickup of 0.2 amperes negative sequence will be applicable.

The FDH level detector must be set such that it will respond to any internal unbalanced fault with a margin of at least 50 percent. That is, the minimum negative sequence current for an unbalanced fault at any location on the protected line must be at least 1.5 times the negative sequence pickup of FDH. An additional requirement on FDG pickup setting is that it be sufficiently above FDL to insure security on external faults. The setting of FDH must establish a margin between the local blocking level (FDL pickup) and the tripping level at the remote terminal (FDH pickup). For two terminal line applications the recommended margin is expressed by the following equation:

$$FDH = (\frac{4}{3})\ FDL$$

If there is significant negative sequence charging current flowing into the protected line during an external fault, it will tend to negate some of the margin provided by the above equation.

Therefore, to account for charging current the equation for FDH pickup becomes:

$$FDH = (\frac{4}{3})\ FDL + I_{C2}$$

where I_{C2} = negative sequence charging current flowing in the protected line section during an external fault.

The negative sequence charging current in the equation above should be:

$$I_{C2} = 0.5 \times I_{C1} \qquad (3)$$

where I_{C1} = positive sequence charging current

$$I_{C1} = \frac{V_{LN}}{Z_{SC}}$$

where Z_{SC} = total impedance of the distributed shunt capacitance

If shunt reactors are present the steady state value of charging current will be diminished. However, this effect should not be considered since coordination is necessary on a transient basis. The value of I_{C2} in equation (3) is an empirically derived value that has been generally applicable where breakers with pre-insertion resistors are used.

A possible restriction on FDL is that it should be set above the negative sequence current that may result from maximum load current flowing through an untransposed line, otherwise continuous carrier may be transmitted.

SELECTION OF K FACTOR

As noted under general comments, the minimum value of K should be selected. For less onerous applications, K = 5 should be selected. K = 5 may be used with an ample margin of safety if the minimum load current is less than 125% of the smallest $I_2(\emptyset G)_y$, $I_2(\emptyset\emptyset G)_x$ and $I_2(\emptyset\emptyset G)_y$. If this relationship is not true, a more rigorous evaluation of the optimum value of K is necessary and the tabulation in Figure 17B should be completed.

The curves in Figures 18A, B and C are provided to allow the selection of the K factor directly, utilizing the data tabulated in Figure 17B. The curves are based on the following:

1. The angle between the keying signals at the two terminals should be no more than 60°.

2. A safety margin is obtained by using only 75% of the calculated negative sequence current.

With reference to Figure 18A, each fault location is checked by plotting the ratio of three phase fault current to load current, $I_{3\emptyset}/I_{1L}$, and the lower of C_x and C_y. If the point is at the upper right of

the top one of the parallel curves, K = 5 will be suitable for that fault location.

If the point falls between the top and the bottom curve, enter the graph at the proper point on the $R_0(\emptyset G)$ scale at the top of the graph, proceed down until the V curve is reached, then horizontally to the left, until the distribution factor C = .03 is intersected. Draw a curve parallel to the existing curve which passes through the intersection of the horizontal line drawn and C = .03. This construction is shown in dashed lines for two arbitrary values of $R_0(\emptyset G)$; one where ØG is limiting and one where ØØG is limiting. If the point C_X (or C_Y) and $I_{3\emptyset}/I_{1L}$ plots above and to the right of the curve constructed for the specific value of $R_0(\emptyset G)$, then K = 5 will be satisfactory. If this point plots below this curve then the procedure must be repeated, starting with K = 7, Figure 18B.

If the initial plot of C and $I_{3\emptyset}/I_{1L}$ lies below and to the left of the bottom curve then K = 5 is not suitable, and the procedure must be repeated, starting with K = 7, Figure 18B. If the procedure is repeated for K = 7 and K = 7 is found unsuitable then proceed to K = 10, Figure 18C.

When the value of K has been found for all fault conditions that may provide the limiting case, select the largest value of K (5, 7, or 10) and apply at both terminals. Different values of K at the terminals could result in a phase shift between the keying signals at each terminal for an unbalanced external fault, with false tripping as a possible consequence.

If desired the angular displacement between the keying signals may be obtained by plotting a phasor diagram of the two keying currents produced by the selected value of K. Figure 19A illustrates the phasor diagram for the fault at F3 where the ØG fault is the limiting condition. I_{KF} is obtained at terminal x by plotting $.75I_{2(\emptyset G)X}$ to an appropriate scale and vectorially subtracting the positive sequence fault component at X, $I_{1F(\emptyset G)X/K}$. Since the worst case of a phase A to ground fault is assumed $I_{1F(\emptyset G)X} = I_{2F(\emptyset G)X}$, and $I_{1F(\emptyset G)X/K}$ is subtracted directly from $.75I_{2(\emptyset G)X}$. From Figure 15, the worst angle between I_{KL} and I_{KF} can be obtained for the lower value of C (C_X). At this angle, I_{KL} is drawn to the same scale as $I_{2(\emptyset G)X}$ and the angle ($\emptyset_1$) between I_K and I_{KF} is obtained by measurement. Similarly at terminal Y, $0.75\ I_{2(\emptyset G)Y}$ can be plotted and $I_{1F(\emptyset G)Y/K}$ can be subtracted directly from it to obtain I_{KF}. I_{KL} can be added to I_{KF} (I_{KL} at Y is 180° out of phase with I_{KL} at X) to obtain I_K at terminal Y. The angle between I_{KF} and I_K at Y ($\emptyset_2$) is added to θ_1 to obtain the total angular displacement between the keying signals at the two terminals.

The angular displacement between the keying signals at the two terminals can be plotted in a similar manner for a case where ØØG fault is the limiting type of fault, with two exceptions. $I_{1F(\emptyset\emptyset G)X}$ is not equal to $I_{2(\emptyset\emptyset G)}$ and must be obtained from the tabulation in Figure 17B. $I_{1F(\emptyset\emptyset G)X}$ will not subtract directly from $I_{2(\emptyset\emptyset G)X}$ in the worst type of fault, but at 60°. The fault at location F1 is plotted in Figure 20A.

If the line under consideration is series capacitor compensated, K = 7 should be used, and there is no need to follow the procedure above. This K value was determined on an empirical basis and represents an optimum compromise value.

SETTING OF FDM

As explained previously a combination of load current and shunt capacitance can combine to produce a false trip on an external fault. To assure that keying cannot occur for this case, FDM should be set above 50% of the keying signal produced by the positive and negative sequence charging currents.

$$FDM = I_{c2} + \frac{I_{c1}}{K}$$

In this case: $I_{c1} = 0.5\ \frac{V_{LN}}{Z_{shunt}}$

where: $Z_{shunt} = \frac{Z_{sc}\ \ (Z_{sr})}{Z_{sc} + Z_{sr}}$

Z_{sc} = total impedance of the distributed shunt capacitance

Z_{sr} = total impedance of the shunt reactors (if present)

$$I_{c2} = 0.25\ \frac{V_{LN}}{Z_{shunt}}$$

$$FDM = \frac{0.25\ V_{LN}}{Z_{shunt}} + \frac{0.5\ V_{LN}}{(K)Z_{shunt}}$$

The above equation includes a safety margin of 2.

The minimum value of keying signal for an internal fault can be obtained by taking the minimum value of the fault component of the keying signal, I_{KF}, and subtracting the load component of the keying signal, I_{KL}, directly from it.

$$I_K \ (MIN.) = |I_{KF} \ (MIN)| \ - \ |I_{KL} \ (MAX)|$$

I_K(MIN) should be compared with the setting for FDM to assess the margin of safety. Figures 19B and 20B illustrate the minimum keying signal for fault locations F1 and F3.

PICKUP SETTING OF G4

This unit is non-directional and therefore must be set above the maximum through ground fault current ($3I_0$) for faults in either direction. A pickup setting equal to 125% of the maximum steady state through fault current is recommended. For the sample calculation, the maximum through fault current is assumed for faults at F1 and F3. However, if series capacitor compensated parallel lines exist, the maximum through fault current may occur for a fault on a parallel line after it opens at one terminal. On series capacitor compensated lines, a pickup setting equal to 200% of the maximum steady state through fault current is recommended.

Consideration muat also be given to the possibility of unequal ploe closing of the circuit breaker when the line is reclosed at the second terminal. The G4 element must be set above the maximum load transfer over a single phase for the system conditions obtaining at the time of reclosure. The same margins should be obtained in this instance as mentioned previously.

SAMPLE CALCULATIONS (refer to Figure 17)

Setting of FDH and FDL:

Set FDH = 2/3 (I_2 minimum) = (2/3) 0.19 = 0.127 pu

This is the maximum value at which FDH may be safely set.

The maximum FDL setting may be determined from:

$$FDH = \frac{4}{3} FDL + I_{C2}$$

$$FDL = \frac{4}{3} (FDH - I_{C2}) = 0.75 \ (.127 - \frac{0.5}{6})$$

$$FDL = .0327 \text{ p.u.}$$

SELECTION OF K FACTOR:

Utilizing the procedure previously outlined it is found that K = 10 is required for faults at F2 and F3. K = 10 must therefore be used at both terminals.

SETTING OF FDM

$$FDM = \frac{0.25 \ V_{LN}}{Z_{shunt}} + \frac{0.5 \ V_{LN}}{(K)Z_{shunt}}$$

$$Z_{shunt} = \frac{(-j6) \ (j8)}{-j6 + j8} = j24$$

$$FDM = \frac{0.25}{24} + \frac{0.5}{(10) \ (24)}$$

$$= .0104 + .00208$$

$$= .0125 \text{ p.u.}$$

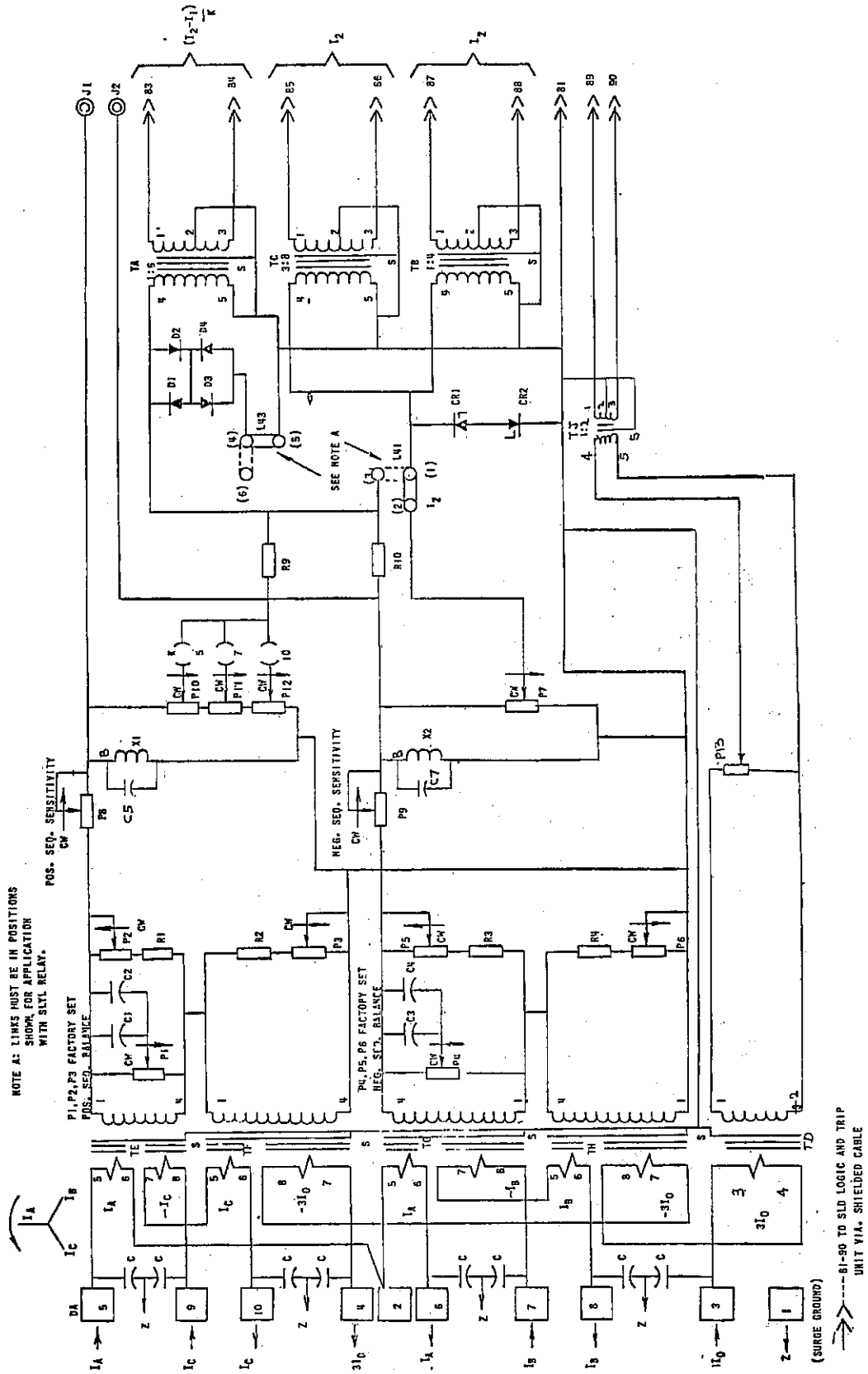


FIG. I (0165B2514-0) Internal Connections Diagram For The SLD42D Network Unit

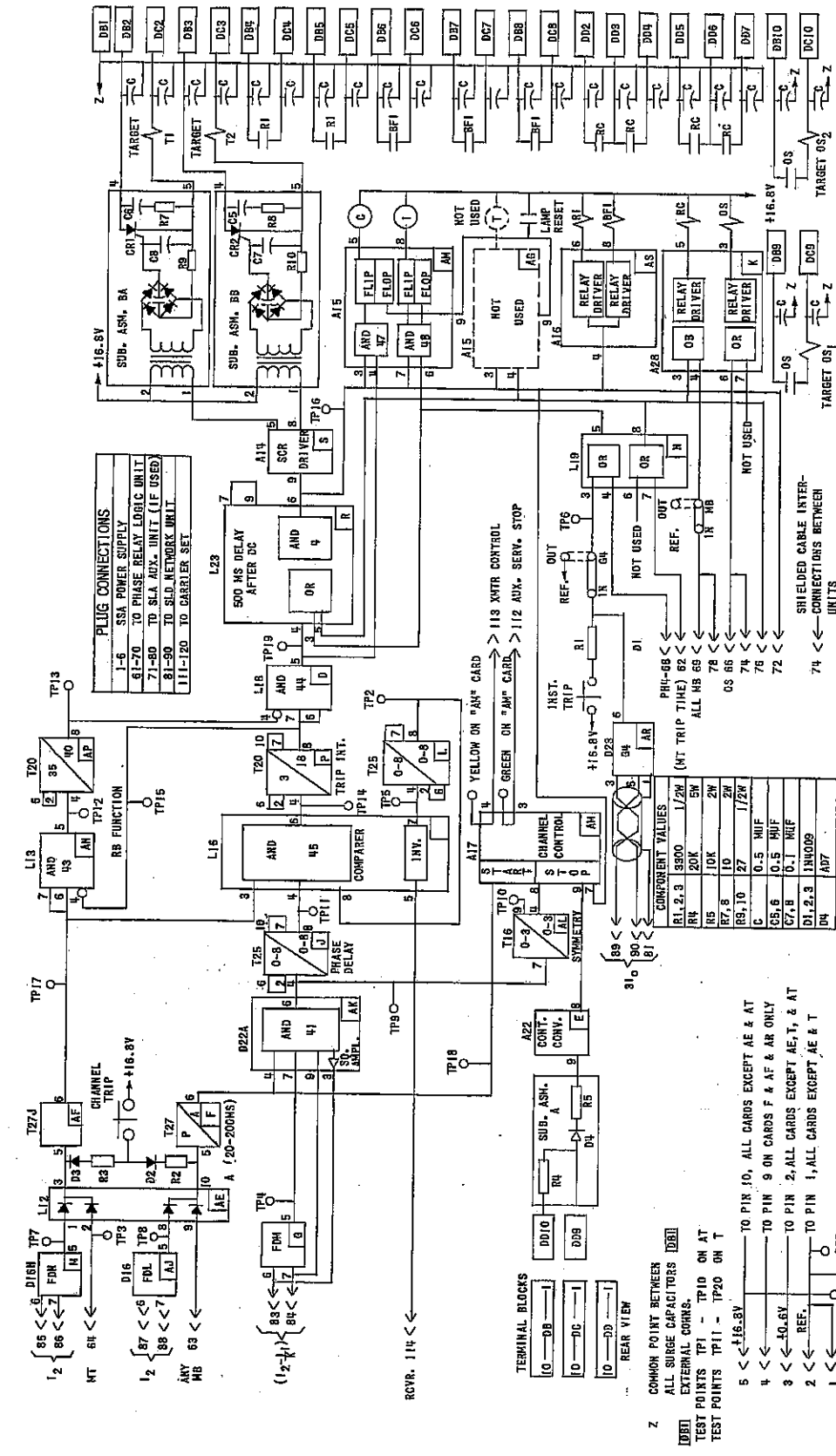


FIG. II ()165B2515-0) Internal Connections Diagram For The SLD42D Logic And Trip Unit

GEK-6877

TYPE SLD42D RELAY

DESCRIPTION

FUNCTIONS

The Type SLD42D relay is a solid state phase comparison pilot relay for differential protection of transmission lines on three-phase, phase-to phase, and phase-to-ground faults. The relay contains both positive and negative sequence networks and the associated phase comparison logic; FDL and FDH negative sequence fault detectors; FDM (positive and negative sequence) keying level detector; G4 direct-trip residual overcurrent function; two SCR (silicon controlled rectifier) trip circuits with hand reset series targets; and auxiliary relay contact outputs for RI (reclosing initiation), BFI (breaker failure initiation), OS (out-of-step), and RC (reclose cancellation).

NETWORK UNIT

The SLD42D is packaged in two separate metal units suitable for mounting on standard 19-inch racks. The Network Unit, which is three rack-units high, includes the positive and negative sequence networks and associated adjustment potentiometers and tap block. The Network Unit also includes voltage limiter circuits and isolation transformers to couple the output voltage signals to the Logic Unit. Fig. 2 shows the outline and mounting dimensions for the Network Unit. The location of the various internal components of the Network Unit are shown in Fig. 3.

LOGIC UNIT

The Logic Unit is four rack units high and contains the various printed circuit cards to provide the functions listed above. All the output functions listed above (trip circuits and auxiliary relays) are located in the Logic Unit. The outline and mounting dimensions are shown in Fig. 4. The printed circuit cards plug in from the front of the unit into sockets which are keyed to prevent insertion into the improper socket. The letter addresses (AE, AF, etc. for the upper row, and D, E, F, etc. for the lower row) appear on the card guide in front of each socket. These addresses are shown on the component location drawing, Fig. 5, and the internal connection diagram, Fig. 14. The signal test points (TP2, TP3, etc.) shown on Fig. 14 are connected to instrument jacks on the Test cards in the AT and T positions. TP1 (top) thru TP10 (bottom) are located on the AT card. TP11 (top) thru TP20 (bottom) are located on the T card. The Logic Unit also includes a CHANNEL TRIP push button to simulate FDL and FDH output, and an INST. TRIP push button to simulate G4 output. A window in the front cover allows observation of the two SCR and two OS targets and the C (carrier) and I (instantaneous overcurrent) trip lamps. Both the targets and trip lamps are reset by push buttons in the window. Moveable links are provided behind the front cover to allow the G4 and RC circuits to be connected or disabled.

ASSOCIATED EQUIPMENT

The SLD42D requires a Type SSA D.C. power supply to supply regulated 17 V D.C. and bias to operate the logic and output circuits. A high speed carrier channel (Type CS26) is used with each SLD42D to transmit and receive signals proportional to line current phase angle, to obtain differential protection between remote ends of a protected line. A type SLYL12 distance relay is also used to obtain the required fault detector sensitivity on balanced three phase faults, where FDL and FDH (operated by negative sequence), may not respond.

The signal interconnections between the SLD42D and the SLYL12, CS26, and SSA are provided by plug-in type multi-conductor shielded cables. These signal interconnections between the SLD42D, SLYL12, and CS26 are shown on the typical overall logic diagram of Fig. 8.

The incoming current connections to the SLD42D Network Unit from the C.T.s are made via a Test and Connection Receptacle, which is connected to the DA terminal strip on the unit by a 10-conductor cable. This Test and Connection Receptacle (shown in Fig. 6) allows disconnection from the C.T.s by removal of the connection plug, and A.C. testing with the standard Type XLA relay test plug. The various trip and auxiliary output circuits connected to the Logic Unit DB, DC, DD terminal strips are similarly connected to the external circuits via three additional Test and Connection Receptacles (TDB, TDC, TDD). A typical external connection diagram for the SLD42D is shown in Fig. 7.

RATINGS

TEMPERATURE

65° C maximum ambient outside the relay cases.

ELECTRICAL

5 amp, 60 cycle continuous, and 250 amp, 60 cycle for one second for all input current circuits.

125 volts DC, 30 amp tripping duty on SLD42D1 trip circuits. 250 volts DC, 30 amp tripping duty on SLD42D2 trip circuit. 1 amp, DC targets on all series targets for OS and SCR. 0.5 amp inductive interrupting rating at 125 V DC all auxiliary relay contacts. 0.25 amp inductive interrupting rating at 250 V DC all auxiliary relay contacts. 3 amp DC continuous rating on all auxiliary relay contacts.

BURDEN

10 volt-amperes maximum current burden per phase pair at 5 amp, 60 cycles.

ADJUSTMENT RANGES

FDL pickup = 0.2-1.6 amp. Neg. Sequence (I_2)
FDH pickup = 0.5-4 amp. Neg. Sequence (I_2)
K (Ratio of Neg. to Pos. Seq. Sensitivity) = 5/7/10
FDM pickup = 0.2-0.6 amp. Neg. Sequence ($I_1 = 0$)
FDM pickup = 0.2K-0.6K amp. Pos. Sequence ($I_2 = 0$)
G4 pickup = 4-40 amp. residual (3Io)

FDL, FDH, FDM, and G4 are continuously adjustable over the above specified ranges by means of the adjusting screw on the front of the corresponding level detector cards. The selection of the K ratio is made by means of a tap block on the front of the Network Unit.

OPERATING TIMES

Phase Comparison tripping time is 1 cycle maximum for all faults except balanced three phase faults. (Maximum tripping time for balanced three phase faults using SLYL12 supervising relay is 1 3/4 cycle.)

G4 direct tripping time on ground faults is 1/2 cycle maximum.

The pickup and dropout times of the auxiliary relays are shown in the following table:

OPERATING TIME (IN CYCLES)

AUX. RELAY	PICKUP	DROPOUT
RI	1	8-10
BFI	1	1
RC	3/4	8-10
OS	3/4	8-10

OPERATING PRINCIPLES

PHASE COMPARISON

A phase-comparison pilot relaying scheme operates on the basic principle that a fault can be judged to be either internal or external to a protected line section by comparing the relative phase positions of the fault currents at the two ends of the line. In practice the quantities used in making the comparison between the two ends of the line are single-phase voltages which are obtained by combining the CT secondary currents at each end. The single-phase voltages are used to produce a square-wave signal which modulates the channel transmitter and attempts to trip the local breaker on alternate half-cycles. This basic operation of a phase comparison scheme is illustrated in Fig. 10.

In the SLD42D relays the single-phase voltage, which will be referred to as a "keying signal", is obtained by combining the outputs of a negative-sequence and a positive-sequence network with the resultant output weighted to favor the negative-sequence component by a multiplying factor "K". That is, the resultant keying signal is proportional to $I_2 - \frac{I_1}{K}$.

NEGATIVE-SEQUENCE NETWORK

These positive and negative-sequence networks are contained in the Network Unit. The complete internal connections are shown in Figure 11. It will be noted that the postive- and negative-sequence networks are similar but differ in the way they are connected to the CT secondaries. Both networks consist of two transactors, each with two primary windings and an adjustable resistive load across a secondary winding. The positive-sequence network consists of transactors TE and TF with adjustment potentiometers P_1, P_2 and P_3. The negative-sequence network consists of transactors TG and TH with adjustment potentiometers P4, P5, and P6.

The term "transactor" is a contraction of transfer-reactor. It is essentially an air-gap current transformer with secondary current, and hence secondary voltage across the loading resistor, proportional to the vector sum of the input currents in the leading direction. The performance of a transactor in a circuit is described by its transfer impedance Z_T and the associated angle θ_T:

$$Z_T = \frac{V_{out}}{I_{in}} \angle\theta_T \qquad (1)$$

Where: V_{out} = Secondary output voltage

I_{in} = Vector sum of the input currents

θ_T = Angle by which V_{out} leads I_{in}.

The negative-sequence network will be used to explain the operating principles of the sequence network in the SLD42D relay. This network is represented in simplified form in Figure 12. A negative-sequence network is, of course, one which produces an output proportional to the negative-sequence component of the input currents, and further produces no output for the positive- or zero-sequence components of the input current. It can be shown that using two transactors as in Figure 12 the output will be proportional only to negative-sequence current if the transactor angles are 30° apart and if the transactor with the lower angle has a transfer impedance higher than the other by a $\sqrt{3}$ ratio. In the SLD negative-sequence network the angles are 75° and 45°, and the impedances are 2 and $2\sqrt{3}$ ohms respectively.

As shown in Figure 12 the 75° transactor windings are connected to phase-A and reversed phase-B CT currents. The output voltage, therefore, is:

$$\bar{V}_{75} = 2\,(\bar{I}_A - \bar{I}_B) \qquad (2)$$

The 45° winding transactor is energized by phase-B CT current and reversed CT residual current ($3I_o$), but since the residual winding has one-third the turns of the phase-B winding, the output voltage can be expressed by:

$$V_{45} = 2\sqrt{3}\,(I_B - I_o) \qquad (3)$$

If the transactor secondaries are connected in series, as shown in Figure 12, the network output voltage V_T can be expressed as follows:

$$\bar{V}_T = \bar{V}_{75} + \bar{V}_{45} = 2(\bar{I}_A - \bar{I}_B)\angle 75^\circ + 2\sqrt{3}\,(\bar{I}_B - \bar{I}_o)\angle 45^\circ \qquad (4)$$

It can be shown that this network output voltage is proportional to the negative-sequence component of the input currents. That is:

$$\bar{V}_T = 2\sqrt{3}\,I_2 \angle 105^\circ \qquad \text{Where I is phase-A} \qquad (5)$$

This relationship can best be shown graphically. Figure 13A shows that for a pure positive-sequence system the magnitudes and angles of the transactor secondary voltages are such that the voltages are equal and 180° apart. Thus the secondary voltages cancel and the network output V_T is zero.

Figure 13B shows the response of the network to a three-phase system of pure negative-sequence currents. Note that the network output voltage is now equal to $2\sqrt{3}\ I_2 \angle 105^\circ$, with the angle referenced on the phase-A current, i.e., I_{A2}. This agrees with equation (5) above.

Figure 13C shows the response of the network to a phase-A to ground fault. Here we see that the zero-phase sequence component of the fault current has been eliminated from the network response by the action of the I_o winding of the 45° transactor, and that the network output voltage is again $2\sqrt{3}\ I_2 \angle 105^\circ$.

POSITIVE-SEQUENCE NETWORK

It can be shown that a positive-sequence network can be obtained by means of the same components used in the negative-sequence network described

above, provided only that the phase-C current is used instead of phase-B. That is:

$$\bar{V}_T = \frac{2}{3}(\bar{I}_A - \bar{I}_C) \angle 75^\circ + \frac{2\sqrt{3}}{3}(\bar{I}_C - \bar{I}_o) \angle 45^\circ \quad (6)$$

$$\bar{V} = \frac{2}{3}\sqrt{3}\ \bar{I}_{A1} \angle 105^\circ \quad (7)$$

This can be demonstrated by a graphical analysis similar to that used for the negative-sequence network. The 1/3 factor in equations (6) and (7) results from the use of 1/3 as many primary turns in the positive-sequence transactors.

It should be emphasized that the 105° angle which appears in equations (5) and (7) above results from calculations based on the open circuit condition of the network. In practice the loading effect of the low-pass filter will cause the angle of the network output voltage to deviate from the 105° calculated value, but since the loading will be practically the same in the network units as the two ends of the line, the angles will also be the same.

It should be noted also that the choice of 75° and 45° for the transactor angles is one of practicality rather than necessity. The only requirement in the basic design is the 30° difference between the two angles and the $\sqrt{3}$ relation between the transfer impedances. It is important, however, that the angles be the same from network to network to insure coordination between terminals.

LOGIC CIRCUITS

The operation of the logic circuits are best explained by referring to the Logic Unit Internal Connection Diagram, Fig. 14. AND 45 (N) is the comparer previously described. The keying input signal at TP11 is obtained from the mixed (positive and negative sequence) network output which has been passed through the squaring amplifier (AK). The squared keying signal is supervised by the FDM keying level fault detector (G) and the FDL blocking level fault detector (AJ) at AND 41 (AK). The FDH tripping level fault detector (M) output is supplied to the comparer at TP17. Both FDL and FDH operate on negative-sequence voltage from the Network Unit to obtain maximum sensitivity on unbalanced faults, while remaining insensitive to balanced load currents. The FDL and FDH functions on balanced three-phase faults are provided by the lens-type MB and MT function in the associated type SLYL12 distance relay. These signals are connected into the Logic Unit via shielded cable pins 63 and 64. The pulse stretchers (F) and (AF) are present to provide a continuous output for cases where the apparent impedance seen by the SLYL12 MB and MT functions immediately after fault inception may not allow a continuous signal.

In the previous discussion of phase-comparison operation (and in Fig. 10) it was shown that the keying signal must operate the transmitter during the half cycles which the comparer is not being energized. This is accomplished by the application of a continuous "start" signal to the channel control card (AM) at TP18 when FDL operates, and applying the squared keying signal from TP9 to the channel control "stop" input. The key-off signal is passed through the symmetry card (AL) to allow adjustment of the carrier on-off times to achieve a symmetrical receiver output at remote terminal. This unsymmetrical transmitter modulation is necessary to compensate for differences in the turn-on and turn-off of the remote receiver.

The local receiver output is connected to the NOT input to the comparer via an inverter and an 0-8/0-8 card (L). This 0-8/0-8 (L) provides an integrating time on received carrier to avoid possible incorrect blocking due to momentary bursts of carrier on gap flashover during an internal fault. The phase delay (J) card is present to compensate for channel delay and the carrier integrator (L) and provide the optimum relation between the comparer keying input and the comparer blocking input. The receiver output is passed through the inverter (N) to provide signal compatibility between the positive referenced CS26 carrier and the negative referenced SLD42D logic. A similar signal inversion occurs in the CS26 transmitter control at the SLD42D channel control interface.

An external fault above FDH pick up level does not produce a comparer output because half cycle blocking signals are present at TP2 in phase with the TP11 keying signal. An internal fault above the FDH pickup level will produce comparer output at TP14 on the half cycles corresponding to TP11 keying, since the TP2 comparer blocking signal will not be present during that half cycle. The comparer output is passed through the trip integrator (P) to provide a continuous signal to the trip bus at the TP16 via AND 44 and AND 46.

AND 44 provides supervision of the trip integrator (P) output by the RB transient blocking function. The RB function consists of AND 43 (AN) plus the 25/40 timer (AP). If a system fault occurs, operating FDH, and there is no trip integrator output within 25 milliseconds, an RB output will be produced at TP13. This RB output will block AND 44 until 40 milliseconds after the fault is cleared and FDH drops out. Since the RB pickup time is longer than the maximum tripping time for internal faults, the RB blocking function can only get set up on external faults. For internal faults the trip integrator output at TP15 will block AND 43 and prevent the 25/40 timer from timing and blocking tripping at AND 44. In this way the RB function acts to block any tripping until about 2 1/2 cycles after an external fault is cleared.

AND 46 (R) provides 500 timer supervision of all tripping signals. The purpose of this 500 timer supervision is to prevent a trip output at the TP16 trip bus until the DC supply to the equipment has been energized for approximately one-half second. This eliminates the possibility of undesired trips when the DC is initially switched on.

The G4 direct trip overcurrent function (AR) is operated from the output of the TD residual current ($3I_0$) transactor in the Network Unit. The G4 output at TP6 is passed through an OR circuit (H) and through an OR input to the AND 46 500 timer supervision to the trip bus at TP16. The other (H) OR input is connected to PH4 direct trip phase overcurrent function in the associated SLYL12 relay.

A contact converter circuit is provided to stop all carrier by closing an external normally-open contact. The output of this contact converter (E) is connected directly to a second OR input to the channel control (AM) "stop". The third OR input to the "stop" portion of the channel control card is connected to the TP16 trip bus. Any of the three "stop" inputs to the channel control card has preference over the "start" input.

OUTPUT CIRCUITS

A signal of the trip bus at TP16 produces a series of pulses from the SCR driver (S). These pulses are connected to the tripping SCR gate circuits by isolating transformers on sub-assemblies BA and BB. The anode-cathode junction of the SCR will conduct during the gating pulse interval, and will remain in the conductive state as long as the external circuit is completed and continues to draw current through the anode-cathode junction. This loss of gate control once the SCR is "fired" provides an effective "seal-in" on the trip circuit. It also means that the SCR trip circuit must be interrupted by an auxiliary contact on the breaker which will open when the breaker has been tripped. A hand-reset electro-mechanical target is connected in series with each SCR trip circuit.

The C (carrier) target lamp is turned on by the presence of TP16 trip bus signal and a TP19 (phase comparison trip) signal at AND 47 (AN). The I (instantaneous overcurrent) target lamp is turned on by the presence of a TP16 trip bus signal and a G4 or PH4 signal from the OR circuit on the (H) card. These C and I lights will remain on until the reset button is operated.

The BFI and RI auxiliary telephone-type relays are operated by the presence of a TP16 trip bus signal at the drivers (AS). The RC relay is operated via the upper relay driver on the (K) card by a three-phase SLYL12 fault detector (ALL MB) signal, or the optional time-delayed trip circuits (if used). If these SLYL12 circuits are used, the RC function will provide a contact output to cancel reclosing for three-phase faults or second zone faults. The lower relay driver (K) operates the OS relay for an out-of-step signal from the SLYL12. The 8-10 cycle time delay drop out time on RI, RC, and OS is obtained by diodes on their respective driver cards which are connected in parallel with the relay coils.

The detailed operation of the individual logic functions (AND, NOT, etc.,) may be understood by referring to the various card internal connection diagrams shown in Fig. 26A-26S.

APPLICATION

GENERAL

The Type SLD42D phase comparison relays (in conjunction with the SLYL12A) are particularly adapted to the protection of lines where the presence of mutual induction with split busses, or series capacitor compensation, makes the application of directional comparison relaying difficult or unreliable.

The SLD42D relay uses mixed positive plus negative sequence excitation. As explained previously, this is accomplished by passing the three phases of the CT secondary current through a positive and then a negative sequence filter. A portion of the single-phase output of the positive-sequence filter is then vectorially subtracted from the full single-phase output of the negative sequence filter to yield a single-phase quantity that is proportional to:

$$I_K = I_2 - \frac{I_1}{K} \qquad (8)$$

where K can be set for 5, 7, or 10. The phase angle of this quantity is compared with the phase angle of a similarly obtained quantity at the remote end of the line, if the negative sequence fault detectors FDL and FDH (or distance fault detectors) and the signal magnitude detector FDM, operate on an internal or external fault.

The basic idea behind the mixed excitation is to have the negative sequence (I_2) swamp out the positive sequence (I_1/K) for all faults except three-phase faults so that for all unbalanced faults the phase comparison will essentially be on a negative sequence basis. For three-phase faults, there will be no negative sequence current (except that which results from unbalances introduced by such things as non-transposition of lines, current transformer saturation, or load unbalance) so the phase comparison will be on a positive sequence basis. It is important to recognize that, neglecting load current, I_1 and I_2 in equation (8) above, will be equal to each other for phase-to-ground faults. For double phase-to-ground faults, I_1 will always be greater than I_2 by an amount that depends on the ratio of the system zero sequence to positive sequence impedance. For this reason, it is necessary to consider double phase-to-ground faults as well as single-phase-to-ground faults in the application of the SLD42D relay. For a given fault location, the negative-sequence component of current for a phase-to-phase fault will always be half of the three-phase positive-sequence fault current and eqaul to, or greater than, the negative sequence component in a double-phase-to-ground fault, so there is no need to consider phase-to-phase faults separately.

Where the SLD42D relay is applied to long, heavily loaded HV or EHV transmission lines with series capacitor compensation, the influence of load current, shunt capacitance, shunt reactors, and series capacitors requires more detailed consideration for optimum reliability than would be the case for short lines.

LOAD CURRENT

For an internal fault, the carrier signals illustrated in Figure 10 assume that the load current is negligible and therefore, the received carrier

is in phase with the transmitted carrier. The presence of a substantial load current, which continues to flow through the line during an internal fault, may cause the keying signals at the two ends to be shifted out of phase; thereby increasing the time that carrier is received beyond one half cycle, and reducing the carrier off time below one half cycle. Tripping is obtained if the duration of the carrier received signal is less than 300°. Reliable tripping is assured if the phase angle between the keying signals at each terminal is limited to no more than 60°.

The optimum value of K in equation (8) is the smallest value that will restrict the phase angle between keying signals on unbalanced faults to 60°, thereby assuring maximum sensitivity on 3Ø faults.

I_1 of equation (8) is the sum (by superposition) of the prefault load and the fault component determined by Thevenin's theorem. The influence of load current on equation (8) is most readily obtained by evaluating the keying signal resulting from fault components of current I_{KF} and comparing it with the keying signal resulting from the load component of I_1, I_{KL}.

Equation (8) can be rewritten:

$$I_K = I_{KF} - I_{KL} = (I_2 - \frac{I_{1F}}{K}) - \frac{I_{1L}}{K} \qquad (9)$$

On the assumption that the positive source impedance is equal to the negative source impedance, and the sources at both ends of the line have the same impedance angle, I_{KF} will have the same phase angle at both terminals. I_{KL} may be assumed equal in magnitude at both terminals and opposite in polarity.

It is assumed that I_{KL} may have any phase relationship to I_{KF}, the worst angle being a function of the negative (and positive) distribution factor (C) as illustrated in Figure 15. The method of selecting the optimum value of K is covered under the calculation of settings.

SHUNT CAPACITANCE

The current flowing into the shunt capacitance during an external fault will cause the sequence currents seen at the two terminals to be dissimilar. The negative sequence fault detectors FDH and FDL have a difference in setting larger than the negative sequence current flowing in the shunt capacitance to assure that the tripping element FDH is not picked up at one end before the carrier start element FDL is energized at the other.

A further consideration is that the keying signal I_{KF} may be larger at one terminal than it is at the other for an external fault. If I_{KL} is opposite in polarity and equal in magnitude to the mean of I_{KF} at the two terminals the keying signals I_K would have opposite polarity at the two terminals. FDM should be set to preclude keying at one terminal for this condition.

The inrush into the shunt capacitance on line energization, particularly with unequal pole closing of the breaker, may limit the setting of FDH that can be safely used.

The current drawn by the shunt reactors, if connected in the protected zone will reduce the steady state charging current of the shunt capacitance seen by the relays, but may not reduce the transient inrush on line energization.

SERIES CAPACITANCE

The series capacitance may affect the phase comparison indirectly if spurious carrier is generated when the protective gaps flashover. It is anticipated that these bursts of spurious carrier will be in the order of one millisecond duration which could reset the phase comparator timer if allowed to block AND 45 (Ref. Fig. 14). An integrating timer is employed ahead of AND 45 with an adjustable on and off delay. The factory setting of 2 ms/2 ms will preclude resetting on the 1 ms burst of carrier.

The low frequency transient component of fault current associated with series capacitors may cause intermittent operation of the fault detectors. The transient blocking circuit input (AND 43 Fig. 14) and the phase comparison circuit supervision input (AND 45 Fig. 14) are maintained by timer P/A for a preselected time, assuring continuous phase comparison regardless of the resetting of fault detectors. To assure coordination, the carrier start signal must be sealed in by a second P/A timer with a reset delay set longer than the P/A timer on the trip supervision.

INFORMATION REQUIRED FOR SETTING CALCULATIONS

In order to establish the optimum settings for the SLD42D relay, it is necessary to obtain the following system data:

1. Maximum load current that will flow in the line for each system configuration to be considered.

2. Minimum positive sequence fault current that will flow in each terminal for internal three phase faults near each terminal and the midpoint of the line for each system configuration.

3. Minimum positive and negative sequence fault current that will flow in each terminal for single line to ground faults near the midpoint of the line and near each terminal for each system configuration.

4. Minimum positive and negative sequence fault current that will flow in each terminal for double line to ground faults near each of the terminals for each system configuration.

5. The ratio R_O (ØG) of I_O for single line to ground faults to $I_{3Ø}$ for 3 phase faults for each fault location and each system configuration.

If the information is not available directly in the form required, it can be derived if the fault study provides for each location:

1. The total 3 phase fault current and the distribution factors.

2. The total zero sequence fault current for a single line to ground fault.

3. The maximum load current.

The total negative sequence fault current for single line to ground fault ($I_{2(\emptyset G)}$) will be equal to I_o, as will the total fault component of the positive sequence current ($I_{1F(\emptyset G)}$).

The ratio $R_o(\emptyset G)$ may be used to obtain the positive ($I_{1F(\emptyset\emptyset G)}$) and negative ($I_{2(\emptyset\emptyset G)}$) sequence components of fault current for double line to ground faults in conjunction with $I_{3\emptyset}$ at the same fault location.

$$I_{1F(\emptyset\emptyset G)} = R_{1(\emptyset\emptyset G)}\ I_{3\emptyset} = I_{3\emptyset}\ \frac{1-R_{o(\emptyset G)}}{2-3R_{o(\emptyset G)}}$$

$R_{1(\emptyset\emptyset G)}$ can be read directly from Fig. 16A

$$I_{2(\emptyset\emptyset G)} = R_{2(\emptyset\emptyset G)} \qquad I_{3\emptyset} = I_{3\emptyset}\ \frac{1-2R_{o(\emptyset G)}}{2-3R_{o(\emptyset G)}}$$

$R_{2(\emptyset\emptyset G)}$ can be read directly from Fig. 16B

The distribution of negative and positive sequence components of fault current at terminals X and Y can be obtained by multiplying the total sequence components of fault current by the distribution factors C_x and C_y.

CALCULATION OF SETTINGS

The installation adjustments of the SLD42D consist of the pickup settings of G4, FDH, FDL, FDM, and the value of K which determines the relative emphasis on the positive and negative sequence inputs to the keying signals. The settings will be discussed in the sequence in which they will be calculated. A sample calculation is made for the system in Figure 17A, which is presumed to provide for the protected line the most onerous application from a consideration of load studies and equipment outages.

Figure 17B illustrates the tabulation of data for the sample system.

The load current I_{1L} is obtained from load flow studies for the system configuration under study.

$I_{3\emptyset}$ is the total 3 phase fault current at the fault location.

I_o is the total zero sequence current for a single line to ground fault at the fault location. $R_{o(\emptyset G)}$ is the ratio of $I_o/I_{3\emptyset}$.

C_x and C_y are the positive sequence distribution factors for the fault location, and are assumed equal to the negative sequence distribution factors.

Before calculating $I_{2(\emptyset G)_x}$, which is equal to $I_{2(\emptyset G)}C_x$, $R_{o(\emptyset G)}$ should be evaluated to ascertain if the lowest negative sequence current is associated with single line to ground faults or double line to ground faults. If $R_{o(\emptyset G)}$ is .333 or lower, $I_{2(\emptyset G)}$ will be equal or lower than $I_{2(\emptyset\emptyset G)}$, and $I_{2(\emptyset G)}$ should be calculated. Conversely, if $R_{o(\emptyset G)}$ is larger than .333, $I_{2(\emptyset\emptyset G)}$ will be smaller, and should be calculated.

PICKUP SETTINGS OF FDH AND FDL

To provide coordination between the fault detectors at the two terminals, the setting of FDH at one terminal should be at least 4/3 the setting of the FDL at the other terminal. If the negative sequence current in the shunt capacitance of the line is significant, then the setting of FDH should be increased so that:

$$FDH = I_{2SC} + 4/3\ FDL$$

where I_{2SC} is the negative sequence current in the shunt capacitance (or the net shunt current if shunt reactors used) for a fault at the line terminals with minimum I_2 flowing through the line.

I_{2SC} may be calculated by first obtaining the minimum I_2 for fault locations, F1 or F3, Fig. 17A. The negative sequence voltage V2 at that fault location would be V_{LN} multiplied by $R_{o(\emptyset G)}$ if $I_{2(\emptyset G)}$ is less than $I_{2(\emptyset\emptyset G)}$. If $I_{2(\emptyset\emptyset G)}$ is smaller than $I_{2(\emptyset G)}$, multiply V_{LN} by $R_{2(\emptyset\emptyset G)}$.

The average negative sequence voltage on the line

$$(V_{2AV}) = V_2 - I_2\ (C_x)\ \frac{ZL}{2} \quad \text{For fault location F3}$$

$$\text{or} \quad (V_{2AV}) = V_2 - I_2\ (C_y)\ \frac{ZL}{2} \quad \text{For fault location F1}$$

$$I_{2SC} = \frac{V_{2AV}}{\frac{Z_{SC}(Z_{SR})}{Z_{SC} + Z_{SR}}}$$

where Z_{SC} is the total impedance of the shunt capacitance. Z_{SR} is the total impedance of the shunt reactors.

A further restriction of FDH is that it should be no more than 2/3 of the minimum I_2 at the terminal considered for an internal fault.

A possible restriction on FDL is that it should be set above the negative sequence current that may result from maximum load current flowing through an untransposed line, otherwise continuous carrier may be transmitted.

Because the system represents a long line, FDH is set equal to 2/3 I_2 minimum to minimize the possibility of FDH picking up on line inrush.

SELECTION OF K FACTOR

As noted under general comments, the minimum value of K should be selected. For less onerous applications, K = 5 should be selected. K = 5 may be used with an ample margin of safety if the maximum load current is less than 125% of the smallest of $I_{2(\emptyset G)x}$, $I_{2(\emptyset G)y}$, $I_{2(\emptyset\emptyset G)x}$, and $I_{2(\emptyset\emptyset G)y}$. If this

relationship is not true, a more rigorous evaluation of the optimum value of K is necessary and the tabulation in Fig. 17B should be completed.

The curves in Figures 18A, B and C are provided to allow the selection of the K factor directly, utilizing the data tabulated in Fig. 17B. The curves are based on the following:

1. The angle between the keying signals at the two terminals should be no more than 60^{o}.

2. A safety margin is obtained by using only 75% of the calculated negative sequence current.

With reference to Figure 18A, each fault location is checked by plotting the ratio of 3Ø fault current to load current, $I_{3\emptyset}/I_{1L}$, and the lower of C_x and C_y. If the point is at the upper right of the top one of the parallel curves, K = 5 will be suitable for that fault location.

If the point falls between the top and the bottom curve, enter the graph at the proper point on the $R_{o(\emptyset G)}$ scale at the top of the graph, proceed down until the V curve is reached, then horizontally to the left, until the distribution factor C =.03 is intersected. Draw a curve parallel to the existing curves which passes through the intersection of the horizontal line drawn and C = .03. This construction is shown in dashed lines for two arbitrary values of $R_o(\emptyset G)$, one where ØG is limiting, and one where ØØG is limiting. If the point C_x (or C_y) and $I_{3\emptyset}/I_{1L}$ plots above and to the right of the curve constructed for the specific value of $R_o(\emptyset G)$, then K=5 will be satisfactory. If it plots below this curve then the procedure must be repeated, starting with Figures 18B, for K=7.

If the initial plot of C and $I_{3\emptyset}/I_{1L}$ lies below and to the left of the bottom curve then K=5 is not suitable, and the procedure must be repeated, starting with Figure 18B for K=7.

If the procedure is repeated for K=7, and K=7 is found unsuitable, then proceed to Figure 18C for K=10.

When the value of K has been found for all fault conditions that may provide the limiting case, select the largest value of K (5, 7, or 10) and apply at <u>both</u> terminals. Different values of K at the terminals could result in a phase shift between the keying signals at each terminal for an unbalanced external fault, with false tripping as a possible consequence.

If desired, the angular displacement between the keying signals may be obtained by plotting a phasor diagram representing the 2 keying currents produced by the selected value of K.

Figure 19A illustrates the phasor diagram for the fault at F3, where the ØG fault is the limiting condition. I_K is obtained at terminal x by first plotting .75 $I_{2(\emptyset G)}{}^{x}$ to an appropriate scale. The positive sequence

component of the fault at x, $I_{1F(\emptyset G)x}$, will be equal to $I_{2(\emptyset G)x}$. Since the worst case of a phase A to G is assumed, $I_{1F(\emptyset G)x/K}$ is subtracted directly from .75 $I_{2(\emptyset G)}$ to give I_{KF}. From Fig. 15, the worst angle between I_{KL} and I_{KF} can be obtained for the lower value of C (C_x). At this angle, I_{KL} is drawn to the same scale as $I_{2(\emptyset G)X}$ and the angle (θ_1) between I_K and I_{KF} is obtained by measurement.

Similarly at terminal Y, 0.75 $I_{2(\emptyset G)Y}$ can be plotted (to a different scale if desirable) and $I_{1F(\emptyset G)y/K}$ can be subtracted directly from it to obtain I_{KF}. I_{KL} (to the same scale as $I_{2(\emptyset G)y}$) can be added to it 180° out of phase with I_{KL} at terminal X, to obtain I_K. The angle between I_{KF} and I_K at Y (θ_2) is added to (θ_1) to obtain the total angular displacement between the keying signals at the two terminals.

The angular displacement between the keying signals at the two terminals can be plotted in a similar manner for a case where a ØØG fault is the limiting type of fault, with two exceptions. $I_{1F(\emptyset\emptyset G)X}$ is not equal to $I_{2(\emptyset\emptyset G)X}$ and must be obtained from the tabulation in Fig. 17B. $I_{1F(\emptyset\emptyset G)x}$ will not subtract directly from $I_{2(\emptyset\emptyset G)X}$ in the worst type of fault, but at 60°. The fault at location F1 is plotted in Fig. 20A.

SETTING OF FDM

On some external faults, the fault component of the keying signal, I_{KF} may be approximately equal in magnitude, and opposite in polarity, to the load component of the keying signal, I_{KL}. In this event, the net keying signal I_K will approach zero, and the sequence current flowing in the shunt capacitance may cause I_K at one terminal to be 180° out of phase with I_K at the other terminal. To preclude keying at one, or both, ends for this possible condition, FDM should be set above 50% of the keying signal, produced by the positive and negative sequence charging currents.

$$\text{FDM} = \frac{V_2\ (AV)}{Z\ \text{shunt}} + \frac{V_1\ (AV)}{KZ\ \text{shunt}} \qquad \text{(Minimum setting)}$$

$$\text{or} \quad \frac{V_2(AV)}{Z\ \text{shunt}} + \frac{V_{LN} - V_2(AV)}{KZ\ \text{shunt}}$$

Where V_{2AV} is the average negative sequence voltage on the line for the minimum I_2 for fault locations F1 and F3. Z shunt is the net shunt impedance in the protected zone. The formula includes a recommended safety margin of 2.

The minimum value of keying signal for an internal fault can be obtained by taking the minimum value of the fault component of the keying signal, I_{KF}, and subtracting the load component of the keying signal, I_{KL}, directly from it.

$$I_K \text{ min.} = \left| I_{KF} \text{ min.} \right| - I_{KL} \text{ max.}$$

I_K min. should be compared with the setting for FDM to assess the margin of safety. Fig. 19B and 20B illustrate the minimum keying signal for fault locations F1 and F3.

PICKUP SETTING OF G4

This unit is non-directional and therefore must be set above the maximum through ground fault current ($3I_o$) for faults in either direction. For the sample calculation, the maximum through fault current is assumed for faults at F_1 and F_3. However, if series capacitor compensated parallel lines exist, the maximum through fault current may occur for a fault on a parallel line after it opens at one terminal. On series capacitor compensated lines, a pickup setting equal to 200% of the maximum steady state through fault current is recommended.

Consideration must also be given to the possibility of unequal pole closing of the circuit breaker when the line is reclosed at the second terminal. The G4 element must be set above the maximum load transfer over a single phase for the system conditions obtaining at the time of reclosure.

SAMPLE CALCULATIONS (Refer to Fig. 17)

Setting of FDH & FDL

Set FDH = 2/3 min. I_2 = .19 (2/3) = .127 pu.

$$FDH = 4/3\ FDL + I_{SC}$$

$$I_{SC} = \frac{V_2\ AV}{\frac{Z_{SC}\ (Z_{SR})}{Z_{SC} + Z_{SR}}} = \frac{V_2 - I_2\ (Cx)\ \frac{ZL}{2}}{\frac{Z_{SC}\ (Z_{SR})}{Z_{SC} + Z_{SR}}}$$

$$= \frac{V_{LN}\ (R_o(\phi G)) - I_2(C_x)Z_L/2}{\frac{Z_{SC}\ (Z_{SR})}{Z_{SC} + Z_{SR}}} = \frac{1\ (.246) - (.19)\ (.5)}{\frac{-6\ (8)}{-6+8}}$$

$$= \frac{.151}{-24} = .0063 \text{ pu.}$$

$$FDL = (.127 - .0063)\ 3/4 = .09 \text{ pu.}$$

If shunt reactors not included in protected zone

$$I_{SC} = \frac{V_2\ AV}{Z_{SC}} = \frac{.151}{-6} = .025 \text{ pu.}$$

$$FDL = (.127 - .025)\ 3/4 = .0765 \text{ pu.}$$

SELECTION OF K FACTOR

K = 10 is required for faults F2 and F3. K = 10 must therefore be used at both terminals.

SETTING OF FDM

$$FDM = \frac{V_2(AV)}{Z \text{ shunt}} + \frac{V_1(AV)}{K\ Z \text{ shunt}}$$

$$= \frac{.151}{-24} + \frac{1-.151}{10(-24)} \quad \text{(From FDL setting calculation)}$$

$$= .0063 + .0035$$

$$= .0098 \text{ pu. (Minimum)}$$

If shunt reactors not included in protected zone

$$FDM = \frac{V_2 \ (AV)}{Z \text{ shunt}} + \frac{V_1 \ (AV)}{K \ Z \text{ shunt}}$$

$$= \frac{.151}{-6} + \frac{.849}{-60} = .025 + .014$$

$$= .039 \text{ pu}$$

TESTING

GENERAL

The SLD42D relay will generally be supplied from the factory mounted and wired in a static relay with the associated SSA, SLYL12, test panel and CS26 carrier. The AC test inputs can conveniently be supplied to the SLD Network Unit by the insertion of an XLA test plug in the TDA test receptacle on the test panel.

The Logic Unit must be energized with the regulated 17 volt DC and bias outputs of the associated SSA to operate any of the functions or obtain trip or auxiliary outputs. Be certain that the output circuit connection plugs (TDB, TDC, TDD) are removed from any circuits connected to the power system prior to making any tests on the relay. The output of the positive and negative-sequence networks can be checked from J1 and J2 respectively to reference. The output signals from the various logic functions can be measured at the various test points in Logic Unit with respect to TP1 (reference). These signals will be from +5 to +15 volts for the ON condition and less than +1 volt for the OFF condition. These signals can be checked with an oscilloscope, the test panel voltmeter, or a portable high-impedance voltmeter. When the test panel voltmeter is used, its negative terminal will normally be connected to the logic reference. Therefore, it is only necessary to connect the panel voltmeter test jack (meter positive) to the desired test point and depress the voltmeter pushbutton to obtain a test reading. A dual-trace oscilloscope with calibrated horizontal sweep, and external triggering facility is recommended for checking or adjusting the various time delay cards such as phase delay (J), trip integrator (P), etc.

Caution: It is a design characteristic of most electronic instruments that one of the signal input terminals is connected to the instrument chassis. Since the SLD reference voltage, which normally will be connected to the ground input of the instrument, is near the (+) station battery voltage level, the instrument chassis must be insulated from station ground. If the instrument power cord contains a third lead, that lead must NOT be connected to station ground.

NETWORK BALANCE CHECK

The Network Unit circuits have been accurately preset at the factory to obtain positive-sequence cancellation in the negative-sequence network and negative-sequence cancellation in the positive-sequence network. No further adjustments should be required in the field. It is recommended, however, that the following checks be made at the time of installation to insure that nothing has occurred during shipment to upset the networks.

The basic circuit used in checking both networks is shown in Figure 21. This arrangement provides means of obtaining two test currents of equal magnitude but separated by 60°. Then by appropriate connections to the networks it is possible to simulate either a balanced 3-phase positive-sequence current (Figure 21B), or a balanced negative-sequence current (Figure 21C). During the following tests the basic current level in each branch will be 5 amps, and since these currents will add at a 60° angle, the total load in the Variac will be about 8.7 amps. It is desirable that the 110 volt scale of the phase angle meter be used to minimize the effect of this potential circuit on the relation between the two test currents. It is further desirable that the Variac be set near its maximum voltage output and that the load boxes be set to obtain approximately 5 amps as a preliminary step, since this will provide the greatest possible voltage to the phase angle meter and will insure the best possible accuracy.

a. Negative Sequence Network

To check the negative-sequence network for positive sequence cancellation, arrange a Type XLA test plug as shown in Figure 21B and connect the branch "A", branch "B", and common return leads as shown to simulate a balanced positive sequence input to the relay. This is accomplished by setting one current (branch "A") to lag a second equal current (branch "B") by 60° and by reversing the branch "B" current at the relay. Branch "A" current now simulates phase A relay current and reversed branch "B" current which lags branch "A" by 120°, simulates phase B relay current. Phase C current is not used in the negative sequence network.

The above mentioned phase notation assumes relay external connections corresponding to phase sequence A-B-C. For phase sequence C-B-A the external connections to the relay would be such that branch "A" test current would simulate phase C; and that the phase A current would not be involved in the negative sequence network.

The following procedure is suggested:

1. Adjust the branch "B" load box to obtain approximately 5 amps when the Variac is set for 110 volts.
2. Adjust the branch "A" load box until the phase angle meter indicates a 60° lag of current with respect to voltage.
3. Readjust the branch "B" load box until branch "A" and "B" currents are equal.
4. Adjust the Variac until both currents are 5 amps.
5. Touch up branch "A" load box for angle trimming and branch "B" load box for magnitude trimming.

Now jumper J1 (positive sequence network output) to REF. jack and connect an oscilloscope with its ground at the TP1 test point in the SLD Logic Unit and its vertical input at the J2 test jack on the Network Unit. Set the scope sensitivity to observe the waveform with readable deflection. This should be a distorted wave at system frequency. With perfectly balanced currents and a network which has been perfectly adjusted, the waveform observed at J2 should consist solely of harmonics (primarily third and fifth).

Since perfection is seldom realized, the branch "A" and branch "B" load boxes should now be touched up until the waveform contains no fundamental component, and then the Variac readjusted until the branch "B" current is again 5 amps. Branch "A" current should be 5 amps $\pm$ 0.5 amps, and the angle between the "A" and "B" currents should be $60^{\circ} \pm 3^{\circ}$. The peak-to-peak value of the network output, which now will consist solely of harmonics, will depend on the system, but should be on the order of a few tenths of a volt.

b. Positive Sequence Network

To check the positive-sequence network for negative-sequence cancellation, use the test plug arrangment and branch "A" and branch "B" connections shown in Figure 21C to simulate a balanced negative-sequence input to the relay. This is accomplished by the same scheme described in section (a) above, except that the reversed branch "B" current, which lags branch "A" current by 120°, now simulates the phase C relay current. Phase B current is not used in the positive-sequence network for phase sequence A-B-C.

Remove the jumper from J1 to REF., and place a jumper from J2 (negative sequence network output) to REF. Reconnect oscilloscope vertical input to J1. Follow the same procedure described in a.1 to a.5 above for obtaining the 5 ampere branch "A" and branch "B" currents separated by 60°. Trim the "A" and "B" currents and angle to eliminate the fundamental as described above. With the "B" current at 5 amps, "A" current should be 5 amps $\pm$ 0.5 amps, and the angle $60^{\circ} \pm 3^{\circ}$.

If the corrected phase angle meter readings and/or the corrected ammeter readings are outside the limits given above, a readjustment of the network should be considered. However, this should be done only after a thorough verification of the previous measurements. The factory adjustments were made with specialized equipment to obtain an accuracy of the current relationships within much tighter limits than those given above. Any readjustments should be attempted only under very carefully controlled conditions.

CT Phasing, Polarity, & Sequence Check

The following tests on CT phasing, polarity and sequence are desirable to assure that coordination between terminals will be realized, and are readily made when power line carrier is used as the pilot channel. The tests provide a means of checking that for phase sequence A-B-C, phase A CT is connected to the DA5-DA6 circuit of the network unit with the same polarity at both terminals, that phase B CT is similarly connected to the DA7-DA8 circuit, phase C CT to the DA9-DA10 circuit, and that the return current path for CT residual current is properly connected to DA3 and DA4. For phase sequence C-B-A, the phase C CT will connect to DA5-DA6, and phase A CT to DA9-DA10. The carrier channel is used to communicate phase angle information between terminals.

In order to make the test it is necessary that load current be flowing in the line. The magnitude of the load current should be at least five times the single-end-feed line charging current to assure readable through-fault current relationships. If charging current is too high relative to load current, the phase difference between currents at the two ends will make it difficult to interpret correctly the results of the following tests. In the following tests load current in each phase is used independently to simulate a corresponding line to ground fault.

Since the carrier pilot channel is used in this test, it is necessary that the simulated phase-to-ground fault current be above the FDL level detector operating point, so that the FDL, and squaring amplifier in the SLD, will initiate the transmission of carrier Rf on alternate half-cycles offault current (i.e., half-cycle on, half-cycle off). The FDL and FDM level detectors are set at 0.2 amps negative sequence at the factory.

For a simulated phase-to-ground fault the negative-sequence component is one-third the line current. Therefore, it is necessary that the secondary load current be at least 3 x 0.2 amps, or 0.6 amps. If load current exceeds this value, the low-set level detectors (FDL and FDM) should both operate and the squaring amplifier will have a nearly symmetrical output.

The test plug connections in Figure 22A, 22B, and 22C will yield the correct line-to-ground current flow in the Network Unit for phase A, phase B, or phase C CT tests respectively. To obtain a current in the CT residual circuit for checking polarity of connections, it will be necessary to bypass one phase current around the network residual current windings temporarily. If the DA3, DA6, DA8 and DA10 points in the Network Unit connect directly to the relay neutral point, then the phase C current can be safely bypassed as shown in the CT residual test diagram in Figure 22D.

If the DA points do not connect directly to the relay wye point, then the test connections in Figure 22D can be used only if the phase C current can be safely interrupted and the residual current increased to load magnitude in other relays which may be interposed between the DA block and the wye point. (Note that above phase notations refer to phase sequence A-B-C).

The required procedure is outlined below:

1. Connect a Type XLA test plug in accordance with Figure 22A at each terminal of the protected line.

2. Connect the vertical input of a scope to the Rf jack of the CS26 carrier receiver and the ground input of the scope to the carrier chassis.

3. Now insert the test plug into the TDA test receptacle at each end of the line. This will simulate a phase A to ground through fault.

4. Two levels of carrier Rf should be observed on the scope, the higher from the local transmitter and the lower from the remote transmitter. The two levels of carrier should adjoin each other every half-cycle with a dead space between of not more than one-sixth of a half-cycle (30°). While the width of this dead zone between adjacent blocks of carrier Rf is not rigidly limited, it must be small enough to establish that it has not resulted from a CT phasing error. The higher amplitude Rf duration is very close to one-half cycle long and may be used as a time reference.

Repeat the above steps for each of the phase and ground test plug connections. If the results of each test are satisfactory, it indicates that CT phasing and polarity are correct. If the carrier signals do not intermesh properly the connections between the Network Units and CTs, or the phasing of CTs at opposite terminals, should be investigated.

With CT polarity and phasing established, check that the phase sequence is correct by observing the voltage between jack J2 on the network unit and SLD reference (TP1). If the sequence is not correct, the load current will appear as negative-phase-sequence current to the negative sequence network and the output voltage at J2 will be sinusoidal and have an amplitude of approximately 5 times the secondary load current. With correct phase sequence the waveform at J2 will contain a much lower fundamental component and will contain a large percentage of harmonic components.

LEVEL DETECTOR ADJUSTMENT

The following paragraphs cover the checking and adjustment of FDL, FDH, and FDM level detector cards. These level detectors are set at the factory for the minimum pick up point in the published range. The pick up level is increased by turning the card adjusting screw clockwise. The output of each level detector is a continuous positive DC signal measured at the test points shown in the following table:

Function	Test Point	Card	Factory Setting	
			Ø-Ø Test Amps	Equiv.Neg. Seq. Amps
FDL	TP8	AJ	0.35	0.2
FDH	TP7	M	0.87	0.5
FDM	TP4	G	0.35	0.2

FDL, FDH, and FDM should now be set at the operating points determined in the section on CALCULATION OF SETTINGS. The test circuit of Fig. 23 may be used to obtain the proper adjustable test input to simulate ØA-ØB current.

Since FDM responds to both positive and negative sequence, the positive sequence network must be shorted out by jumpering J1 to REF. when making a negative sequence FDM pickup test. Similarly, the negative sequence network should be shorted out by jumpering the J2 to REF. to check the positive operating point of FDM. Be sure that the K tap is in the proper position when checking the positive sequence FDM pickup.

TRANSMITTER DRIVE SYMMETRY SETTING

This adjustment of the transmitter drive symmetry card (AL) refines the duration of the transmitter blocking output at one terminal to produce equal half-cycles of receiver output at the remote terminal. This adjustment compensates for asymmetry in the half-cycle blocking signal which may be introduced by the receiver tuned circuit. Since this adjustment depends on operating conditions in service, it cannot be made at the factory. Before this adjustment is made it is essential that the carrier sets at both terminals be adjusted as prescribed in the INSTALLATION section of the carrier set Instruction Book. This will insure that the symmetry card settings will be made with receiver gain and attenuator settings at the levels which will be experienced when the equipment is in service.

Assume that the protected line section is A-B with A the local terminal and B remote. At station B connect a scope to observe the received blocking signal at TP5. Supply the network unit at station A with phase-to-phase test current using the connections shown in Figure 23. Raise the test current to about 90% of the FDH operating point so as to operate FDL but not FDH. This will cause the carrier set at station A to transmit carrier pulses of approximately half-cycle duration.

At station B set the scope horizontal sweep so that one full cycle is spread across the screen and observe the duration of the "block"(positive) and "non-block" (zero) half-cycle. At station A adjust blocking transmission time by means of the screw adjustment of the T16 symmetry card (AL)

so that the "block" and "non-block" half-cycle at station B are exactly equal. Clockwise rotation of the adjusting screw increases the "non-block" half-cycle. Be sure that the red tap lead on the T16 card is in the "S" position. It is necessary to withdraw the card to see this lead.

The carrier integrator (L) card is set at the factory for 2 milliseconds pickup and 2 milliseconds dropout time. This adjustment can be checked or reset, if required, at station B at this time. This can be done by connecting the second channel of a dual trace scope at station B to TP2, and comparing the TP2 signal to the TP5 signal to see that the proper delay in the received carrier signal exists. Be certain that the carrier integrator output at TP2 has symmetrical on-off times.

The symmetry card at station B must also be adjusted to produce equal "block" and "non-block" half-cycles at station A. This should be done after the sequence networks and level detector checks have been made at B, and after the carrier set installation checkout is completed. The received carrier integrator (L) card at A should also be checked at this time as described above. On multi-terminal lines, when adjusting the symmetry at a given station, observe the receiver output at the nearest remote station.

Phase Delay Adjustment

The object of this adjustment is to set the local trip half-cycle (TP11), which is applied to the comparer, so that it is in phase with the received blocking half-cycle (TP2) which results from transmission of carrier from the remote terminal during a through fault. This adjustment is necessary to compensate for such things as channel delay introduced by the receiver filters and propagation time in the line, the shift in the leading edge of the transmitted signal by the transmitter drive symmetry card and the received carrier integration time of the (L) card. Since the phase delay setting is affected by service conditions, it cannot be made at the factory.

Three possible methods of making the phase delay adjustment are listed below with the limiting conditions shown:

a. Load Current Method

In this test load current in the line is used to simulate negative-sequence current. It is necessary that the secondary load current be greater than the negative-sequence current settings of the FDL fault detector, or that load current be at least equal to the minimum available setting of FDL, which is 0.2A (negative sequence) in which case it will be necessary to temporarily reduce the FDL setting to its minimum value. If this method is to produce an accurate setting, it is also necessary that the ratio of line charging current to through load current be low enough so that the phase displacement between currents at the two ends of the line does not exceed 10 degrees.

If these conditions are met, the procedure outlined below should be followed. If the conditions are not met, it will be necessary to use one of the alternate schemes described in (b) or (c):

At each terminal prepare test plugs with connections as shown in Figure 24. This will cause phase A current to flow in phase B relay coils and vice versa, thereby making balanced load current appear as negative-sequence current to the relay.

If necessary, reduce the operating point of the FDL level detector to 0.2 amps negative sequence (0.35 amps phase-to-phase test current) following the procedure described in the LEVEL DETECTOR ADJUSTMENT section.

At Station A (local) remove AND44 (the L18 card in pos. D), and then connect a 3.3 K resistor from TP19 to +16.8 V at TP20. This will prevent the local transmission of carrier.

At Station B (remote), jumper TP19 to TP1 to prevent a trip output from stopping carrier transmission from that end. Be certain that the output connection plugs (TDB, TDC, TDE) are still removed at both stations.

Using a dual trace scope at Station A, connect trace A vertical input to TP2, trace B vertical input to TP11, and scope ground to TP1. Now insert the test plugs into the TDA test receptacle at each terminal of the protected line. A half-cycle blocking signal (equal "block" and equal "non-block" duration) should appear on trace A as the result of transmission from Station B. The local tripping signal should appear on trace B. The "on" and "off" durations of this half-cycle tripping signal should be very nearly equal, but the tripping signal (trace B) probably will not line up with the received blocking signal (trace A) since this adjustment depends on characteristics of individual receiver filters and must be made under service conditions.

Two adjustments are provided on the phase delay card (T25, pos. J) to bring the tripping signal (TP11) in line with the blocking signal (TP2). The R_1 pot (adjacent to the card) controls the leading edge and the R_2 pot (away from the card) controls the trailing edge of the TP11 signal. Adjust these two pots on the "J" card so that the positive half-cycle of the tripping signal (TP11) lines up with the positive half-cycle of the blocking signal (TP2).

After the phase delay adjustment is completed remove the Type XLA test plugs at both terminals, remove the 3.3 K resistor from TP19 to TP20 at Station A and remove the TP19 to TP1 jumper at Station B.

b. Test Source Method

If the line is not loaded, is carrying insufficient load, or if the ratio of charging current to load current is too high, an AC test

source can be used at each station to operate FDL and FDM, provided the sources are in phase. Use the test connections shown in Figure 23 at Station A, and similar connections at Station B except interchange the connections to relay points 5 and 7 of the test plug. This will simulate a through fault.

Before proceeding with phase delay adjustments, the phase relation of the two test sources should be checked via the carrier channel. With the test plugs inserted at each terminal of the line raise the test current to approximately 90% of the FDH operating point so that FDL will operate but not FDH. At the local terminal connect the vertical input of the scope to the Rf jack of the carrier receiver and the scope ground to the carrier chassis. Two levels of Rf should be observed on the scope, the higher from the local transmitter and the lower from the remote transmitter. If the two test sources are substantially in phase, the two levels of carrier Rf should adjoin each other every half-cycle with very little dead space or overlap between adjacent levels of carrier. For the phase delay adjustment to have any value, the dead space or overlap should not exceed 10°.

The AC source for the test connections of Figure 23 will usually be station service AC, and on long-line applications it will usually be found that the test sources are displaced by too great an angle to be of any use for the installation adjustment of the phase delay.

If at least one of the stations of the protected line is equipped with line-side potential devices or transformers it is possible that substantially in-phase test sources can be obtained at the two ends by supplying the test circuit of Figure 23 from the potential device or transformer and operating the line with the breaker at one end open. The open end is, of course, the location where line-side potential is available. With this arrangement the voltages at the two ends will differ only by the drop in the line inductive reactance caused by the line capacitive charging current, and this will primarily be a magnitude difference. It is, of course, essential that the normal installation adjustments be made on the potential devices prior to this test.

Having obtained AC test sources that are substantially in phase, proceed to adjust the phase delay settings as described in section a above, using a dual-trace scope.

c. Local Signal Method

If neither the (a) or (b) adjustment method can be used, an adjustment of the phase delay can be made on the basis of the local keyed-carrier signal. This method assumes that the carrier receiver gain control and attentuator have been set to provide the normal margin above the cutoff point of the signal received from the remote transmitter, as recommended in the carrier equipment instruction book.

The AC test circuit of Figure 23 will be used. First cause the local transmitter to send a full-strength Rf signal by turning the carrier test switch (CTS on test panel) to SEND. Observe and record where receiver attentuator is set, and then turn the receiver attenuator

in a clockwise direction until the cutoff point is reached (SA relay will dropout and white lamp on relay test panel goes out). Now turn attenuator back to provide the normal margin (as noted in the previous paragraph) from this cutoff point, as determined by the attenuator dial markings. Presumably with this attenuator setting the local transmitter will drive the local receiver at approximately the same level as the Rf signal received from the remote terminal would drive it with installation settings of the transmitter and receiver.

Now raise the test current (Figure 23) to about 90% of FDH pickup. Connect scope channel A to the Rf jack, channel B to TP2 and scope ground to relay REF at TP1 and observe the signals shown in the top two traces of Figure 25. The TP2 signal should be very close to equal "ON" and "OFF" times since the conditions are very close to those for which the symmetry setting was made.

Now shift channel A input to TP11 and set the phase delay card adjustments so that the local trip signal on the comparer (TP11) lines up with the "OFF" time of the B trace (TP2).

This adjustment method neglects propagation time of the carrier signal between the two terminals which is 1 millisecond for 186 miles of line. The setting can be further refined for long lines by calculating the theoretical propagation time for the line and shifting the trip signal (TP11) to the right (delayed) by a time interval equivalent to this propagation time.

After the setting is complete reset the attenuator at its original position as recorded at the start of this test. Remove the test plug and replace the TDA connection plug.

Trip Integrator Time Check

The trip integrator card (P) has been adjusted at the factory to provide a delay of 3 milliseconds between comparer output and trip integrator output, and sufficient delay on release so that once an output is produced it will be continuous with half-cycle repetitive input.

The purpose of the trip integrator card is to insure that tripping does not occur on extraneous spikes of comparer output which may result from transient voltages, network mismatch, phase delay mismatch, or CT errors. Adjustment of the trip integrator time is not considered to be part of the normal installation procedure. However, a check on the integration time may be desirable at the time of installation to be sure that unintentional changes have not occurred.

In the field a quick check of the trip integrator may be made by using a scope with a calibrated time base and an external sweep trigger. Connect the trigger input to TP14. Connect the vertical input to trip integrator output at TP15 and scope ground to SLD reference. Set the scope for calibrated sweep with a sweep rate of 1 millisecond per centimeter, positive slope trigger. Connect a 3.3 K resistor from TP9 to TP20 and remove (AK) to simulate a continuous keying input to the comparer.

Now push the Carrier Trip button in the SLD Logic Unit and observe the trace as it sweeps across the scope screen. The vertical deflection should occur at the 3 millisecond point (± 0.3 M.S.). The operating delay can be adjusted by means of R_1 which is the rheostat next to the (P) card.

To check the release time trigger control to negative slope and sweep to 5 ms/cm. Trace should now sweep when "carrier trip" button is released and output at TP15 should step from 5-8 volts to zero volts in 18 ms ± 1 ms. Release time is controlled by R_2 (outer) pot and normally should not require field adjustment.

RB Logic

The RB transient blocking logic (AND 43 and 25/40) is designed to operate and block phase comparison tripping at AND 44 if a fault detector operation (either FDH, or MT) is not followed by a comparer and trip integrator output within a set time of 25 milliseconds. Once established, the RB circuit will maintain blocking at AND 44 for the duration of its release time, 40 milliseconds.

The operation of the RB function can be checked in the field as follows: Jumper TP15 to REF. (TP1 or REF. jack). Using a scope with a calibrated time base and an external sweep trigger, connect trigger input to TP12, vertical input to TP13, and scope ground to SLD Ref. at TP1. Use positive slope triggering and 5 ms/cm sweep. Push the "Channel Trip" button in the SLD logic unit and observe the trace as it sweeps across the screen. The vertical deflection should occur at the 25 millisecond point (± 2 ms).

The RB 40 millisecond dropout time can be checked by resetting the scope trigger (TP12) to negative trigger on negative slope and initiating RB dropout by releasing the Channel Trip push button. The dropout time should be 40 milliseconds ± 2 millisecond. The 25/40 dropout time is controlled by the outer (away from the card) adjustment. Remove the jumper from TP15 to REF. when RB tests are completed.

Pulse Stretcher Checks

The fault detector pulse stretchers can be checked using the Channel Trip push button and a triggered sweep on the oscilloscope. The FDH pulse stretcher (AF) is normally set for 70 milliseconds ± 5 milliseconds. This can be done by connecting the oscilloscope trigger (negative slope) to pin 5 of the (AF) card using the Card Adapter, and the vertical input to TP17. The dropout time of the pulse stretcher can be measured from as the time from the beginning of the sweep until the vertical output (TP17) goes to zero when the Channel Trip push button is released. The FDL pulse stretcher (F) is normally set for 100 milliseconds ± 5 milliseconds. This can be checked using the same procedure, except the oscilloscope trigger is connected to pin 5 of the F card and the vertical input is connected to TP18.

G4 TRIP LEVEL ADJUSTMENT

The G4 pick up level can be checked and adjusted using the test circuit of Fig. 23, except the test current leads should be connected to relay side

studs 3 and 4 instead of studs 5 and 7. Be sure that the G4 link in the Logic Unit is in the IN position, and connect an oscilloscope or voltmeter from TP6 to TP1. The G4 (AR) operation on gradually increasing current gives a continuous approximately 9-12 volt DC signal at TP6. The pick up level can be adjusted by means of the adjusting screw on the AR card (clockwise rotation increases the pick up level).

OUTPUT CHECKS

The SCR trip circuit operation can be checked by connecting a self-interrupting auxiliary relay such as the G.E. type HEA lockout relay connected by means of XLA test plugs. The G4 input circuit above can be used to check the DB2 (+) to DC2 SCR trip circuit. When the test current is increased to the G4 operating point the SCR should operate the test auxiliary trip relay, the T1 (L.H.) target, and the I target lamp. The BFI and RI auxiliary relay contacts should also close (this can be checked at the XLA test plugs using an ohmmeter or continuity lamp). The DB3 (+) to DC3 SCR trip circuit and and T2 (R.H.) target can be checked in the same manner.

A phase comparison trip test can be made by reconnecting the AC input test circuit of Fig. 23 (test current through studs 5-7 at the XLA), and increasing the current to the FDH pick up level. This will produce a phase comparison trip in the absence of a received blocking signal. The operation of the SCR, target, BFI, and RI will be the same as that described for the G4 trips except that the C target lamp will light instead of the I lamp.

The operation of the OS and RC (if used) auxiliary relay outputs can be checked by supplying the necessary signals from the associated SLYL12 relay.

A trip of the associated breaker or breakers should also be made if possible. This can be done by disconnecting all test circuits and replacing all relay connection plugs, and operating the INST. TRIP pushbutton. Test tripping of the breakers using the CHANNEL TRIP pushbutton can be accomplished if the line current is above FDM pick up.

MAINTENANCE

PERIODIC TESTS

During a periodic check of the equipment the FDL, FDH, and FDM level detector operating points should be checked against the settings made at the time of installation, using the phase-to-phase AC test circuit of Fig. 23. The G4 operating point should also be checked against its original setting using the test circuit described in the TESTING section. The trip and auxiliary relay outputs and targets should also be checked at this time. The SCR trip circuits and series targets may be checked by the use of a test HEA connected through an XLA test plug as described previously in the TESTING section. The operation of the auxiliary telephone relays can be checked with an ohmmeter via the XLA test plug as previous described.

The CS26 carrier output should be checked to be sure that operation of FDL and FDM does produce the expected modulated RF output. Any check of the transmitter drive symmetry or phase delay adjustments requires operators at both terminals of the line, and should not require checking during normal periodic test programs.

TROUBLE SHOOTING

In trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram (similar to Fig. 8) contains the combined logic diagrams of the SLD42D relay and all other associated relays, and the various test points in each unit. By signal tracing using the applicable overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

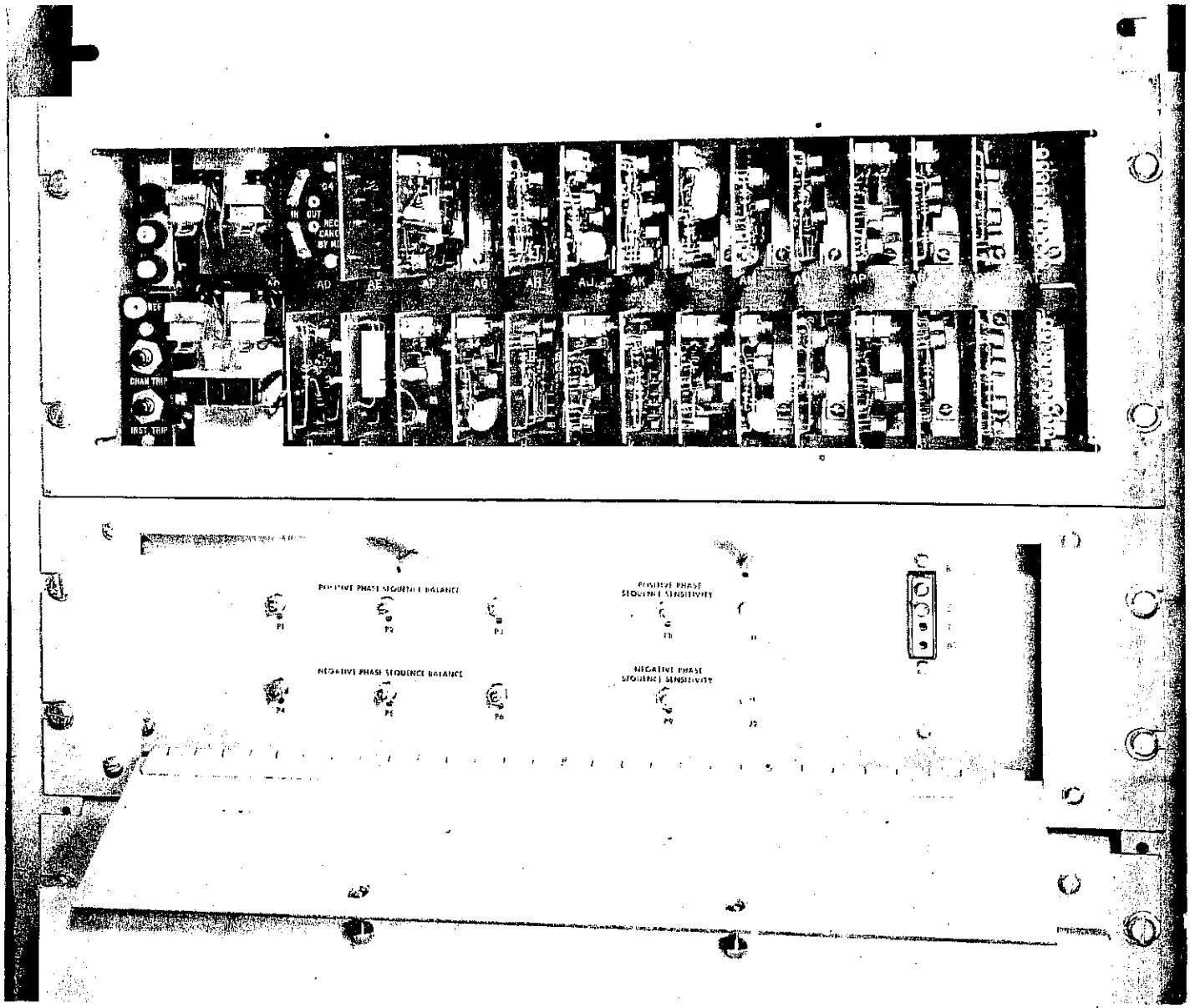
A Test Adapter Card, 0128B2221G1, is supplied with each static relay equipment to supplement the pre-wired test points on the test card. This adapter can be plugged into any card position, and then the logic card for that address can in turn be plugged into the adapter. The unit test card can then be plugged into the second socket in the adapter, giving access to all ten connection points by instrument jacks while the logic card is operating in the circuit. The connections to each pin on the adapter logic card socket are individually removable to allow circuit wiring changes to the logic card during trouble shooting.

An oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace scope with a calibrated sweep is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to repair damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. A list of the types of cards is shown in Fig. 5. The complete wiring diagrams and component values for these cards are shown in Fig. 26A through 26S.

FIG. 1



TYPE SLD42D RELAY

CODE D | GENERAL ELECTRIC | 0165A7754

CONT ON SHEET | SH NO.

0165A7754

CONT ON SHEET | SH NO.

TITLE

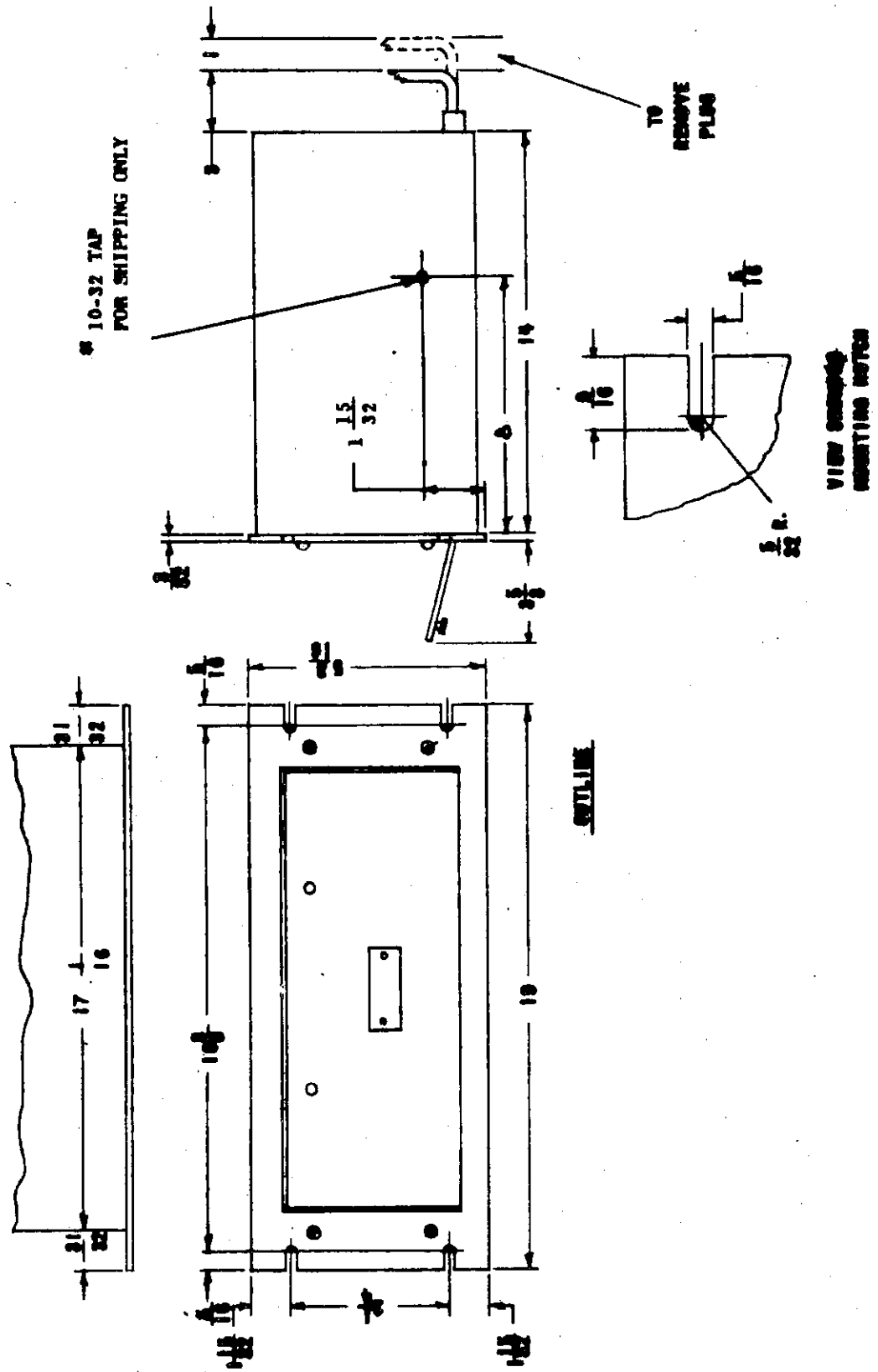
OUTLINE & MOUNTING DIMENSIONS

FIRST MADE FOR 8 BANK UNIT (TAP BLOCK)

FIG-2

REVISIONS

1	JAN 28 '64	JAN 4-64
2		
3		
4		



PRINTS TO

MADE BY R Bechtold DEC. 10, 1963

ISSUED DEC. 19 1963

APPROVALS

L.V. SWITCHGEAR — DIV OR DEPT.

PHILADELPHIA — LOCATION

0165A7754

CONT ON SHEET | SH NO.

CODE IDENT NO.

CODE. A

GENERAL ELECTRIC

0203A8630
CONT ON SHEET SH NO.

REV NO. O

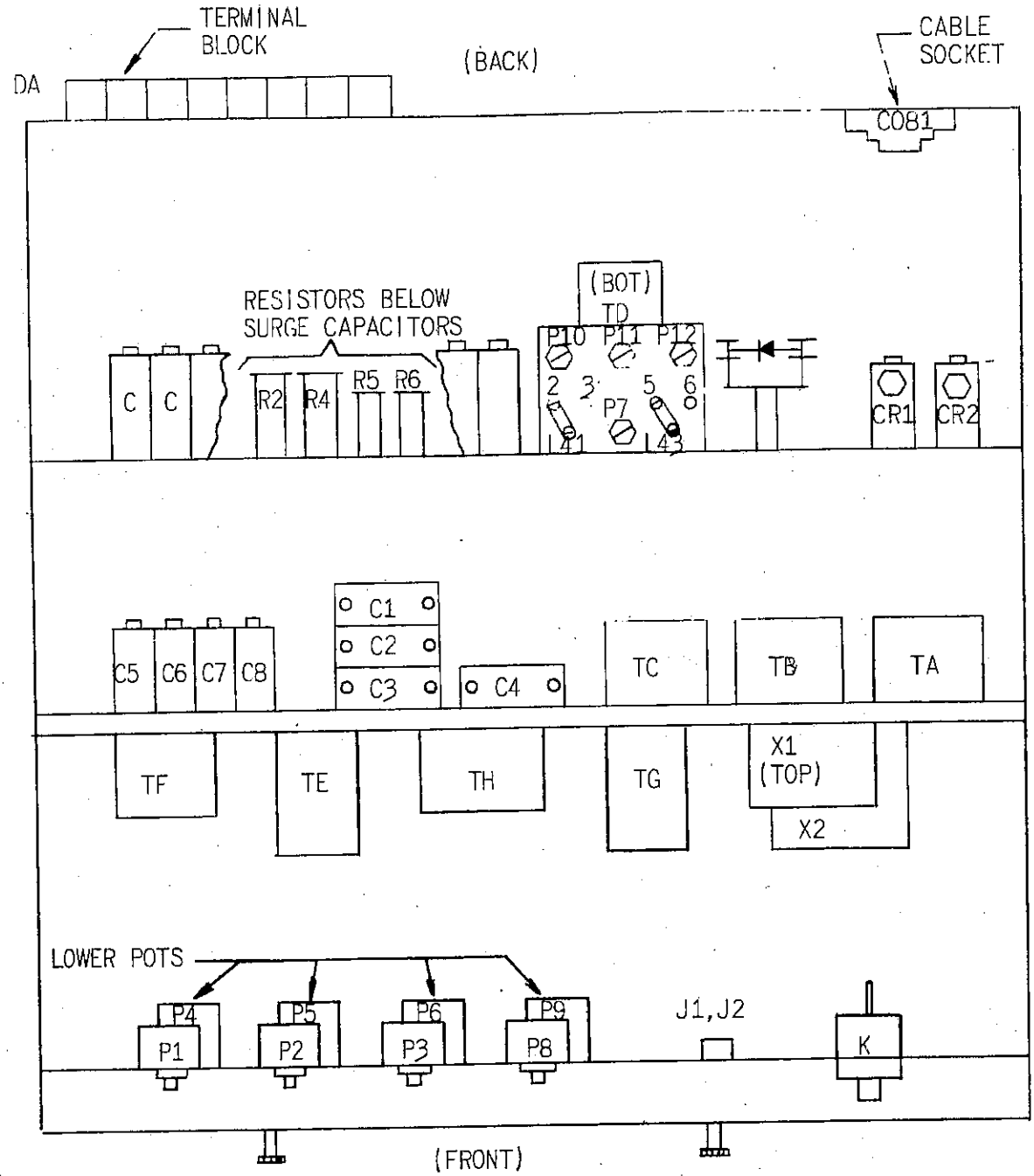
0203A8630
CONT ON SHEET SH NO.

TITLE
LOCATION OF COMPONENTS
TYPE SLD42D NETWORK UNIT
FIRST MADE FOR GEK-6877

FIG. - 3

REVISIONS

- TOP VIEW -
WITH TOP COVER REMOVED
REFER TO INTERNAL CONNECTIONS 0137B9621 (FIG. 14)



NOTE: EACH MTG. PLATE MAY BE REMOVED AS SEPARATE SUB-ASM., WITHOUT DISCONNECTING LEADS, BY REMOVING FOUR MTG. SCREWS. TRANSFORMERS WITH TERMINAL STRIPS HAVE COIL LEAD TERM. NUMBERED FROM LEFT TO RIGHT (FACING TERMINALS).

PRINTS TO

MADE BY A. Gilbert DEC. 9, '66
ISSUED D. 97 1611

APPROVALS K.P.

SWGR. PHILA.
DIV OR DEPT.
LOCATION

0203A8630
CONT ON SHEET SH NO.

CODE D

GENERAL ELECTRIC

0165A7662

CONT ON SHEET SH NO

REV NO. -1-2-3-

0165A7662

CONT ON SHEET SH NO.

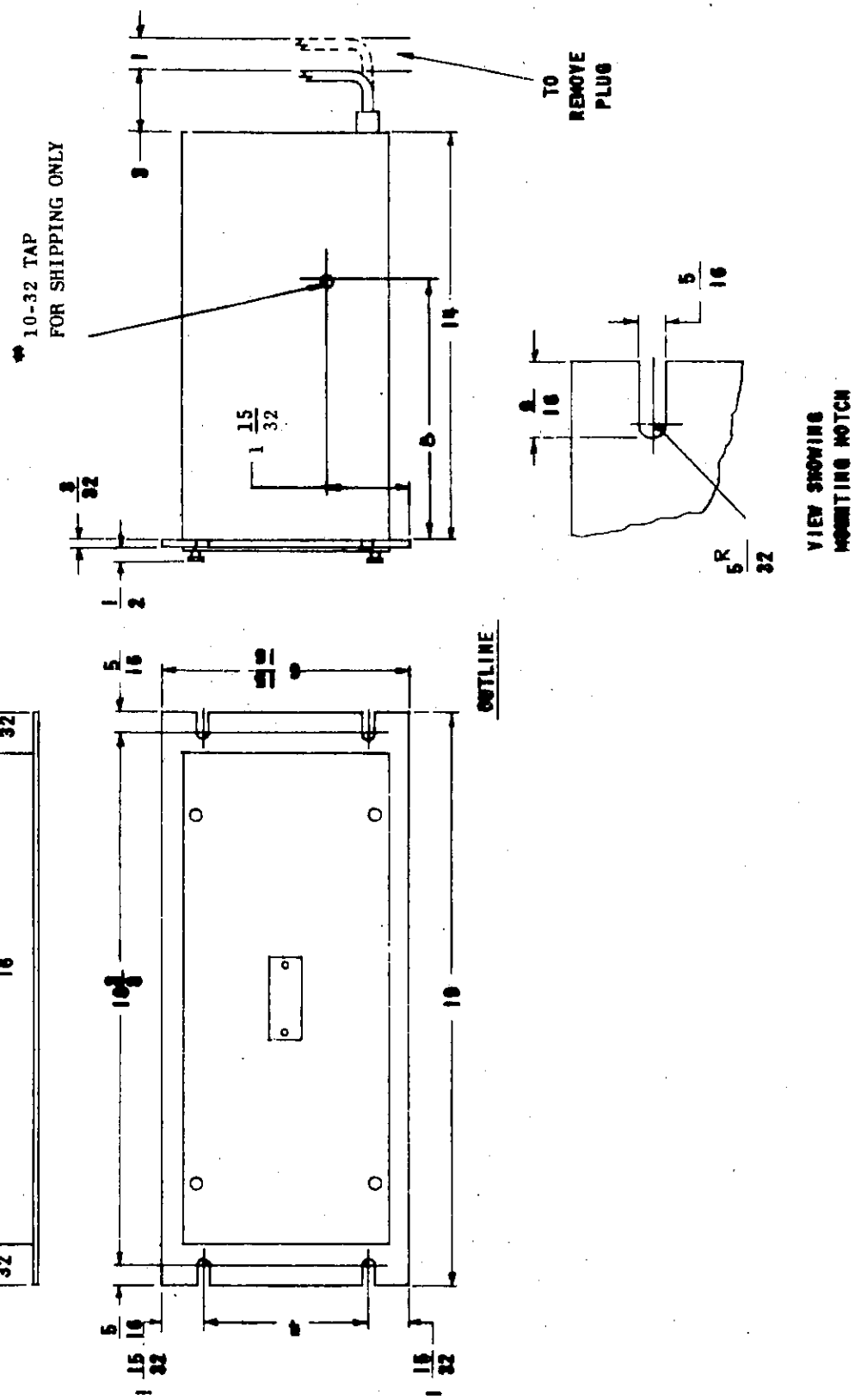
TITLE

OUTLINE & MOUNTING DIMENSIONS

FIRST MADE FOR 4 RACK UNIT (LOGIC)

FIG. 4

REVISIONS



PRINTS TO

MADE BY R Bechtold JUNE 27, 1963

ISSUED July 12, 1963

APPROVALS

L.V. SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0165A7662

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GENERAL ELECTRIC

0203A8629

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0203A8629

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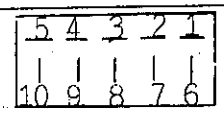
TITLE

LOCATION OF COMPONENTS
TYPE SLD42D LOGIC UNIT

FIG-5

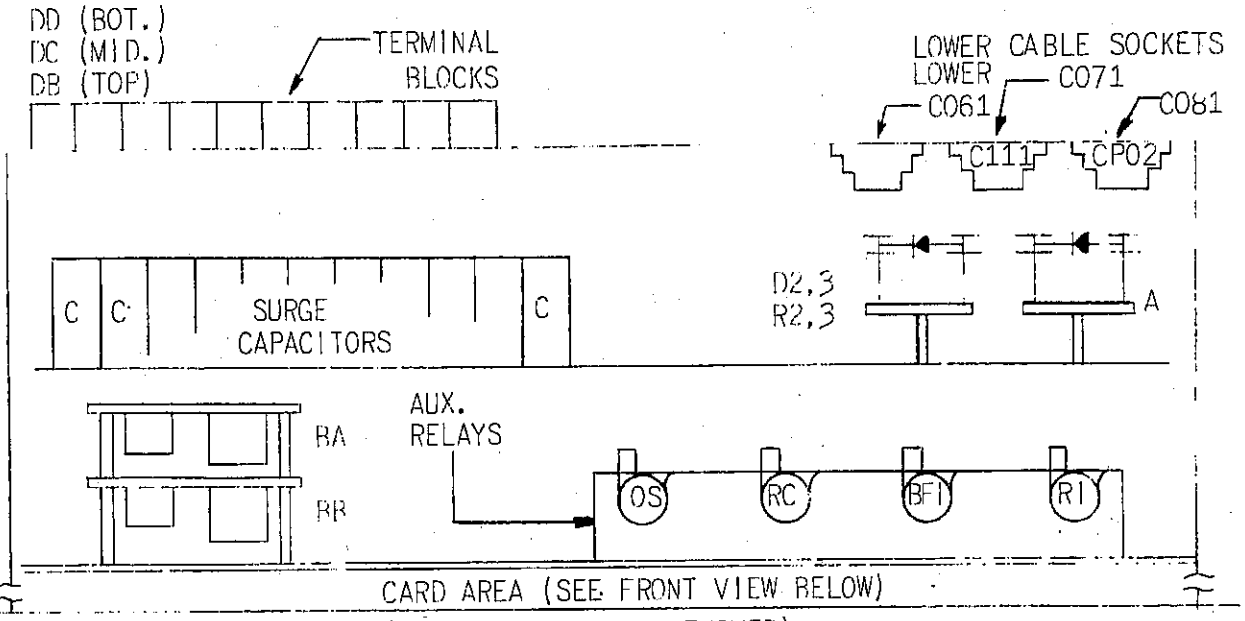
FIRST MADE FOR GEK-6877

REFER TO INTERNAL CONNS. 0137B9622 FIG.-1

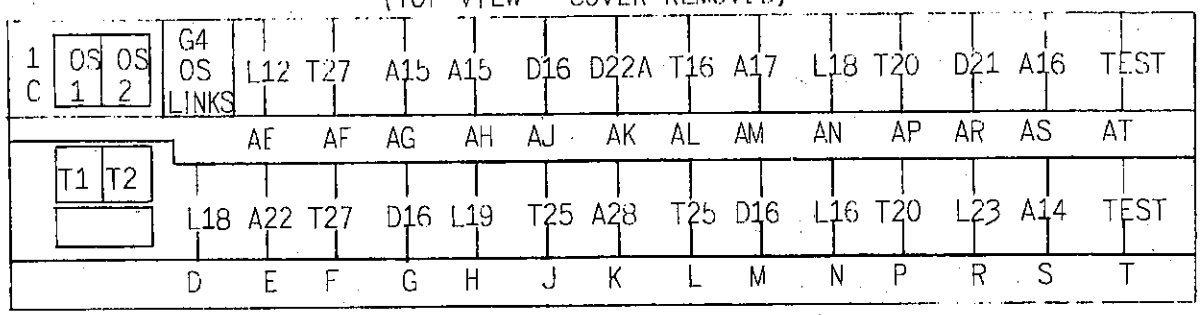


PIN. NOS.

REVISIONS



(TOP VIEW – COVER REMOVED)



(FRONT VIEW – COVER REMOVED)

PRINTED CIRCUIT CARDS

TYPE	CAT. NUMBER	FUNCTION	FIGURE
A14	0127B8192 G1	2 - SCR DRIVERS	A
A15	0127B8194 G2	2 - TARGET DRIVERS	B
A16	0127B8196 G1	2 - RELAY DRIVERS	C
A17	0127B8111 G1	CARRIER CONTROL	D
A22	0128B2248 G1	CONTACT CONVERTER,	E
A28	0137B8389 G1	2 - RELAY DRIVERS	F
D16	0127B8131 G1	LEVEL DETECTOR	G
D21	0128B2286 G1	DIRECT TRIP LEVEL DET.	H
D22A	0137B8309 G2	SQUARING AMPLIFIER	I
L12	0127B8159 G1	2-OR, 2-OR, 2 DIODES	J
L16	0128B2239 G1	COMPARER	K
L18	0127B8117 G1	2 AND WITH NOT	L
L19	0128B2208 G1	2 OR	M
L23	0127B8437 G1	500 M.S. DELAY TIMER	N
T16	0127B8147 G1	SYMMETRY ADJUST	P
T20	0128B2241 G1	TIME DELAY P.U. & D.O.	Q
T25	0137B8313 G1	PHASE DELAY TIMER	R
T27	0137B8356 G1	PULSE STRETCHER	S

PRINTS TO

MADE BY H White 12-15-66

ISSUED Dec 27 1966

APPROVALS

SWGR. DIV OR DEPT.

PHILA. LOCATION

0203A8629

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GENERAL ELECTRIC

0178A5813

CONT ON SHEET SH NO.

REV NO. -2

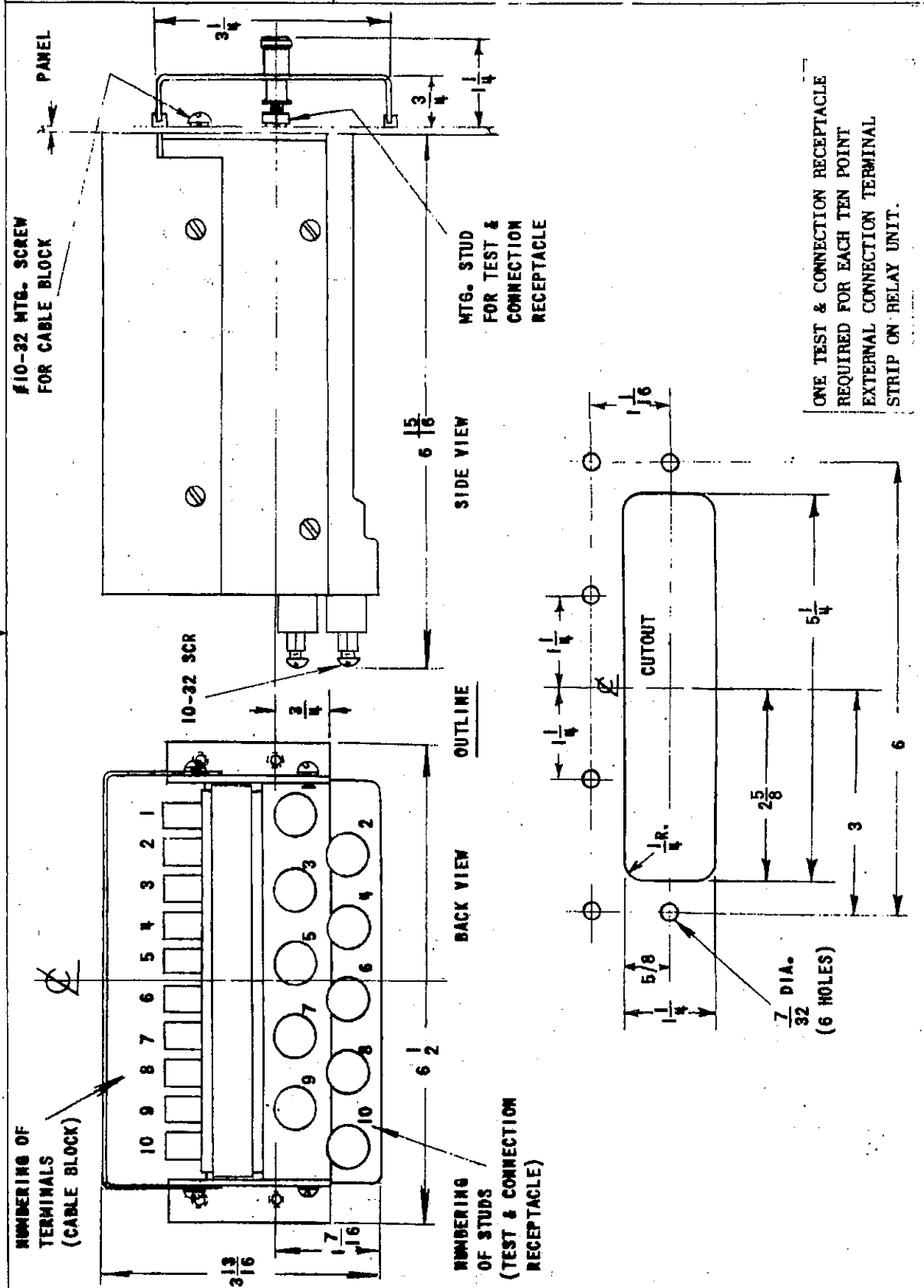
0178A5813

CONT ON SHEET SH NO.

TITLE
OUTLINE & PANEL DRILLING
FOR TEST & CONNECTION RECEPTACLE
FIRST MADE FOR STATIC RELAYS

FIG-6

REVISIONS



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MADE BY J. Connor Feb 7 1964

ISSUED Feb 24 1964

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

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0203A8627
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0203A8627
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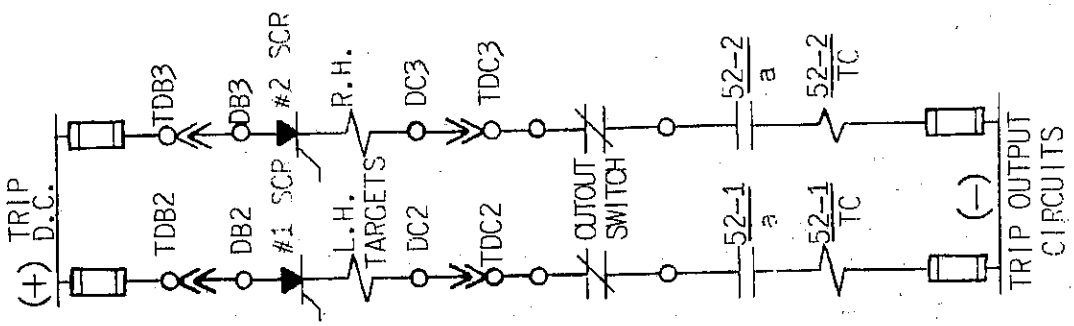
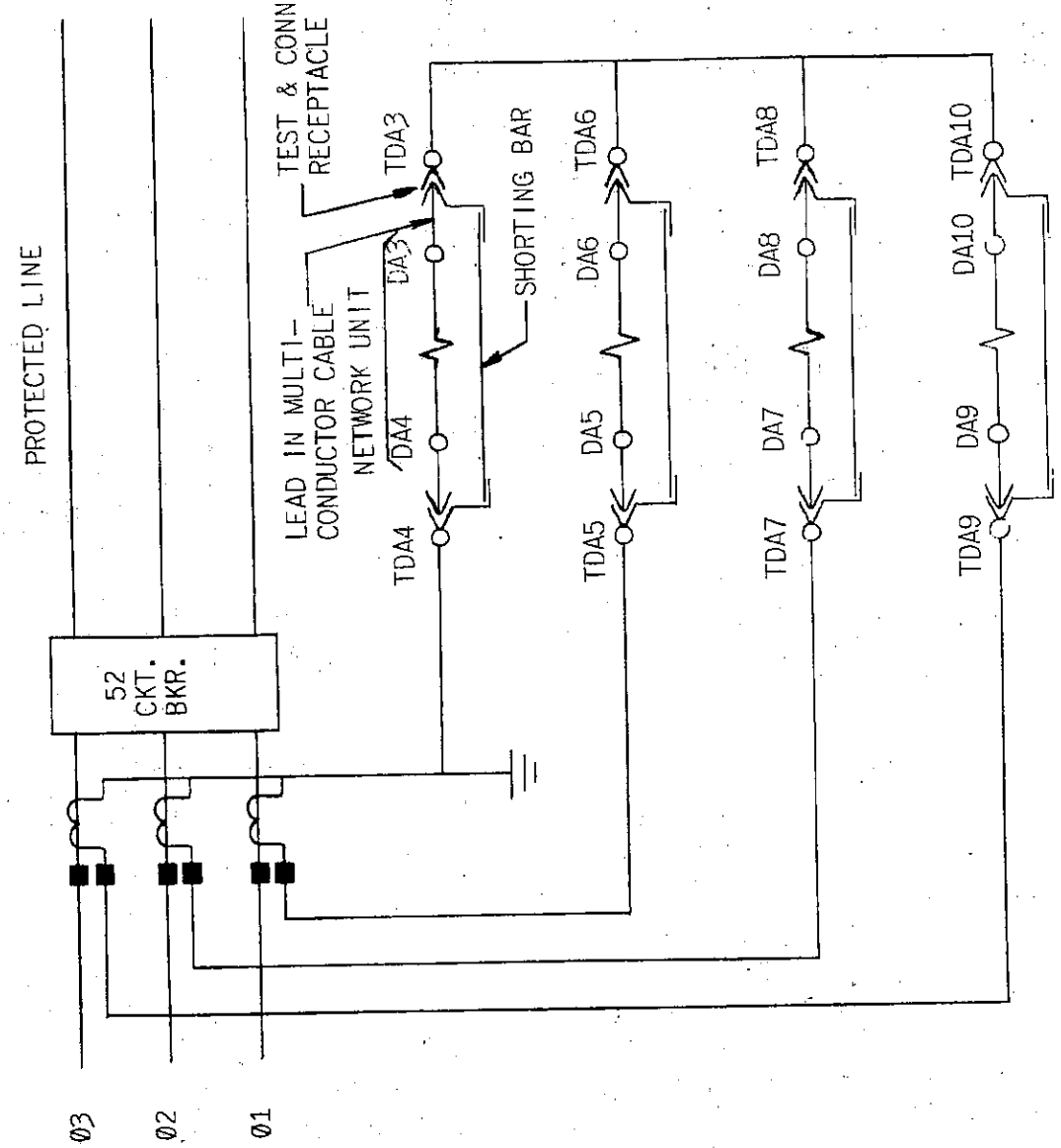
TITLE
TYPICAL EXTERNAL CONNECTIONS
TYPE SLD42D RELAY
FIRST MADE FOR GEK-6877

FIG. - 7

REVISIONS





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APPROVALS Rdp

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LOCATION

0203A8627
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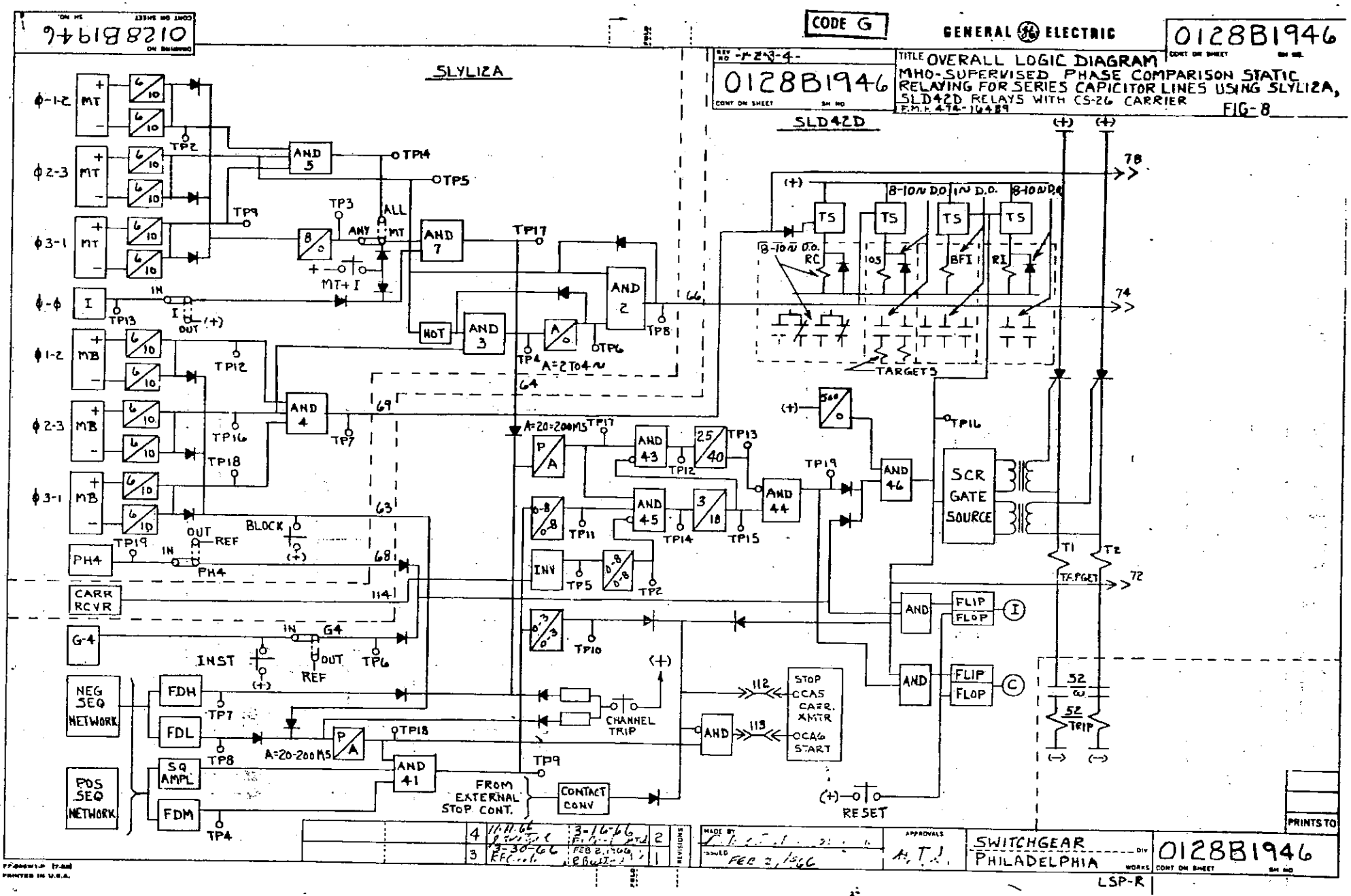
0128B1946
CODE G
GENERAL ELECTRIC
0128B1946
TITLE OVERALL LOGIC DIAGRAM
MHO-SUPERVISED PHASE COMPARISON STATIC RELAYING FOR SERIES CAPACITOR LINES USING SLYLIZA, SLD42D RELAYS WITH CS-26 CARRIER
E.M.F. 474-16489
FIG-8
SLYLIZA
SLD42D
φ-1-2
φ2-3
φ3-1
φ-φ
MT
MB
I
PH4
CARR RCVR
G-4
NEG SEQ NETWORK
POS SEQ NETWORK
FDH
FDL
FDM
SQ AMPL
AND 5
AND 7
AND 2
AND 3
AND 4
AND 41
AND 43
AND 45
AND 44
AND 46
NOT
INV
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
ANY
ALL
MT+I
IN
OUT
REF
BLOCK
INST
A=2 TO 4 MS
A=20-200 MS
CHANNEL TRIP
FROM EXTERNAL STOP CONT.
CONTACT CONV
RESET
STOP CCAS CARR. XMTR
CCAG START
8-10 M D.O.
RC
TS
105
BFI
RI
TARGETS
SCR GATE SOURCE
T1
T2
TARGET
FLIP FLOP
52 a
52 TRIP
78
74
72
66
64
63
68
69
114
112
113
PRINTS TO
SWITCHGEAR
PHILADELPHIA
Div
Works
0128B1946
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A. T. L.
ISSUED FEB 2, 1966
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3-16-66
FEB 2, 1966
3-30-66
11-11-65
PRINTED IN U.S.A.

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GENERAL ELECTRIC

0178A7026
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REV NO. -2-

0178A7026
CONT ON SHEET SH NO.

TITLE
LEGEND FOR SYMBOLS USED ON STATIC RELAY LOGIC DIAGRAMS

FIG-9

FIRST MADE FOR

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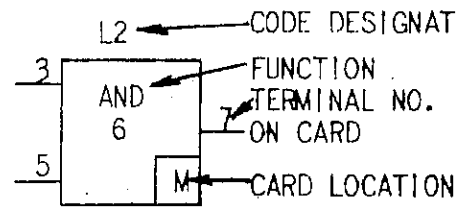
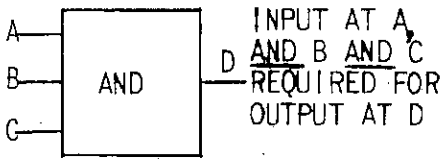
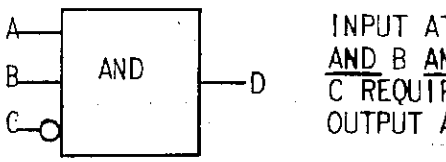
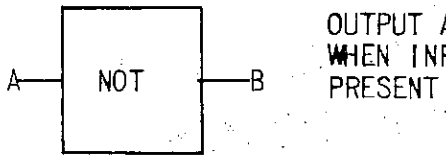
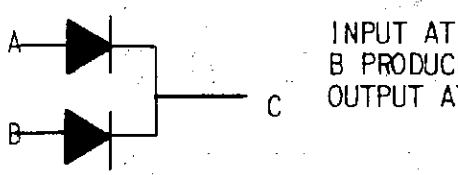
2
7-5-64 RETRACED

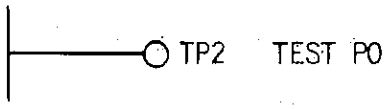


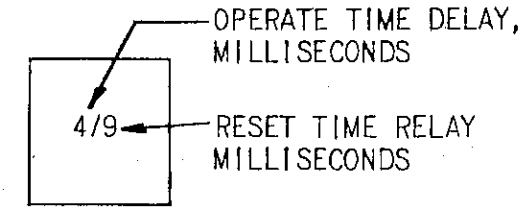


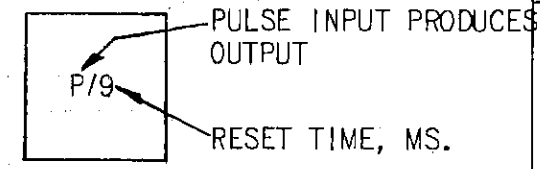


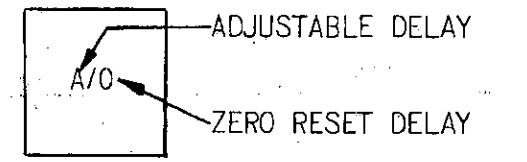


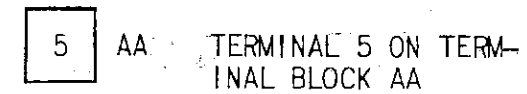


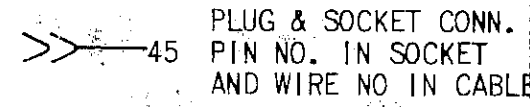


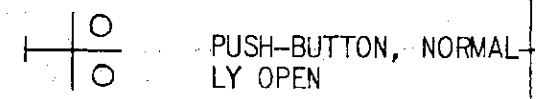


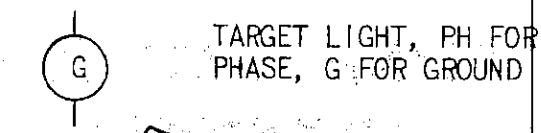


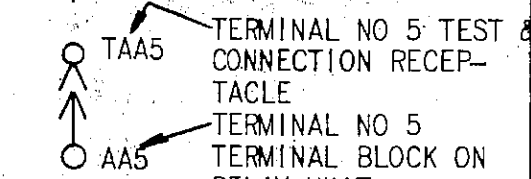


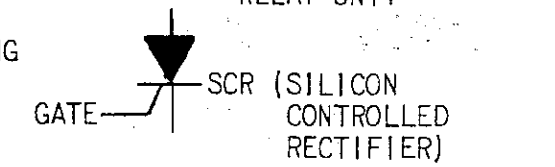












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PHILA. LOCATION

0178A7026
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REV NO. O

0203A8628
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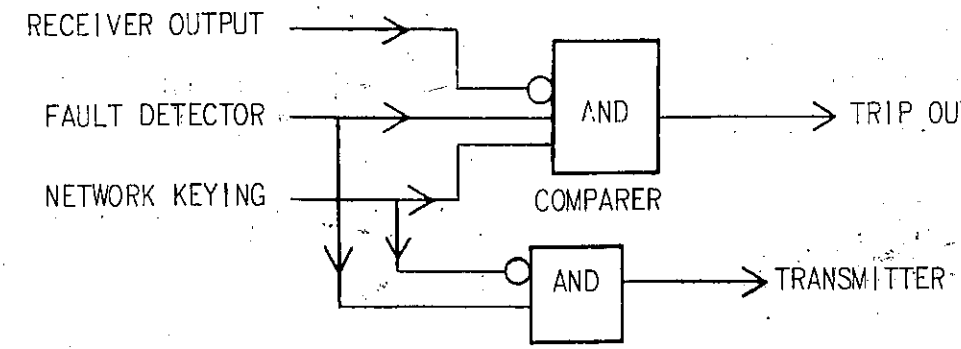
TITLE
PHASE COMPARISON
OPERATING PRINCIPLE

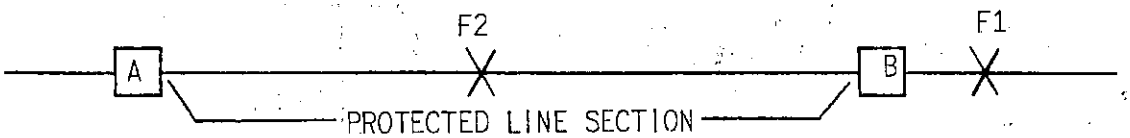
FIRST MADE FOR GEK-6877

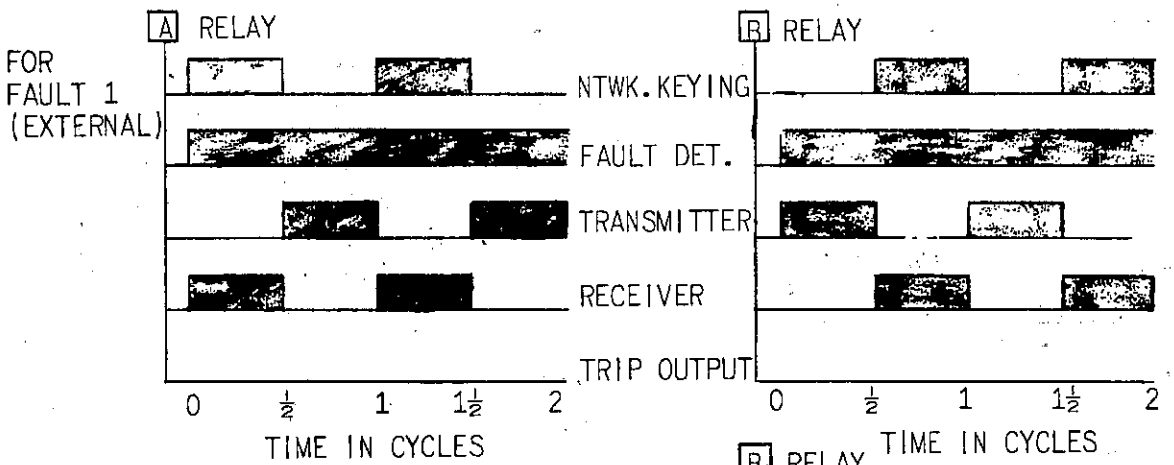
FIG. – 10

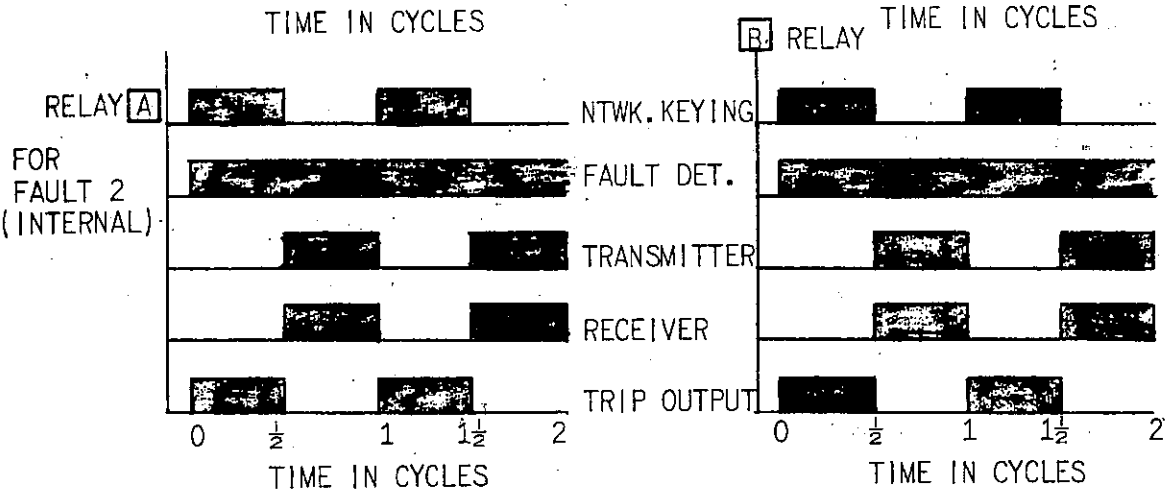
REVISIONS



SIMPLIFIED PHASE COMPARISON RELAY (AT A & B)







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ISSUED Dec 27, 1966

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LOCATION

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CODE L

GENERAL ELECTRIC

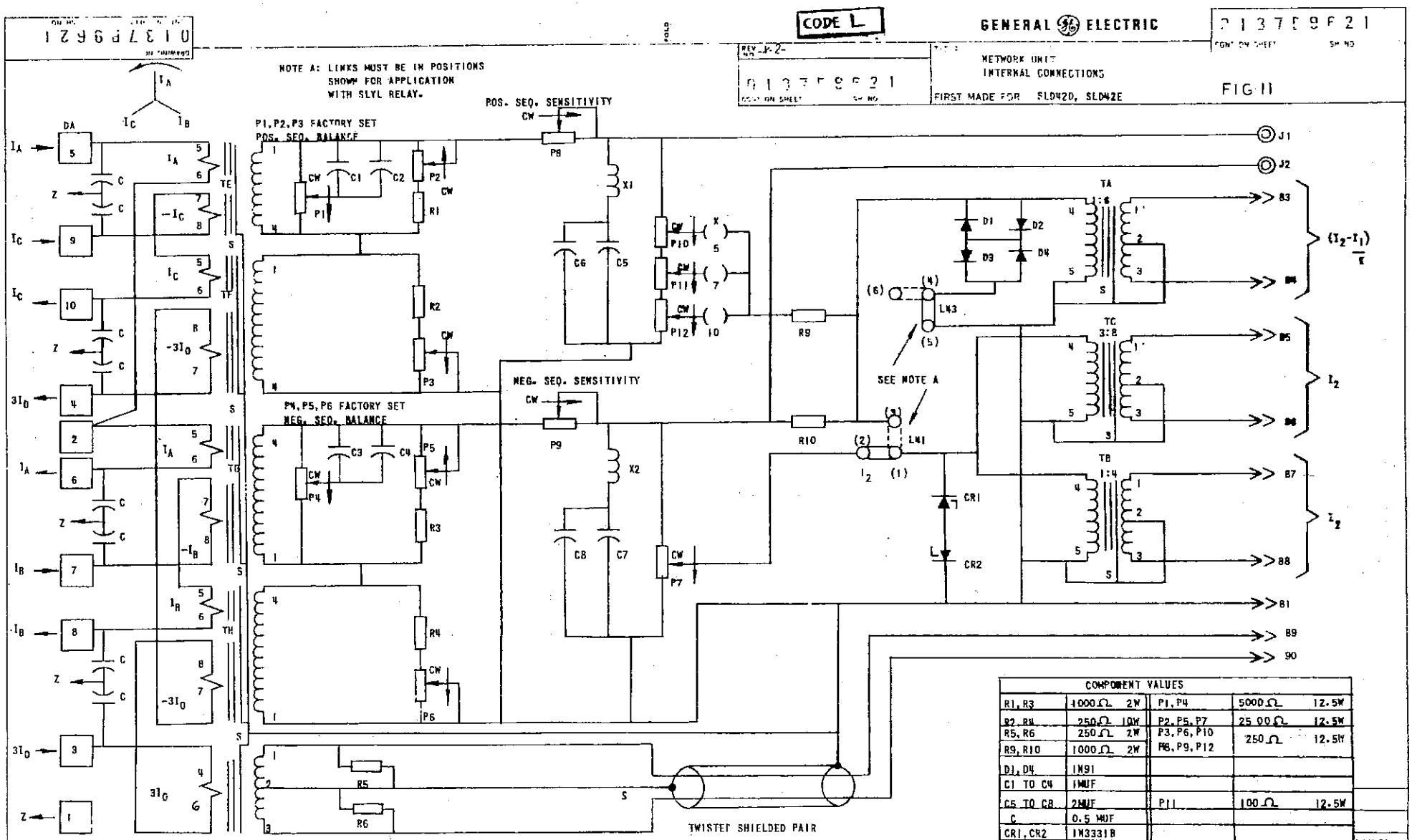
0137F9621

REV. K-2-

0137F9621

NETWORK UNIT
INTERNAL CONNECTIONS
FIRST MADE FOR SLDN2D, SLD42E

FIG 11



COMPONENT VALUES			
R1, R3	1000Ω 2W	P1, P4	5000Ω 12.5W
R2, R4	250Ω 10W	P2, P5, P7	2500Ω 12.5W
R5, R6	250Ω 2W	P3, P6, P10	250Ω 12.5W
R9, R10	1000Ω 2W	P8, P9, P12	
D1, D4	IN91		
C1 TO C4	1MUF		
C5 TO C8	2MUF	P11	100Ω 12.5W
C	0.5 MUF		
CR1, CR2	IN3331B		

PRINTS TO

MADE BY J. J. Connor Jan 566

APPROVALS

SWITCHGEAR
PHILADELPHIA

0137F9621

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GENERAL ELECTRIC

0178A9078
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0178A9078
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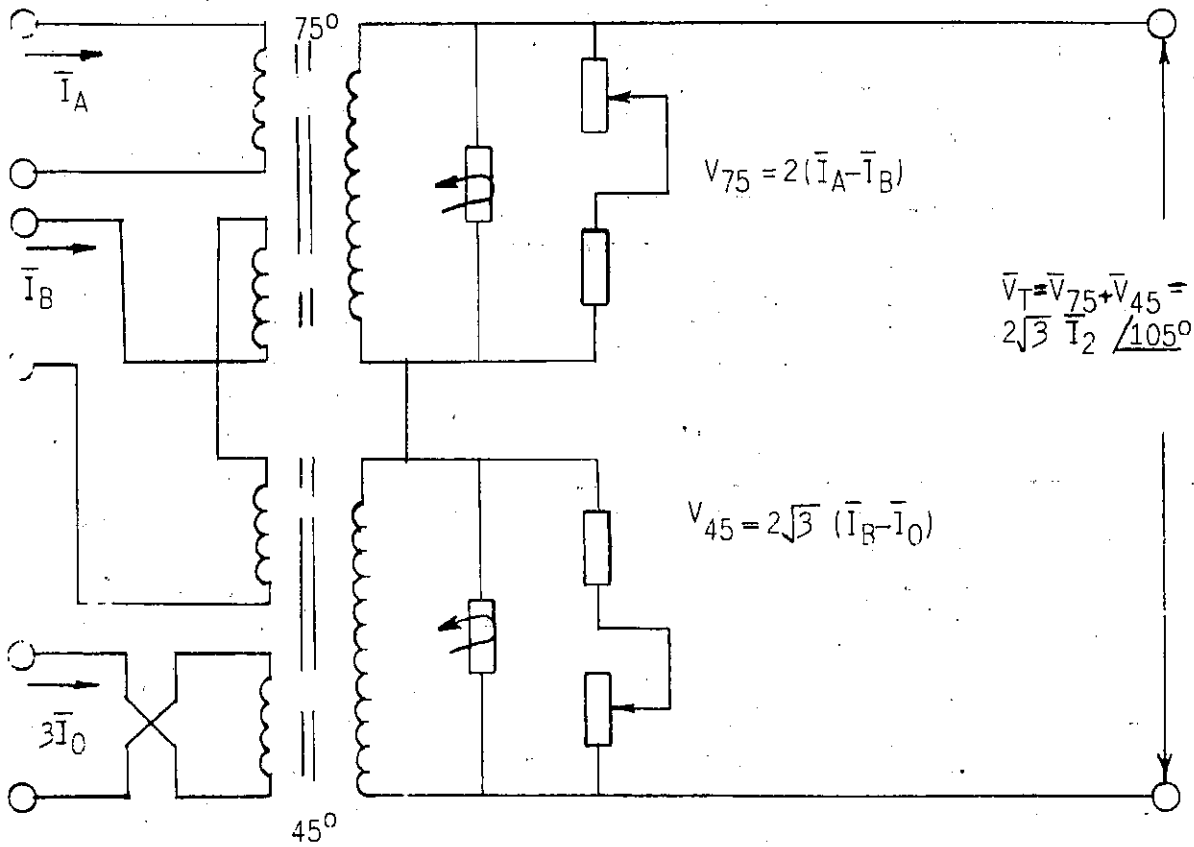
TITLE
SIMPLIFIED NEGATIVE-SEQUENCE NETWORK SCHEMATIC

FIG-12

FIRST MADE FOR RELAY TYPE SLD

REVISIONS



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PHILADELPHIA — LOCATION

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FF-606-WA (6-64)

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CODE H

GENERAL ELECTRIC

0178A9077

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0178A9077

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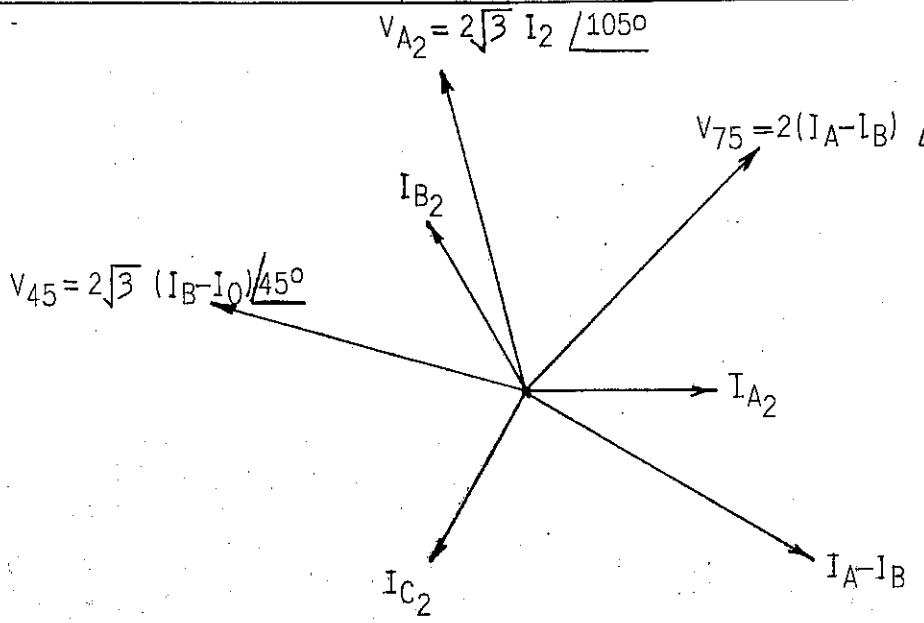
TITLE SLD NETWORK RESPONSE TO NEGATIVE, POSITIVE, AND ZERO SEQUENCE SYSTEMS.

FIRST MADE FOR

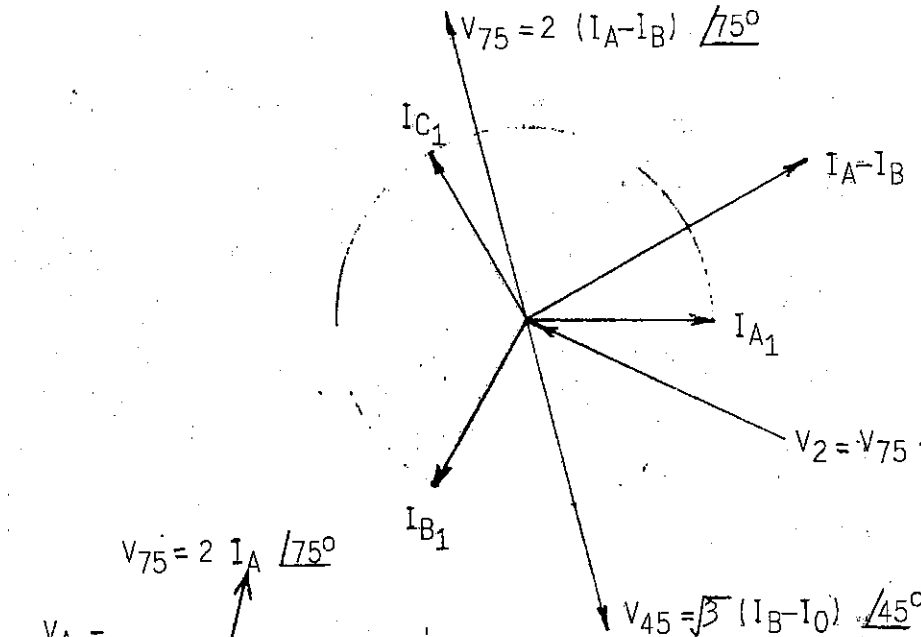
FIG-13

REVISIONS



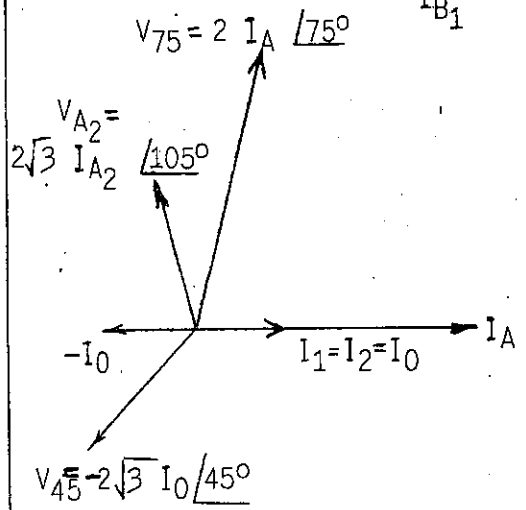
A

NETWORK RESPONSE TO A PURE NEGATIVE SEQUENCE SYSTEM



B.

NETWORK RESPONSE TO A PURE POSITIVE SEQUENCE SYSTEM



C

NETWORK RESPONSE TO A PHASE-A TO GROUND FAULT

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ISSUED [illegible] 1965

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SWITCHGEAR DIV. OR DEPT.

PHILADELPHIA LOCATION

0178A9077

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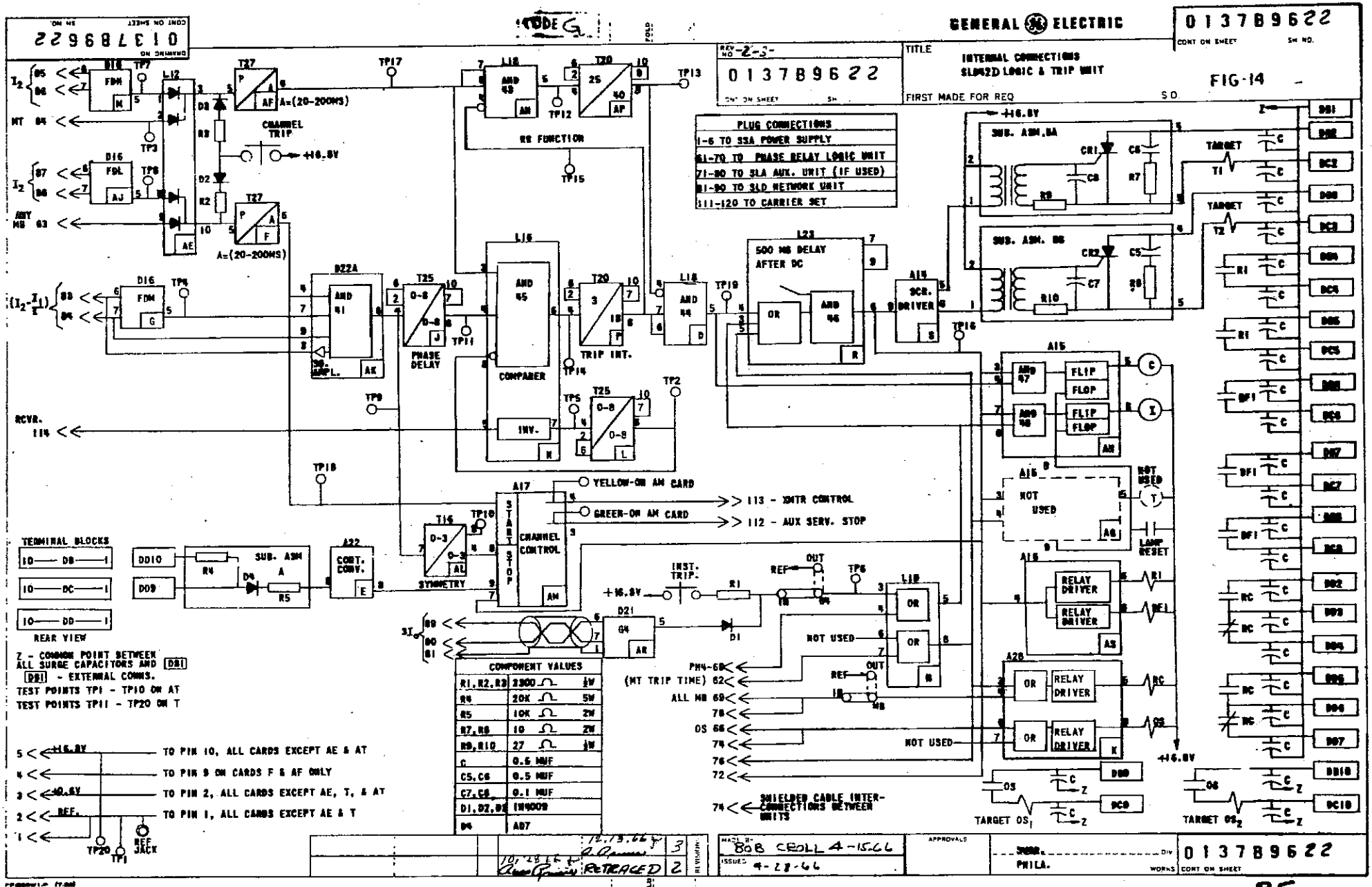
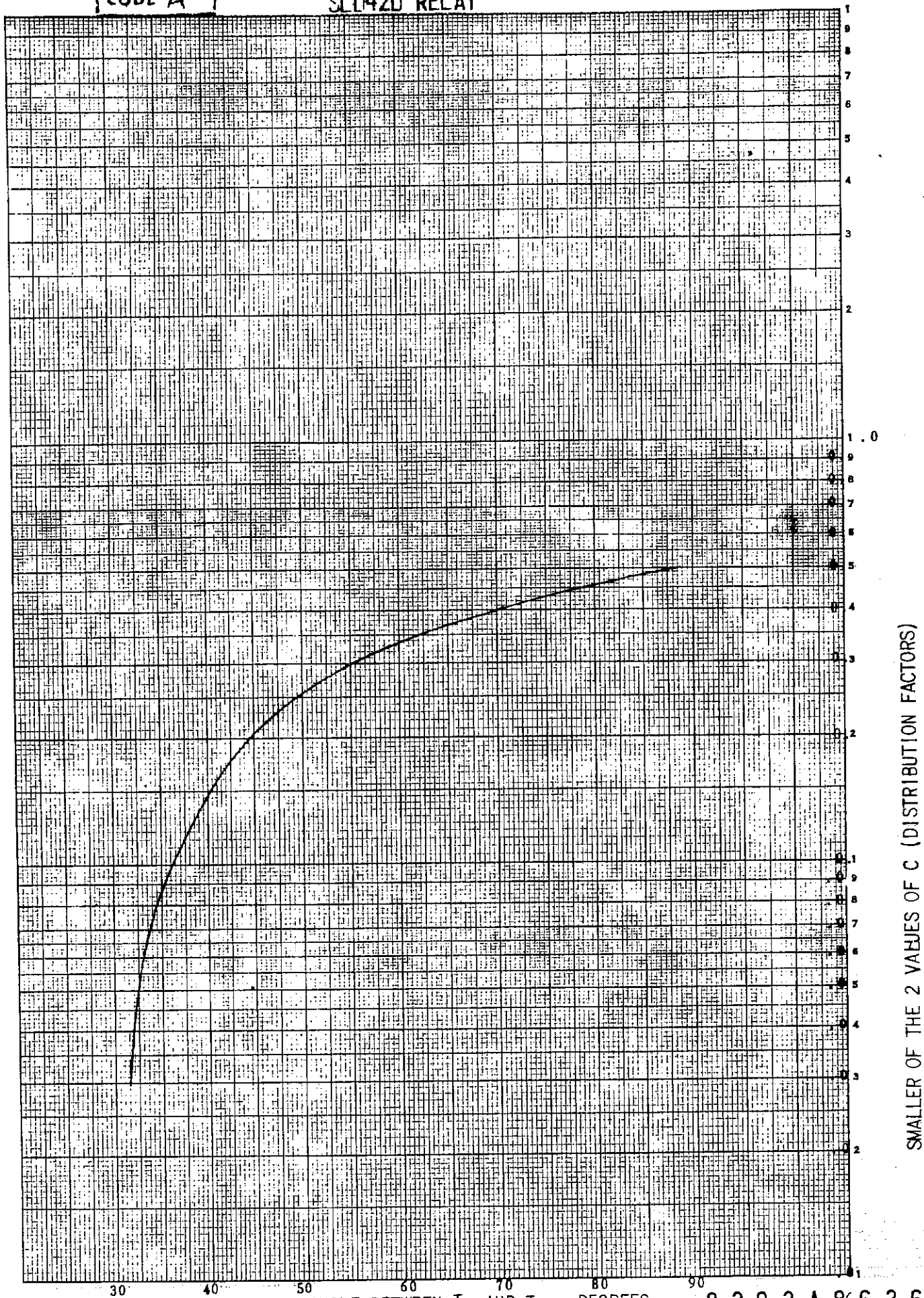

GENERAL ELECTRIC
0137B9622
CODE G
TITLE
INTERNAL CONNECTIONS
SLM92D LOGIC & TRIP UNIT
FIG-14
FIRST MADE FOR REQ
SD
PLUG CONNECTIONS
1-6 TO SSA POWER SUPPLY
61-70 TO PHASE RELAY LOGIC UNIT
71-80 TO SLA AUX. UNIT (IF USED)
81-90 TO SLD NETWORK UNIT
111-120 TO CARRIER SET
SUB. ASM. BA
SUB. ASM. BB
+16.8V
-16.8V
REF.
TARGET T1
TARGET T2
TARGET OS1
TARGET OS2
AND 41
AND 45
AND 46
AND 47
AND 48
AND 44
FLIP FLOP
RELAY DRIVER
SCR. DRIVER
500 MS DELAY AFTER 9C
PHASE DELAY
COMPARER
TRIP INT.
CHANNEL CONTROL
SYMMETRY
CONT. CONV.
SUB. ASM A
NOT USED
LAMP RESET
TERMINAL BLOCKS
REAR VIEW
Z - COMMON POINT BETWEEN ALL SURGE CAPACITORS AND DBI
DBI - EXTERNAL CONNS.
TEST POINTS TP1 - TP10 ON AT
TEST POINTS TP11 - TP20 ON T
TO PIN 10, ALL CARDS EXCEPT AE & AT
TO PIN 9 ON CARDS F & AF ONLY
TO PIN 2, ALL CARDS EXCEPT AE, T, & AT
TO PIN 1, ALL CARDS EXCEPT AE & T
SHIELDED CABLE INTER-CONNECTIONS BETWEEN UNITS
COMPONENT VALUES
R1,R2,R3 2300Ω 1W
R4 20K 5W
R5 10K 2W
R7,R8 10 2W
R9,R10 27 1W
C C5,C6 0.5 MUF
C7,C8 0.1 MUF
D1,D2,D3 IN4009
D4 A87
YELLOW-ON AM CARD
GREEN-ON AM CARD
113 - XMTR CONTROL
112 - AUX SERV. STOP
A=(20-200MS)
CHANNEL TRIP
R8 FUNCTION
INST. TRIP
OUT
REF
NOT USED
(MT TRIP TIME) 62
ALL MB 69
OS 66
PHASE RELAY LOGIC UNIT
SLA AUX. UNIT (IF USED)
SLD NETWORK UNIT
CARRIER SET
808 CELL 4-15-66
ISSUED 4-28-66
PHILA.
RETRACED
12/29/66
10/28/66
0137B9622

0203A8636

FIG. 15

CODE A

I_{KL} & I_{KF} ANGLE CURVE
SLD42D RELAY



0203A8636

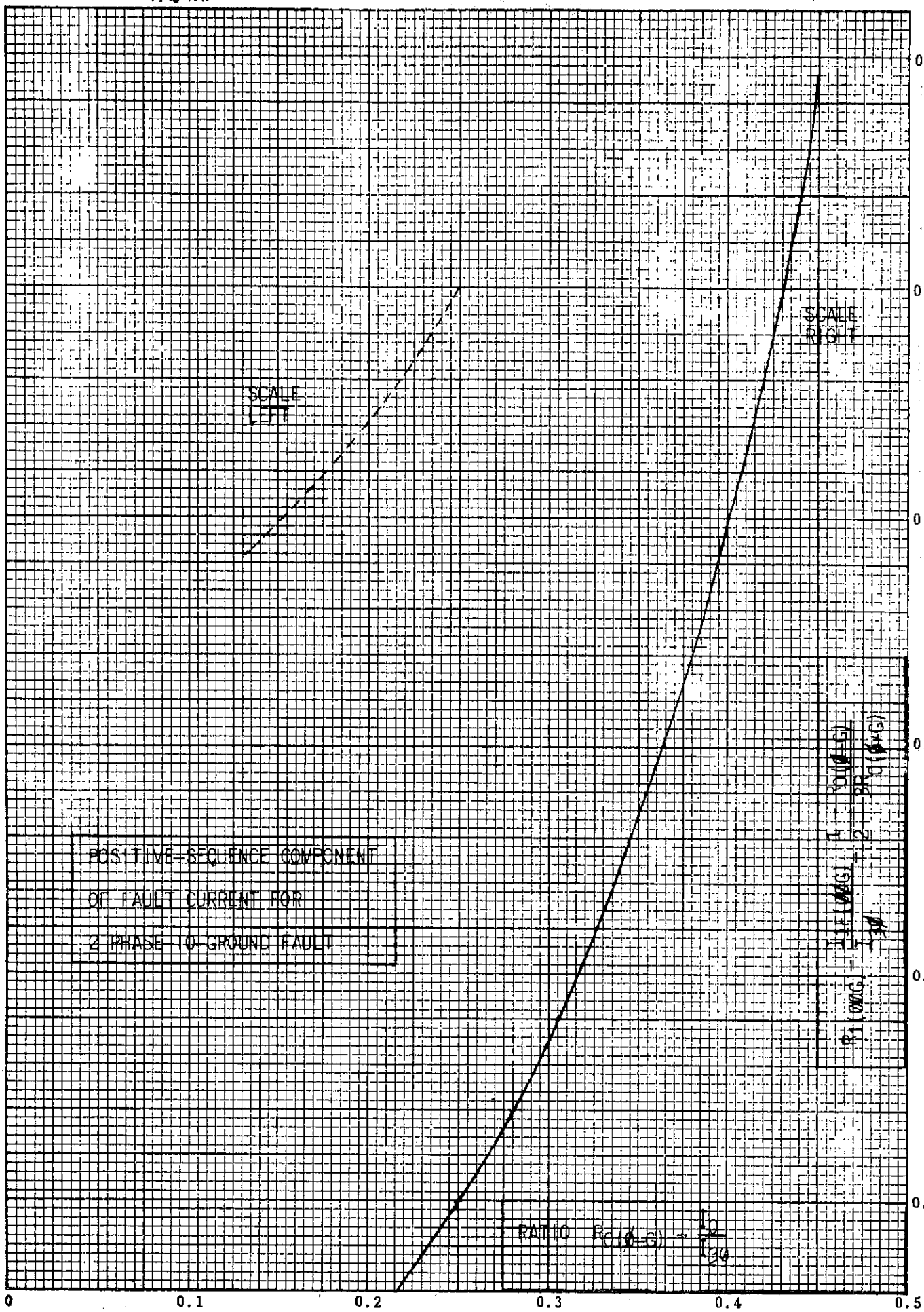
GENERAL ELECTRIC COMPANY SCHENECTADY, N.Y., U.S.A.

3 cyc. ± 1/10 1mm

FN-2(1-50)

I IF IN ØØG FAULTS

FIG. 16A



CODE A

I_2 IN [illegible] FAULTS

0203A8638

FIG. 16B

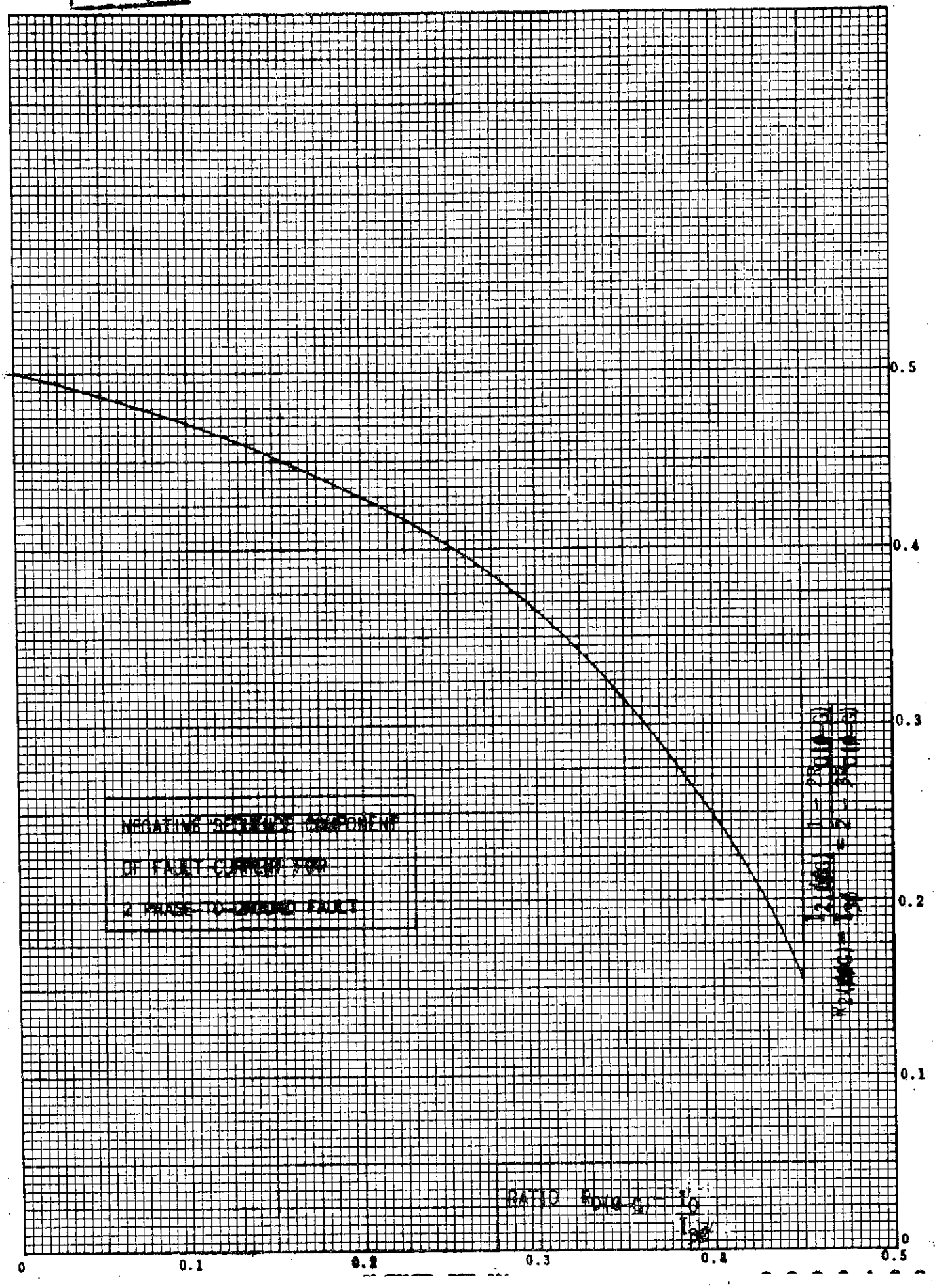
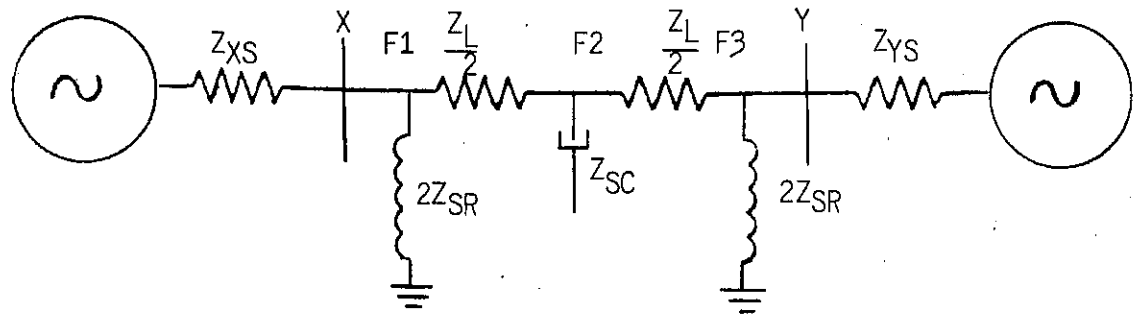


FIGURE 17A SAMPLE SYSTEM



Z_{1XS}-.3pu Z_{1L}-1pu Z_{SC}- 6pu Z_{1YS}-.25pu
Z_{0XS}-.15pu Z_{0L}-3pu Z_{SR}-8pu Z_{0YS}-.5pu

FIGURE 17B DATA TABULATION
Fault and Load Data in pu

Quantity	Fault Location F1	F2	F3	Source of Data
I_{1L}	.75	.75	.75	Load Flow Studies
$I_{3\emptyset}$	4.1	2.58	4.77	Fault Studies
I_0	1.6	.595	1.17	Fault Studies
$R_{0(\emptyset G)}$	.39	.23	.246	$1 \div I_{3\emptyset}$
C_X	.805	.485	.162	Fault Studies
C_6	.195	.515	.838	Fault Studies
$I_{2(\emptyset G)X}$		.288	.19	$I_0 \times C_X$
$I_{2(\emptyset G)Y}$		.306	.98	$I_9 \times C_Y$
$R_{2(\emptyset\emptyset G)}$	.265			$R_{0(\emptyset G)}$ and Fig. 16B
$I_{2(\emptyset\emptyset G)X}$	.88			$R_{2(\emptyset\emptyset G)} \times I_{3\emptyset} \times C_X$
$I_{2(\emptyset\emptyset G)Y}$	.21			$R_{2(\emptyset\emptyset G)} \times I_{3\emptyset} \times C_Y$
$R_{1(\emptyset\emptyset G)}$	.735			$R_{0(\emptyset G)}$ and Fig. 16A
$I_{1F(\emptyset\emptyset G)X}$	2.42			$R_{1(\emptyset\emptyset G)} \times I_{3\emptyset} \times C_X$
$I_{1F(\emptyset\emptyset G)Y}$	.59			$R_{1(\emptyset\emptyset G)} \times I_{3\emptyset}$ c C_Y
$I_{3\emptyset}/I_{1L}$	5.5	3.44	6.36	
K	7	10	10	C_X or C_Y, $I_{3\emptyset}/I_{1L}$, $R_{0(\emptyset G)}$ and Fig 18A, B & C
Worst L I_{KF}, I_{KL}	43	86°	40.5°	C_X or C_Y, Fig. 15

REVISIONS

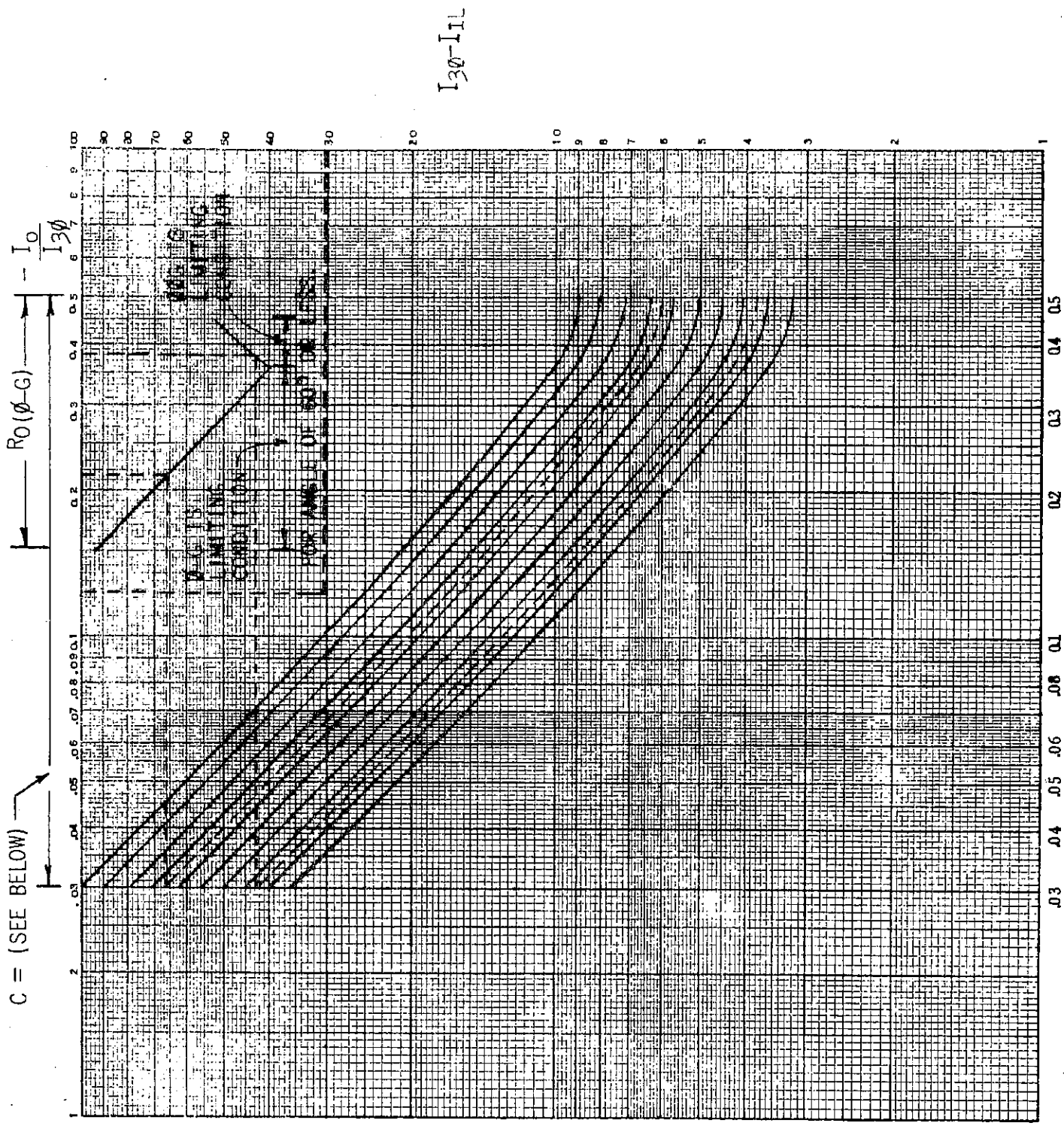
PRINTS TO

A

0203A8631

K SELECTION CURVES (K=5)

FIG. 18A



SLD420 RELAY

0203A8631

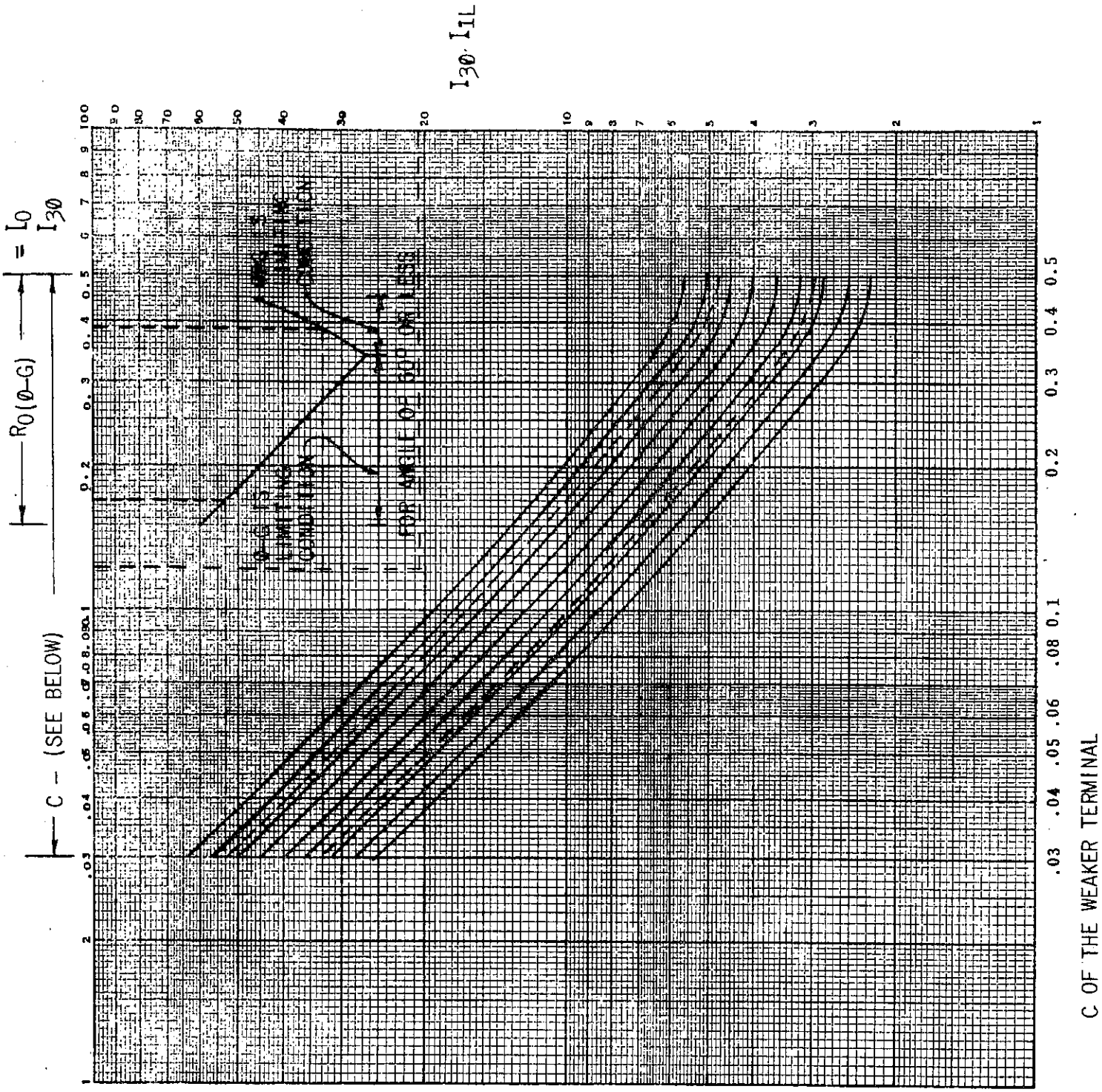
GEK-6877

CODE A

K SELECTION CURVES (K=7)

0 2 0 3 A 8 6 3

FIG. 18B



SLD42D RELAY

0 2 0 3 A 8 6 3

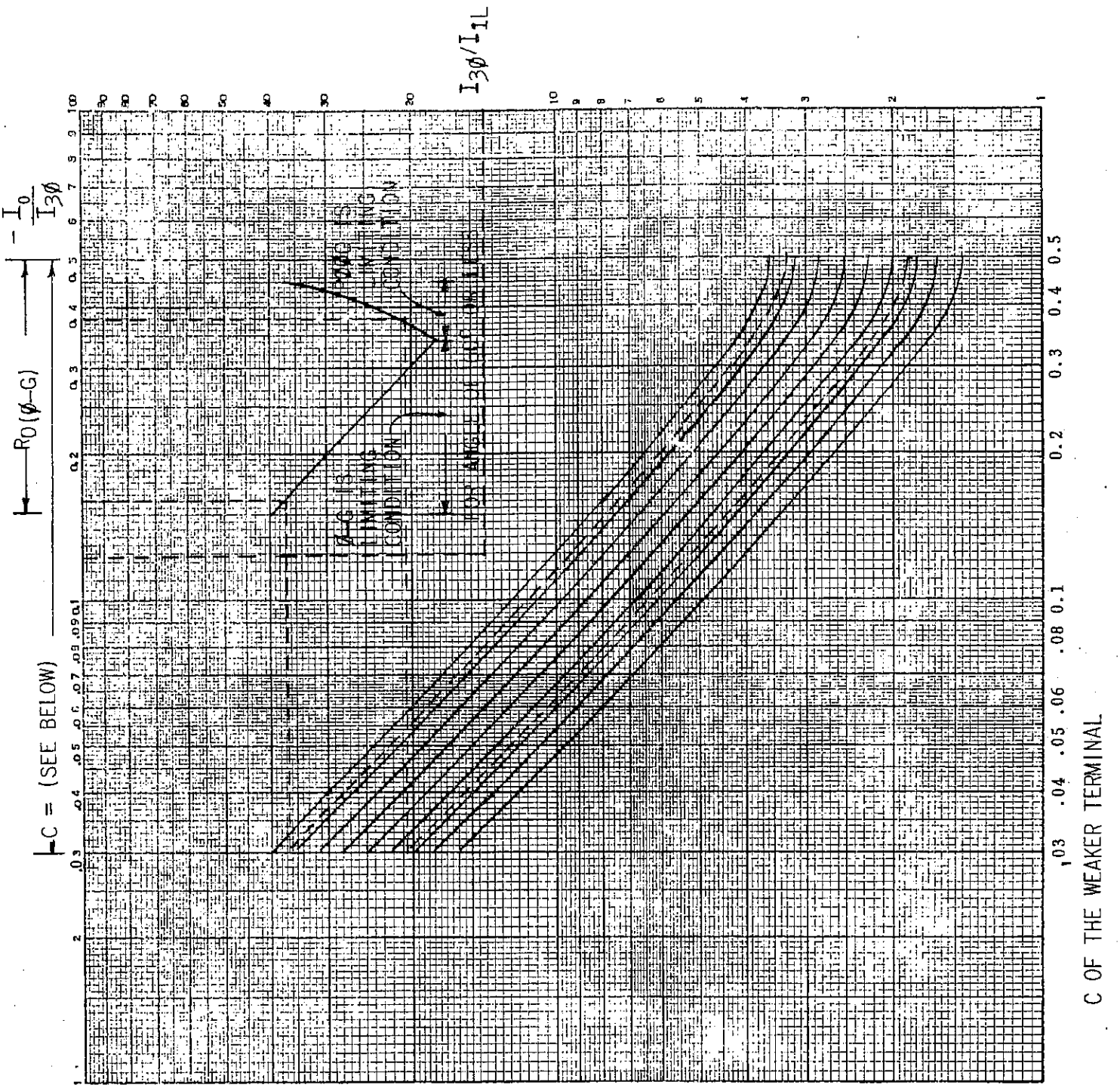
GEK-6877

Dec 27, 1966

A

K SELECTION CURVES (K=10)

FIG. 18C

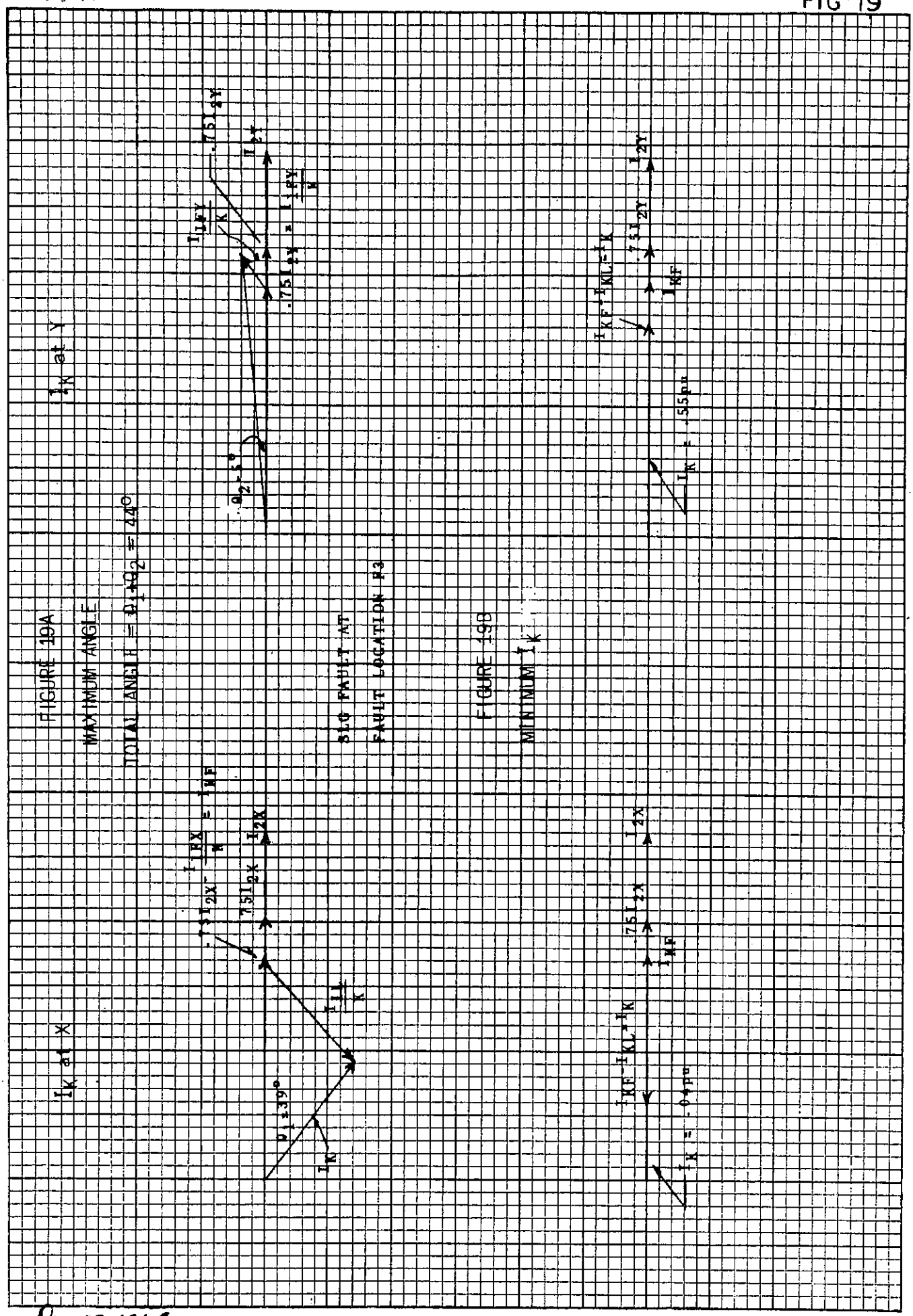


SLD42D RELAY

0203A8632

RELAYING SIGNAL PHASOR DIAGRAM FOR PHASE-TO-GROUND FAULTS (ØG)

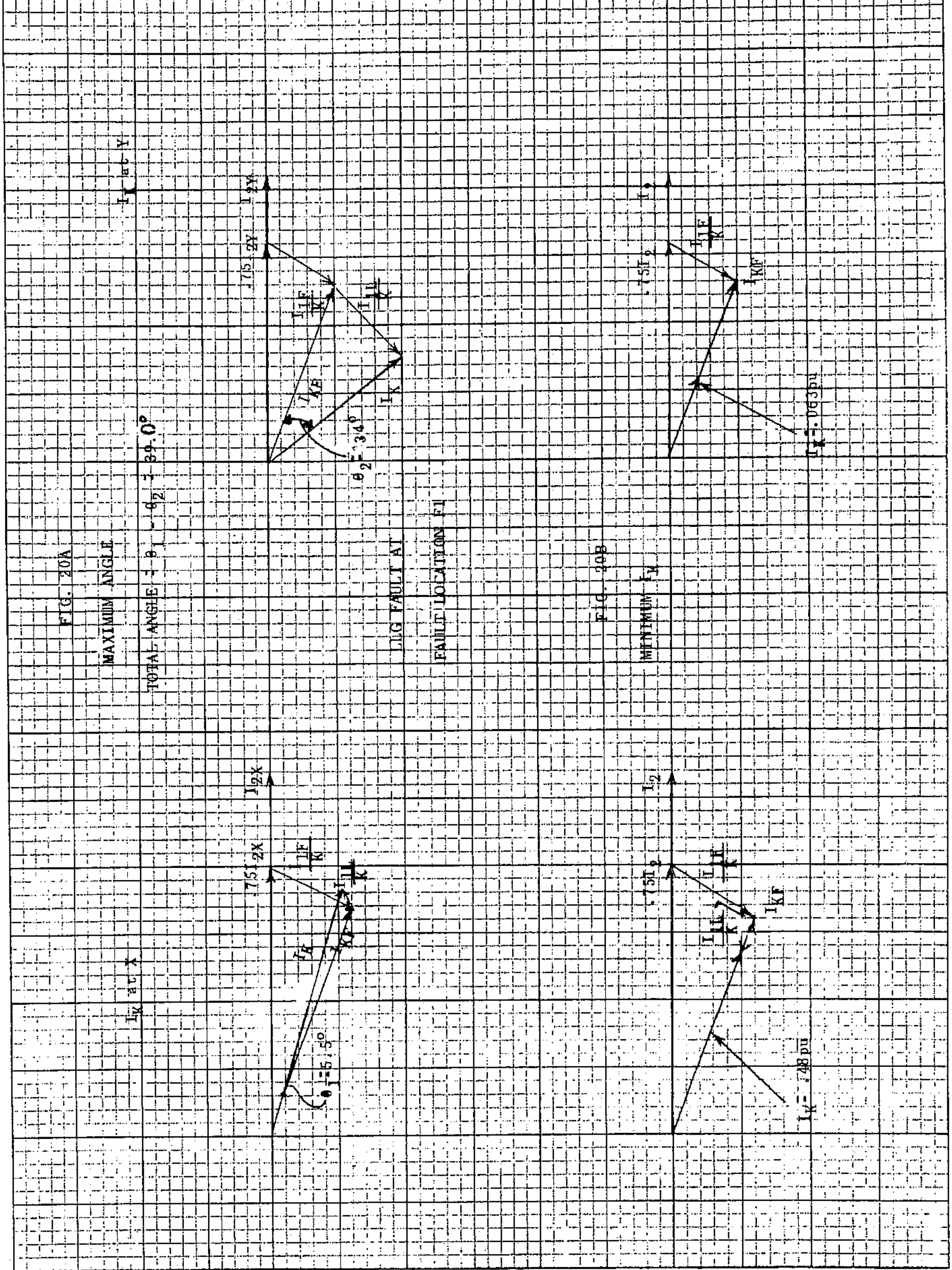
FIG-19



CODE A

FIG-20

KEYING SIGNAL PHASOR DIAGRAM
FOR PHASE - TO - PHASE TO GROUND FAULTS (ØØG)



REV 2 M. Lynch LINES IN FRACTIONS, CHANGE 39.5° TO 39.0°

CODE

GENERAL ELECTRIC

0178A9079

CONT ON SHEET SH NO.

REV NO. 1

0178A9079

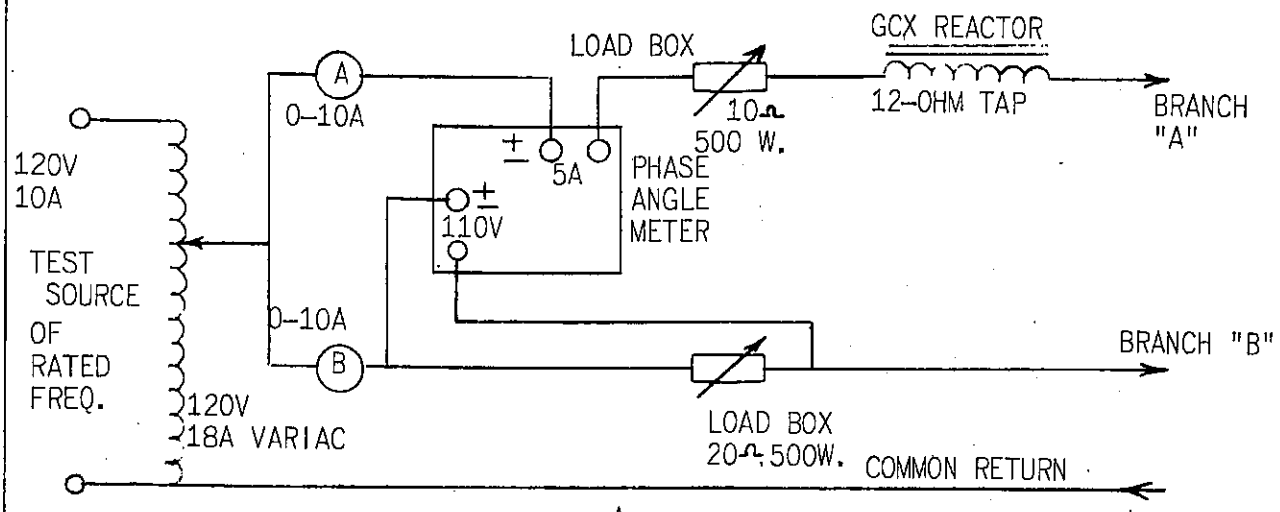
CONT ON SHEET SH NO.

TITLE TEST CONNECTIONS FOR CHECKING BALANCE OF NEGATIVE AND POSITIVE SEQUENCE NETWORKS IN SLD RELAYS.

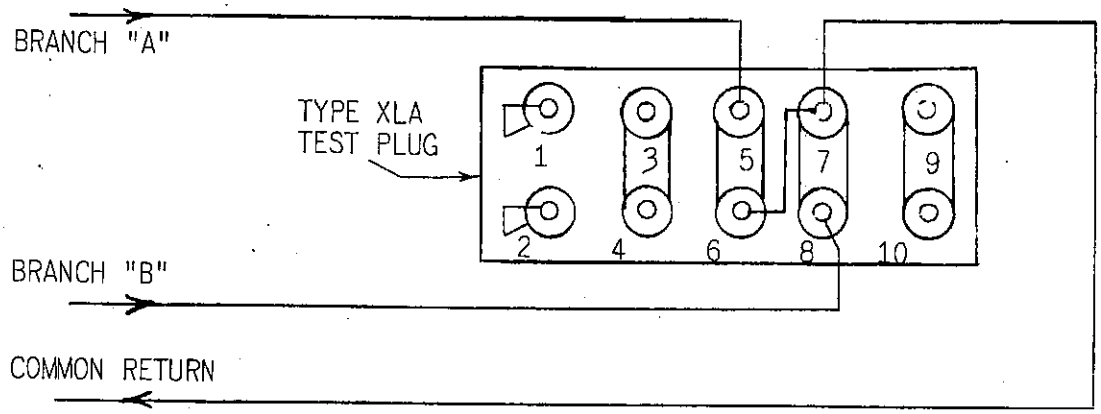
FIRST MADE FOR

FIG-21

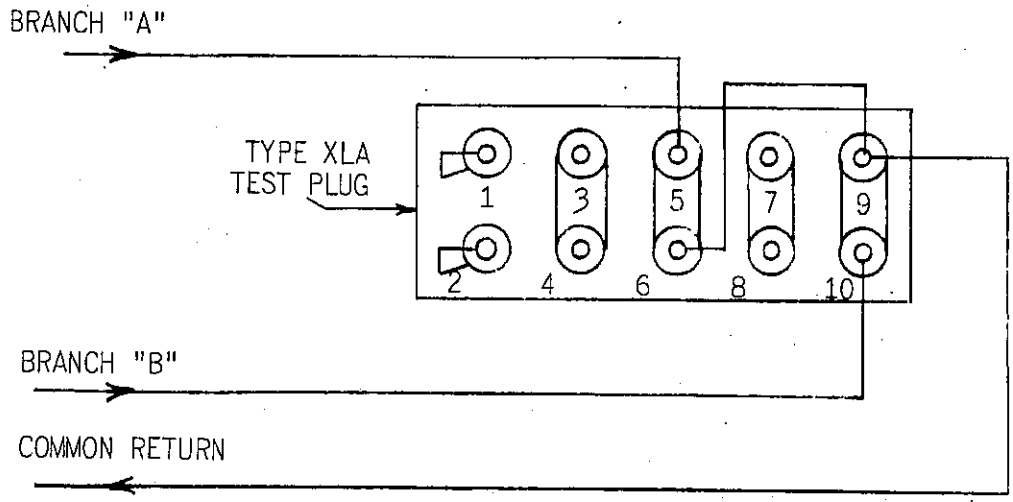
REVISIONS



A



B (NEGATIVE–SEQUENCE NETWORK)



C (POSITIVE–SEQUENCE NETWORK)

PRINTS TO

MADE BY

ISSUED

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0178A9079

CONT ON SHEET SH NO.

FF-803-WA (6-64)

CODE H

GENERAL ELECTRIC

0178A9086

CONT ON SHEET SH NO.

REV. NO.

0178A9086

CONT ON SHEET SH NO.

TITLE

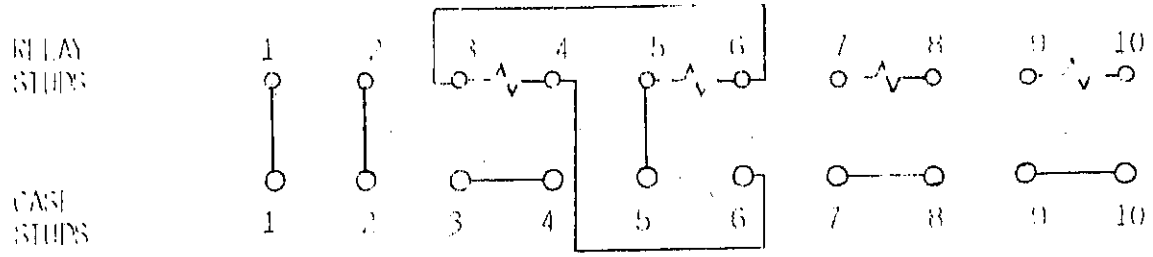
TEST PLUG CONNECTIONS FOR CT PHASING

FIG-22

FIRST MADE FOR

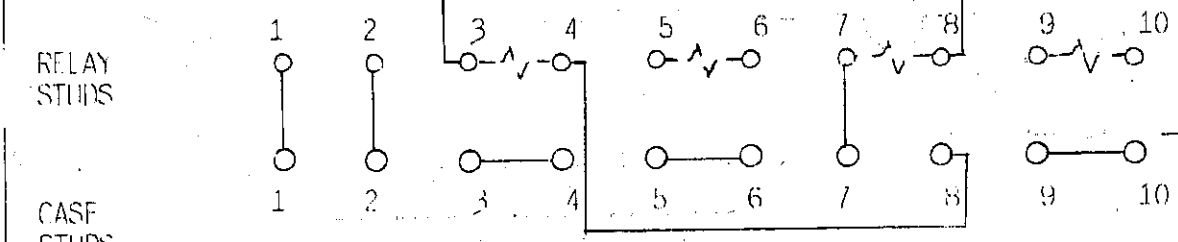
REVISIONS

PHASE-A CT TEST



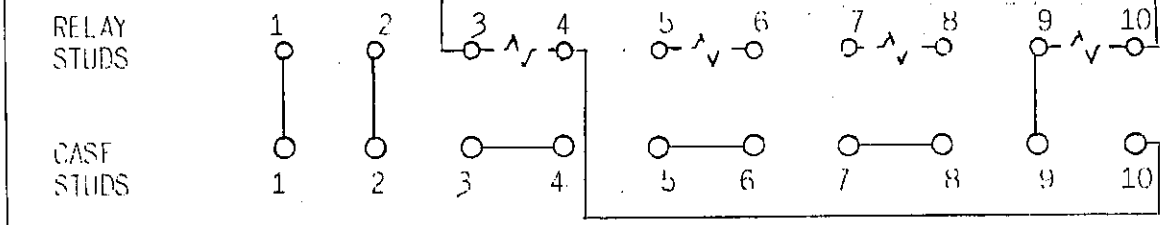
A

PHASE-B CT TEST



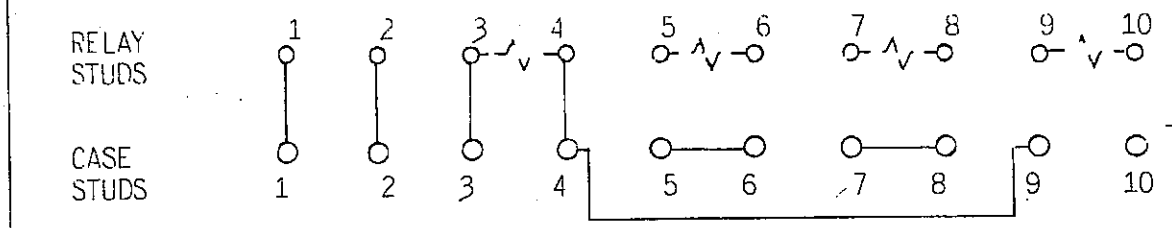
B

PHASE-C CT TEST



C

CT RESIDUAL TEST



D

PRINTS TO

MADE BY

ISSUED

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0178A9086

CONT ON SHEET SH NO.

CODE H

GENERAL ELECTRIC

0178A9C84
CONT ON SHEET SH NO.

REV NO. -1-

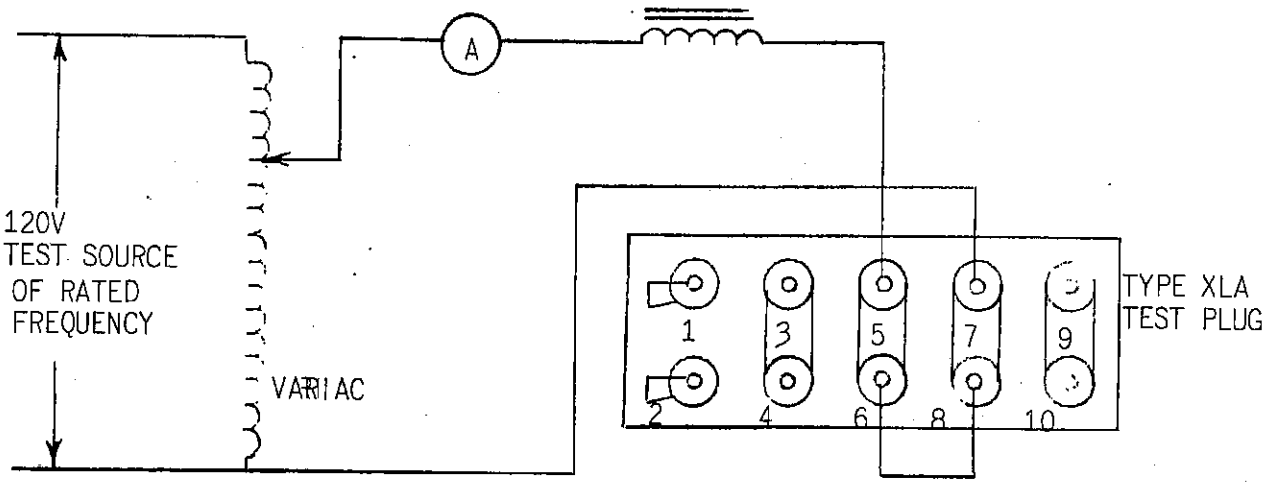
0178A9084
CONT ON SHEET SH NO.

TITLE
TEST PLUG CONNECTIONS FOR CHECKING FDL AND FDH

FIRST MADE FOR

FIG-23

REVISIONS



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PHILADELPHIA LOCATION

0178A9084
CONT ON SHEET SH NO.

FF-803-WA (6-64)
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SP-R

CODE IDENT NO.

GENERAL ELECTRIC

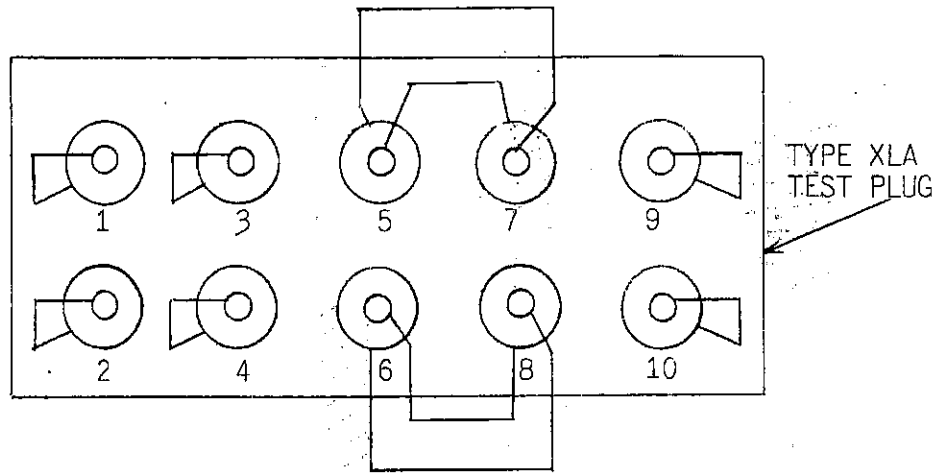
0178A9082
CONT ON SHEET SH NO.

REV NO.
0178A9082
CONT ON SHEET SH NO.

TITLE TEST PLUG CONNECTIONS WHEN LOAD CURRENT IS USED FOR PHASE DELAY ADJUSTMENT.
FIRST MADE FOR

FIG-24

REVISIONS



PRINTS TO

MADE BY
ISSUED
APPROVALS
SWITCHGEAR DIV OR DEPT.
PHILADELPHIA LOCATION

0178A9082
CONT ON SHEET SH NO.

CODE A

GENERAL ELECTRIC

0203A8626
CONT ON SHEET SH NO.

REV NO. 0

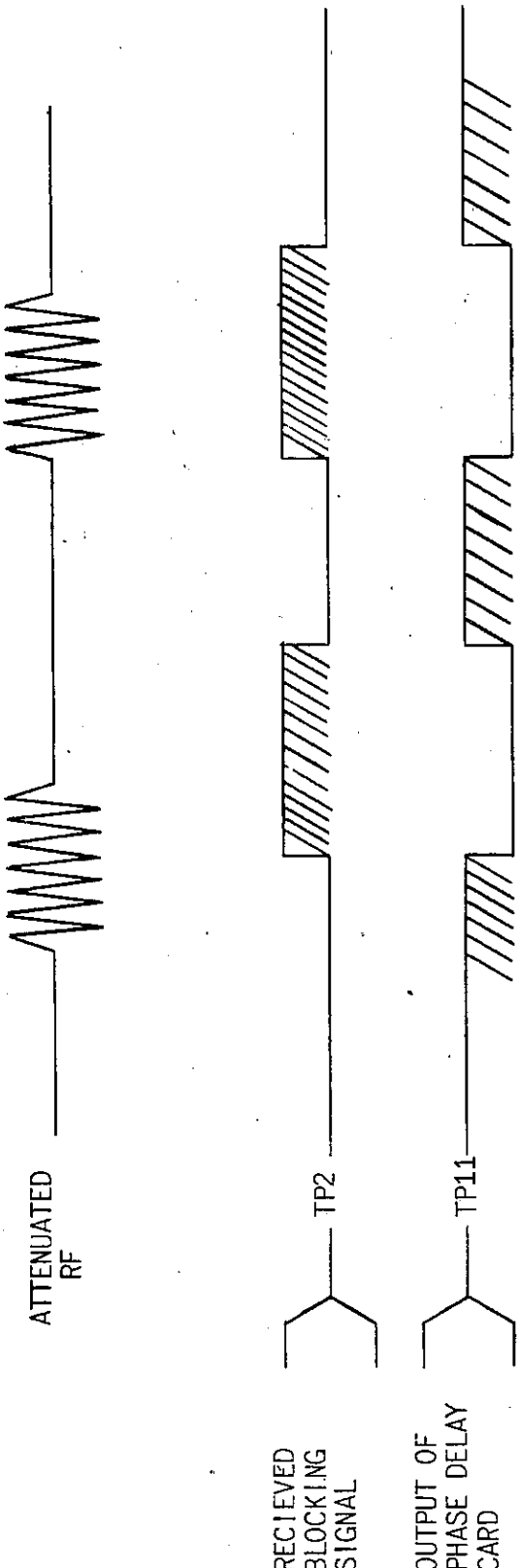
0203A8626
CONT ON SHEET SH NO.

TITLE
ADJUSTMENTS OF PHASE DELAY
BY LOCAL SIGNAL

FIRST MADE FOR SLD42D

FIG. 25

REVISIONS



PRINTS TO

MADE BY H White DEC. 13, 1966
ISSUED Dec 27, 1966

APPROVALS

SWITCHGEAR DIV OR DEPT.
PHILADELPHIA LOCATION

0203A8626
CONT ON SHEET SH NO.

FF-803-WA (4-66)

SP-R

CODE IDENT NO.

H

GENERAL ELECTRIC

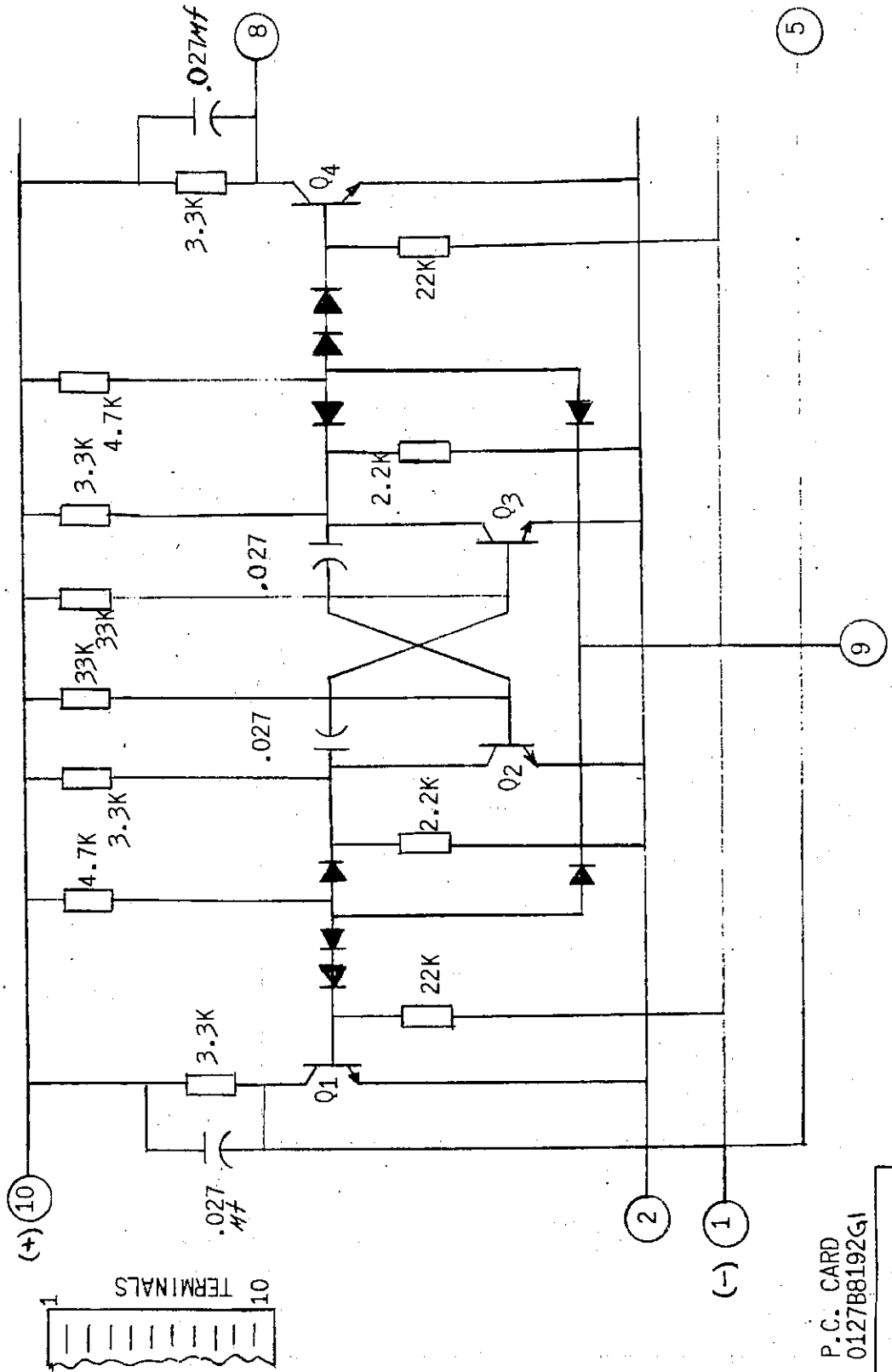
0148A3909AB
CONT ON SHEET SH NO.

REV NO. 1-
0148A3909AB
CONT ON SHEET SH NO.

TITLE
2-SCR DRIVERS
FIRST MADE FOR SLD WITH SLY (A14)

FIG-26A

REVISIONS



INPUT AT ⑨ GIVES PULSES OUT AT ⑤ AND ⑧, 0.3 MS ON, 0.3 MS OFF

P.C. CARD
0127B8192G1

ALL Q-2N697
D-1N4009
R-½W, 10%

PRINTS TO

MADE BY R Beckstead NOV. 17, 1964
ISSUED

APPROVALS

SWITCHGEAR DIV OR DEPT.
PHILADELPHIA LOCATION

0148A3909AB
CONT ON SHEET SH NO.

CODE A

GENERAL ELECTRIC

0148A3907AB

CONT ON SHEET SH NO.

REV NO. 0148A3907AB

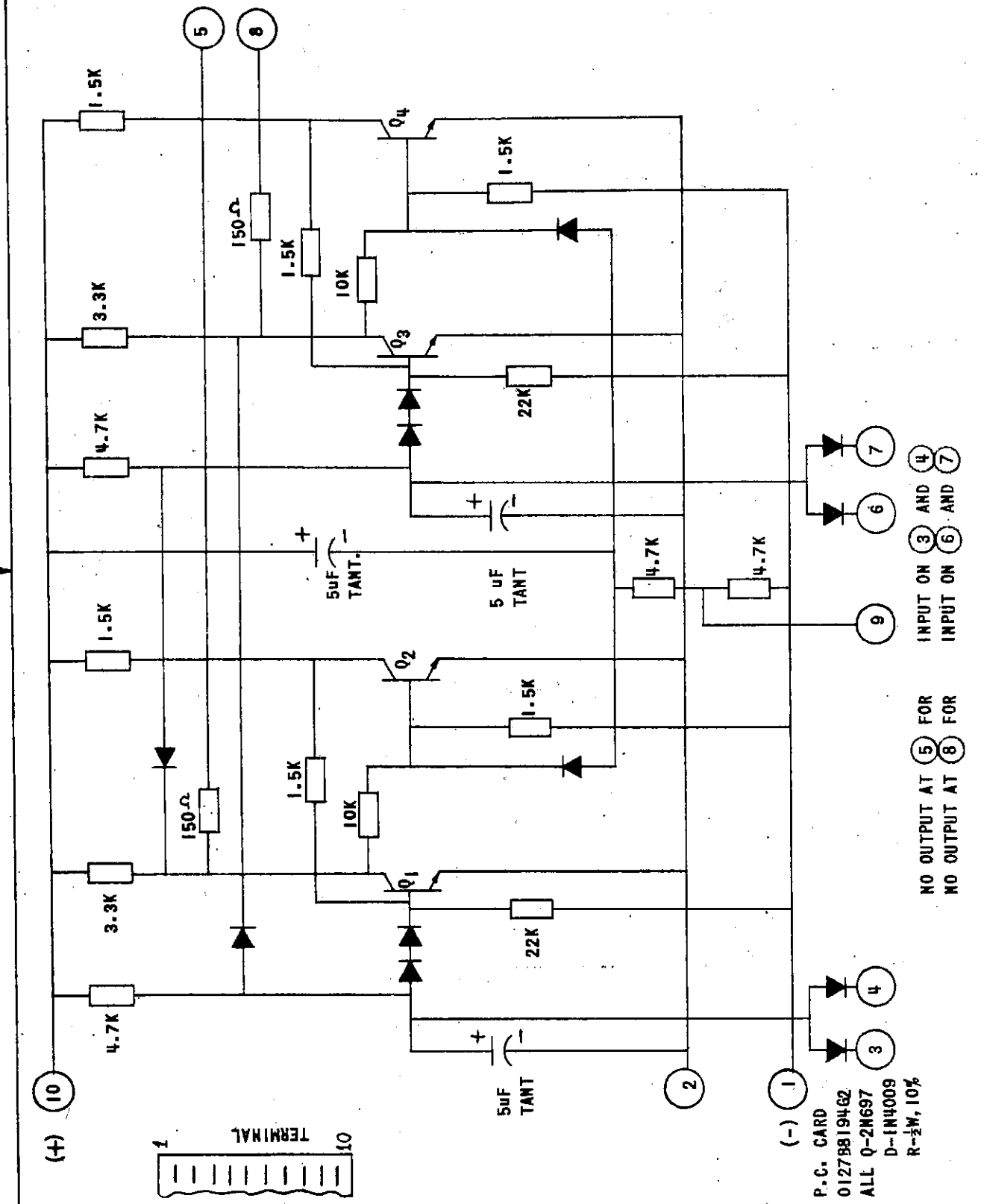
CONT ON SHEET SH NO.

TITLE TARGET LOGIC & DRIVERS WITH SEAL-IN AND RESET LOGIC

FIRST MADE FOR SLD WITH SLY (A15)

FIG-26B

REVISIONS



PRINTS TO

MADE BY 11-15-66

ISSUED May 24, 1966

APPROVALS

SWGR. DIV OR DEPT.

PHILA. LOCATION

0148A3907AB

CONT ON SHEET SH NO.

LSP-R

CODE IDENT NO.

FF-803-WA (4-66)

H

GENERAL ELECTRIC

0148A3918AB

CONT ON SHEET SH NO 1

REV NO.

0148A3918AB

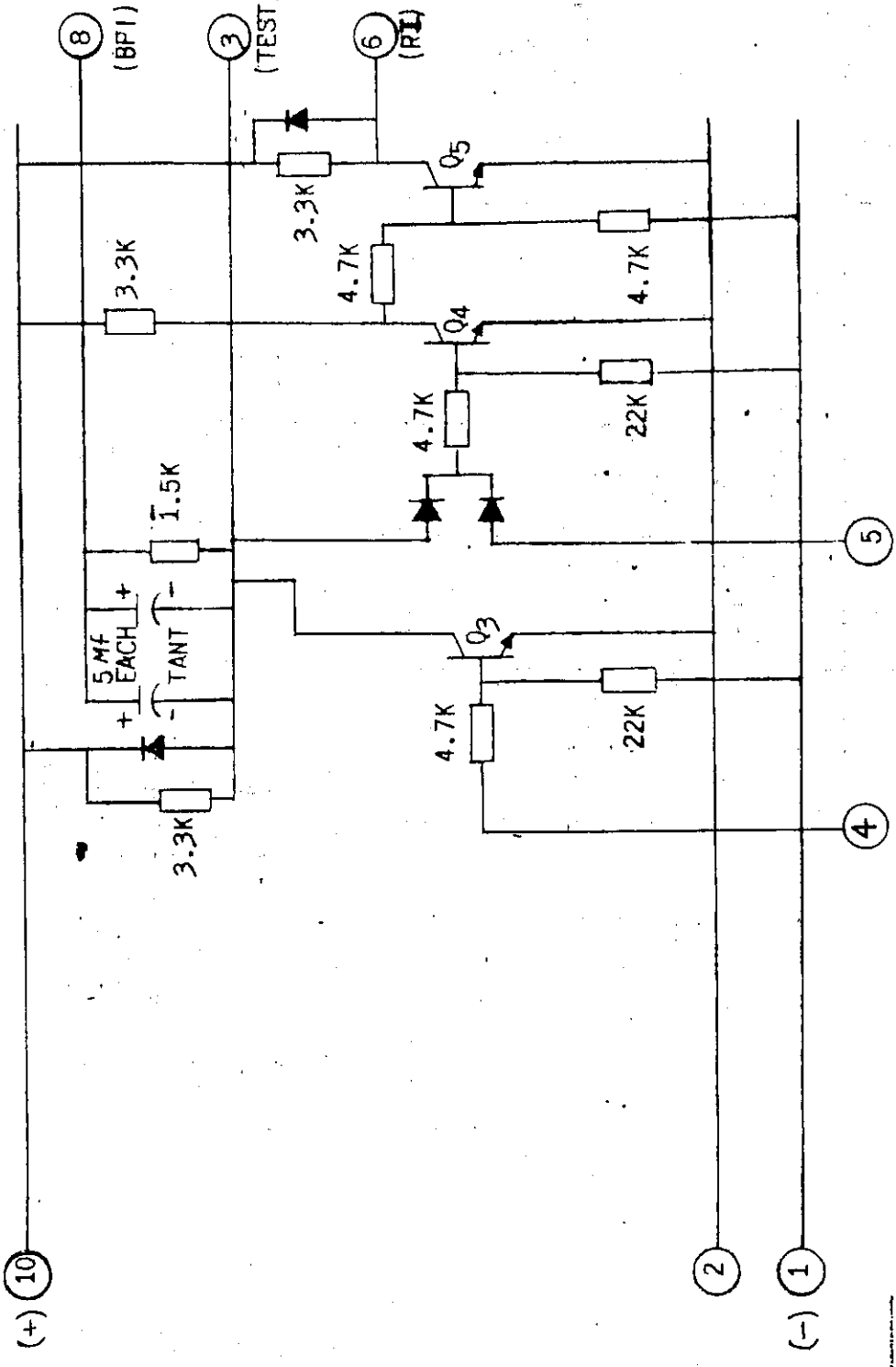
CONT ON SHEET SH NO

TITLE TELEPHONE RELAY DRIVERS (RI, BFI)

FIG-26C (A16)

FIRST MADE FOR 'SLD WITH 'SLY

REVISIONS



P.C. CARD 0127B8196G1

ALL Q-2N697
D-1N4009
R-½W, 10%

PRINTS TO

TERMINALS 1 10

MADE BY P Bechtold NOV. 18, 1964

ISSUED Nov. 30 1964

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0148A3918AB

CONT ON SHEET SH NO.

CODE 4

GENERAL ELECTRIC

0148A3911AE

CONT ON SHEET SH NO.

REV NO.

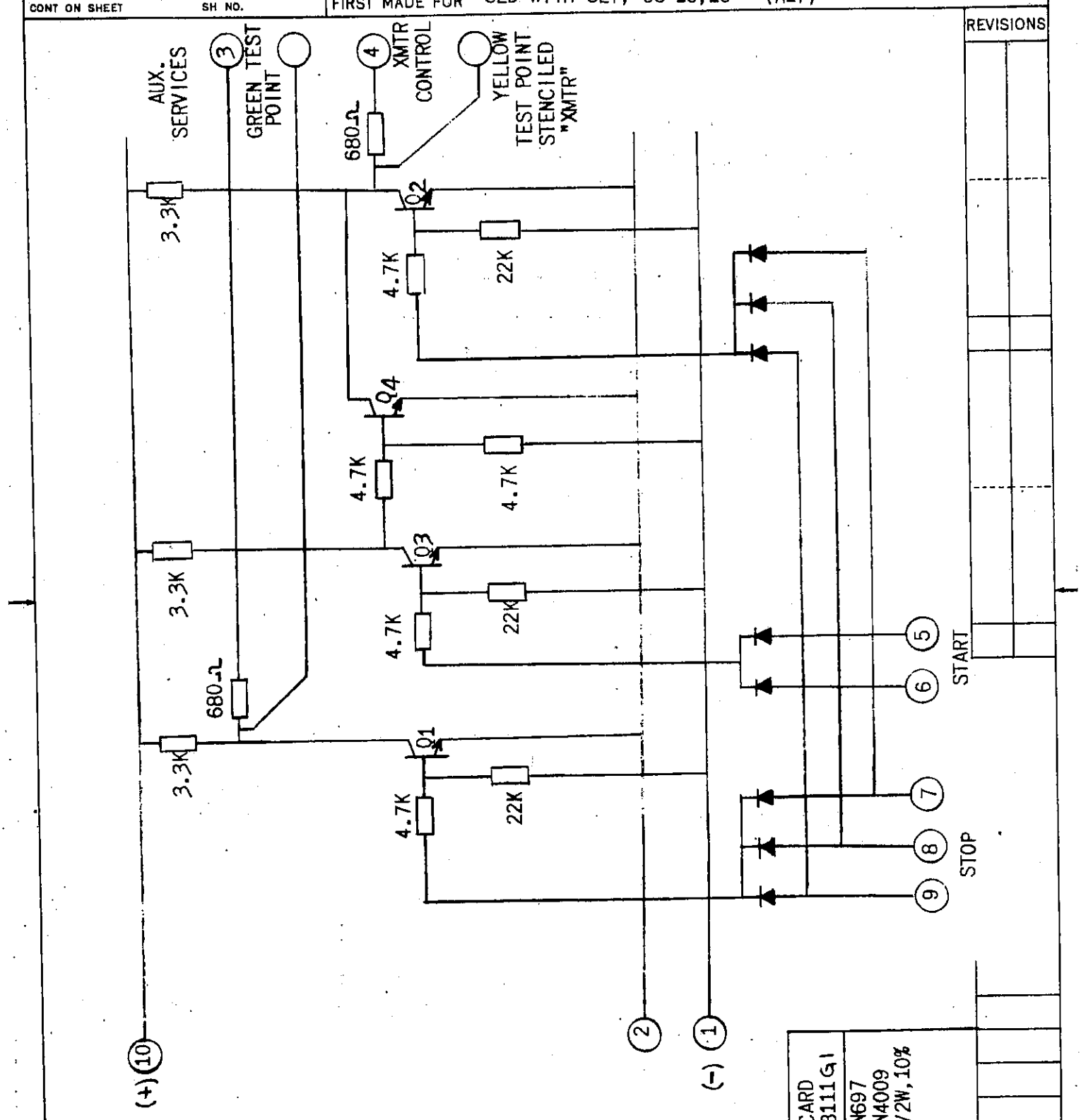
TITLE CARRIER CONTROL

0148A3911AE

CONT ON SHEET SH NO.

FIRST MADE FOR SLD WITH SLY; CS 16,26 (A17)

FIG-26D



REVISIONS

P.C. CARD 0127B8111G1

ALL Q-2N697
D-1N4009
R-1/2W, 10%

PRINTS TO

MADE BY R Buchtold NOV. 17, 1964

ISSUED Nov. 30, 1964

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0148A3911AE

CONT ON SHEET SH NO.

CODE IDENT NO.

ISSD D

EE-403-WA (9-63)

CODE H

GENERAL ELECTRIC

0148A3910AG

CONT ON SHEET SH NO.

REV NO. -1-

0148A3910AG

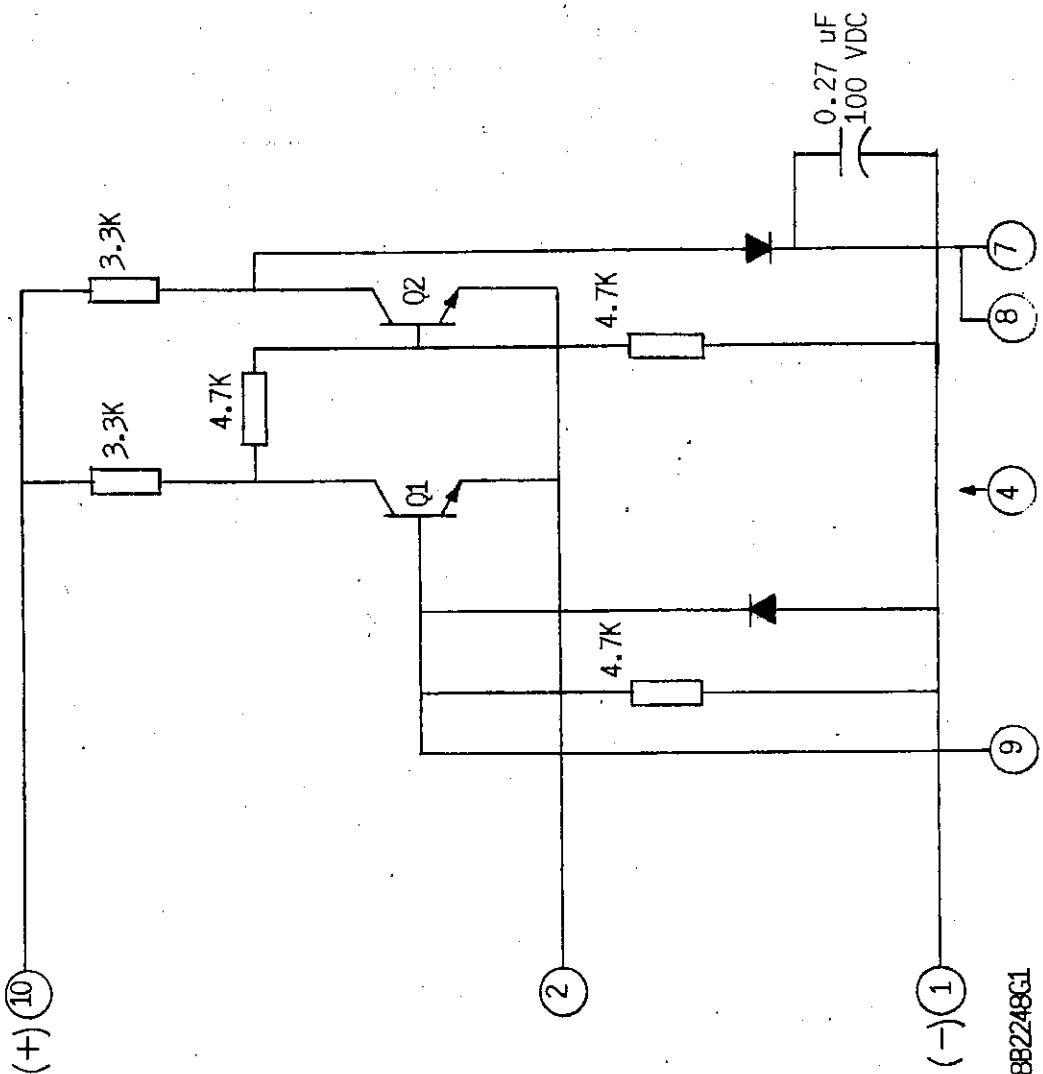
CONT ON SHEET SH NO.

TITLE CONTACT CONVERTER (SINGLE)

FIRST MADE FOR SLD41

FIG-26E (A22)

REVISIONS



1 TERMINALS 10

PC CARD 0128B2248G1
ALL Q-2N697
D-1N4009
R-1/2W,10%

PRINTS TO

MADE BY R Bechtold NOV. 25, 1964

ISSUED

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0148A3910AG

CONT ON SHEET SH NO.

CODE H

GENERAL ELECTRIC

0148A3918AD
CONT ON SHEET SH NO.

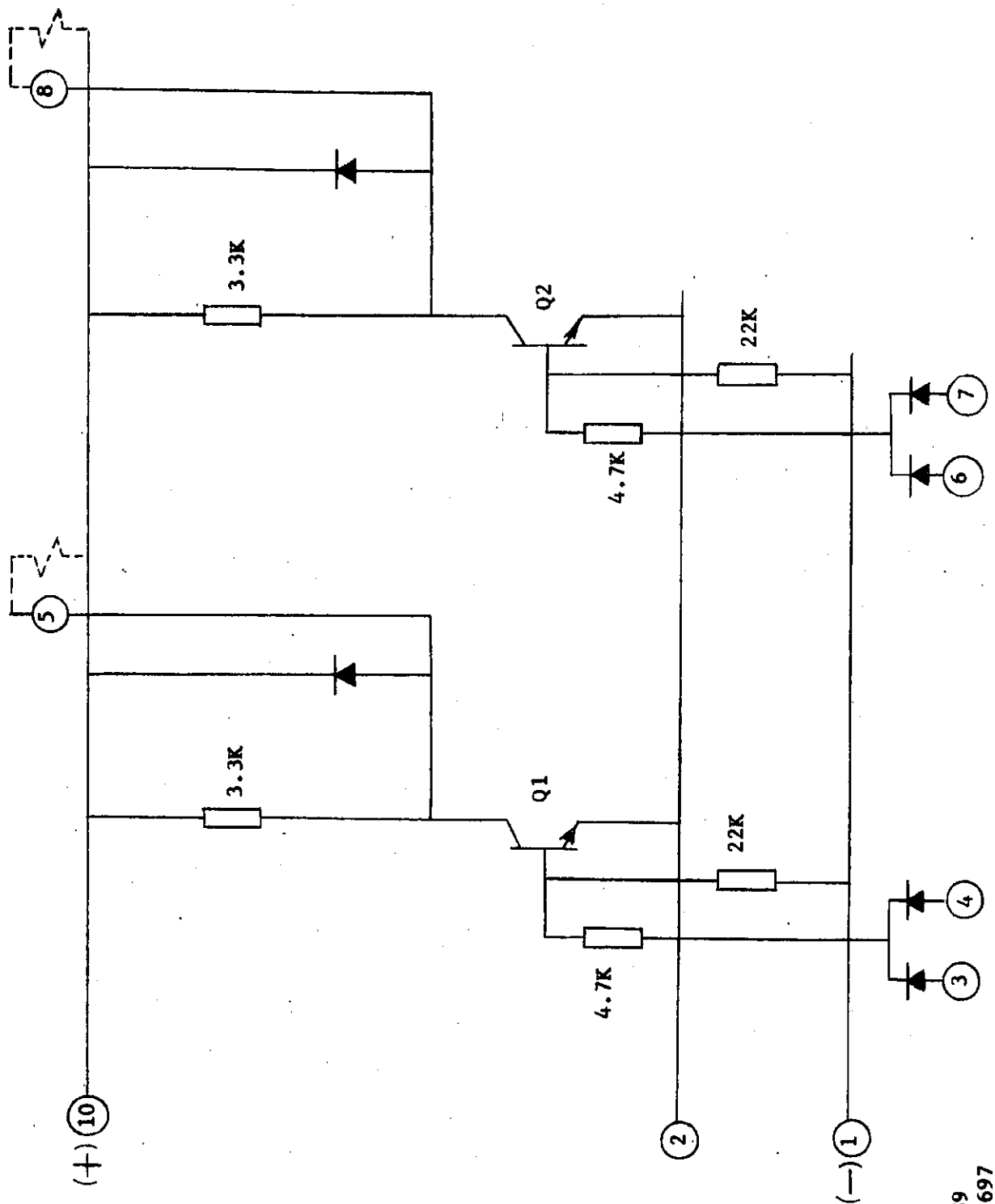
REV NO. 0148A3918AD
CONT ON SHEET SH NO.

TITLE
2 RELAY DRIVERS

FIG-26F

FIRST MADE FOR SLD42D (A28)

REVISIONS



TERMINALS 1 10

PC CARD
0137B8389
ALL Q-2N697
D-1N4009
R-1/2W,10%

PRINTS TO

MADE BY
ISSUED J. Cannon Jan. 15 1965

APPROVALS

SWITCHGEAR
PHILADELPHIA
DIV OR DEPT.
LOCATION

0148A3918AD
CONT ON SHEET SH NO.

FF-802-WA (4-65) REV.
PRINTED IN U.S.A.

SP-R

CODE IDENT NO.

H

GENERAL ELECTRIC

0148A3902AK

CONT ON SHEET SH NO.

REV NO. 1-

0148A3902AK

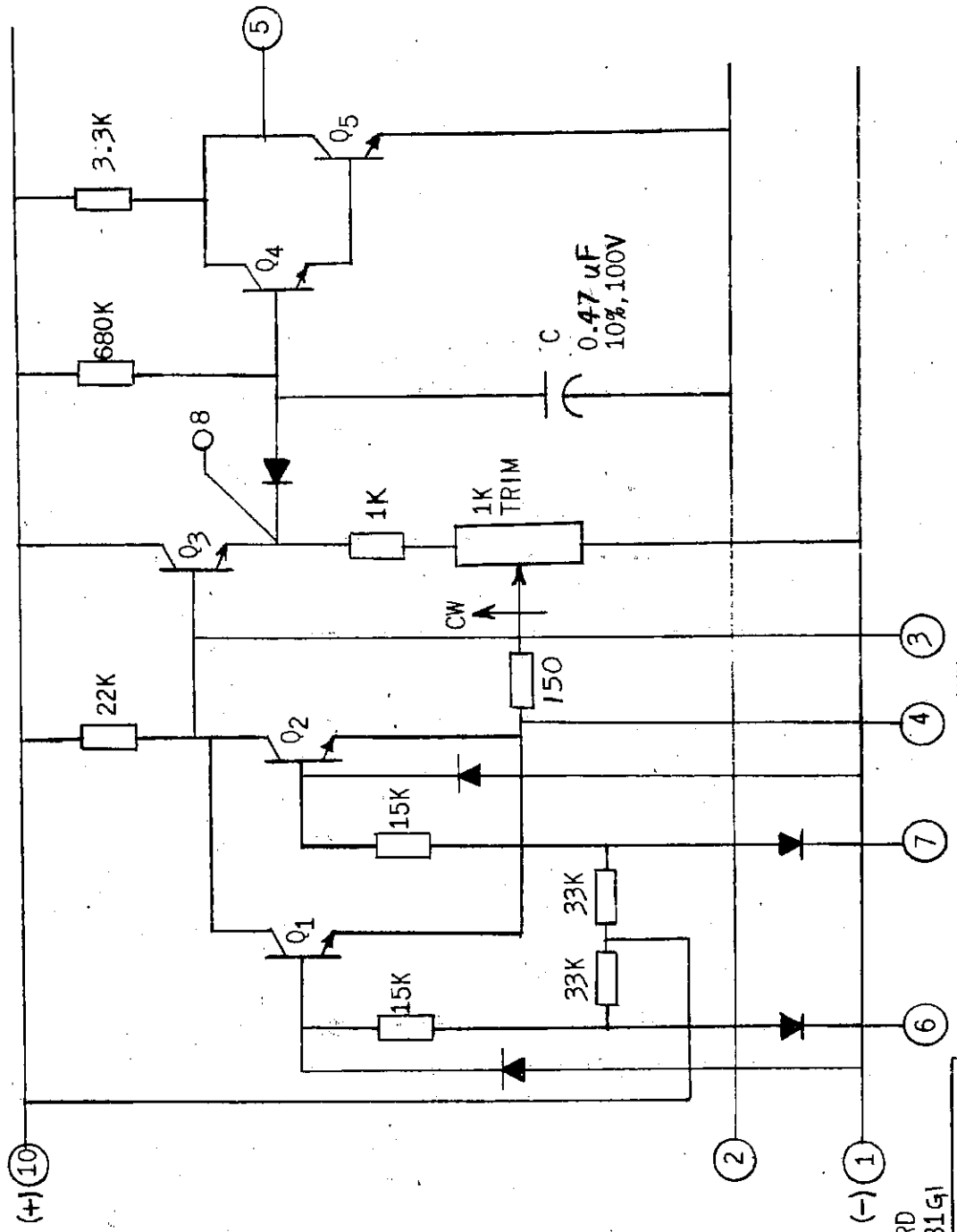
CONT ON SHEET SH NO.

TITLE LEVEL DETECTOR

FIRST MADE FOR SLD WITH SLY (D16)

FIG-26G

REVISIONS



ALL Q - 2N697
D - 1N4009
R - 1/2W, 10%

NOTE: CW ROTATION OF POT INCREASES PICK UP VOLTAGE

PICK UP RANGE 0.4-3.2V RMS AT (7)

P.C. CARD 0127B8131G1

TERMINALS 1 10

PRINTS TO

MADE BY R. Bechtold NOV. 17, 1964

ISSUED December 11, 1964

APPROVALS

SWITCHGEAR — DIV OR DEPT.

PHILADELPHIA — LOCATION

0148A3902AK

CONT ON SHEET SH NO.

A

GENERAL ELECTRIC

0148A3902AM

REV NO. 0148A3902AM

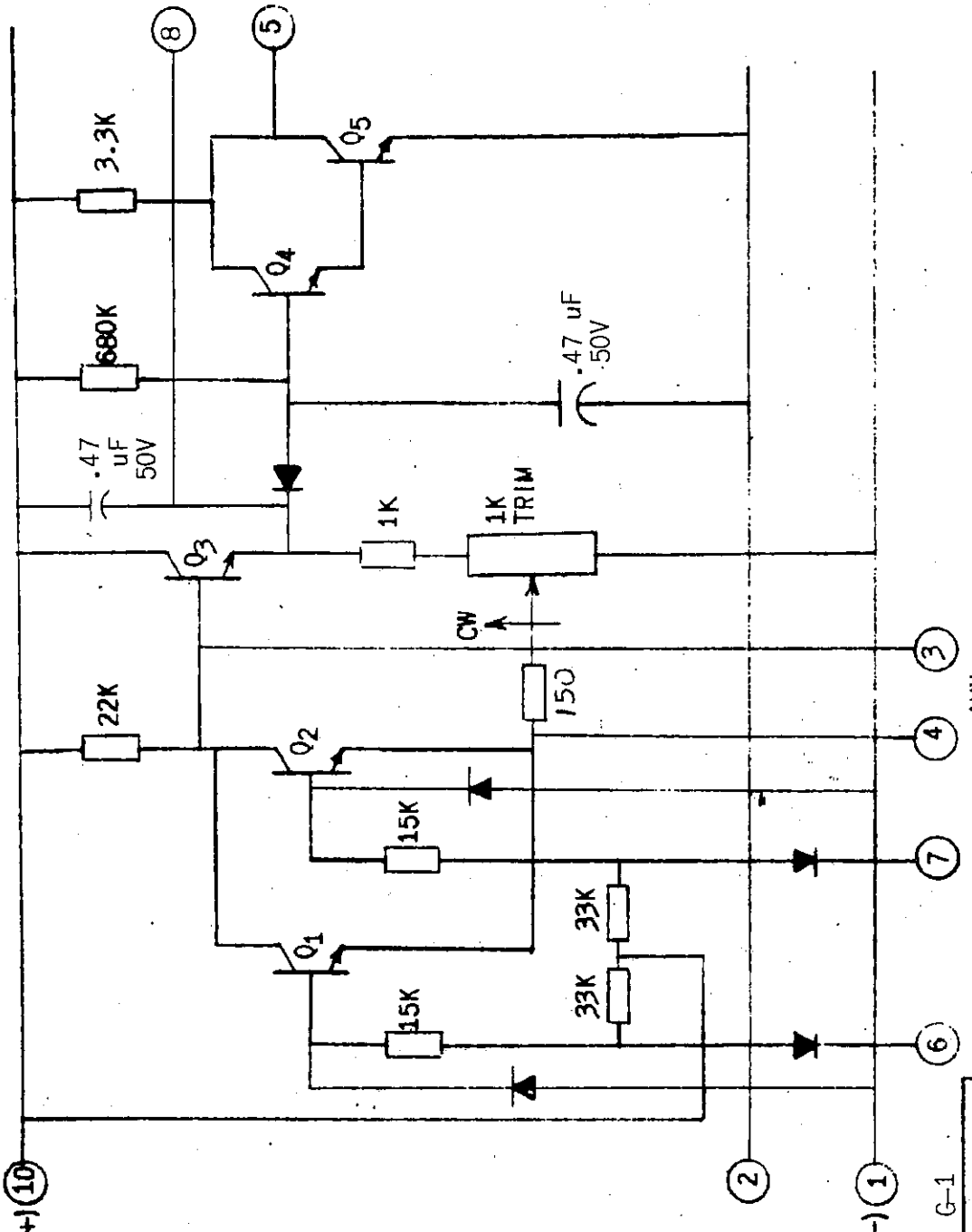
CONT ON SHEET SH NO

TITLE LEVEL DETECTOR FOR DIRECT TRIP APPLICATIONS

FIRST MADE FOR 'SLD WITH 'SLY (D21)

FIG-26H

REVISIONS



ALL Q – 2N697
D – 1N4009
R – 1/2W, 10%

NOTE: CW ROTATION OF POT INCREASES PICK UP VOLTAGE

PICK UP RANGE 0.4-3.2V RMS AT 7

P.C. CARD 0128B2286 G-1

TERMINALS 1 10

PRINTS TO

MADE BY R. Berntold MAR. 11, 1965

ISSUED April 1, 1965

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0148A3902AM CONT ON SHEET SH NO.

USP-R

CODE IDENT NO

CODE A

GENERAL ELECTRIC

0148A3912AC

REV NO

0148A3912AC

CONT ON SHEET NO.

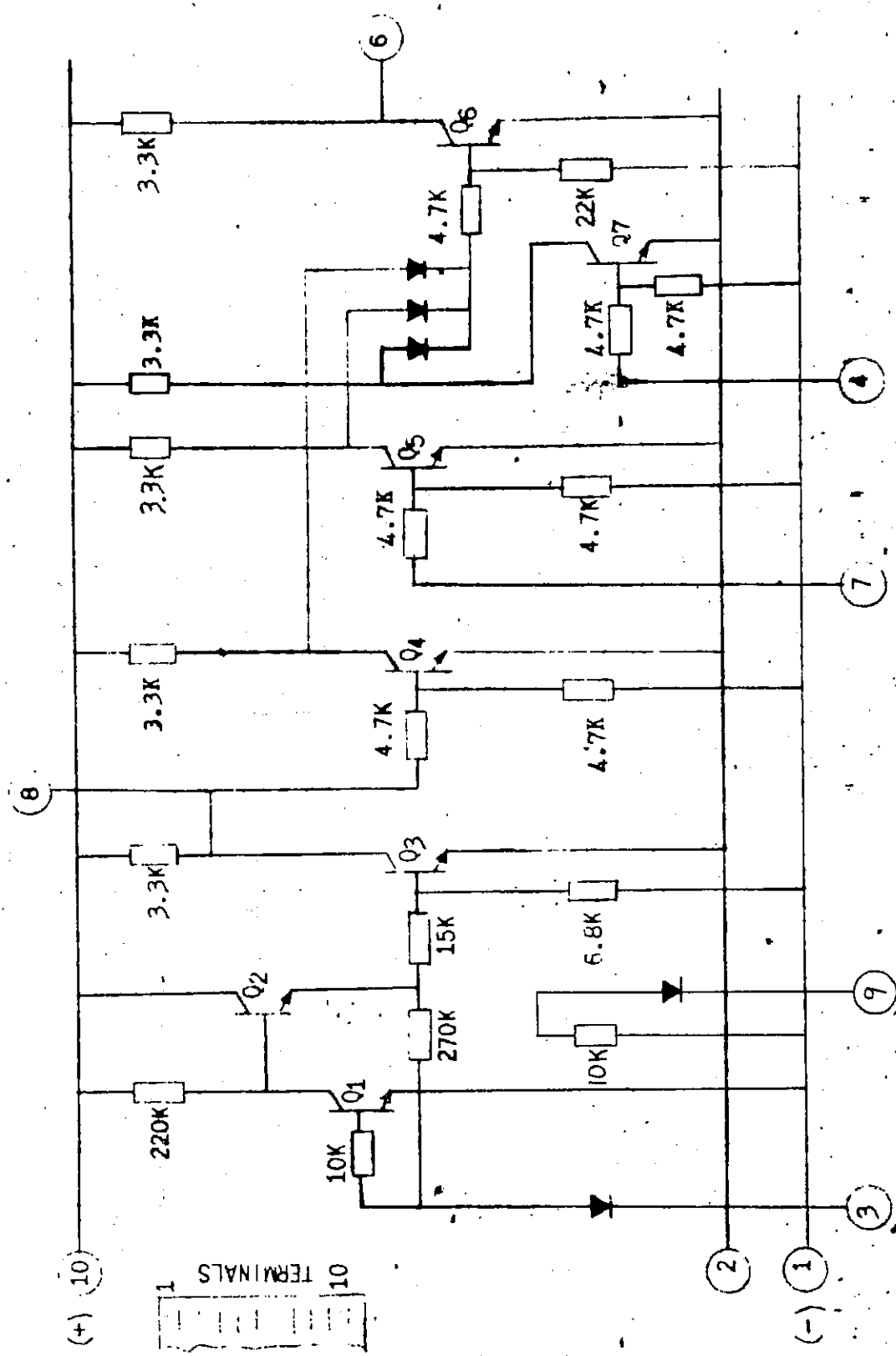
SQUARING AMPLIFIER AND
"AND—41" FUNCTION

FIRST MADE FOR SLD41A

(D22A)

FIG-261

REVISIONS



OUTPUT (8) IS AMPLIFIED (3) INPUT.
OUTPUT AT (6) FOR INPUTS AT (7) (8) AND (4)

P.C. CARD
0137B8309G-2

ALL Q - 2N697
D - 1N4009
R - ½W, 10%

PRINTS TO

DRAWN BY	APPROVALS		
J. Wetzel Jan. 10, 66 Jan. 12, 1966		SWITCHGEAR PHILADELPHIA	DIV OR DEPT LOCATION

0148A3912AC

DRAWING NO

SH NO

A

GENERAL ELECTRIC

C148A3901AY

CONT ON SHEET SH NO.

REV

C148A3901AY

CONT ON SHEET SH NO.

TITLE

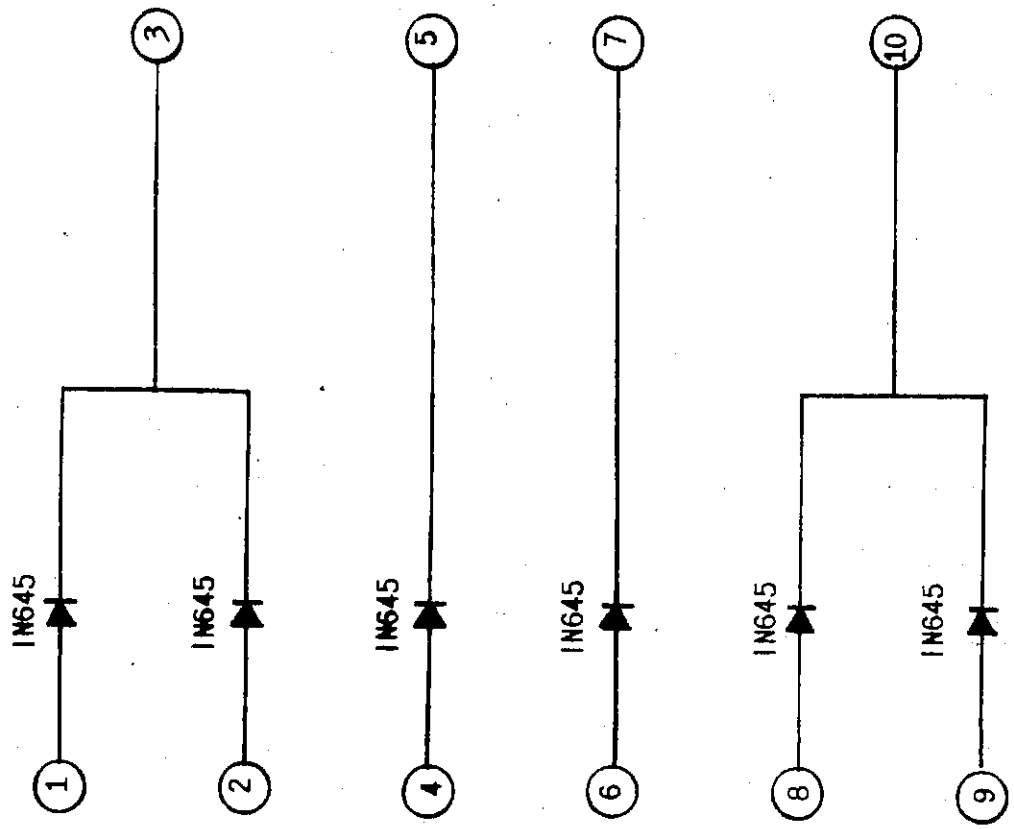
2 OR; 2 OR; 2 DIODES

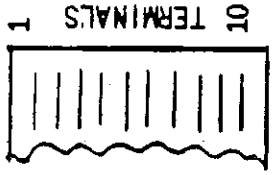
FIG-26J

L12

FIRST MADE FOR SLA13A

REVISIONS





PC CARD 0127B8159 G1

PRINTS TO

MADE BY G. Sudnick March 2, 1964

ISSUED March 9, 1964

APPROVALS REP

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

C148A3901AY

CONT ON SHEET SH NO.

FF-803-WA (6-63)

GENERAL ELECTRIC

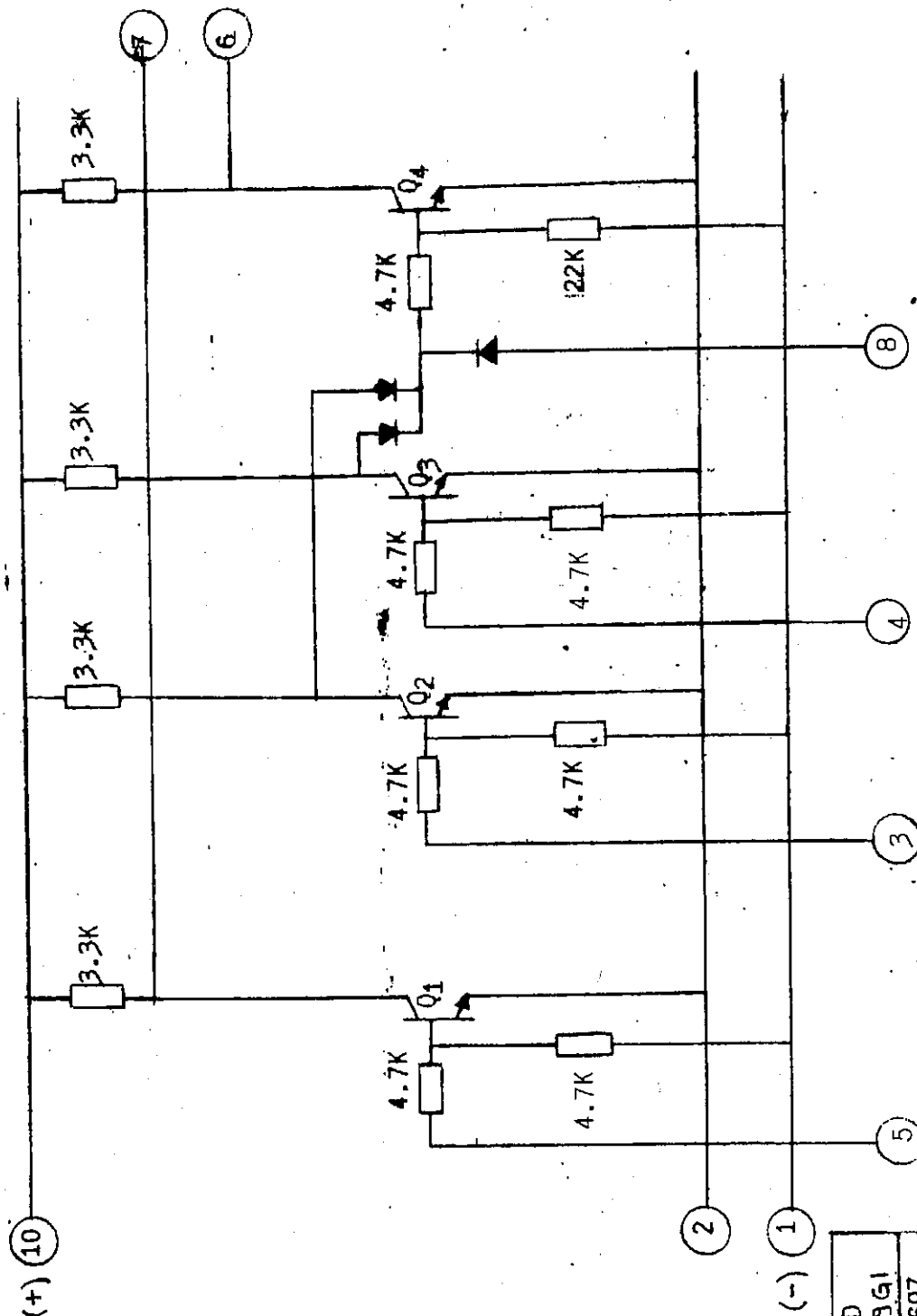
0148A3901BB
CONT ON SHEET SH NO.

REV NO.
0148A3901BB
CONT ON SHEET SH NO.

TITLE
LOGIC FUNCTION-3 INPUTS

FIRST MADE FOR SLD (L16) FIG-26K

REVISIONS



TERMINALS 1 10

P.C. CARD
D128B2393G1
ALL Q -2N697
D -1N4009
R -¼W, 10%

PRINTS TO

MADE BY R Bechtold NOV. 17, 1964
ISSUED December 14, 1964
APPROVALS
SWITCHGEAR DIV OR DEPT.
PHILADELPHIA LOCATION
0148A3901BB
CONT ON SHEET SH NO.

GENERAL ELECTRIC

0148A3901BH
CONT ON SHEET SH NO.

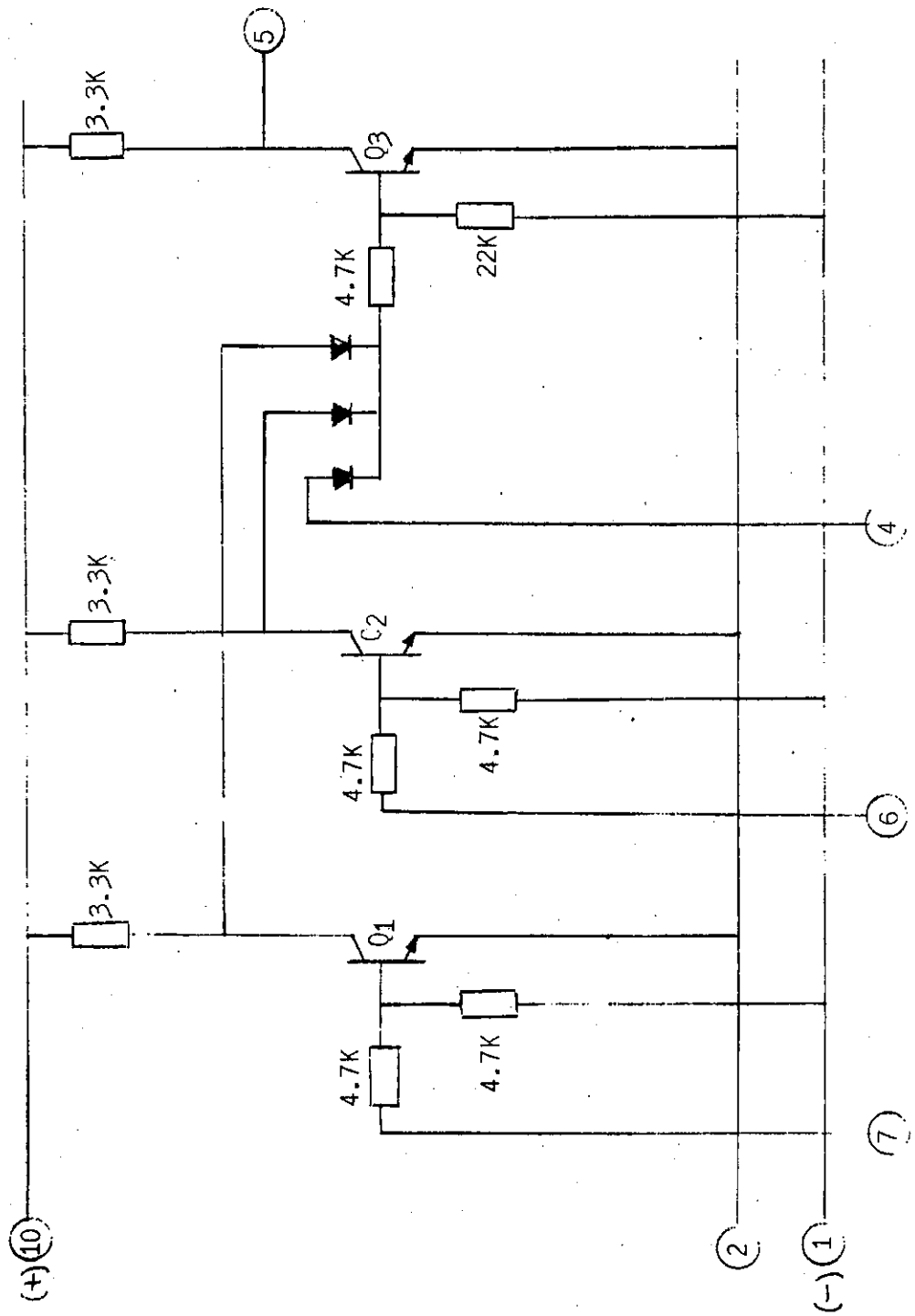
REV NO. 0148A3901BH
CONT ON SHEET SH NO.

TITLE
LOGIC FUNCTION

FIG-26L

FIRST MADE FOR SLD WITH SLY (L18)

REVISIONS



OUTPUT AT (5) FOR INPUTS AT (6) AND (7) AND NOT (4)

P.C. CARD 0127B8117G1
ALL Q - 2N697
D - 1N4009
R - 1/2W, 10%

PRINTS TO

MADE BY R Berkstresser NOV. 17, 1964
ISSUED

APPROVALS

SWITCHGEAR DIV OR DEPT.
PHILADELPHIA LOCATION

0148A3901BH
CONT ON SHEET SH NO.

FE-803-WA (9-63)

CODE IDENT NO

CODE H

GENERAL ELECTRIC

0148A3901BG

CONT ON SHEET SH NO.

REV NO.

0148A3901BG

CONT ON SHEET SH NO.

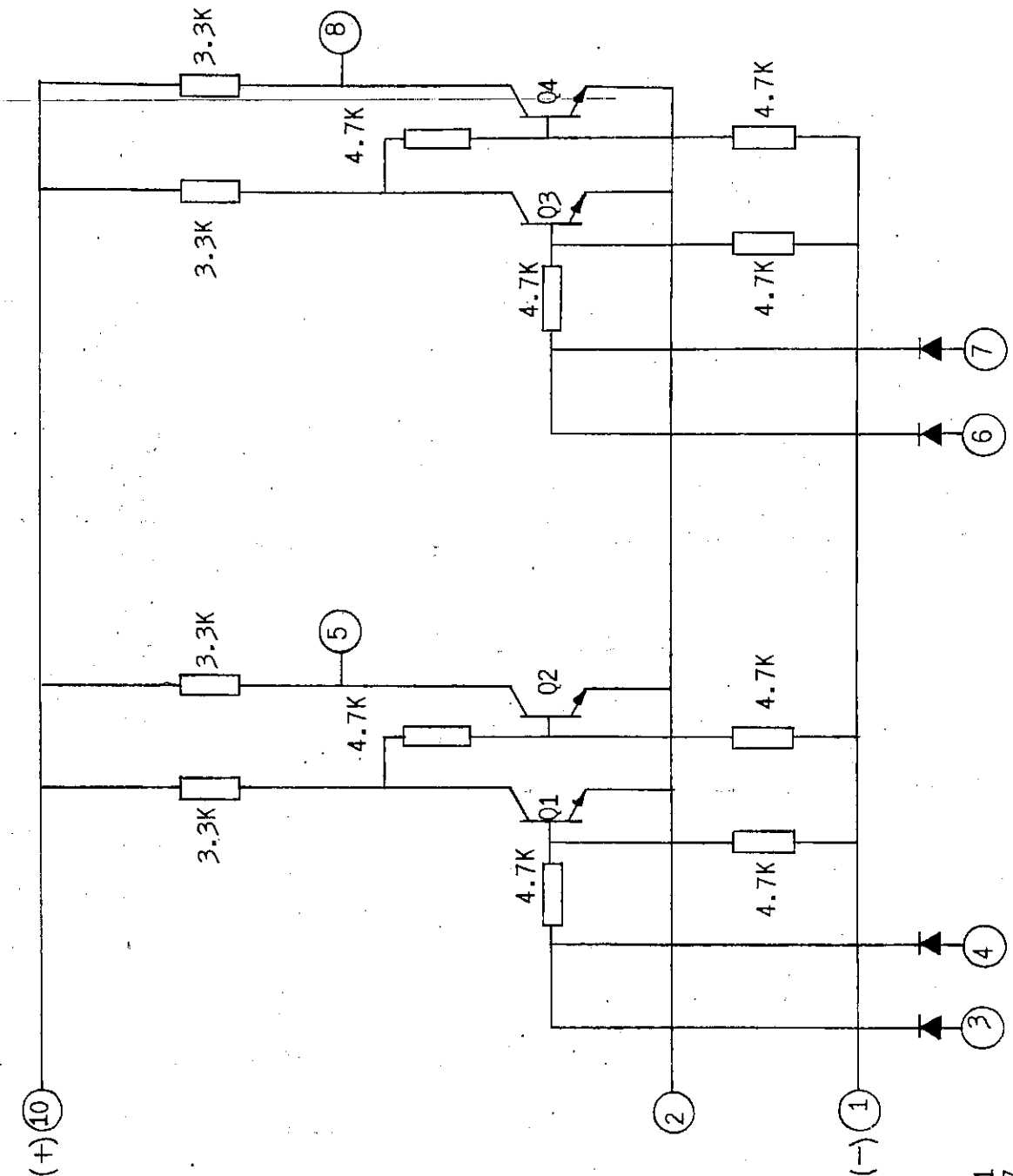
TITLE LOGIC FUNCTION

FIG-26M

(L19)

FIRST MADE FOR SLD41

REVISIONS



OUTPUT AT (5) FOR INPUT AT (3) OR (4)
OUTPUT AT (8) FOR INPUT AT (6) OR (7)

PC CARD
0128B2208G1
ALL Q-2N697
D-1N4009
R-½W, 10%

TERMINALS 1 10

PRINTS TO

MADE BY R Bichtold NOV 20, 1964

ISSUED December 19, 19--

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0148A3901BG

CONT ON SHEET SH NO.

CODE A

GENERAL ELECTRIC

0148A3901BM
CONT ON SHEET SH NO.

REV NO. X-3-

0148A3901BM
...T ON SHEET SH NO.

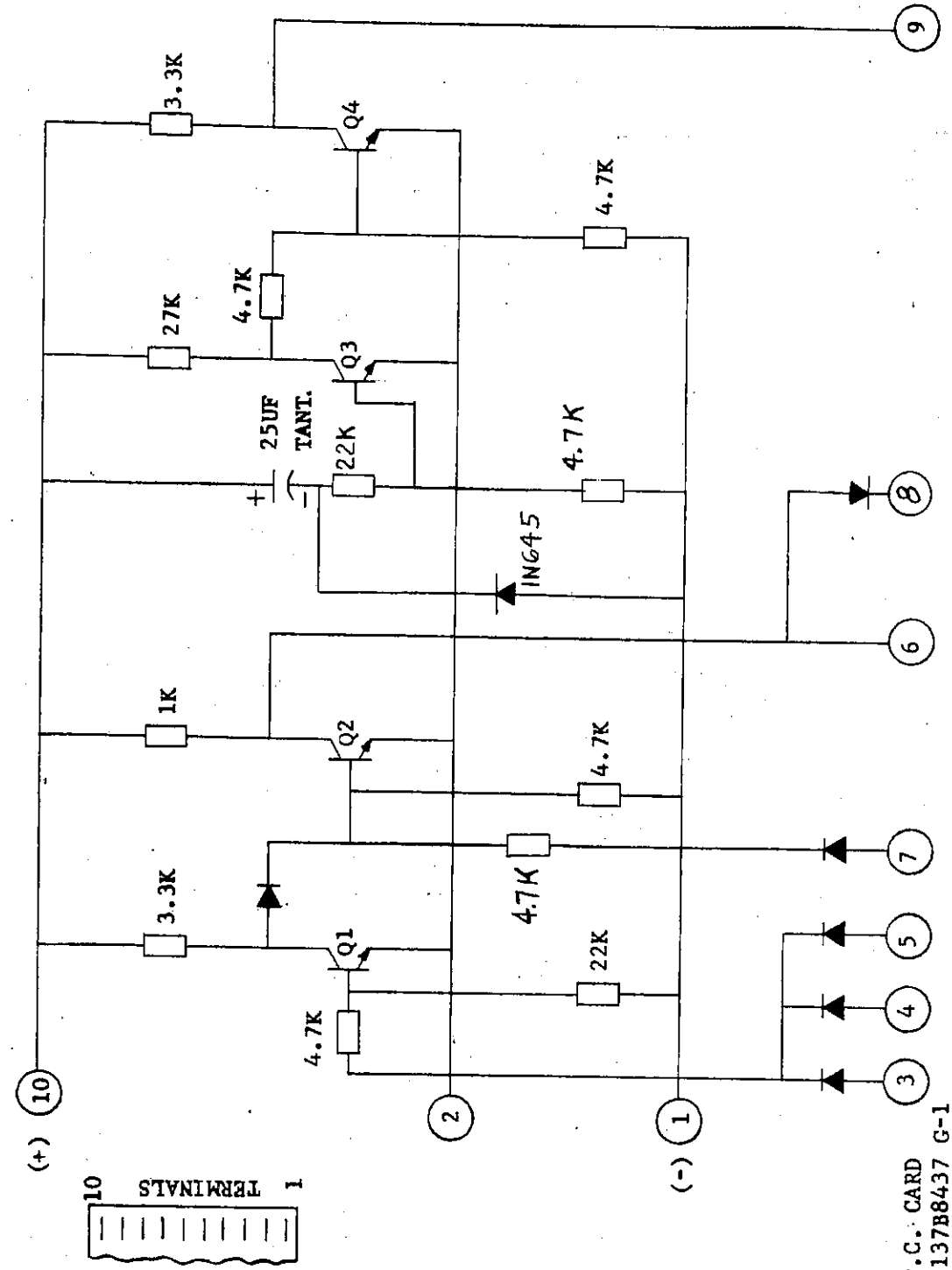
TITLE
TRIP LOGIC WITH 500 MS
TIME DELAY AFTER D.C.

FIG-26N

FIRST MADE FOR SLD WITH SLYL

(L23)

REVISIONS



PRINTS TO

MADE BY J. Katz 7 Apr. 7, 66

ISSUED [illegible] 22 1966

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

SP-R

0148A3901BM
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CODE IDENT NO.

FF-803-WA (6-65)
PRINTED IN U.S.A.

CODE H GENERAL ELECTRIC

0148A3906AN

CONT ON SHEET SH NO.

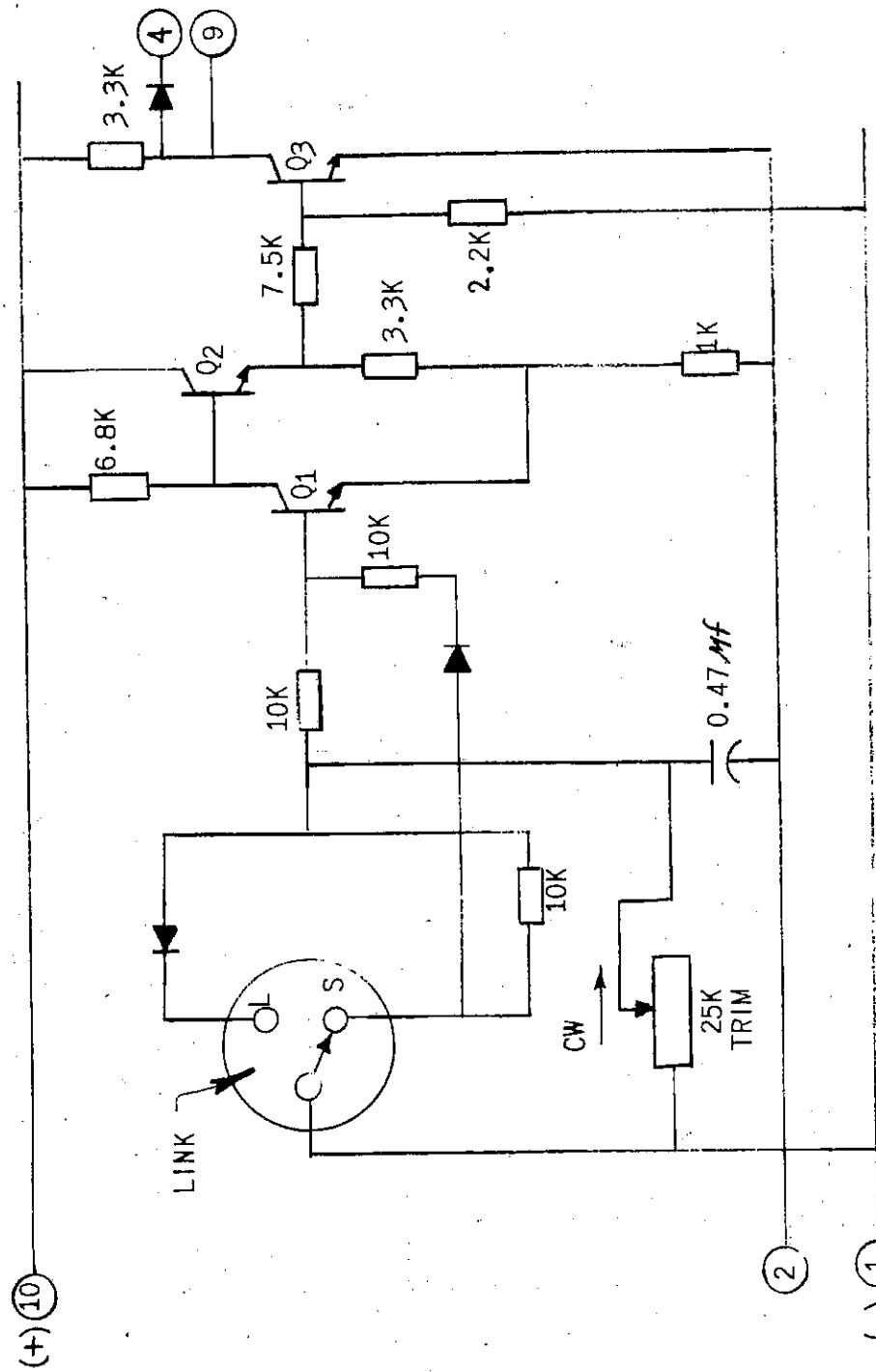
REV NO. /-

0148A3906AN

CONT ON SHEET SH NO.

TITLE
SYMMETRY ADJUST

FIRST MADE FOR SLD WITH SLY (T16) FIG-26P



LINK FUNCTIONS:
L: OUTPUT AT ⑨ HAS TIME DELAY ON PICK-UP, FROM INPUT AT ⑦ THIS MAKES OUTPUT PULSE SHORTER THAN INPUT; CARRIER TRANSMISSION PULSES ARE LONGER.
S: OUTPUT HAS TIME DELAY DROP-OUT, SO CARRIER PULSES ARE SHORTER.

ALL Q-2N697
D-1N4009
R-1/2W, 10%
C-100V, 10%

P.C. CARD
0127B8147G1

CW ROTATION OF POT INCREASES TIME DELAY PICK-UP OR DROP-OUT AT ④ AND ⑨ FOR ⑦ INPUT

1 TERMINALS 10

REVISIONS

PRINTS TO

MADE BY R. Bechtold Nov. 17, 1964
ISSUED

APPROVALS

SWITCHGEAR DIV OR DEPT.
PHILADELPHIA LOCATION

0148A3906AN

CONT ON SHEET SH NO.

CODE L

GENERAL ELECTRIC

0148A3906AL

CONT ON SHEET SH NO.

REV NO. 1-2-3-

0148A3906AL

CONT ON SHEET SH NO.

TITLE

TIME DELAY PICKUP & DROPOUT

FIG-26Q

T20

FIRST MADE FOR SLD41

REVISIONS

3	11-11-64	J. Wetzel	
2	9-23-64	J. Wetzel	
1			

TIME DELAY PICKUP

FOR TIME DELAY DROP-OUT, JUMPER TERM. ⑥ TO ②, GET 7-50 MS.

JUMPER TERM. ⑦ TO ⑩ FOR 7-14 MS
JUMPER TERM. ⑨ TO ⑩ FOR 14-28 MS
NO JUMPER FOR 28-40 MS

NOTE: CLOCKWISE ROTATION OF
R1 INCREASES PICK-UP TIME DELAY
R2 INCREASES DROP-OUT TIME DELAY

ALL D-IN4009
ALL Q-2N697
ALL R-1/2W, 10%
ALL Z-1N754 (6.8 V)

PC CARD 0128B2241G1

PRINTS TO

MADE BY J. Wetzel Dec. 8, 64

ISSUED

APPROVALS

SWITCHGEAR
PHILADELPHIA

DIV OR DEPT.
LOCATION

0148A3906AL

CONT ON SHEET SH NO.

LSP-R

CODE IDENT NO.

FF-503-WA (1-64)
PRINTED IN U.S.A.

CODE A

GENERAL ELECTRIC

0148A3906AY

CONT ON SHEET SH NO.

REV NO. -X2-3-

0148A3906AY

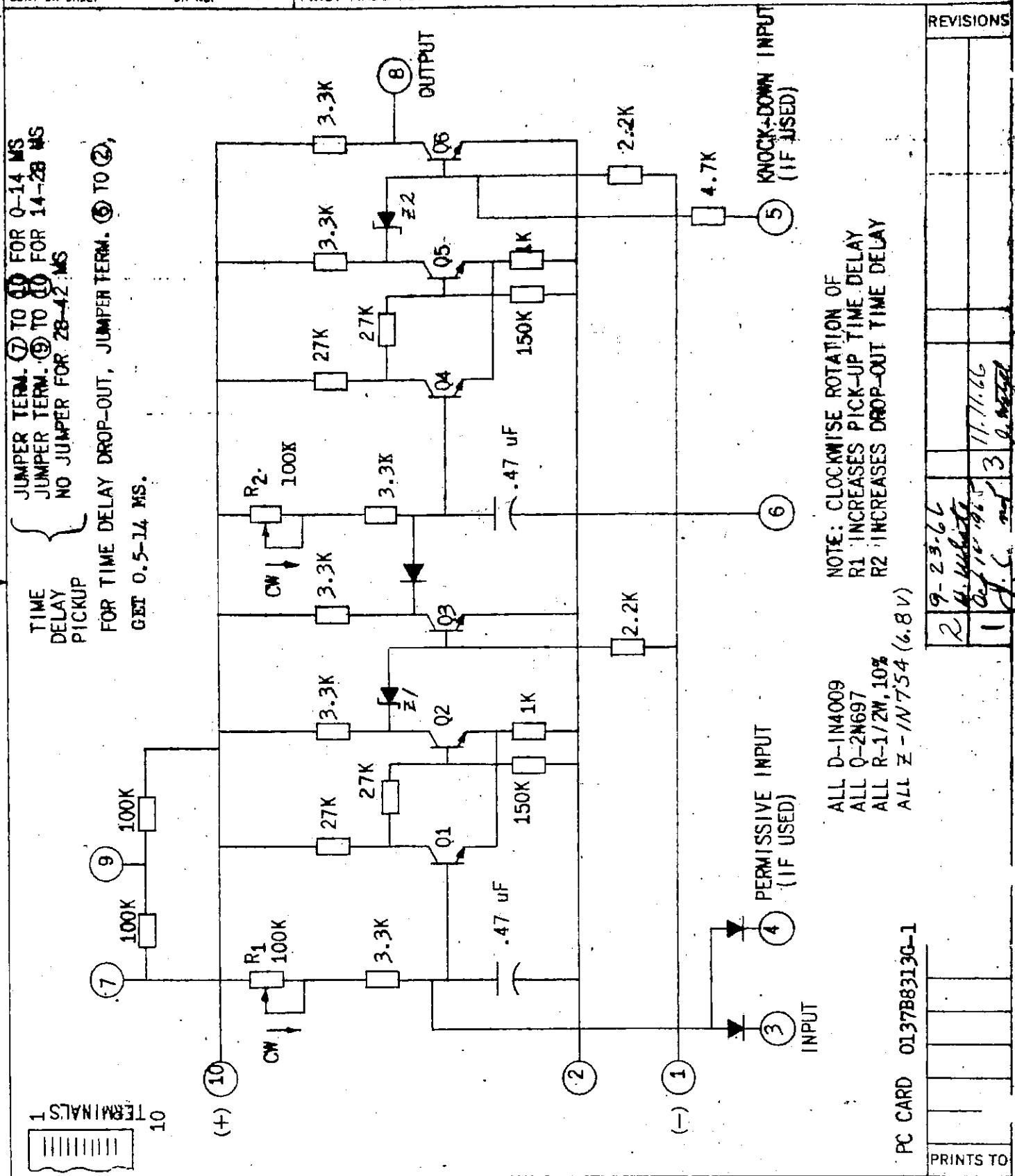
CONT ON SHEET SH NO.

TITLE

PHASE DELAY TIMER

FIG-26R

FIRST MADE FOR SLD41 (T25)



REVISIONS

3	11.11.66		
2	9-23-66		
1	8-10-65		

PC CARD 0137B8313G-1

PRINTS TO

MADE BY J. Conner Aug. 31, 1965

ISSUED September 15, 1965

APPROVALS

SWITCHGEAR DIV OR DEPT.

PHILADELPHIA LOCATION

0148A3906AY

CONT ON SHEET SH NO.

CODE A

GENERAL ELECTRIC

0148A3913AD

CONT ON SHEET SH NO.

REV NO. 1-

0148A3913AD

CONT ON SHEET SH NO.

TITLE

PULSE STRETCHER WITH ADJ. D.O. TIME (20-200MS.)

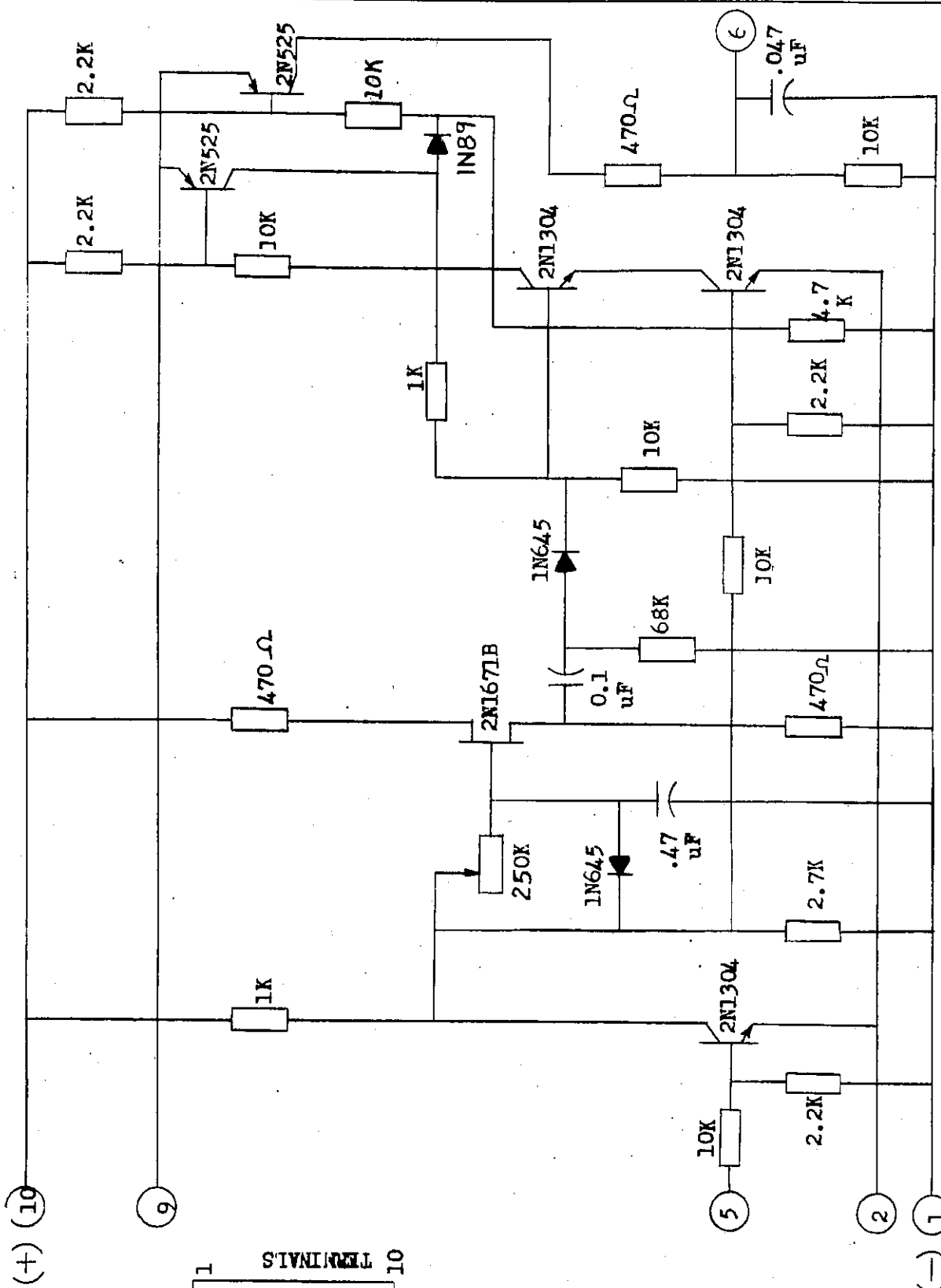
FIG-26S

FIRST MADE FOR SLA17

T27

REVISIONS

1-19-66 J. Nuttall



PC CARD 0137B8356G-1

PRINTS TO

MADE BY Lucas Prince Nov. 3, 1965

ISSUED Nov 8, 1965

APPROVALS

SWGR PHILA

DIV OR DEPT.

LOCATION

0148A3913AD

CONT ON SHEET SH NO.

TF-803-WA (8-64)

CODE IDENT NO