INSTRUCTIONS

GEK-36791C
Supersedes GEK-36791B

# STATIC PHASE COMPARISON RELAY

## TYPE SLD51A

GENERAL ELECTRIC

CONTENTS



NOTE: This instruction book has been revised to include the 50 hertz model of the SLD51A Relay.

# STATIC PHASE COMPARISON RELAY

# TYPE SLD51A

## DESCRIPTION

The Type SLD51A relay is a static phase comparison relay designed to provide high speed protection of transmission lines. The SLD51A is packaged in one two-rack unit case, as shown in Figure 1. The component location diagram is shown in Figure 2, and the internal connections diagram is shown in Figure 3.

The SLD51A is not intended to be used by itself, but rather as part of a complement of equipment that forms a phase comparison protective relaying scheme. Typically in addition to the SLD51A relay, a Type SLAT auxiliary logic and output relay, and a Type SSA power supply are required to complete a protective scheme. Additional relays may be required, such as a suitable phase distance relay for a combined phase and directional comparison scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and the associated logic description supplied with each terminal of equipment. Since the SLD51A relay is always supplied as part of an overall equipment, the external connections are shown on the elementary diagram supplied with each terminal of equipment.

## APPLICATION

The Type SLD51A phase comparison relay is designed to provide high-speed protection of transmission lines against all phase and ground faults when operated in the mixed excitation mode. The term "mixed excitation," when applied to phase comparison, describes a scheme that mixes different sequence quantities in a given proportion and phase angle, then performs the phase comparison based on this mix. The best overall results are obtained by using a single-phase quantity proportional to the vector quantity $(I_2 - I_1/K)$, where K is an integer scalar quantity, selectable by tap settings as 5, 7 or 10. It is also possible to select K equal to infinity, such that the phase comparison is performed on the basis of negative sequence excitation only.

When mixed excitation is employed, the SLD51A is applied in a straight phase comparison scheme; when pure negative sequence is employed, the SLD51A is applied in a combined phase and directional comparison scheme. In a combined scheme, the negative sequence phase comparison protects against all unbalanced faults, and a suitable phase distance relay is used to protect against three phase faults. A straight phase comparison scheme is not recommended where negative sequence excitation is employed. A balanced external three phase fault may result in spurious negative sequence outputs at each terminal due to CT saturation. The amount of saturation is dependent upon CT quality, amount of residual magnetism in the core, and fault current magnitude. Consequently, the poorer the CTs, the more residual magnetism is present; the higher the fault current magnitude, the greater

the spurious negative sequence quantity. On a statistical basis, the phase angle between these spurious negative sequence outputs may be such that a trip output can result for this external fault condition. In a combined phase and directional comparison scheme, the phase distance functions will respond to this external three phase fault, and the directional comparison portion of the scheme will take preference over the phase comparison, thus preventing a misoperation. When mixed excitation is employed, consideration must also be given to the spurious negative sequence output that may result from an external three phase fault. One consideration in selecting the K factor is that a sufficient through-fault positive sequence quantity must be produced, such that the total phase comparison keying quantity, $(I_2 - I_1/K)$, maintains the proper phase relationship for an external three phase fault. If high fault current magnitudes are coupled with poor CT quality, the highest value of K (K = 10) can prove inadequate from this security point of view. For this reason, each application should be initially attempted with K = 7 to meet the other constraints on the K factor, as outlined below.

The Type SLD51A relay is most frequently used with mixed excitation in a blocking mode incorporating an ON-OFF type of power line carrier channel equipment. It can also be used with mixed excitation in either (1) a blocking or permissive mode utilizing frequency shift tones on microwave or a pilot wire, or (2) an unblocking mode utilizing a frequency shift power line carrier channel.

The following application considerations will be divided into three main headings: (1) Straight Phase Comparison-Blocking Mode; (2) Straight Phase Comparison-Permissive Mode; (3) Combined Phase and Directional Comparison. Each mode of operation has unique application considerations, and the mode of operation of a particular equipment will be stated in the logic description associated with the overall logic diagram for that equipment.

## STRAIGHT PHASE COMPARISON-BLOCKING MODE

In a straight phase comparison scheme, the single phase quantity $(I_2 - I_1/K)$ is used as the keying quantity to perform the phase comparison between the terminals of the line, and the same quantity is used to operate the level detectors, FDL and FDH.

The following settings must be made prior to placing the equipment in service:

### FDL Level Detector Settings:

Where the channel may also perform other functions, it is usually considered objectionable to key continuously. Consequently, FDL pickup must be set above the $I_1/K$ output of the mixing network for the maximum expected load. With other types of channels, e.g., tones on microwaves, where a separate channel independent of other functions is asigned to the phase comparison relaying, the channel may be keyed continuously. In such cases, FDL could be set well below the $I_1/K$ output of the mixing network resulting from maximum load.

Assuming a 10 percent margin above full load, the FDL setting is defined by:

$$FDL = 1.1 \left(\frac{I_{1L}}{K}\right) \qquad \text{(Eq. 1)}$$

where: FDL = required pickup setting of FDL in negative sequence amperes
$I_1L$ = maximum load (secondary) in amperes
K = setting of K tap (5, 7, 10)

FDH Level Detector Setting

In this blocking mode application, the setting of FDH must be sufficiently above the pickup of FDL at the remote terminal of the protected line to insure proper coordination when an external fault occurs. Equations to determine the required FDH setting for two-terminal or three-terminal lines are given below. These equations take into account the negative sequence charging current flowing in the line during an external fault. This negative sequence charging current can be expressed in terms of the total positive sequence charging current present under normal conditions (see Appendix I).

Two-terminal:

$$FDH = \left(\frac{4}{3}\right) FDL + 0.375\ I_{C1} \qquad \text{(Eq. 2)}$$

Three-terminal:

$$FDH = \left(\frac{8}{3}\right) FDL + 0.375\ I_{C1} \qquad \text{(Eq. 3)}$$

where: FDH = required pickup setting of FDH in negative sequence amperes
$I_{C1}$ = total positive sequence charging current under normal conditions

FDL can be set lower than the value defined in equation 1, on applications involving channels where continuous keying is not objectionable. However, it must be emphasized that in the straight phase comparison scheme, FDH must be set high enough so that it will not operate on maximum load, regardless of the FDL pickup level. On any internal fault, regardless of the type of fault or the phases involved, the sequence network output $(I_2 - I_1/K)$ at each terminal must be sufficient to operate FDH. Application of the SLD51A relay in a straight phase comparison mode is obviously limited to lines where the minimum three phase fault current is higher than maximum load current. Where FDL may be set at below full load, FDH should be set at least 15 percent above full load.

$$FDH = 1.15 \left(\frac{I_{1L}}{K}\right) \qquad \text{(Eq. 4)}$$

To retain the same margins defined by equations 2 and 3, FDL must be set for the values defined below:

Two-terminal:

$$FDL \leq \frac{3}{4} (FDH - 0.375\ I_{C1}) \qquad \text{(Eq. 5)}$$

Three-terminal:

$$FDL \leq \frac{3}{8} (FDH - 0.375\ I_{C1}) \qquad \text{(Eq. 6)}$$

K Tap Setting:

Three K taps of 5, 7 or 10 are available. A high K tap setting tends to minimize the undesirable effects of load flow during an internal fault, and thus permit broader application limits. However, low K tap settings result in greater security on external three phase faults for reasons previously stated. The K tap selected directly influences the phase angle between the keying quantities at each terminal during unbalanced internal faults. For any internal fault, regardless of type of fault, combination of phases, or presence of load flow, the maximum phase angle between the keying quantities ($I_2 - I_1/K$) at all terminals must be small enough to assure tripping with adequate margin. It is recommended that the intermediate tap, K = 7, be considered first on any proposed application.

A rigorous and precise determination of the magnitude and relative phase angle of the keying quantity ($I_2 - I_1/K$) for all types of faults, on all combination of phases, for all reasonable system conditions including the effects of load flow during the fault, would require extensive and time consuming calculations. However, a simple and reliable approach has been developed, and is outlined below. All of the following results are based on the assumption that the ratio of system zero sequence impedance to system positive sequence impedance ($Z_0/Z_1$), as viewed from any fault location on the protected line, falls within the range of 0.3 to 3.0. The ratio, $Z_0/Z_1$, for an effectively grounded transmission system is equal to or less than 3.0. Consequently, 3.0 is generally the upper limit on the range of $Z_0/Z_1$. The lower limit on $Z_0/Z_1$ is generally determined for a fault at a generating station where the positive sequence impedance of the generator-transformer combination is significantly greater than the zero sequence impedance. In the majority of cases, $Z_0/Z_1$ for the generator-transformer combination will be no less than 0.3

If $Z_0/Z_1$, as viewed from any fault location on the protected line, can be less than 0.3 or greater than 3.0; or if the constraints on the ratio of minimum internal three phase fault current to maximum load current, as outlined below, cannot be met, then refer the application to the nearest General Electric Company Sales Office. A memo describing a more rigorous and less conservative application approach will be supplied upon request, that may allow a particular application to be implemented, even though the constraints of the simplified approach cannot be met.

The simplified approach is as follows:

1) Select K = 7

2) Determine the maximum load current in secondary amperes. Use K = 7 and equations 1, 2 and 3 to calculate FDL and FDH settings.

3) Determine the ratio of K times FDH setting to minimum full load current (i.e., $K(FDH)/I_{FL}$).

4) Enter the curve of Figure 4 with the value determined from 3) above, and note the ratio of $I_{3\phi}/I_{FL}$ for that abscissa value and K = 7.

5) Determine the minimum secondary current at each terminal for a three phase fault anywhere on the protected line, and divide this by the magnitude of full load current determined in 2) above. If this ratio is equal to or greater than the value of $I_{3\phi}/I_{FL}$ from the curve of Figure 4, then the application can be made with the assurance that any internal fault will result in a margin of at least 50 percent above FDH pickup.

If the calculated ratio of minimum internal three phase fault current to full load current is less than the required ratio, as determined from the curve of Figure 4, then repeat steps 1) through 5) above with K = 10. If the resulting ratio is still not adequate, or if K = 10 is deemed to be unacceptable from a security viewpoint, then the application is not proper based on the above approach. Note that the straight phase comparison scheme may still be applied if less conservative application considerations, such as those outlined in the memo mentioned previously, are utilized. If straight phase comparison cannot be applied, some other scheme, such as combined phase and directional comparison, should be considered.

If the calculated ratio of minimum internal three phase fault current to full load current is substantially greater than the required ratio, as determined from the curve of Figure 4, additional security should be obtained by either raising the FDH pickup setting (leaving FDL alone), or by setting K = 5. In either case, the application would then have to be rechecked. While both higher FDH/FDL settings and lower K settings add to the security of the scheme, there is probably more to be gained by increasing the ratio of FDH/FDL settings than in going from K = 7 to K = 5.

## STRAIGHT PHASE COMPARISON-PERMISSIVE MODE

In a straight phase comparison scheme, the single phase quantity $(I_2 - I_1/K)$ is used as the keying quantity to perform the phase comparison between the terminals of the line, and the same quantity is used to operate the level detectors, FDL and FDH.

The following settings must be made prior to placing the equipment in service.

### FDL Level Detector Setting:

FDL is used as a breaker pole position indicator in permissive mode applications. When FDL drops out to indicate an open breaker, the scheme logic is arranged to continuously key the associated channel to the trip frequency. As such, FDL should be set on its minimum setting.

It is important to note that to maintain true permissive mode operation, FDL must be continuously picked up on minimum load flow in the quiescent state. If it is possible for minimum load to fall below the FDL setting, the channel will be keyed continuously to the trip frequency. This then requires FDL and FDH to coordinate for an external fault, as in a blocking mode appliction, to prevent the possibility of a false trip. Because of this possibility, FDL and FDH level coordination should be assured by using equation 5 or 6 as a check.

FDH Level Detector Setting:

Since this is a permissive mode of application, and it is assumed that continuous keying of the channel is not objectionable, the only constraint on the tripping level detector, FDH, is that it be set above full load. Equation 4 defines the required FDH setting. On any internal fault, regardless of the type of fault or the phases involved, the sequence network output ($I_2 - I_1/K$) at each terminal must be sufficient to operate FDH.

K Tap Setting:

Three K taps of 5, 7 or 10 are available. A high K tap setting tends to minimize the undesirable effects of load flow during an internal fault, and thus permit broader application limits. However, low K tap settings result in greater security on external three phase faults. The K tap selected directly influences the phase angle between the keying quantities at each terminal. For any internal fault, regardless of type of fault, combination of phases, or presence of load flow, the maximum phase angle between the keying quantities ($I_2 - I_1/K$) at all terminals must be small enough to assure tripping with adequate margin. It is recommended that the intermediate tap, K = 7, be considered first on any proposed application.

A rigorous and precise determination of the magnitude and relative phase angle of the keying quantity ($I_2 - I_1/K$) for all types of faults, on all combinations of phases, for all reasonable system conditions including the effects of load flow during the fault, would require extensive and time consuming calculations. However, a simple and reliable approach has been developed, and is outlined below. All of the following results are based on the assumption that the ratio of system zero sequence impedance to system positive sequence impedance ($Z_0/Z_1$), as viewed from any fault location on the protected line, falls within the range of 0.3 to 3.0. The ratio, $Z_0/Z_1$, for an effectively grounded transmission system is equal to or less than 3.0. Consequently, 3.0 is generally the upper limit on the range of $Z_0/Z_1$. The lower limit on $Z_0/Z_1$ is generally determined for a fault at a generating station where the positive sequence impedance of the generator-transformer combination is significantly greater than the zero sequence impedance. In the majority of cases, $Z_0/Z_1$ for the generator-transformer combination will be no less than 0.3

If $Z_0/Z_1$, as viewed from any fault location on the protected line, can be less than 0.3 or greater than 3.0; or if the constraints on the ratio of minimum internal three phase fault current to maximum load current, as outlined below, cannot be met, then refer the application to the nearest General Electric Company Sales Office. A memo describing a more rigorous and less conservative application approach will be supplied upon request, that may allow a particular application to be implemented, even though the constraints of the simplified approach cannot be met.

The simplified approach is as follows:

1) Select K = 7

2) Determine the maximum load current in secondary amperes. Use K = 7 and equation 4 to calculate the FDH setting.

3) Check that the FDL setting, as calculated by equation 5 or 6, is greater than or equal to the actual FDL setting. FDL should be set at its minimum pickup.

4) Determine the minimum secondary current at each terminal for a three phase fault anywhere on the protected line, and divide this by the magnitude of full load current determined in 2) above. If this ratio is equal to or greater than the value of Table I, then the application can be made with the assurance that any internal fault will result in a margin of at least 50 percent above FDH pickup.

If the calculated ratio of minimum internal three phase fault current to full load current is less than the required ratio, as determined from Table I, then repeat steps 1) through 4) above with K = 10. If the resulting ratio is still not adequate, or if K = 10 is deemed to be unacceptable from a security viewpoint, then the application is not proper based on the above approach. Note that the straight phase comparison scheme may still be applied if less conservative application considerations, such as those outlined in the memo mentioned previously, are utilized. If straight phase comparison cannot be applied, some other scheme, such as combined phase and directional comparison, should be considered.

If the calculated ratio of minimum internal three phase fault current to full load current is substantially greater than the required ratio, as determined from Table I, additional security should be obtained by either raising the FDH pickup setting (leaving FDL alone) or by setting K = 5. In either case, the application would then have to be rechecked. While both higher FDH/FDL settings and lower K settings add to the security of the scheme, there is probably more to be gained by increasing the ratio of FDH/FDL settings than in going from K = 7 to K = 5.

TABLE I

| K | 5 | 7 | 10 |
|---|---|---|---|
| $I_{3\emptyset}/I_{FL}$ | 3.45 | 2.6 | 1.73 |

## COMBINED PHASE AND DIRECTIONAL COMPARISON

A combined phase and directional comparison scheme combines the principles of both phase and directional comparison in a single scheme, utilizing a common communication channel. In the SLD51A relay, K is set at infinity and the resulting single phase quantity, ($I_2$), is used as the keying quantity to perform the phase comparison between the terminals of the line. This same $I_2$ quantity is used to operate the level detectors FDL and FDH. Since the SLD51A relay now employs negative sequence excitation, it provides protection for unbalanced faults only. Such a scheme will operate for three phase faults that produce currents well below full load values, since the associated phase distance relays are basically able to discriminate between fault currents and load currents. The application considerations and required settings for the associated phase distance relays are described in the instruction book for that particular relay.

The following settings should be made prior to placing the equipment in service.

FDL Level Detector Setting

The FDL level detector should be set as low as possible without the risk of operation on maximum expected load unbalance. FDL should be set at its minimum point, provided this setting is at least 1.25 times the maximum negative sequence unbalance current.

FDH Level Detector Setting

The FDH level detector must be set such that it will respond to any internal unbalanced fault with a margin of at least 50 percent. That is, the minimum negative sequence current for an unbalanced fault at any location on the protected line must be at least 1.5 times the negative sequence pickup of FDH. An additional requirement on the FDH pickup setting is that it be sufficiently above the remote FDL setting to insure security on external faults.

Equations 2 and 3 establish this margin for two-terminal and three-terminal lines, respectively.

## RATINGS

The SLD51A relay is designed for use in an environment where the air temperature outside the case is between minus 20°C and plus 65°C.

The SLD51A requies a plus or minus 15 volt DC power source which can be obtained from a suitable SSA power supply.

The SLD51A relay is available in 50 or 60 hertz models with one amp or five amp continuous current ratings. The one second current rating on one amp models is 60 amps, and on five amp models, 300 amps.

## BURDENS

DIRECT CURRENT

The SLD51A relay presents a burden of 40 milliamperes to both the plus 15 volt DC and minus 15 volt DC supplies of the SSA power supply.

ALTERNATING CURRENT

With the complete primary windings of the three phase auxiliary current transformer energized, and with the secondary links in the 1.0 x R position, the SLD51A relay has an AC current burden of:

| Five Amp Models | One Amp Models |
|---|---|
| 0.022 ohms $\angle 23^{o}$ | 0.55 ohms $\angle 23^{o}$ |

## RANGES

The pickup range of FDL and the operating point of the squaring amplifier depend on the position of links on the secondary of the three phase auxiliary current transformer. They also depend on the amount of the primary windings being energized. This amount is determined by the input terminal point connections to the relay. Refer to Table II for the FDL pickup range and squaring amplifier operating point in negative sequence amperes for each combination of terminal point connections and link positions.

TABLE II

SLD51A SENSITIVITY RANGES

| $I_A$ Curr. Term. | | $I_B$ Curr. Term. | | $I_C$ Curr. Term. | | Curr. Term. Conn. Ratio | Ø1-2 Ø2-3 Ø3-1 Links | FDL Pickup Range | Keying Sig.Opr. Point | FDL Pickup Range | Keying Sig.Opr. Point |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Neg. Seq. Amps | | Neg. Seq. Amps | |
| IN | OUT | IN | OUT | IN | OUT | R | | 5 Amp Models | | 1 Amp Models | |
| DB1 | DB4 | DB5 | DB8 | DB9 | DB12 | 1 | 1.0 x R | 0.20-0.50 | 0.10 | 0.04-0.10 | 0.02 |
| DB1 | DB4 | DB5 | DB8 | DB9 | DB12 | 1 | 2.5 x R | 0.50-1.25 | 0.25 | 0.10-0.25 | 0.05 |
| DB2 | DB4 | DB6 | DB8 | DB10 | DB10 | 2 | 1.0 x R | 0.40-1.00 | 0.20 | 0.08-0.20 | 0.04 |
| DB2 | DB4 | DB6 | DB8 | DB10 | DB12 | 2 | 2.5 x R | 1.00-2.50 | 0.50 | 0.20-0.50 | 0.10 |
| DB3 | DB4 | DB7 | DB8 | DB11 | DB12 | 4 | 1.0 x R | 0.80-2.00 | 0.40 | 0.16-0.40 | 0.08 |
| DB3 | DB4 | DB7 | DB8 | DB11 | DB12 | 4 | 2.5 x R | 2.00-5.00 | 1.00 | 0.40-1.00 | 0.20 |

The squaring amplifier operating point is the negative sequence current level that will give output pulses, or blocks from the squaring amplifier, six milliseconds wide on 60 hertz models, or 7.2 milli seconds wide on 50 hertz models.

The pickup level of FDH can be set for one to seven times the particular FDL pickup setting.

There are K taps in the SLD51A relay that determine the ratio of the response of the relay for the positive sequence component of the input current, compared to the response for the negative sequence component of the input current. The available K tap settings are K = 5, 7, 10 or infinity. For K = infinity, the relay responds to the negative sequence component of the input current only. For K = 10, the fault detectors will pick up for a positive sequence current that has a magnitude ten times the negative sequence pickup setting. For K = 7, the fault detectors will operate for a positive sequence current seven times the negative sequence pickup setting. For K = 5, the fault detectors will operate for a positive sequence current five times the negative sequence pickup setting.

## OPERATING PRINCIPLES AND CHARACTERISTICS

### INTRODUCTION

There are four major components in the SLD51A: The three phase auxiliary current transformer and the printed circuit cards in the N, P and R card positions.** The three phase auxiliary current transformer converts the current received by the relay into low level signals suitable for operation in the filter/network card in the N position. This circuit card is a mixing network. The fault detectors are energized by the settings on this card. The card in position P is a filter/keying circuit. The input signals to this card are the output signals from the card in position N. This card produces filtered signals, which are the inputs to the fault detectors. This card also produces square wave output signals for keying the transmitter in a complete phase comparison relay scheme. The fault detectors are on the printed circuit card in the R position. The low set fault detector, FDL, usually establishes the blocking level of the scheme, and the high set fault detector, FDH, usually establishes the tripping level.

**Note: On 60 hertz models, these cards are the F115, F116 and D106, respectively.
On 50 hertz models, these cards are the F168, F169 and D130, respectively.

### THREE PHASE AUXILIARY CURRENT TRANSFORMER

The three phase auxiliary current transformer is a wye-delta transformer. This delta secondary connection eliminates zero sequence current in the SLD51A relay. Therefore, the only currents available are positive and negative sequence currents. The transformer also steps down the current, which steps up the voltage from primary to secondary. The load on the secondary of the transformer is three 5.0 ohm resistors connected in a wye configuration with the neutral connected to relay logic reference. This combination of turns-ratio and resistive load makes the transformer output appear as a voltage source to the printed circuit card in the N position. Therefore, the outputs of the three phase auxiliary current transformer circuit are three phase-to-neutral voltages proportional to the three phase current inputs to the SLD51A relay. The equations for this relationship can be expressed as follows:

$$V_{AB} = N(I_A - I_B)$$
$$V_{BC} = N(I_B - I_C)$$
$$V_{CA} = N(I_C - I_A)$$

$V_{AB}$, $V_{BC}$ and $V_{CA}$ are the three voltage outputs from the three phase auxiliary current transformer circuit. They are also the voltage input signals for the mixing network. N is a multiplying constant, and its value depends on the turns-ratio being used in the three phase auxiliary current transformer and on the 5.0 ohm load resistors. The N value for each configuration is given in Table III. $I_A$, $I_B$ and $I_C$ are the three input currents to the SLD51A relay.

TABLE III

| $I_A$ | | $I_B$ | | $I_C$ | | ØA-B, ØB-C, ØC-A LINK | N |
|---|---|---|---|---|---|---|---|
| IN | OUT | IN | OUT | IN | OUT | | |
| DB1 | DB4 | DB5 | DB8 | DB9 | DB12 | 1.0 x R | 0.0625 |
| DB1 | DB4 | DB5 | DB8 | DB9 | DB12 | 2.5 x R | 0.025 |
| DB2 | DB4 | DB6 | DB8 | DB10 | DB12 | 1.0 x R | 0.0313 |
| DB2 | DB4 | DB6 | DB8 | DB10 | DB12 | 2.5 x R | 0.0125 |
| DB3 | DB4 | DB7 | DB8 | DB11 | DB12 | 1.0 x R | 0.0157 |
| DB3 | DB4 | DB7 | DB8 | DB11 | DB12 | 2.5 x R | 0.0063 |

MIXING NETWORK, F115 OR F168 PRINTED CIRCUIT CARD

The mixing network card has four K taps (SA, SB, SC and SD). Each K tap has four available positions, K = 5, 7, 10 and infinity. All four taps must be in the same position at all times. The output of this card is proportional to $(I_2 - I_1/K)$. The internal connection diagrams for the F115 and F168 circuit cards are shown in Figures 5 and 5A. If the four K taps are in the K = infinity position, then the mixing network is a pure negative sequence network, and the output is proportional to the negative sequence component of the input current. If the K taps are in the K = 5, 7 or 10 position, the output signal is proportional to $(I_2 - I_1/K)$. There are actually two mixing networks on this card. Each network receives the same input signals and functions just as described above, except that the two output signals are 90 degrees out-of-phase. These two complementary signals help improve the overall speed of the relay. This will be more fully explained in the disucssion on fault detectors.

Figures 6 and 6A show the mixing networks in a pure negative sequence mode; that is, the K taps are in the K = infinity position. The three input signals applied to pins 3, 4 and 5 are called $V_{AB}$, $V_{BC}$ and $V_{CA}$. The two output signals appearing at pins 8 and 9 will be called $V_X$ and $V_Y$ for purposes of discussion. The equations for the two networks of Figures 6 and 6A are as follows:

$$V_X = 2.49\ V_{AB}\underline{/180^o} + 2.88\ V_{BC}\underline{/150^o} + 1.44\ V_{CA}\underline{/150^o}$$

and

$$V_Y = 1.44\ V_{AB}\underline{/180^o} + 2.88\ V_{BC}\underline{/180^o} + 2.49\ V_{CA}\underline{/150^o}$$

Assume that the input currents to the relay are:

$$I_A = I_{A0} + I_{A1} + I_{A2}$$

$$I_B = I_{A0} + a^2 I_{A1} + aI_{A2}$$

$$I_C = I_{A0} + aI_{A1} + a^2 I_{A2}$$

Then $V_{AB} = N(I_A - I_B)$

$= N(I_{A0} + I_{A1} + I_{A2} - I_{A0} - a^2 I_{A1} - a I_{A2})$

$= N\left[(1 - a^2)\, I_{A1} + (1 - a)\, I_{A2}\right]$

$V_{AB} = N(\sqrt{3}\, I_{A1}\underline{/30^o} + \sqrt{3}\, I_{A2}\underline{/-30^o})$

$V_{BC} = N(I_B - I_C)$

$= N(I_{A0} + a^2 I_{A1} + a I_{A2} - I_{A0} - a I_{A1} - a^2 I_{A2})$

$= N\left[(a^2 - a)\, I_{A1} + a - a^2)\, I_{A2}\right]$

$V_{BC} = N(\sqrt{3}\, I_{A1}\underline{/-90^o} + \sqrt{3}\, I_{A2}\underline{/90^o})$

$V_{CA} = N(I_C - I_A)$

$= N(I_{A0} + a I_{A1} + a^2 I_{A2} - I_{A0} - I_{A1} - I_{A2})$

$= N\left[(a - 1)\, I_{A1} + (a^2 - 1)\, I_{A2}\right]$

$V_{CA} = N(\sqrt{3}\, I_{A1}\underline{/150^o} + \sqrt{3}\, I_{A2}\underline{/-150^o})$

Substituting these expressions for $V_{AB}$, $V_{BC}$ and $V_{CA}$ into the equations for $V_X$ and $V_Y$, gives the following relationships:

$V_X = 2.49\, N\sqrt{3}\,(\, I_{A1}\underline{/180^o + 30^o} + I_{A2}\underline{/180^o - 30^o}\,)$

$+ 2.88\, N\sqrt{3}\,(\, I_{A1}\underline{/150^o - 90^o} + I_{A2}\underline{/150^o + 90^o}\,)$

$+ 1.44\, N\sqrt{3}\,(\, I_{A1}\underline{/150^o + 150^o} + I_{A2}\underline{/150^o - 150^o}\,)$

$= 4.3\, N(I_{A1}\underline{/210^o} + I_{A2}\underline{/150^o})$

$+ 4.99\, N(I_{A1}\underline{/60^o} + I_{A2}\underline{/240^o})$

$+ 2.49\, N(I_{A1}\underline{/300^o} + I_{A2}\underline{/0^o})$

$= 4.3\, N\, I_{A1}(-0.866 - j0.50) + 4.3\, N\, I_{A2}(-0.866 + j0.50)$

$+ 4.99\, N\, I_{A1}(0.50 + j0.866) + 4.99\, N\, I_{A2}(-0.50 - j0.866)$

$+ 2.49\, N\, I_{A1}(0.50 - j\,0.866) + 2.49\, N\, I_{A2}$

$= -3.73\, N\, I_{A1} - j2.15\, N\, I_{A1} - 3.73\, N\, I_{A2} + j2.15\, N\, I_{A2}$

$+ 2.49\, N\, I_{A1} + j4.30\, N\, I_{A1} - 2.5\, N\, I_{A2}$

$- j4.30\, N\, I_{A2} + 1.24\, N\, I_{A1} - j2.15\, N\, I_{A1} + 2.49\, N\, I_{A2}$

$= 3.74\, N\, I_{A2} - j2.15\, N\, I_{A2}$

$V_X = 4.32\, N\, I_{A2}\underline{/210^o}$

$V_Y$ can be calculated in a similar manner:

$$V_Y = 4.32\ N\ I_{A2}\underline{/300^o}$$

When the K taps are set at a value other than K = infinity, then the equations for $V_X$ and $V_Y$ are slightly different. The response of the network to the input currents can be calculated in a similar manner to the response for K = infinity.

For K = 10:

$$V_X = 2.49\ V_{AB}\underline{/180^o} + 3.00\ V_{BC}\underline{/150^o} + 1.32\ V_{CA}\underline{/150^o} + 0.24\ V_{CA}\underline{/180^o}$$

$$V_X = 0.432\ N\ I_{A1}\underline{/30^o} + 4.32\ N\ I_{A2}\underline{/210^o}$$

and

$$V_Y = 1.32\ V_{AB}\underline{/180^o} + 0.24\ V_{AB}\underline{/150^o} + 3.00\ V_{BC}\underline{/180^o} + 2.49\ V_{CA}\underline{/150^o}$$

$$V_Y = 0.432\ N\ I_{A1}\underline{/120^o} + 4.32\ N\ I_{A2}\underline{/300^o}$$

For K = 7:

$$V_X = 2.49\ V_{AB}\underline{/180^o} + 3.10\ V_{BC}\underline{/150^o} + 1.26\ V_{CA}\underline{/150^o} + 0.35\ V_{CA}\underline{/180^o}$$

$$V_X = 0.617\ N\ I_{A1}\underline{/30^o} + 4.32\ N\ I_{A2}\underline{/210^o}$$

and

$$V_Y = 1.26\ V_{AB}\underline{/180^o} + 0.35\ V_{AB}\underline{/150^o} + 3.10\ V_{BC}\underline{/180^o} + 2.49\ V_{CA}\underline{/150^o}$$

$$V_Y = 0.617\ N\ I_{A1}\underline{/120^o} + 4.32\ N\ I_{A2}\underline{/300^o}$$

For K = 5:

$$V_X = 2.49\ V_{AB}\underline{/180^o} + 3.15\ V_{BC}\underline{/150^o} + 1.15\ V_{CA}\underline{/150^o} + 0.49\ V_{CA}\underline{/180^o}$$

$$V_X = 0.865\ N\ I_{A1}\underline{/30^o} + 4.32\ N\ I_{A2}\underline{/210^o}$$

and

$$V_Y = 1.15\ V_{AB}\underline{/180^o} + 0.49\ V_{AB}\underline{/150^o} + 3.15\ V_{BC}\underline{/180^o} + 2.49\ V_{CA}\underline{/150^o}$$

$$V_Y = 0.865\ N\ I_{A1}\underline{/120^o} + 4.32\ N\ I_{A2}\underline{/300^o}$$

Note that in all cases, the sensitivity of the output voltage, $V_X$ or $V_Y$, to the negative sequence component of the input current is always the same. For K = 10, K = 7 or K = 5, the sensitivity of the output voltage to the positive sequence component of input current is either one-tenth, one-seventh or one-fifth, respectively, of the sensitivity to the negative sequence component. In all three cases, the portion of output voltage caused by the negative sequence component of input current is 180 degrees out-of-phase with the portion of output voltage caused by the positive sequence component. This is why the output voltage is proportional to the quantity $(I_2 - I_1/K)$.

The above expressions for the mixing network output voltage as a function of input current to the relay apply an output voltage up to approximately 2.5 volts RMS. For the case when the entire primary windings of the three phase current transformer are energized, and the links are in the 1.0 x R position, 2.5 volts RMS output voltage results from an input current of approximately two times relay rated (10 or 2) amps RMS pure negative sequence. For other conditions, the input current is higher, to give an output voltage of 2.5 volts RMS. As the input signal becomes larger than this, the gain of the network decreases. This non-linear response assures that the amplifier in the mixing network will never go into saturation, and that the output of the network is always sinusoidal. It is important to guarantee that the output voltage remain sinusoidal because of the active filters on the filter/keying card. These filters will not give the proper response for a saturated signal. Proper filtering is dependent on a sinusoidal voltage signal.

## FILTER/KEYING CIRCUIT, F116 OR F169 PRINTED CIRCUIT CARD

The filter/keying circuit contains five filter circuits: Two identical band pass "tee" filters, two identical low pass "tee" filters, and an INIC memory filter. The internal connection diagrams for the F115 and F169 printed circuit cards are shown in Figures 7 and 7A. The two input signals to pins 4 and 5 are the the output signals ($V_X$ and $V_Y$) from the mixing network. These two signals are sinusoidal, equal in magnitude and 90 degres out-of-phase. The two input filters are band pass "tee" filters. The output signals from the band pass filters are fed into low pass "tee" filters and into a summing amplifier. The output signals from the low pass filters at pins 6 and 7 are the signals that drive FDL and FDH. The low pass filters have a non-linear gain characteristic such that the greater the input signal, the lower the gain. This non-linear gain produces a wider input signal operating range without going into saturation. This is necessary to produce the wide operating range of FDL and FDH. A side effect of this non-linear gain is that the output signals from the filters are not perfectly sinusoidal, but are slightly misshapened.

The rest of the circuitry on this card is associated with the squaring amplifier function, which is used to key the transmitter in a complete phase comparison scheme. The output from the summing amplifier is the signal that drives the squaring amplifier. This signal is fed through an amplifier with an adjustable gain to set the sensitivity of the squaring amplifier. The sensitivity is set by adjusting potentiometer P61. The signal is then passed through a narrow band pass INIC filter which provides memory action. If the system is operating in a condition

that gives a full squaring amplifier output signal, and then the input signal is removed, the squaring amplifier will continue to provide four or five cycles of output signal due to the memory action of the INIC filter. There are actually two output signals from the squaring amplifier. The output signal at pin 9 is a series of positive pulses with respect to logic reference, corresponding to the positive half-cycles of the AC input signal. The output signal at pin 8 is a series of positive pulses corresponding to the negative half-cycles of the AC input signal. Since the signal that drives the squaring amplifier is the sum of two AC signals 90 degrees out-of-phase, the phase relationship of the output signal at pin 9 is approximately midway between the two AC signals. In many phase comparison schemes, only the output signal corresponding to the positive half-cycle of the input signal is used; however, both are available.

## FAULT DETECTOR CIRCUIT, D106 OR D130 PRINTED CIRCUIT CARD

The fault detector circuit contains an orthophase rectifier circuit, a low-set fault detector, FDL, and a high set fault detector, FDH. The internal connection diagrams of the D106 and D130 printed circuit cards are shown in Figures 8 and 8A. The inputs to the orthophase rectifier are at pins 3 and 4. The output of this rectifying circuit can be seen at pin 5. This signal drives the FDL level detector directly, and it drives the FDH level detector through a voltage follower circuit. The output of the voltage follower circuit can be seen at pin 6. The FDL output is pin 9; the FDH output is pin 7. Pins 5 and 6 are for test monitoring only, and are not intended for input or output connections.

The two input signals to the orthophase rectifier at pins 3 and 4 are two relay rated frequency signals, equal in magnitude and 90 degrees out-of-phase. The circuit combines the two signals, and the combination is full wave rectified. If just one of the two input signals were applied, then the signal appearing at pin 5 would be a full wave rectified signal, with one positive peak occurring every half cycle on a relay rated frequency basis, and with a ripple frequency of two times relay rated frequency. With both input signals applied, the output signal appearing at pin 5 will have a positive peak occurring every quarter cycle with a ripple frequency of four times rated frequency. In other words, one single phase signal is full wave rectified, and a second signal, equal in magnitude to the first, but 90 degrees out-of-phase with it, it also full wave rectified and superimposed on the first signal.

The orthophase rectifier is an amplifier as well as a rectifier. The magnitude of the signal at pin 5 depends on the gain of the circuit. The gain is adjustable and can be set by adjusting potentiometer P11. This adjustment establishes the pickup setting for FDL. As the signal at pin 5 exceeds five volts, the gain decreases non-linearly from the gain established by setting P11. This non-linearity is necessary because of the wide range of possible FDL and FDH pickup settings. If the amplifier were to saturate there would be no further variation in the output signal level.

The voltage follower circuit is simply an amplifier; therefore, the signal at pin 6 is directly related to the signal at pin 5. If potentiometer P21 is adjusted fully counterclockwise, the magnitude and phasing of the signal at pin 6 will be exactly the same as that at pin 5. If potentiometer P21 is adjusted in

the clockwise direction, then the magnitude of the signal at pin 6 will be some percentage of the magnitude of the signal at pin 5, depending on the voltage divider effect of potentiometer P21 and resistors R21 and R22; however, the phasing of the signals will remain the same.

The FDL and FDH level detector circuits are exactly the same except for the value of the capacitor in the feedback circuit. This capacitor determines the dropout time of the circuit. On 60 hertz models, the FDL dropout varies from 26 milliseconds plus or minus 3 milliseconds (at input levels of 1.5 x FDH pickup) to 36 milliseconds plus or minus 3 milliseconds (at input levels of 10 x FDH pickup). FDH dropout varies from 12 milliseconds plus or minus 3 milliseconds (at input levels of 1.5 x FDH pickup) to 21 milliseconds plus or minus 3 milliseconds (at input levels of 10 x FDH pickup). On 50 hertz models, the FDL dropout varies from 31 plus or minus 3 milliseconds (at input levels of 1.5 x FDH pickup) to 43 milliseconds plus or minus 3 milliseconds (at input levels of 10 x FDH pickup). FDH dropout varies from 14 milliseconds plus or minus 3 milliseconds (at input levels of 1.5 x FDH pickup) to 25 milliseconds plus or minus 3 milliseconds (at input levels of 10 x FDH pickup). The threshold for each level detector is approximately 2.5 volts DC as determined by zener diode Z91 and resistor R91. If the signal at pin 5 or 6 is less than 2.5 volts, then the output signal at pin 9 or 7 is 0 to -0.6 volt DC. If the signal at pin 5 or 6 is greater than 2.5 volts, then the output signal at pin 9 or 7 is 13 to 15 volts DC. The output signal will remain at the positive voltage level for the duration of the dropout time after the input signal drops below the threshold. The output will return to 0 to -0.6 volt DC level.

The FDL and FDH level detectors operate on the instantaneous value of the input signal. Therefore, whenever the peak value of input signal exceeds the threshold, the level detector will produce an output. The effect of the two operating signals 90 degrees out-of-phase and of the orthophase rectifier, is to help speed up the operation of the level detectors right at the threshold or minimum pickup level. With four peaks per cycle rather than two, there are more chances to operate just at threshold. If the incidence angle of the fault is such that it just missed one peak, the wait for the next peak is only a quarter-cycle, rather than a half-cycle. This decreases the operating time at minimum pickup.

There is a resistor and capacitor combination used as a feedback circuit from the FDL output at pin 9 to the threshold input of FDH. This feedback slightly delays the operation of FDH when FDL operates. When an input signal that will operate both FDL and FDH is applied, FDL will always operate first. This eliminates possible transient race problems between FDL and FDH in a complete scheme.

The pickup level of FDL is determined by the gain of the orthophase rectifier. In other words, the gain of the rectifying circuit determines the magnitude of the input signal required at pins 3 and 4 to exceed the threshold of the FDL level detector, and produce an output signal at pin 9. The pickup level of FDH is determined by the signal supplied to the voltage follower circuit. The minimum FDH pickup level is equal to the particular FDL pickup level as determined by the set gain of the orthophase rectifier. The pickup level of FDH can then be increased to seven times that FDL pickup setting by adjusting the input signal to the voltage follower circuit.

## CALCULATION OF SETTINGS

The following calculation example will illustrate the use of the simplified approach for determining settings as outlined in the section on **APPLICATION.** This calculation uses typical values for a five ampere relay. Assume a blocking mode application on a two-terminal line utilizing power line carrier channel. The maximum load is 3.75 amperes, minimum three phase fault current is 12.5 amperes, and normal positive sequence charging current is 0.2 amperes. The ratio of $Z_0/Z_1$, as viewed from any fault location on the protected line, falls within the range of 0.3 to 3.0.

The calculation procedure is:

1) Initially, select K = 7

2) Using equation 1, determine the FDL setting:

$$FDL = \frac{(3.75)\ (1.1)}{7} = 0.59 \text{ amps } I_2$$

Using equation 2, determine the FDH setting:

$$FDH = (\tfrac{4}{3})\ (0.59) + (0.375)\ (0.2)$$

$$= 0.787 + 0.075$$

$$= 0.862 \text{ amps } I_2$$

3) $(K)\ (FDH)/I_{FL} = (7)\ (0.862)/(3.75)$

$$= 1.61$$

4) Enter the curve of Figure 4 with an abscissa value of

$$(K)\ (FDH)/I_{FL} = 1.61$$

The corresponding ordinate value for K = 7 is $I_{3\phi}/I_{FL} = 3.2$

5) The actual ratio of minimum three phase fault current to full load current is:

$$I_{3\phi}/I_{FL} = \frac{12.5}{3.75} = 3.34$$

Since the actual ratio of $I_{3\phi}/I_{FL}$ is greater than the value read from the curve of Figure 4, the application can be made with K = 7.

## CONSTRUCTION

The SLD51A relay is packaged in an enclosed metal case with a hinged front cover and a removable top cover. The case is suitable for mounting on a standard 19-inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2, respectively.

On the rear of the case are two cable sockets and two 12-point terminal strips. The four-point cable socket is labeled CP03, and is the DC power supply connection for this relay. The ten-point cable socket is labeled C041, and is the connection point for the logic signal leads which must go to a suitable SLA or SLAT relay in a complete scheme. One terminal strip is labeled DA and the other DB. In a complete equipment, DA1 is usually connected to surge ground. DB1 through DB12 are the input AC current connections. DB1 through DB4 are for phase A, DDB5 through DB8 are for phase B, and DB9 through DB12 are for phase C. The particular terminal points to be used in the operation of the relays depends on the desired pickup ranges of the fault detectors. Refer to Table II in the **RANGES** section of this book, or to the chart on the internal connection diagram for the SLD51A relay shown in Figure 3.

There are three printed circuit cards and one test card in the SLD51A relay. The location of these cards is given in the component location diagram in Figure 2. For the identification of test points, refer to the internal connection diagram, Figure 3.

There is a link plate containing three links and two pushbuttons in the front of the SLD51A. The links are labeled ØA-B, ØB-C, and ØC-A, and are used to determine the pickup ranges of the fault detectors. Refer to Table II in the **RANGES** section of this book, or to the chart on the internal connection diagram in Figure 3. The test pushbuttons are labeled TRIP and CARRIER TEST. In a complete phase comparison scheme, these pushbuttons are typically used to simulate FDH and FDL output signals, respectively.

## RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, unpack and examine it for any damage sustained in transit. If damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Apparatus Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust and metallic chips and severe atmospheric contaminants.

The top shipping support bracket should be removed from each side of all relay units just prior to final installation to facilitate possible future unit removal for maintenance. These shipping support brackets are approximately eight inches back from the relay unit front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR, OR TO THE SHIPPING PALLET, TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

## INSTALLATION TESTS

The SLD51A relay is usually supplied from the factory mounted and wired in a static relay equipment. All units of a given terminal have been calibrated together

at the factory and will have the same summary number on the unit nameplates. These units must be tested and used together.

The following checks and adjustments should be made by the user in accordance with the procedures given in **DETAILED TESTING INSTRUCTIONS** before the relays are put in service. Some of the following items are checks of factory calibrations and settings, or of installation connections; therefore, they do no normally require readjustment in the field. Other items cover settings or adjustments which depend on installation conditions, and must be made on the installed equipment. The tests should be made in the order given in the list below. The channel signal symmetry adjustment and phase delay adjustment are actually made in the associated SLA or SLAT relay, if required.

1. Mixing network balance check
2. CT phasing, polarity and sequence check
3. Squaring amplifier check
4. Fault detector adjustments
5. Channel signal symmetry adjustment
6. Phase delay adjustment

Before beginning the installation tests, check for installation of all interconnecting cables between the various relays and associated test equipment which may be supplied. Also check that all terminal board connections are tight.

## GENERAL TESTING INSTRUCTIONS

### Input Circuits

The three phase input currents enter the SLD51A relay on a terminal block, labeled DB1 through DB12, located on the rear of the relay case. The actual terminal connections depend on the desired pickup ranges for the fault detectors. Refer to the **RANGES** section of this book, or to the internal connections diagram, Figure 3, for these connections.

### Output Signals

Pin 1 on the test card (TP1) in position T is connected to relay logic reference, pin 2 (TP2) to minus 15 volts DC and pin 10 (TP10) to plus 15 volts DC. Output signals are measured with respect to the relay logic reference at TP1. The output signals from FDL, FDH and the squaring amplifier are logic signals. Logic signals are approximately plus 15 volts DC for the ON or LOGIC-ONE condition, and less than one volt DC for the OFF or LOGIC-ZERO condition. The output signals from the mixing network card and the filter portion of the filter/keying card are AC signals measured with respect to relay logic reference.

The logic output signals can be monitored with an oscilloscope, a high impedance DC voltmeter, or the test panel voltmeter, if available. When the test panel meter is supplied, it will normally be connected to relay logic reference. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. The output of the squaring amplifier is best checked with an oscilloscope. The AC output signals can be monitored with an oscilloscope or a high impedance AC voltmeter.

CAUTION: THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

## DETAILED TESTING INSTRUCTIONS

Before proceeding with the following test program, be sure to open the trip circuits in the associated SLAT relay.

### Mixing Network Balance Check

The mixing network as designed is not adjustable; however, the balance should be checked to make sure that no damage has occurred during transit.

Method I - Three Phase Test Source:

To check the null of the mixing network, place all K taps on the printed circuit card in the N position in the K = infinity position. Use the test circuit of Figure 9, and the test connections of Table IV. Applying relay rated current will provide the best resolution. All three currents must be equal in magnitude.

TABLE IV

| TEST FIGURE POINT | D | E | F | G | H | I |
|---|---|---|---|---|---|---|
| SLD51A Terminal | DB8 | DB5 | DB4 | DB1 | DB9 | DB12 |

Touch up the adjustments on the three test currents to give the best null at both mixing network outputs, TP3 and TP4. The three currents should be within a few percent of each other in magnitude and the two output signals should be less than 0.06 volt peak-to-peak. The output signals will have very little fundamental frequency, but perhaps a large amount of third and fifth harmonics.

If three load boxes, or test reactors, or ammeters, are not available, a test using a three phase source can be performed using two load boxes, test reactors and ammeters. Use the test circuit of Figure 9, leaving connections H and I open circuited, and omit the ammeter, the load box and the test reactor in the branch. Make the test connections of Table V. The input current magnitudes should be equal within a few percent, and be 60 degrees out-of-phase. The output voltages should be less than 0.06 volt peak-to-peak.

TABLE V

| TEST ≠ | TEST CIRCUIT CONNECTION POINT | | | |
|---|---|---|---|---|
| | D | E | F | G |
| 1 | DB1 | DB4 | DB8 | DB5 |
| 2 | DB5 | DB8 | DB12 | DB9 |
| 3 | DB9 | DB12 | DB4 | DB1 |

≠NOTE: To fully test the three phase input, three separate tests are required with this procedure.

Method II - Single Phase Test Source:

The basic circuit used in checking the network is shown in Figure 10. This arrangement provides means of obtaining two test currents of equal magnitude, but separated by 60 degrees. By appropriate connections to the network, it is then possible to simulate a balanced three-phase positive sequence current (Table VI). During the following tests, the basic current level in each branch will be relay rated current, and since these currents will add at a 60 degree angle, the total load in the variac will be about 1.73 times relay rated current. The 110 volt scale of the phase angle meter should be used to minimize the effect of this potential circuit on the relationship between the two test currents. Further, the variac should be set near its maximum voltage output, and the load boxes should be set to obtain approximately relay rated current as a preliminary step, since this will provide the greatest possible voltage to the phase angle meter, and will insure the best possible accuracy.

TABLE VI

| TEST ≠ | TEST CIRCUIT CONNECTION POINT | | |
|---|---|---|---|
| | A | B | C |
| 1 | DB1 | DB5 | DB4, DB8 |
| 2 | DB5 | DB9 | DB8, DB12 |
| 3 | DB9 | DB1 | DB12, DB4 |

≠NOTE: To fully test the three phase input, three separate tests are required with this procedure.

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Set all K taps on the card in the N position to K = infinity. Place all links in the 1.0 x R position. Balanced positive sequence current will be simulated by setting branch "A" current to lead branch "B" current by 60 degrees, and by setting branch "A" and "B" currents equal to relay rated current.

Since it is difficult to obtain perfect settings, branches "A" and "B" load boxes should now be touched up until the waveform contains a minimum fundamental component, and then the variac readjusted until the branch "B" current again is at relay rated current. Branch "A" current should be within ten percent of branch "B" current, and the angle between the "A" and "B" currents should be 60 degrees plus or

minus three degrees. The peak-to-peak value of the network output, which now will consist primarily of harmonics, will depend on the system, but should be on the order of 0.06 volt peak-to-peak or less. Again the network outputs can be monitored at TP3 and TP4.

CT Phasing, Polarity and Sequence Check

The following tests on CT phasing, polarity, and sequence should be made to assure that coordination between terminals is realized. These tests are easily made when power line carrier is used as the pilot channel. The tests provide a means of checking that for phase sequence A-B-C, phase A current transformer is connected to the DB1-DB4 winding of the three phase auxiliary current transformer with the same polarity at both terminals, that phase B current transformer is similarly connected to DB5-DB8, and that phase C current transformer is similarly connected to DB9-DB12. The carrier channel is used to communicate phase angle information between terminals.

In order to make the test, it is necessary that load current is flowing on the line. The magnitude of the load current should be at least five times the single-end feed line charging current to assure readable through-fault current relationships. If charging current is too high relative to load current, the phase difference between currents at the two ends will make it difficult to correctly interpret the results of the following tests. In the following tests, load current in each phase is used independently to simulate a corresponding line-to-ground fault.

Since the carrier pilot channel is used in this test, it is necessary that the simulated phase-to-ground fault current be above the FDL level detector operating point. The associated SLA or SLAT relay must be energized so that the FDL and squaring amplifier in the SLD51A will initiate the transmission of carrier RF on alternate half cycles of fault current (i.e., half-cycle on, half-cycle off). The FDL level detector was factory set for 0.2 amp negative sequence (five amp relays) or 0.04 amp negative sequence (one amp relays). The squaring amplifier was set to have six millisecond output blocks at the factory setting input; therefore, an input of two times this negative sequence current will produce full half-cycle output blocks.

For a simulated phase to ground fault, the negative sequence component is one-third the line current. Therefore, it is necessary that the secondary load current be at least three times 0.2 amp, or 0.6 amp (five amp relays) or three times 0.04 amp, or 0.12 amp (one amp relays). If load current exceeds this value, the low-set level detector, FDL, will operate and the squaring amplifier will have a nearly symmetrical output.

To simulate a phase A to ground fault, connect the input current circuits so that the phase A current flows through the relay, but phase B and C currents bypass the relay. To simulate a phase B to ground fault, connect phase B current to flow through the relay, and phase A and C currents to bypass the relay. To simulate a phase C to ground fault, connect phase C current to flow through the relay, and phase A and B currents to bypass the relay.

The required procedure is outlined below:

1. Make the connections to simulate a phase A to ground at each terminal.

2. Connect the vertical input of a scope to the RF jack of the CS26 carrier receiver and the ground input of the scope to the carrier chassis.

3. Two levels of carrier RF should be observed on the scope, the higher from the local transmitter, and the lower from the remote transmitter. The two levels of carrier should adjoin each other every half cycle with a dead space between them of not more than one-sixth of a half cycle (30 degrees). While the width of this dead zone between adjacent blocks of carrier RF is not rigidly limited, it must be small enough to establish that it has not resulted from a CT phasing error. The higher amplitude RF duration is very close to one half cycle long, and may be used as a time reference.

Repeat the above steps for each of the phase test connections. If the results of each test are satisfactory, it indicates that CT phasing and polarity are correct. If the carrier signals do not properly intermesh, the connections between the relays and CTs, or the phasing of CTs at opposite terminals, should be investigated.

With CT polarity and phasing established, check that the phase sequence is correct by properly connecting the three phase load current to the relay. Place the K taps on the card in the N position in the K = infinity position. Check the signal level at TP3 and TP4. If the phase sequence is correct, the signal at TP3 and TP4 will be similar to the null signal obtained when checking the mixing network balance. If the phase sequence is reversed, the signal will be a much larger relay rated frequency sine wave.

Squaring Amplifier Check

The operating level of the squaring amplifier can be checked using the single phase test circuit of Figure 11. The operation of the squaring amplifier cannot be checked until the desired pickup level of FDL is determined, because the operating level of the squaring amplifier and the A and B connections in Figure 11 are determined by the FDL pickup level. Refer to Table II in **RANGES** of this book for the necessary link positions and terminal point connections to give the range that includes the desired FDL pickup level. Table II also gives the proper operating level for the squaring amplifier.

When the FDL pickup range has been established, make the proper link connections and terminal point connections as given in Table II. All three links (ØA-B, ØB-C and ØC-A) should be in the same positions (1.0 x R or 2.5 x R) at all times. When the SLD51A is shipped as part of a complete equipment, the wiring to the terminal block on the rear of the relay is usually connected to DB1 and DB4, DB5 and DB8 and DB9 and DB12. The connections to DB4, DB8 and DB12 are intended to be fixed, and should not be moved. The wire connected to DB1 has enough slack that it can be moved to DB2 or DB3; similarly, the wire connected to DB5 can be moved to DB6 or DB7, and the wire connected to DB9 can be moved to DB10 or DB11. Connect these wires to the proper terminal points. Since these connections are in the AC current circuit, the relay equipment must be disconnected from the system current transformers before any changes are made in the connections. Make sure that all connections are made per Table II.

Use the test circuit of Figure 11 to check the operating level of the squaring amplifier. Make the B connection to DB4 and the A connection to DB1 or DB2 or DB3, depending on the FDL pickup range chosen. Make sure the links are in the proper position. Place the K taps on the card in position N in the K = infinity position. Apply a test current equal to three times the squaring amplifier negative sequence operating current level, as given in Table II. In other words, the relay responds the same for the single phase test current as it does for a negative sequence current of one-third the magnitude. For example, if the squaring amplifier operating level is 0.1 amp negative sequence, then apply a single phase test current of 0.3 amp.

Apply the proper test current and observe the squaring amplifier output signal at TP9 on an oscilloscope. This output signal will be a repetitive pulse train of relay rated frequency, and an output pulse width of 6.0 ±0.5 milliseconds (60 hertz relays) or 7.2 ±0.6 milliseconds (50 hertz relays). The pulse magnitude will be approximately 15 volts DC and the off magnitude will be less than one volt DC. If the pulse width is not within stated times, adjust potentiometer P61 on the card in position P. Adjusting P61 clockwise decreases the pulse width for a given input current level, and adjusting P61 counterclockwise increases the pulse width. Once it has been determined that the proper output pulse width has been obtained, do not readjust P61.

If the SLD51A relay is being used in a relaying scheme which uses both squaring amplifier ouput signals, then the signals at pins 8 and 9 of the card in position P should be observed on an oscilloscope. The two signals will be very nearly identical relay rated frequency pulse trains, except they will be 180 degrees out of phase. Since the pulse width of the two signals may not be exactly the same, P61 should be adjusted such that both signal pulse widths are as near to 6.0 milliseconds (60 hertz relays) or 7.2 milliseconds (50 hertz relays) as possible for the proper single phase input test current.

FDL and FDH Pickup Settings

The pickup settings for FDL and FDH in the SLD51A can be made using a single phase test circuit as in Figure 11. The A and B connections in Figure 11 are determined by the desired pickup level of FDL. Refer to Table II in the **RANGES** section of this book for the necessary link positions and terminal point connections to give the range that includes the desired pickup level. These connections and link positions must be the same as those used to check the operation of the squaring amplifier. Make the B connection to DB4 and the A connection to DB1 or DB2 or DB3, depending on the pickup level of FDL. Make sure that the K taps on the card in position N are set for K = infinity.

Apply a single phase test input current of three times the desired FDL negative sequence current pickup level. Adjust potentiometer P11 on the card in position R to just pick up FDL. FDL pickup occurs when the signal at TP7 steps from less than one volt DC to approximately 15 volts DC. The pickup level is increased by adjusting P11 in the clockwise direction, and is decreased by adjusting P11 in the counterclockwise direction. Lower and raise test current several times to assure that FDL picks up at the proper level of input current. Refine the adjustment of P11 if necessary. When the desired FDL pickup level is achieved, make no further adjustments to P11.

Use the same test setup used for setting the pickup level of FDL to set the pickup level of FDH. Since the FDH setting depends on the FDL setting, make sure that FDL is properly set before attempting to set the pickup level of FDH. Apply a single phase test current equal to three times the desired negative sequence current pickup level. Adjust potentiometer P21 on the card in position R until FDH just picks up. FDH pickup occurs when the signal at TP8 steps from less than one volt DC to approximately 15 volts DC. The pickup level is increased by adjusting P21 clockwise and is decreased by adjusting P21 counterclockwise. Lower and raise the test current several times to assure that FDH picks up at the proper level of input current. Refine the adjustment of P21 if necessary. When the desired FDH pickup level is achieved, make no further adjustments to P21.

If the SLD51A relay is to be used with a K tap other than K = infinity, set all the K taps on the card in position N for the proper value. On an A phase to ground test for K = 10, FDL and FDH will have a single phase test current pickup level, which is approximately 11 percent greater than their pickup level for K = infinity. For K = 7, the single phase test current pickup level for FDL and FDH will be approximately 17 percent greater than their pickup level for K = infinity. For K = 5, the single phase test current pickup level for FDL and FDH will be approximately 25 percent greater than their pickup level for K = infinity. On a B or C phase to ground test, the pickup level will be less than the level for K = infinity by 4.8 percent for K = 10, 7.4 percent for K = 7, and 10 percent for K = 5.

Channel Signal Symmetry Adjustment

The adjustment of the channel signal symmetry refines the duration of the block and trip half cycles of the channel signal. This adjustment compensates for asymmetry in the channel signal which may be caused by the receiver-tuned filters. Since this adjustment depends on operating conditions in service, it cannot be made at the factory. Before making this adjustment, it is essential that the channel receiver and transmitter be adjusted as prescribed in the INSTALLATION ADJUSTMENT section of the channel set instruction book. The actual channel symmetry adjustment is made in the associated SLA or SLAT relay of a complete phase comparison scheme. The procedure is detailed herein because it is necessary to energize the SLD51A to make the adjustment.

Assume that the protected line is A to B, with A being the local terminal and B the remote terminal. At station B, connect an oscilloscope to observe the received channel signal in the SLA or SLAT relay. Supply the SLD51A at A with a single phase test current as in Figure 11. Make the same terminal connections as were used for setting FDL and FDH at A. Apply a test current which exceeds the FDL test pickup level and which is at least twice the squaring amplifier test operating level. In some cases a test current which meets these two conditions may also pick up FDH. If this is objectionable, temporarily adjust FDH for a higher pickup level, and then later readjust it as previously described in this book. Applying this input current to the relay at A will assure that the keying signal is fairly symmetrical.

At station B, set the oscilloscope horizontal sweep such that one full cycle of the received signal can be observed. Note the duration of the block and trip half cycles. Adjust the pickup and/or the dropout time delay of the symmetry adjustment

timer to make the duration of the block and trip half cycles as nearly equal as possible. The frequency of this signal should be relay rated frequency. In many cases this symmetry adjustment timer will be located in the received signal logic in the SLA or SLAT relay at B; in some cases, it may be located in the keying signal logic of the SLA or SLAT relay at A. In either case, the received signal must be symmetrical. The upper potentiometer on the symmetry adjustment timer adjusts pickup time. Turning this potentiometer clockwise increases pickup time. The lower potentiometer on the symmetry adjustment timer adjusts dropout time. Turning this potentiometer clockwise increases dropout time. Refer to the instruction book for the associated SLA or SLAT relay for more specific information which may be required about this timer.

The received channel signal at station A must also be adjusted for symmetry between the block and trip half cycle. This should be done in the same manner as just described. This should only be done after the fault detectors are properly set at B.

Phase Delay Adjustment

The object of the phase delay adjustment is to set the local trip half cycle at A to be in phase with the received block half cycle from B. This condition results from a through fault. This adjustment is necessary to compensate for such things as channel delay introduced by the receiver filters and propogation time of the line. Since the phase delay is affected by service conditions, it cannot be made at the factory. Phase delay is also affected by channel symmetry, and therefore the channel symmetry adjustment must be made before the phase delay adjustments are made.

Three possible methods of making the phase delay adjustment, with the limiting conditions of each, are given below:

Load Current Method:

In this test, load current in the line is used to simulate negative sequence current. It is necessary that the secondary load current be greater than the negative sequence current setting of the FDL and FDH fault detectors, or that load current be at least equal to twice the minimum available setting of FDL, in which case it will be necessary to temporarily reduce the FDL and FDH setting to their minimum values. If this method is to produce an accurate setting, it also is necessary that the ratio of line charging current to through-load current be low enough so that the phase displacement between currents at the two ends of the line does not exceed ten degrees.

If these conditions are met, the procedure outlined below should be followed. If they are not met, it will be necessary to use one of the alternate schemes described below.

At each terminal, reverse the phase B and phase C system connections to the SLD51A. In other words, connect phase C current to DB5 or DB6 or DB7 and DB8, and connect phase B current to DB9 or DB10 or DB11 and DB12. This will make balanced load current look like negative sequence current to the relay. This current must be greater than the negative sequence current pickup level of FDL and FDH, and it must

be at least twice the negative sequence operating level of the squaring amplifier. If necessary, temporarily reduce the operating levels of the squaring amplifier, FDL and FDH, and later return them to their proper settings as previously described.

At station A (local) a continuous signal must be applied to the channel stop logic in the SLA or SLAT relay to prevent local transmission of the channel signal. At station B (remote) a trip output must be prevented from stopping transmission of a channel signal from that end. Before applying test signals to or removing cards from the logic circuitry, be sure to refer to the instruction book for the particular SLA or SLAT relay and to the MOD III printed circuit card instruction book, GEK-34158, for the proper precautions and limitations.

Using a dual trace oscilloscope at A, connect one trace to the symmetrically adjusted received signal from B and the other to the output of the phase delay timer at A. The received signal from B will be a symmetrical square wave with equal block and trip half cycles. The output signal from the phase delay timer will also be nearly symmetrical. However, the trip half cycle of the local signal will probably lead the block half cycle of the remote signal by a few milliseconds. Adjust the pickup delay and the dropout delay of the phase delay timer so that the local trip half cycle is exactly in phase with the received block half cycle, and so that the local block half cycle is exactly in phase with the received trip half cycle. The upper potentiometer on the phase delay timer adjusts pickup time. Turning this potentiometer clockwise increases pickup time. The lower potentiometer on the phase delay timer adjusts dropout time. Turning this potentiometer clockwise increases dropout time.

When these adjustments are complete, do not readjust the phase delay timer. Return the relay connections to their proper locations, and readjust the operating levels of the squaring amplifier, FDL and FDH, if necessary.

Test Source Method:

If the line is not loaded, is carrying insufficient load, or if the ratio of charging current to load current is too high, an AC test source can be used at each station to operate FDL, FDH and the squaring amplifier, provided the sources are in phase. Use the test connections shown in Figure 11 at station A and similar connections at station B, except interchange the connections to A and B. In other words, at station A connect A to DB1 or DB2 or DB3, and connect B to DB4. At station B, connect A to DB4 and connect B to DB1 or DB2 or DB3. This will simulate a through-fault condition.

Before proceeding with phase delay adjustments, the phase relation of the two test sources should be checked to insure that the two sources are in phase. If power line carrier is used, the following procedure is applied. With the test connections as just described at each terminal of the line, raise the single phase test current to a level which is at least twice the test operating level of the squaring amplifier, and which is greater than the test pickup level of FDL. If this level also exceeds the test pickup level of FDH, temporarily readjust FDH for a higher level and later readjust FDH for the proper level as described previously in this book. FDH must be readjusted to its proper pickup setting before making the actual phase delay setting.

At the local terminal, connect the vertical input of the scope to the RF jack of the carrier receiver and the scope ground to the carrier chassis. Two levels of the RF should be observed on the scope; the higher from the local transmitter, and the lower from the remote transmitter. If the two test sources are substantially in phase, the two levels of carrier RF should adjoin each other every half cycle with very little dead space or overlap between adjacent levels of carrier. For the phase delay adjustment to have any value, the dead space, or overlap, should not exceed 10 degrees.

The AC source for the test connections of Figure 11 will usually be station service AC. On long line applications, it will be found that the test sources are displaced by too great an angle to be of any use for the installation adjustment of the phase delay.

If at least one of the stations of the protected line is equipped with line-side potential devices or transformers, it is possible that substantially in-phase test sources can be obtained at the two ends by supplying the test circuit of Figure 11 from the potential device or transformer, and operating the line with the breaker at one end open. The open end is the location where line-side potential is available. With this arrangement, the voltages at the two ends will differ only by the drop in the line inductive reactance caused by the line capacitive charging current, and this will primarily be a magnitude difference. It is essential that the normal installation adjustments be made on the potential devices prior to this test.

Having obtained AC test sources that are substantially in phase, proceed to adjust the phase delay settings as described in Load Current Method, above.

Local Signal Method:

If neither of the above adjustment methods can be used, an adjustment of the phase delay can be made on the basis of the local keyed-carrier signal. This method assumes that power line carrier is used, and the carrier receiver gain control and attenuator have been temporarily reset to provide the "normal margin" above the cutoff point of the received signal due to local transmission. The recommended "normal margin" is given in the carrier equipment instruction book section on INSTALLATION ADJUSTMENTS.

First, cause the local transmitter to send a full-strength RF signal. Observe and record where receiver attenuator is set, and then turn the receiver attenuator in a counterclockwise direction until the cutoff point is reached. Now turn the attenuator back to provide the normal margin (as noted previously) from this cutoff point, as determined by the attenuator dial markings. Presumably with this attenuator setting, the local transmitter will drive the local receiver at approximately the same level as the RF signal received from the remote terminal would drive it, with the installation settings of the transmitter and receiver.

The test circuit of Figure 11 will be used. Make connection A to DB1 or DB2 or DB3 and make connection B to DB4. Apply a single phase test current which is at least twice the test operating current level of the squaring amplifier and which will cause FDL and FDH to pick up.

Using a dual trace oscilloscope, connect one scope input to the RF jack on the carrier set and connect the other scope input to the received carrier signal. Connect scope reference to relay logic reference. The received carrier signal should be very close to those for which the symmetry adjustment was made. Now shift the scope input, which was monitoring the RF, to the output of the phase delay timer. Adjust the pickup delay and dropout delay of the phase delay timer so that the trip output from the phase delay timer is exactly in phase with the received trip signal, and that the block output from the phase delay timer is exactly in phase with the received block signal.

This adjustment method neglects propogation time of the carrier signal between the two terminals, which is one millisecond for 186 miles of line. The setting can be further refined for long lines by calculating the theoretical propagation time for the line, and shifting the trip signal to the right (delayed) by a time interval equivalent to this propagation time.

After the setting is complete, reset the attenuator at its original position as recorded at the start of this test.

## PERIODIC CHECKS AND ROUTINE MAINTENANCE

### PERIODIC CHECKS

Before starting any periodic tests on the SLD51A relay, the trip coil circuit from the associated SLAT relay to the circuit breaker trip coil should be disconnected.

During a periodic check of the equipment, the squaring amplifier operating level and the FDL and FDH pickup levels should be checked against the factory settings, or against the settings made during installation tests. These should be checked using the procedures outlined in the DETAILED TESTING INSTRUCTIONS section of this book.

### TROUBLESHOOTING

In troubleshooting a complete relay equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment contains the combined logic of the SLD51A relay and other associated relays. It also gives the location of the various test points in each unit. By signal tracing, using the overall logic diagram, and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the pre-wired test points on the test cards. Use of the adapter card is described in the MOD III printed circuit card instruction book, GEK-34158. The internal connections diagrams of the printed circuit cards used in the SLD51A relay are shown in that book, as well as in Figures 5, 5A, 7, 7A, 8 and 8A of this book.

At no time should an external test signal be jumpered into a test point without first removing the printed circuit card which normally supplies the signal to that point.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift and operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

## SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust.

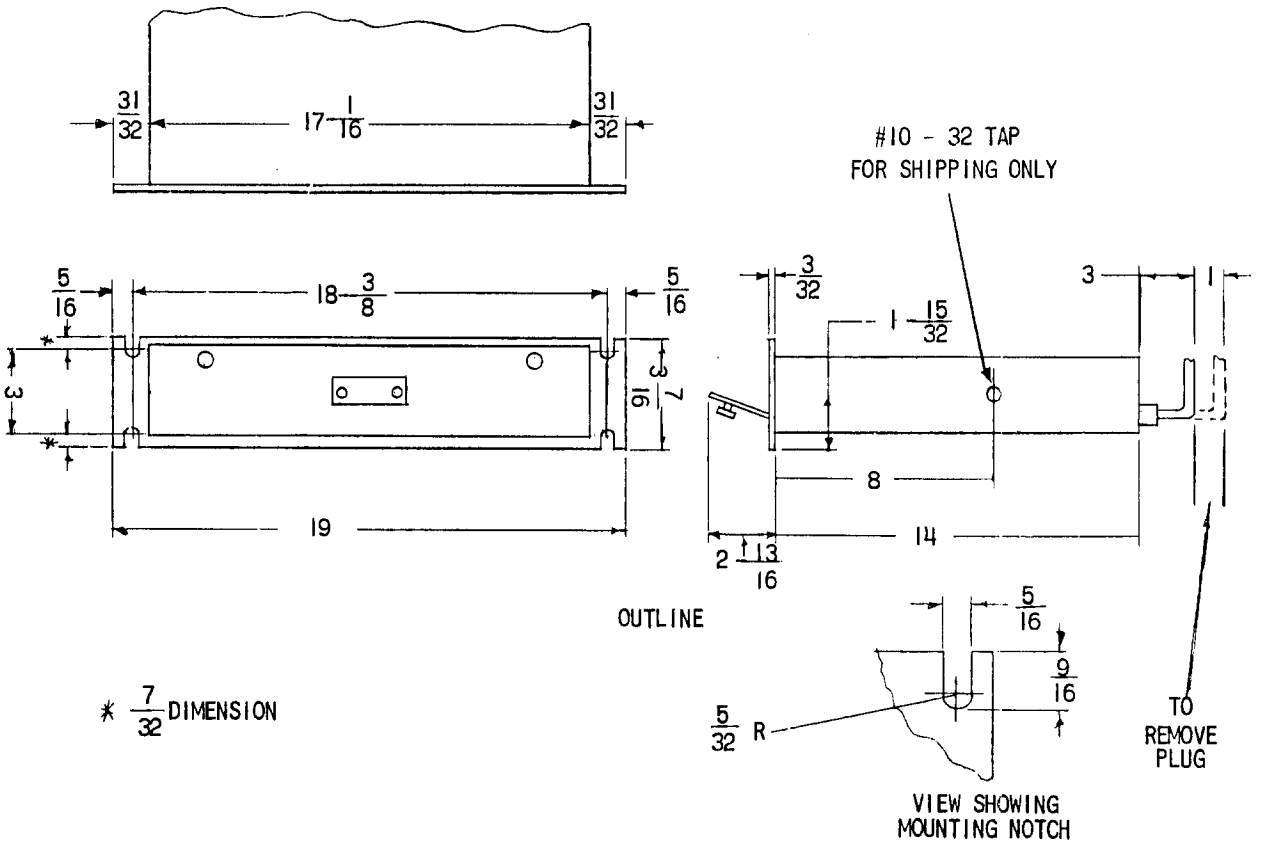
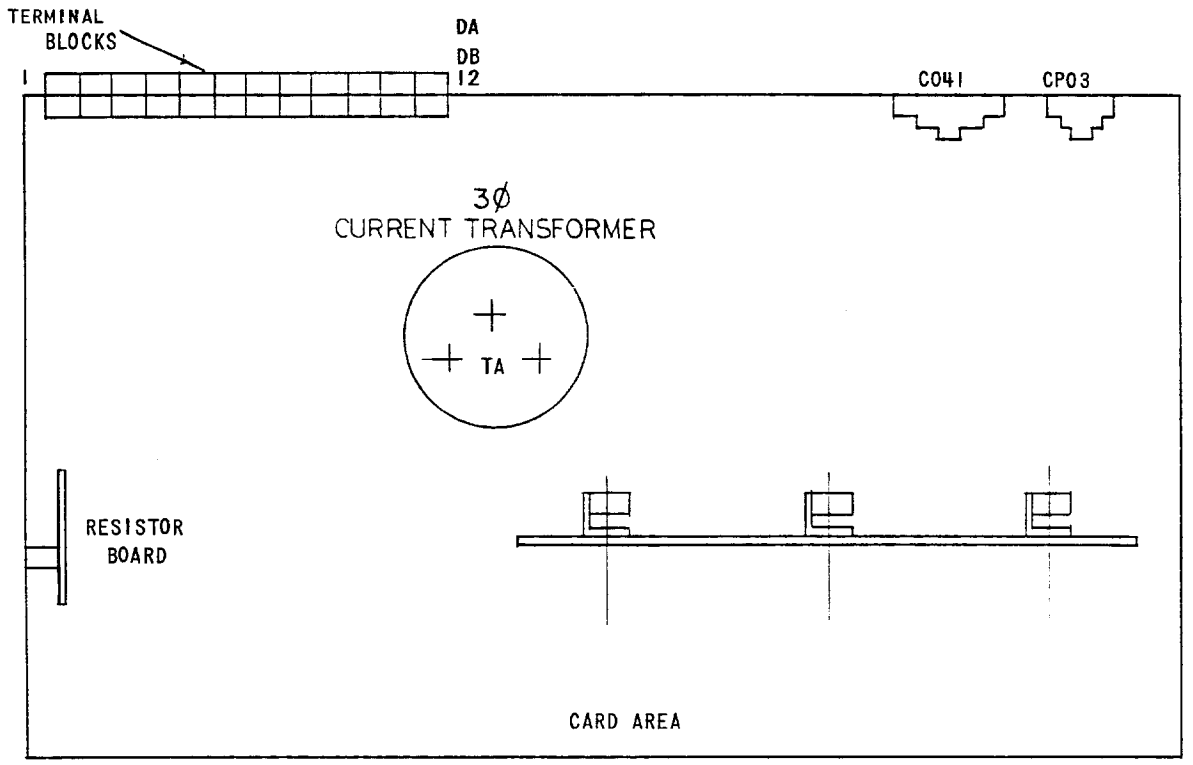



Figure 1 (0227A2036-0) Outline and Mounting Dimensions for Type SLD51A Relay



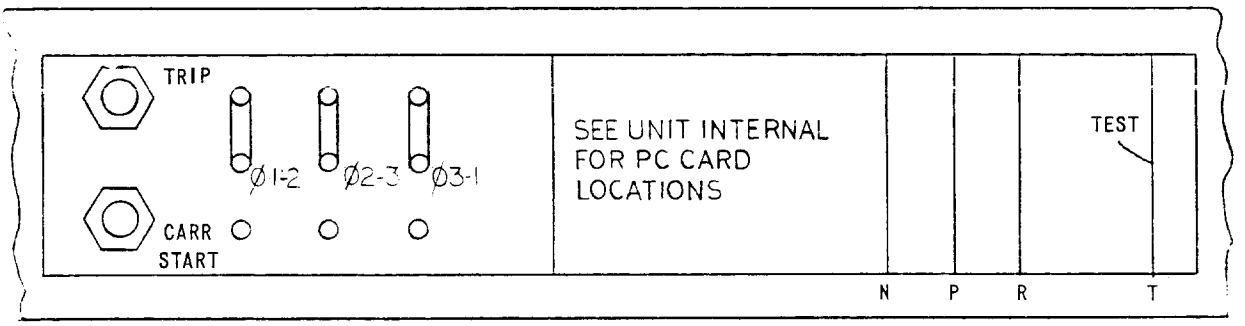
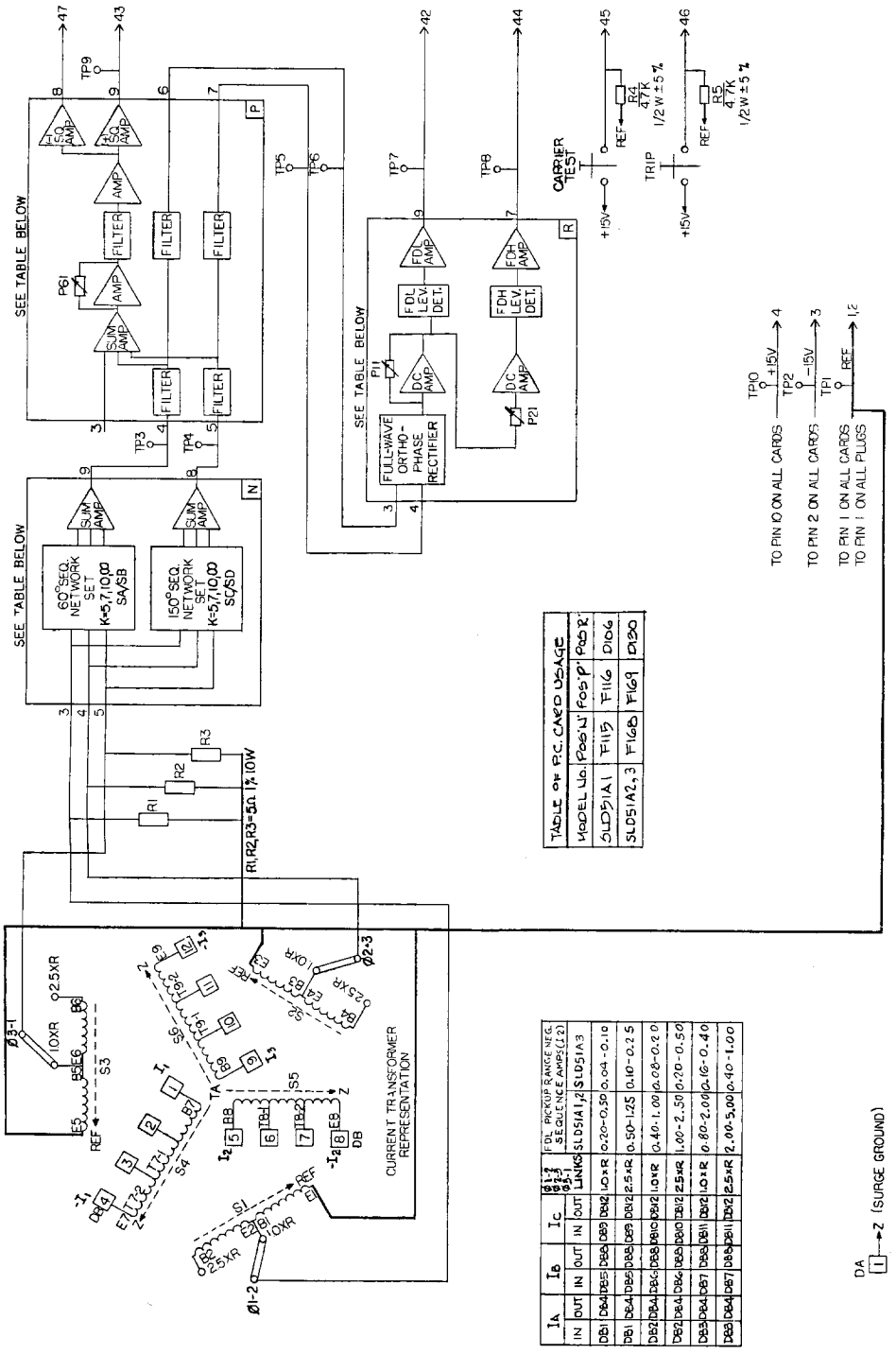




Figure 2 (0246A6561-2) Component Location Diagram for Type SLD51A Relay




| TABLE OF P.C. CARD USAGE | | | |
|---|---|---|---|
| MODEL No. | POS'N | POS'P | POS'R |
| SLD51A1 | F115 | F116 | D104 |
| SLD51A2,3 | F168 | F169 | D130 |

| Ia IN | Ia OUT | Ib IN | Ib OUT | Ic IN | Ic OUT | 81:1 81:2 81:3 LINKS | FDL PICKUP RANGE NEG. SEQUENCE AMPS (I2) SLD51A1,2 | SLD51A3 |
|---|---|---|---|---|---|---|---|---|
| DB1 | DB4 | DB5 | DB3 | DB9 | DB2 | 1.0 X R | 0.20-0.50 | 0.04-0.10 |
| DB1 | DB4 | DB5 | DB5 | DB9 | DB2 | 2.5 X R | 0.50-1.25 | 0.10-0.25 |
| DB2 | DB4 | DB6 | DB6 | DB10 | DB2 | 1.0 X R | 0.40-1.00 | 0.08-0.20 |
| DB2 | DB4 | DB6 | DB7 | DB10 | DB2 | 2.5 X R | 1.00-2.50 | 0.20-0.50 |
| DB3 | DB4 | DB7 | DB5 | DB11 | DB2 | 1.0 X R | 0.80-2.00 | 0.16-0.40 |
| DB3 | DB4 | DB7 | DB7 | DB11 | DB2 | 2.5 X R | 2.00-5.00 | 0.40-1.00 |

Figure 3 (0149C7244-6) Internal Connections Diagram for Type SLD51A Relay

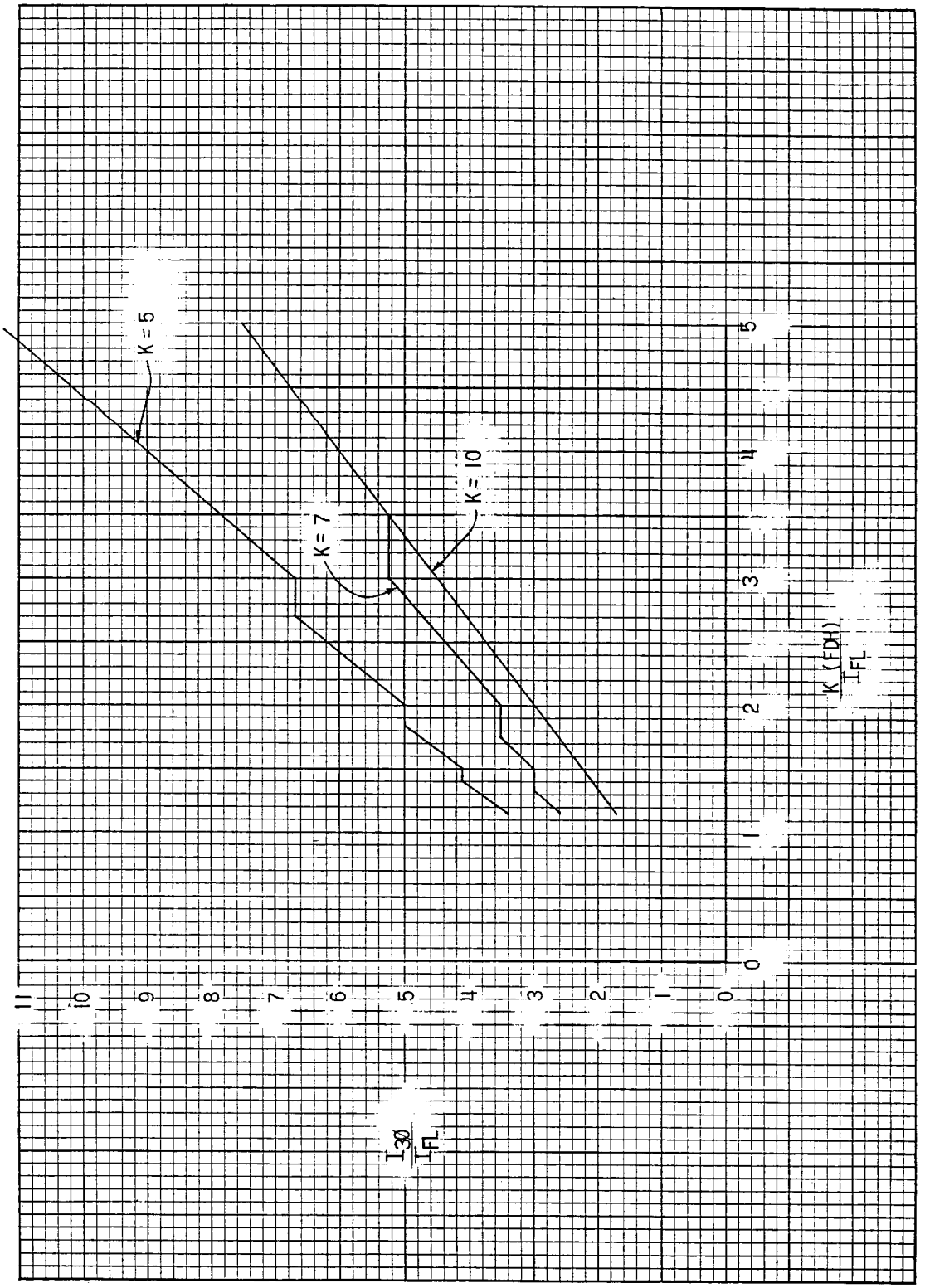



Figure 4 (0257A3297-0) $I_{3\emptyset}/I_{FL}$ Versus $K(FDH)/I_{FL}$ for Three Values of K

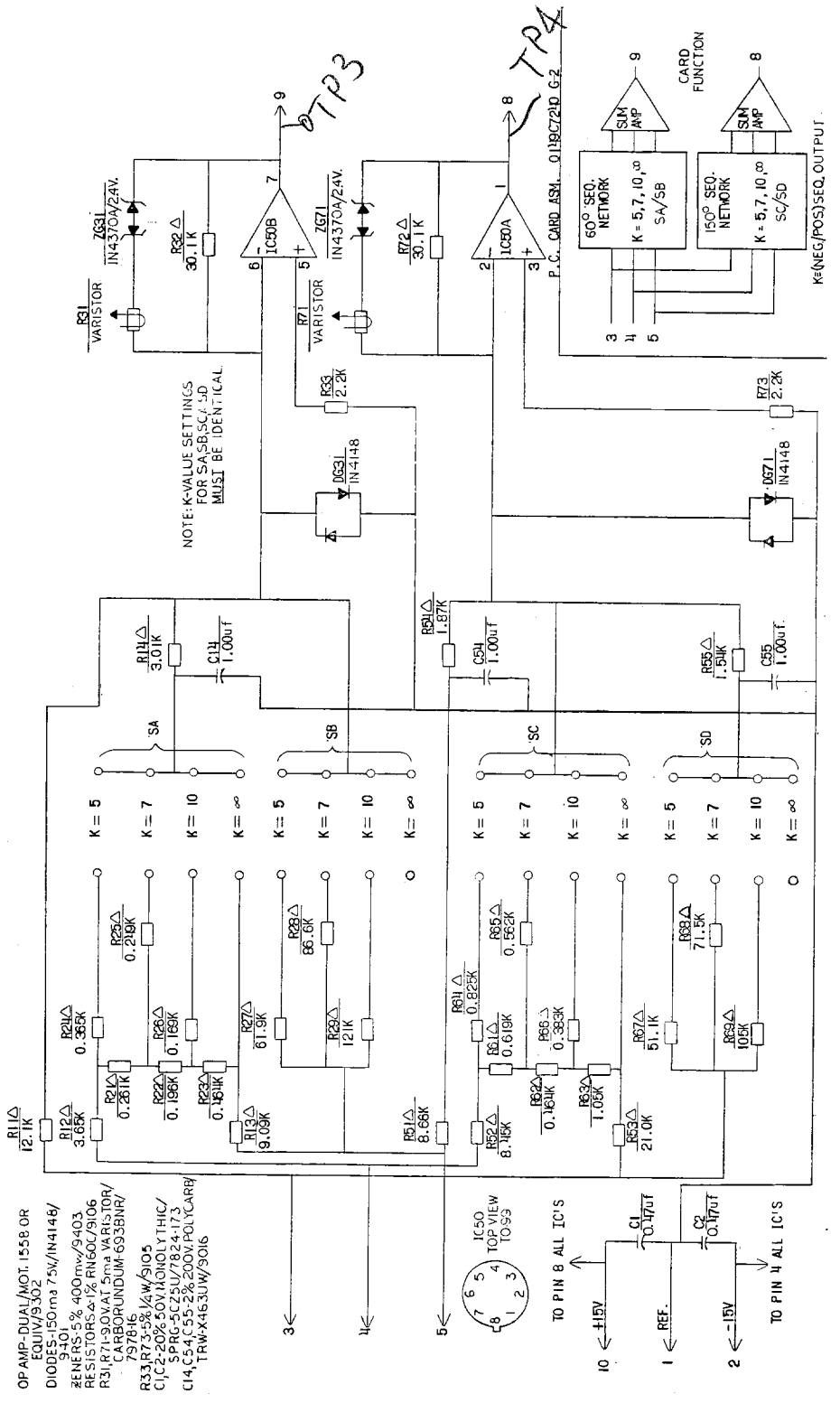



Figure 5 (0108B9683AB-0) Internal Connections Diagram for the F115 Mixing Network Card (60 hertz)

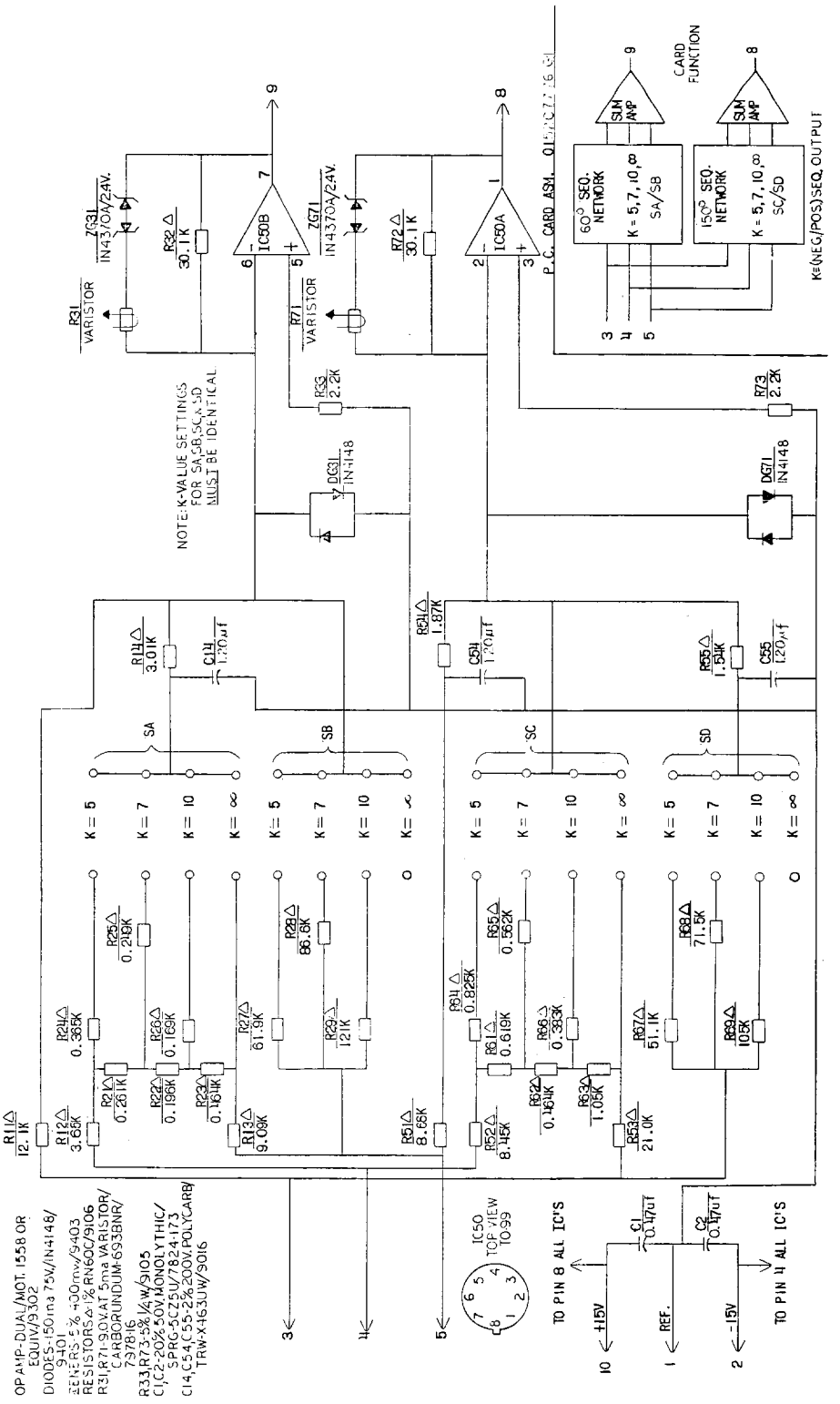



Figure 5A (0108B9683AC-0) Internal Connections Diagram for the F168 Mixing Network Card (50 hertz)

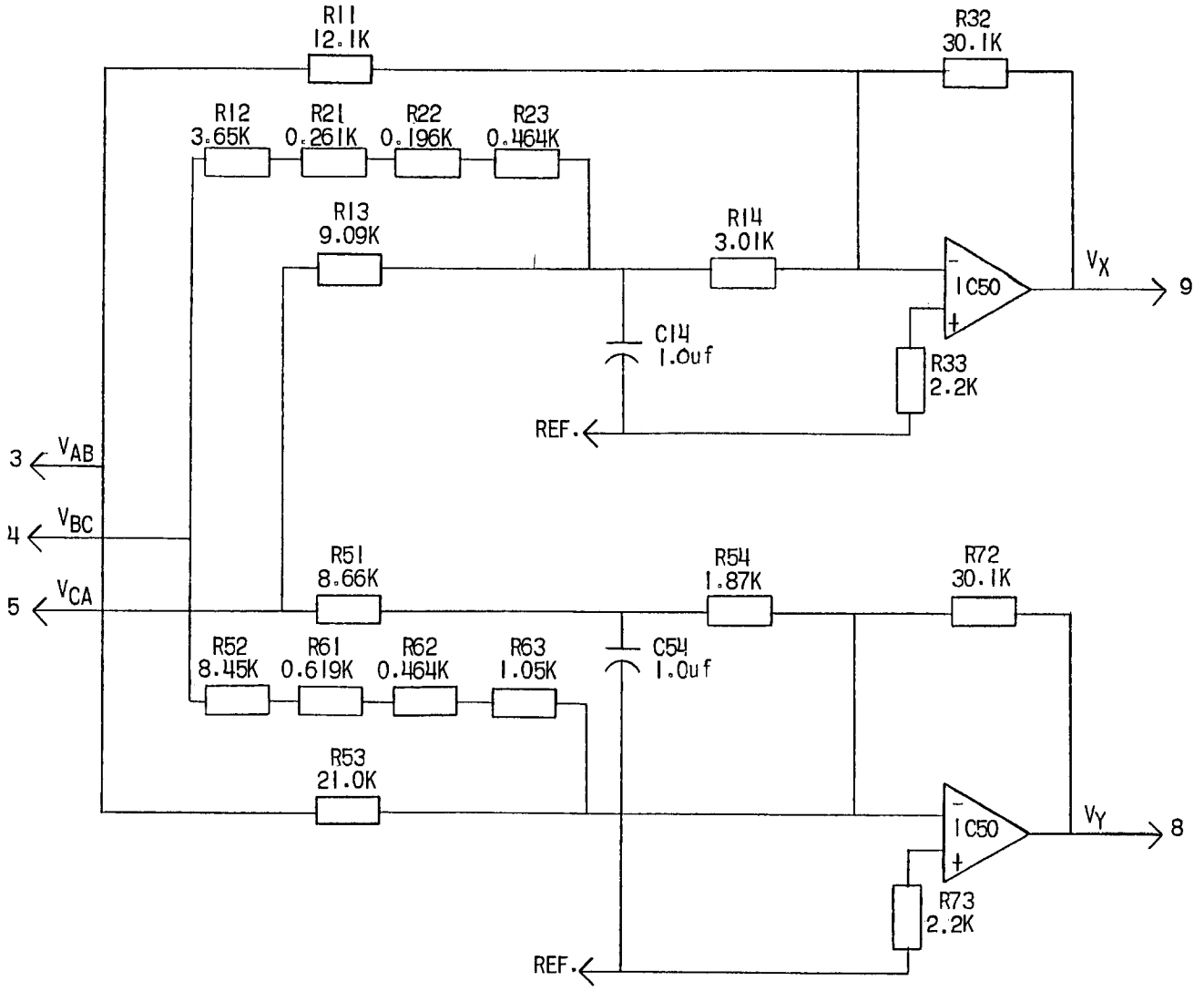



Figure 6 (0257A5046-0) Pure Negative Sequence Mixing Network (60 hertz)

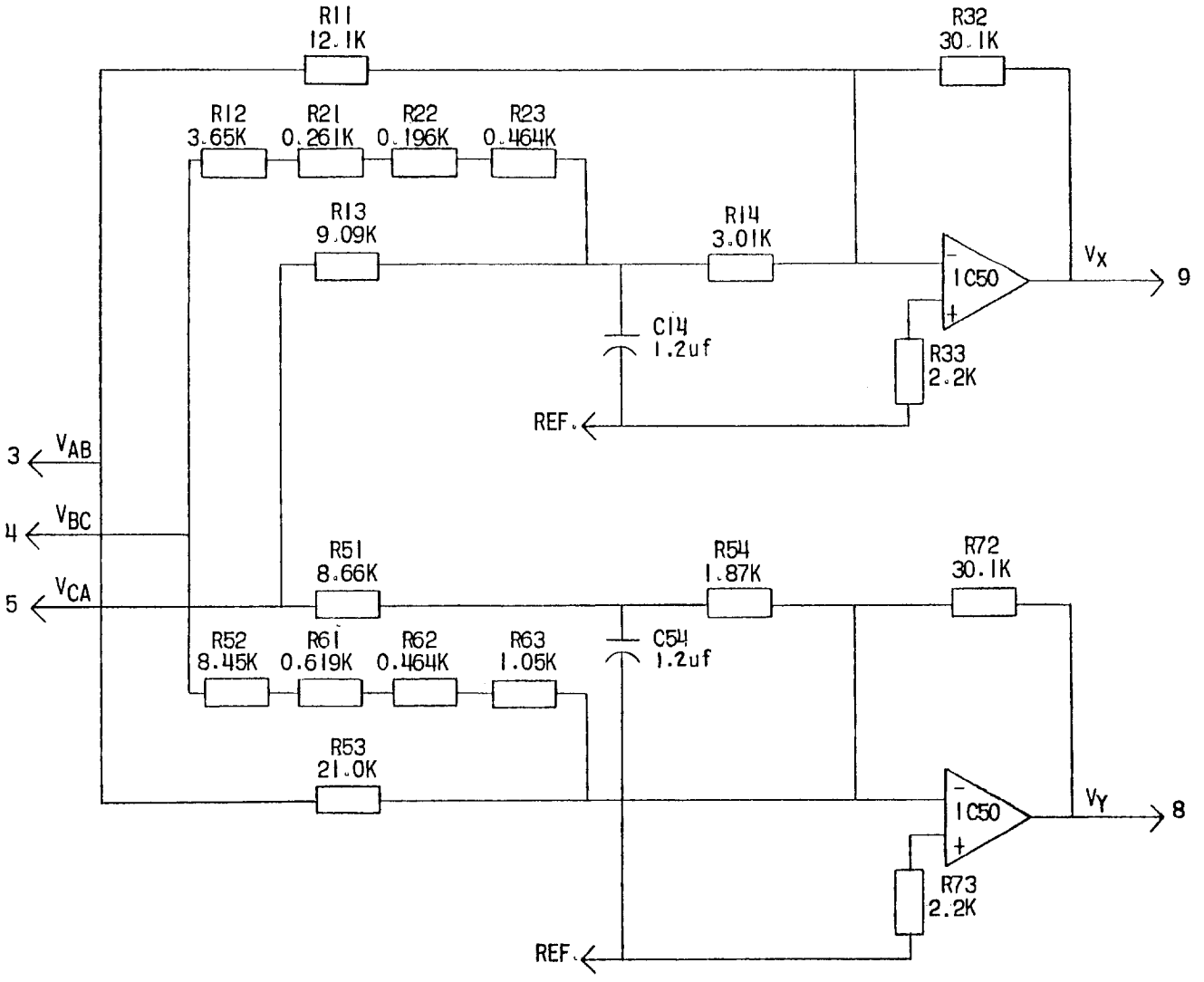



Figure 6A (0285A8137-0) Pure Negative Sequence Mixing Network (50 hertz)

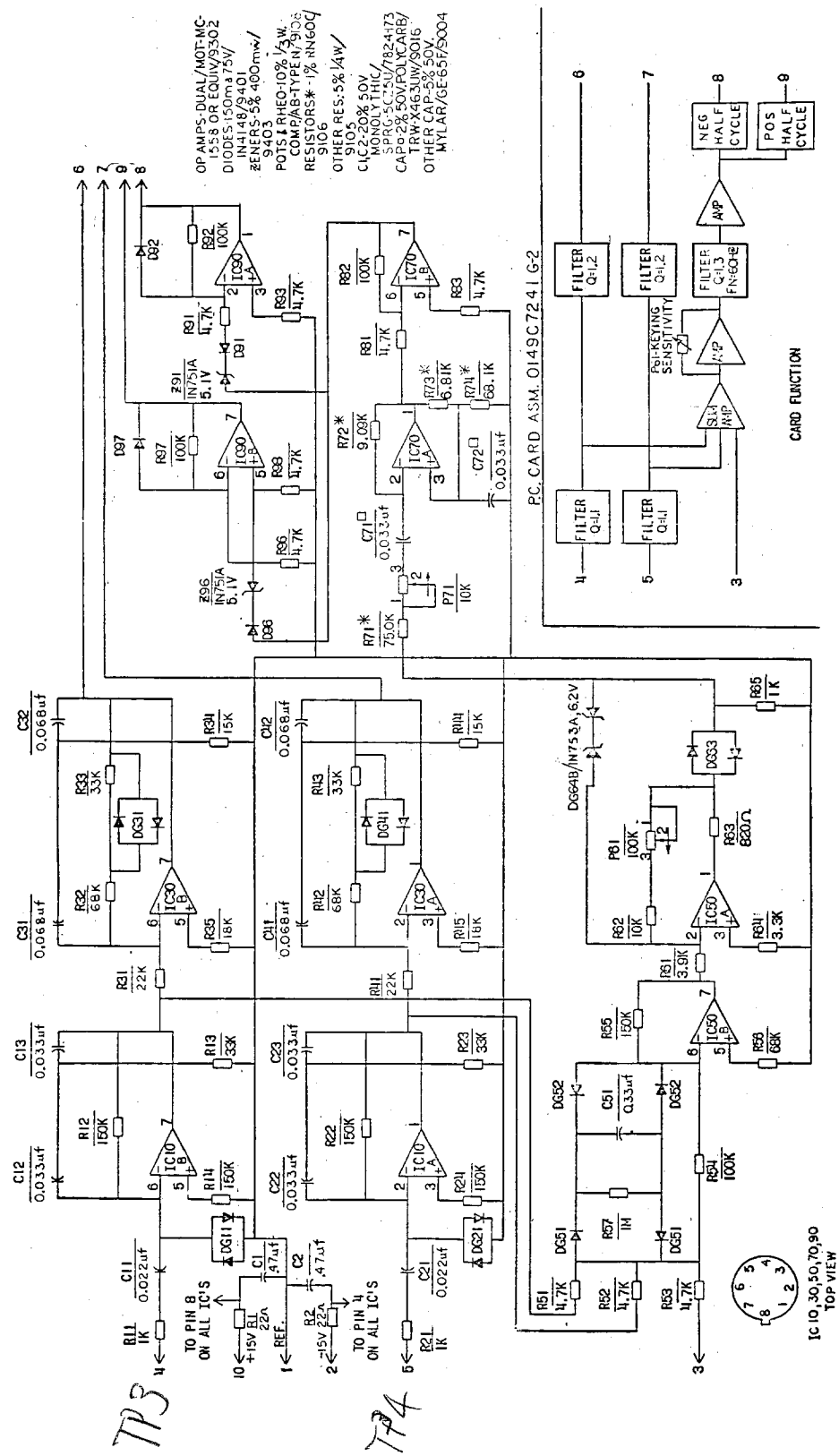



Figure 7 (0183B4556AB-1) Internal Connections Diagram for the F116 Filter/Keying Card (60 hertz)

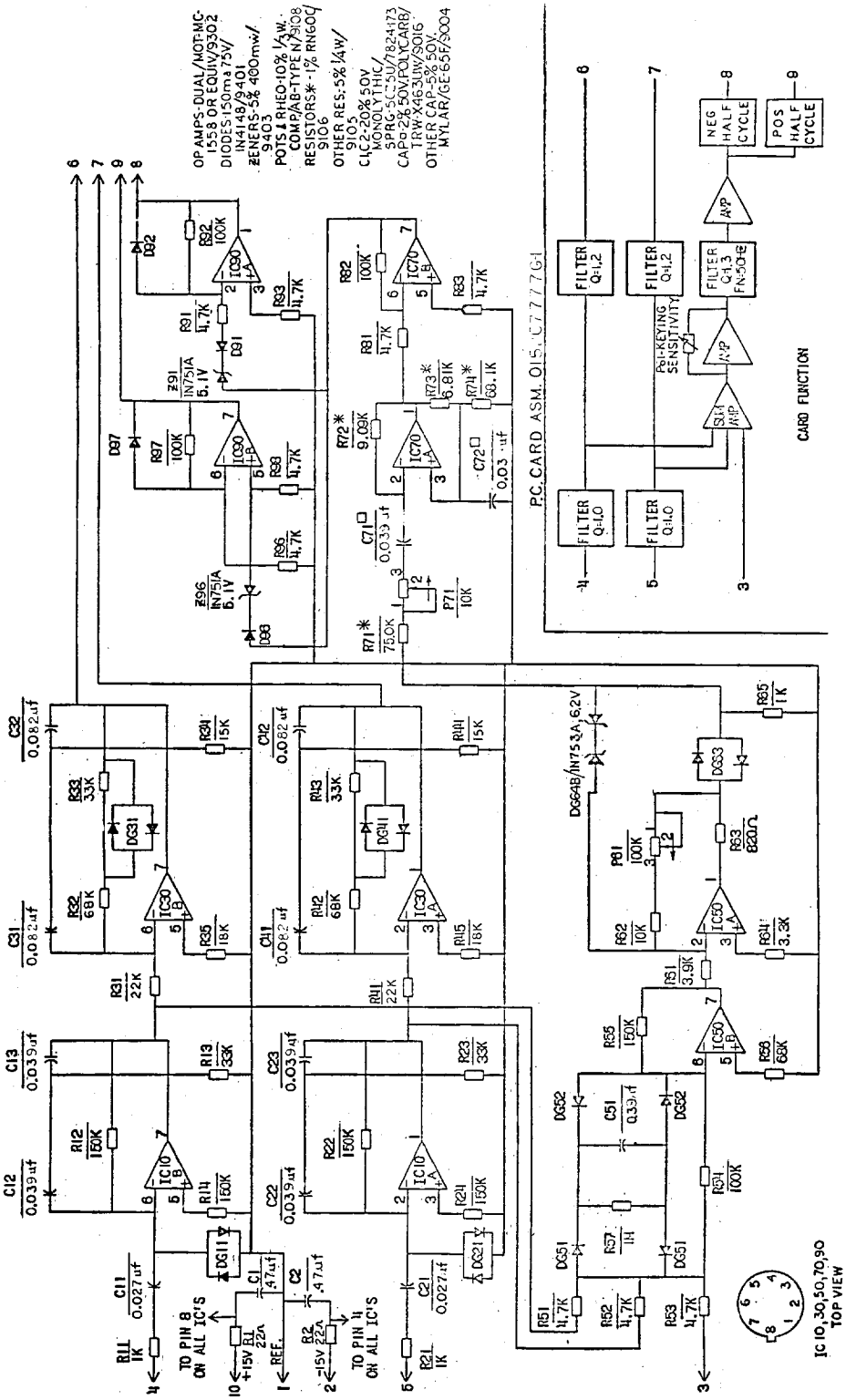



Figure 7A (0183B4556AC-0) Internal Connections Diagram for the F169 Filter/Keying Card (50 hertz)

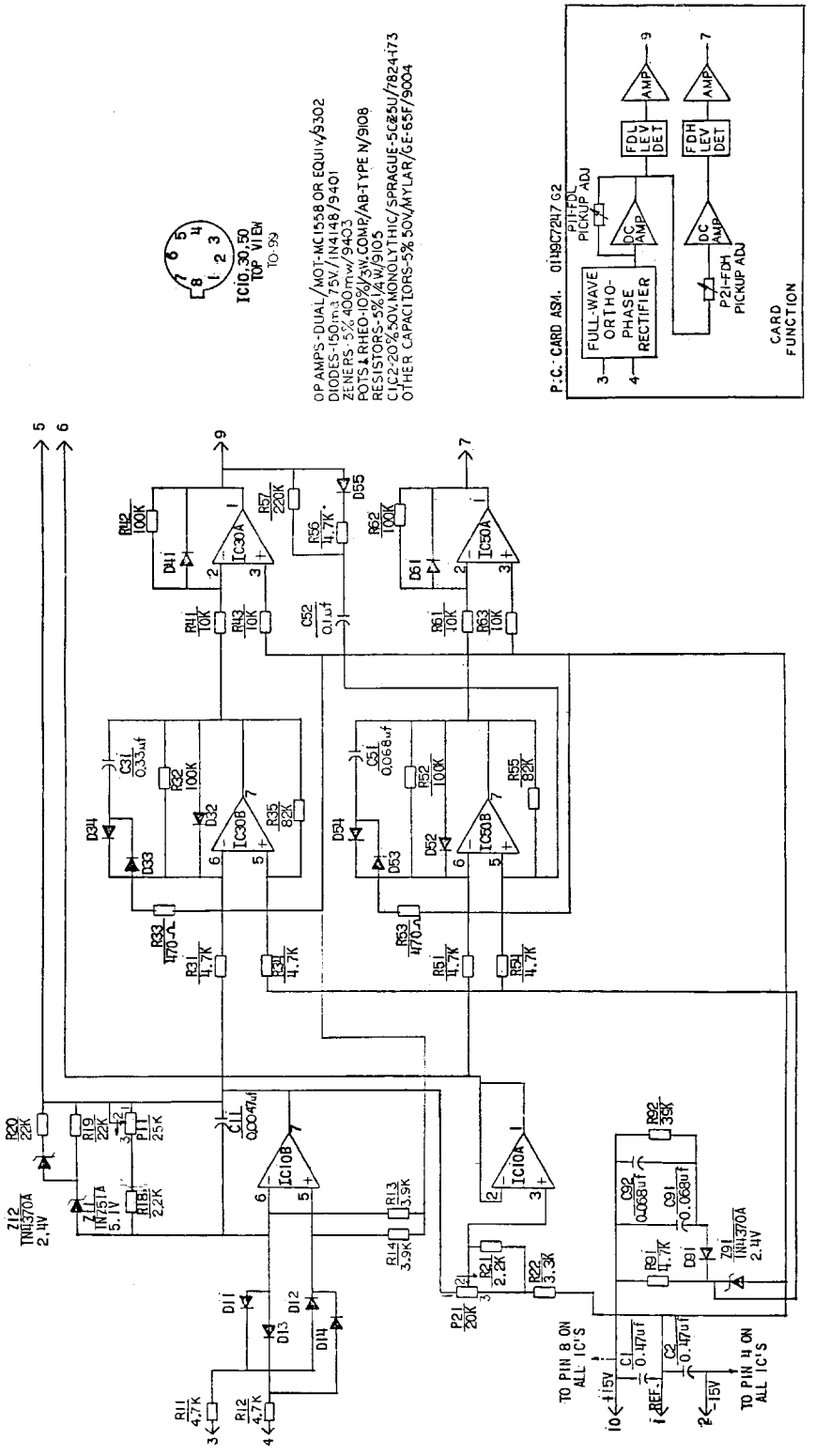



Figure 8 (0183B4557AB-2) Internal Connections Diagram for the D106 Fault Detector Circuit Card (60 hertz)

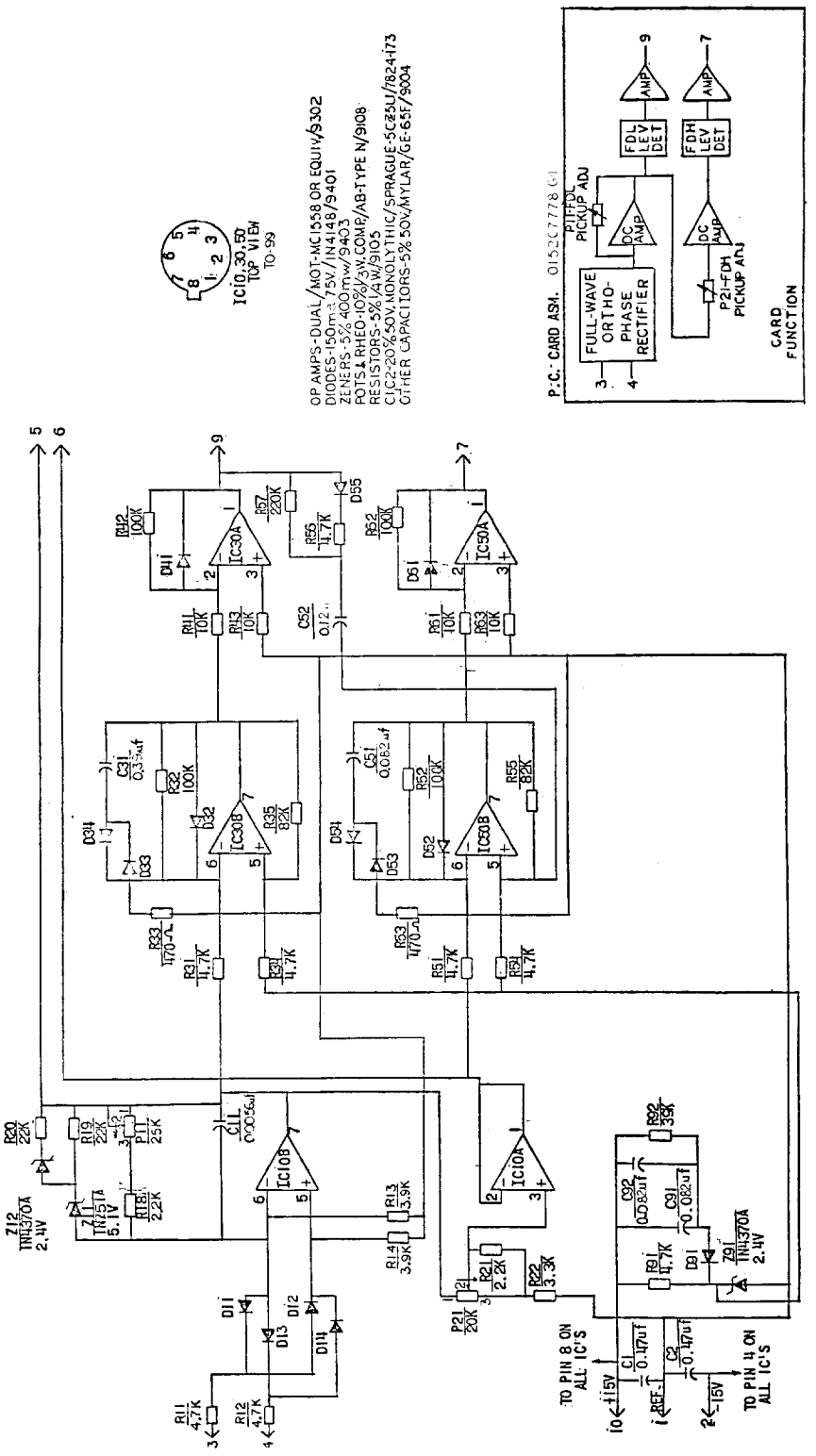



Figure 8A (0183B4557AC-0) Internal Connections Diagram for the D130 Fault Detector Circuit Card (50 hertz)

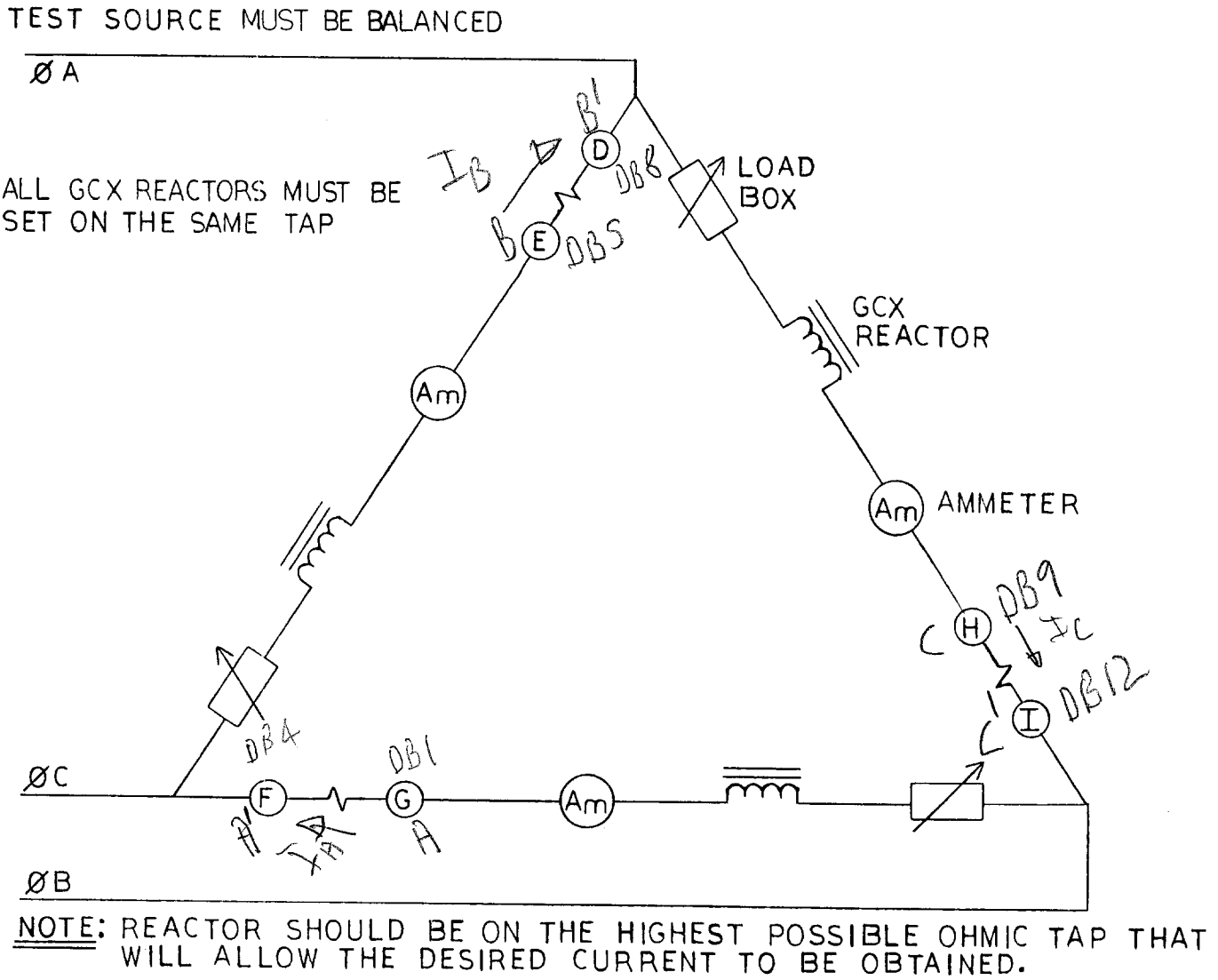



Figure 9 (0246A6883-1) SLD51A Mixing Network Test Connections - Method I

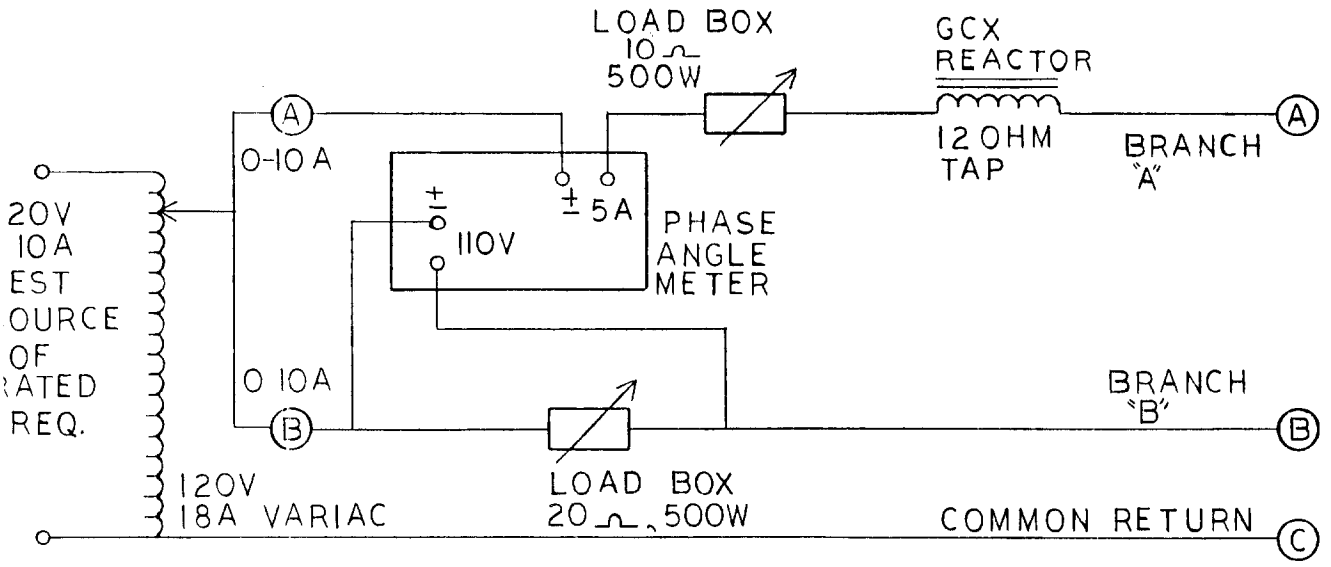
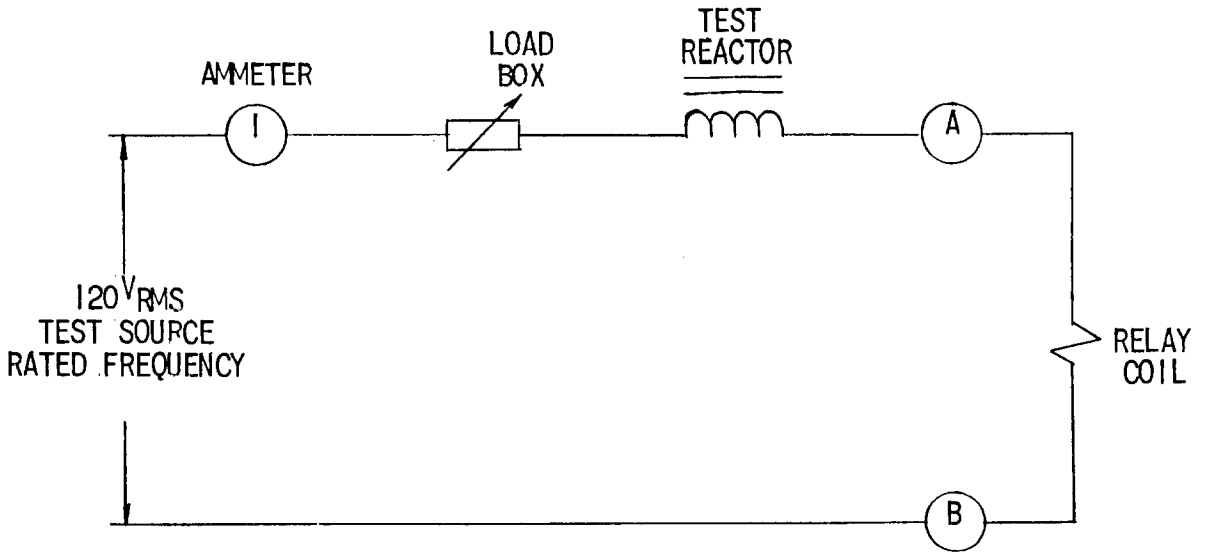



Figure 10 (0246A6882-1) SLD51A Mixing Network Test Connections - Method II




NOTE: THE REACTOR SHOULD BE ON THE HIGHEST POSSIBLE OHMIC TAP THAT WILL ALLOW THE DESIRED CURRENT TO BE OBTAINED.

Figure 11 (0227A2185-0) SLD51A Single Phase Fault Detector Test Circuit

# APPENDIX I

## EFFECTS OF LINE CHARGING CURRENTS ON FDH AND FDL PICKUP SETTINGS

When an unbalanced fault occurs on a power system, negative sequence fault currents will flow and negative sequence voltages will be present. These voltages will cause negative sequence charging currents to flow as a result of the distributed capacitance of the system.

In general, when an unbalanced fault occurs adjacent to the line being protected, the negative sequence current in the protected line and in the associated relays will be made up of fault plus charging components of current. This is illustrated in Figure I-1. Thus, the negative sequence current ($I_X$) entering one terminal will differ from the negative sequence current ($I_Y$) that is leaving the other terminal, this difference being due to the negative sequence line charging current ($I_C$).

Since $I_C$ is capacitive and $I_X$ and $I_Y$ are inductive, $I_C$ will be 180 degrees out of phae with $I_X$ and will cancel some of it. For this reason, $I_Y$ will be smaller than $I_X$ by the magnitude of $I_C$. The magnitude of $I_C$ will depend on the magnitude of $C_2$, which in turn, depends on the length of the line. The magnitude of $I_C$ also depends on the negative sequence voltage distributed along the line, which in turn, is dependent on the system impedances.

Coordination of a phase comparison scheme on an external fault is dependent on FDL at one end of the line having a lower pickup than FDH at the other end. This insures proper blocking on external faults. However, if there is significant charging current ($I_C$) flowing for an external fault, $I_X$ will be greater than $I_Y$, and this will tend to negate the difference on pickup settings. This must be considered when setting FDH and FDL.

For two-terminal lines, the relation between the FDH settings at one end, to FDL settings at the other end, should be:

$$FDH_X \quad I_C + \frac{4}{3} FDL_Y \qquad \text{(Eq. I-1)}$$

For three-terminal lines, this should be: (see Figure I-2)

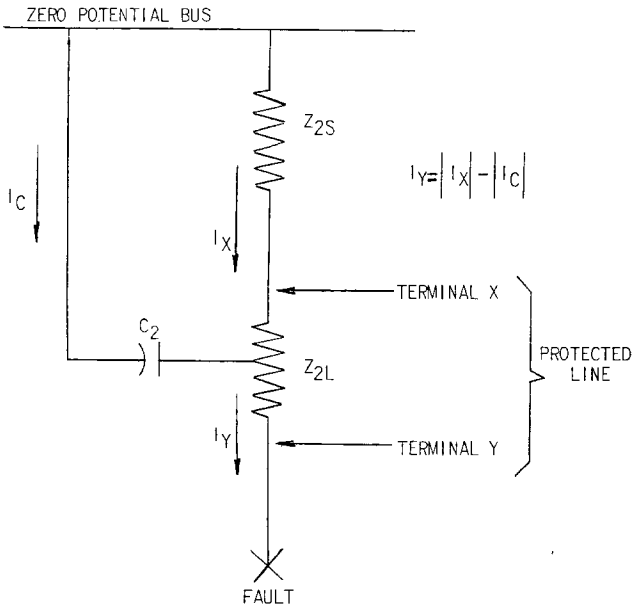
$$FDH_X \quad I_C + \frac{8}{3} FDL_Y \qquad \text{(Eq. I-2a)}$$

$$FDH_X \quad I_C + \frac{8}{3} FDL_Z \qquad \text{(Eq. I-2b)}$$

For equations I-1 and I-2, and Figures I-1 and I-2, it is apparent, particularly for three-terminal lines, that a simplified approach for the evaluation of $I_C$ is desirable. A method to do this is outlined below.

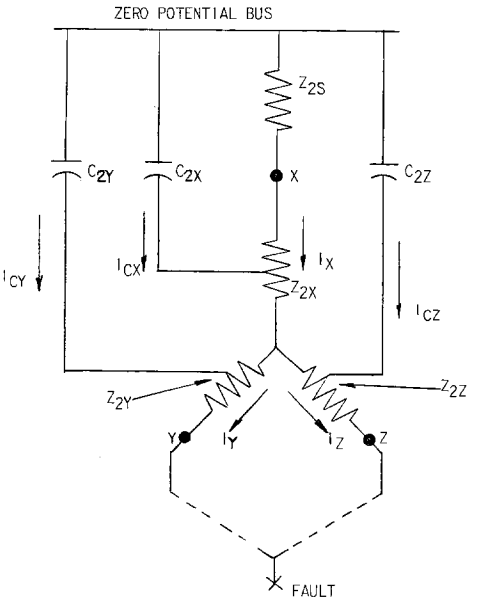
The maximum negative sequence charging current will flow when the maximum negative sequence voltage appears on the line. The maximum negative sequence voltage will appear on the line when a phase-to-phase fault exists at or near one of the terminals. This voltage will be one-half the system normal phase-to-neutral positive sequence voltage. It will appear at the point of the fault, and diminish along the line back toward the zero potential bus. If it is assumed that the system negative sequence impedance, $Z_2S$, is large compared to the line impedance, then the voltage will not diminish very much along the line. On the other hand, if the system impedance is negligible, then the voltage diminishes to zero. Since charginc current will not be a significant factor unless the line is long, a reasonable compromise is to assume that the voltage diminishes to about half of its maximum value. This results in an average negative sequence voltage of three-eights of the normal system phase-to-neutral voltage of the line.

Since the negative sequence distributed capacitance of the line is equal to the positive sequence capacitance, the maximum negative sequence charging current would be three-eights of the normal positive sequence charging current of the line. Thus, a reasonable value for $I_C$ in equations I-1 and I-2 would be 0.375 times the total positive sequence charging current of the line.




$Z_{2L}$= NEGATIVE SEQUENCE IMPEDANCE OF LINE
$Z_{2S}$= NEGATIVE SEQUENCE IMPEDANCE OF SYSTEM
$C_2$ = NEGATIVE SEQUENCE DISTRIBUTED CAPACITANCE OF THE LINE

Figure I-1 (0195A9198-0) Negative Sequence Network, Fault Current Plus Charging Current




$Z_{2X}$, $Z_{2Y}$, $Z_{2Z}$ = NEGATIVE SEQUENCE IMPEDANCE OF THE 3 SECTIONS OF THE LINE
$Z_{2S}$ = NEGATIVE SEQUENCE IMPEDANCE OF SYSTEM
$C_{2X}$, $C_{2Y}$ & $C_{2Z}$ = NEGATIVE SEQUENCE DISTRIBUTED CAPACITANCE OF THE 3 SECTIONS OF THE LINE.

Figure I-2 (0195A9199-0) Negative Sequence Network, Three-Terminal Line

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