GE Industrial Systems

L60 Line Phase Comparison System

UR Series Instruction Manual

L60 Revision: 5.4x

Manual P/N: 1601-0082-**R1** (GEK-113348)

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GE Multilin's Quality Management System is registered to ISO9001:2000

QMI # 005094
UL # A3775

ADDENDUM

This addendum contains information that relates to the L60 Line Phase Comparison System, version 5.4x. This addendum lists a number of information items that appear in the instruction manual GEK-113348 (revision **R1**) but are not included in the current L60 operations.

The following functions/items are not yet available with the current version of the L60 relay:

- N/A

Version 4.0x and higher releases of the L60 relay includes new hardware (CPU and CT/VT modules).

- The new CPU modules are specified with the following order codes: 9E, 9G, 9H, 9J, 9K, 9L, 9M, 9N, 9P, and 9R.
- The new CT/VT modules are specified with the following order codes: 8F, 8H, 8L, 8N 8P.

The following table maps the relationship between the old CPU and CT/VT modules to the newer versions:

MODULE	OLD	NEW	DESCRIPTION
CPU	9A	9E	RS485 and RS485 (Modbus RTU, DNP)
	9C	9G	RS485 and 10Base-F (Ethernet, Modbus TCP/IP, DNP)
	9D	9H	RS485 and redundant 10Base-F (Ethernet, Modbus TCP/IP, DNP)
	--	9J	RS485 and multi-mode ST 100Base-FX
	--	9K	RS485 and multi-mode ST redundant 100Base-FX
	--	9L	RS485 and single mode SC 100Base-FX
	--	9M	RS485 and single mode SC redundant 100Base-FX
	--	9N	RS485 and 10/100Base-T
	--	9P	RS485 and single mode ST 100Base-FX
	--	9R	RS485 and single mode ST redundant 100Base-FX
CT/VT	8A	8F	Standard 4CT/4VT
	8C	8H	Standard 8CT
	--	8L	Standard 4CT/4VT with enhanced diagnostics
	--	8N	Standard 8CT with enhanced diagnostics
	--	8P	Special 4CT module with communications channel for L60

The new CT/VT modules can only be used with the new CPUs (9E, 9G, 9H, 9J, 9K, 9L, 9M, 9N, 9P, 9R), and the old CT/VT modules can only be used with the old CPU modules (9A, 9C, 9D). To prevent any hardware mismatches, the new CPU and CT/VT modules have blue labels and a warning sticker stating **"Attn.: Ensure CPU and DSP module label colors are the same!"**. In the event that there is a mismatch between the CPU and CT/VT module, the relay will not function and a **DSP ERROR** or **HARDWARE MISMATCH** error will be displayed.

All other input/output modules are compatible with the new hardware.

With respect to the firmware, firmware versions 4.0x and higher are only compatible with the new CPU and CT/VT modules. Previous versions of the firmware (3.4x and earlier) are only compatible with the older CPU and CT/VT modules.

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Please read this chapter to help guide you through the initial setup of your new relay.

1.1.1 CAUTIONS AND WARNINGS

WARNING CAUTION

Before attempting to install or use the relay, it is imperative that all WARNINGS and CAUTIONS in this manual are reviewed to help prevent personal injury, equipment damage, and/or downtime.

1.1.2 INSPECTION CHECKLIST

- Open the relay packaging and inspect the unit for physical damage.
- View the rear nameplate and verify that the correct model has been ordered.

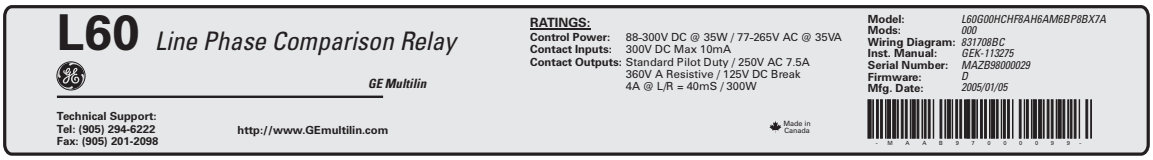

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Figure 1–1: REAR NAMEPLATE (EXAMPLE)

- Ensure that the following items are included:
  - Instruction manual
  - GE EnerVista CD (includes the EnerVista UR Setup software and manuals in PDF format)
  - mounting screws
  - registration card (attached as the last page of the manual)
- Fill out the registration form and return to GE Multilin (include the serial number located on the rear nameplate).
- For product information, instruction manual updates, and the latest software updates, please visit the GE Multilin website at http://www.GEmultilin.com.

NOTE **If there is any noticeable physical damage, or any of the contents listed are missing, please contact GE Multilin immediately.**

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1.2.1 INTRODUCTION TO THE UR

Historically, substation protection, control, and metering functions were performed with electromechanical equipment. This first generation of equipment was gradually replaced by analog electronic equipment, most of which emulated the single-function approach of their electromechanical precursors. Both of these technologies required expensive cabling and auxiliary equipment to produce functioning systems.

Recently, digital electronic equipment has begun to provide protection, control, and metering functions. Initially, this equipment was either single function or had very limited multi-function capability, and did not significantly reduce the cabling and auxiliary equipment required. However, recent digital relays have become quite multi-functional, reducing cabling and auxiliaries significantly. These devices also transfer data to central control facilities and Human Machine Interfaces using electronic communications. The functions performed by these products have become so broad that many users now prefer the term IED (Intelligent Electronic Device).

It is obvious to station designers that the amount of cabling and auxiliary equipment installed in stations can be even further reduced, to 20% to 70% of the levels common in 1990, to achieve large cost reductions. This requires placing even more functions within the IEDs.

Users of power equipment are also interested in reducing cost by improving power quality and personnel productivity, and as always, in increasing system reliability and efficiency. These objectives are realized through software which is used to perform functions at both the station and supervisory levels. The use of these systems is growing rapidly.

High speed communications are required to meet the data transfer rates required by modern automatic control and monitoring systems. In the near future, very high speed communications will be required to perform protection signaling with a performance target response time for a command signal between two IEDs, from transmission to reception, of less than 3 milliseconds. This has been established by the IEC 61850 standard.

IEDs with the capabilities outlined above will also provide significantly more power system data than is presently available, enhance operations and maintenance, and permit the use of adaptive system configuration for protection and control systems. This new generation of equipment must also be easily incorporated into automation systems, at both the station and enterprise levels. The GE Multilin Universal Relay (UR) has been developed to meet these goals.

a) UR BASIC DESIGN

The UR is a digital-based device containing a central processing unit (CPU) that handles multiple types of input and output signals. The UR can communicate over a local area network (LAN) with an operator interface, a programming device, or another UR device.

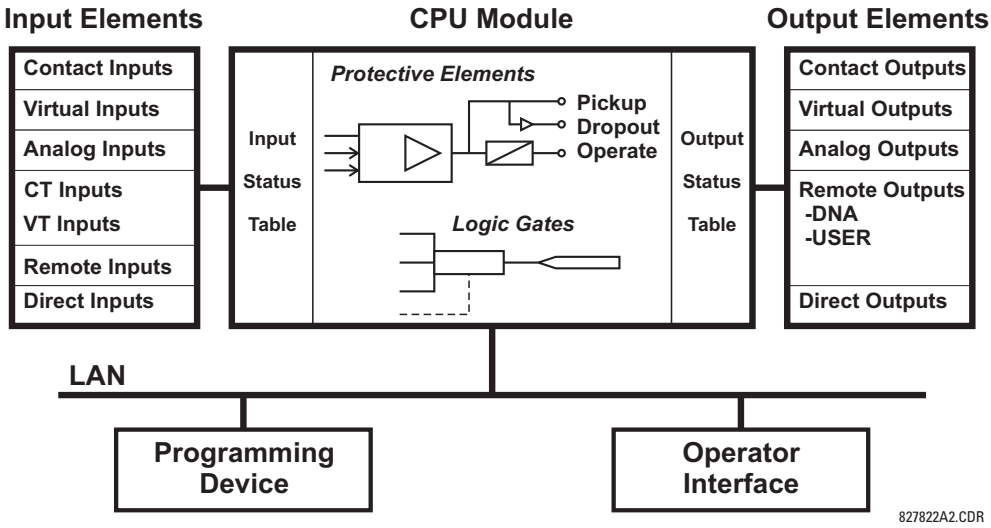


Figure 1–2: UR CONCEPT BLOCK DIAGRAM

The **CPU module** contains firmware that provides protection elements in the form of logic algorithms, as well as programmable logic gates, timers, and latches for control features.

Input elements accept a variety of analog or digital signals from the field. The UR isolates and converts these signals into logic signals used by the relay.

Output elements convert and isolate the logic signals generated by the relay into digital or analog signals that can be used to control field devices.

b) UR SIGNAL TYPES

The **contact inputs and outputs** are digital signals associated with connections to hard-wired contacts. Both 'wet' and 'dry' contacts are supported.

The **virtual inputs and outputs** are digital signals associated with UR-series internal logic signals. Virtual inputs include signals generated by the local user interface. The virtual outputs are outputs of FlexLogic™ equations used to customize the device. Virtual outputs can also serve as virtual inputs to FlexLogic™ equations.

The **analog inputs and outputs** are signals that are associated with transducers, such as Resistance Temperature Detectors (RTDs).

The **CT and VT inputs** refer to analog current transformer and voltage transformer signals used to monitor AC power lines. The UR-series relays support 1 A and 5 A CTs.

The **remote inputs and outputs** provide a means of sharing digital point state information between remote UR-series devices. The remote outputs interface to the remote inputs of other UR-series devices. Remote outputs are FlexLogic™ operands inserted into IEC 61850 GSSE and GOOSE messages.

The **direct inputs and outputs** provide a means of sharing digital point states between a number of UR-series IEDs over a dedicated fiber (single or multimode), RS422, or G.703 interface. No switching equipment is required as the IEDs are connected directly in a ring or redundant (dual) ring configuration. This feature is optimized for speed and intended for pilot-aided schemes, distributed logic applications, or the extension of the input/output capabilities of a single relay chassis.

1

c) UR SCAN OPERATION

The UR-series devices operate in a cyclic scan fashion. The device reads the inputs into an input status table, solves the logic program (FlexLogic™ equation), and then sets each output to the appropriate state in an output status table. Any resulting task execution is priority interrupt-driven.

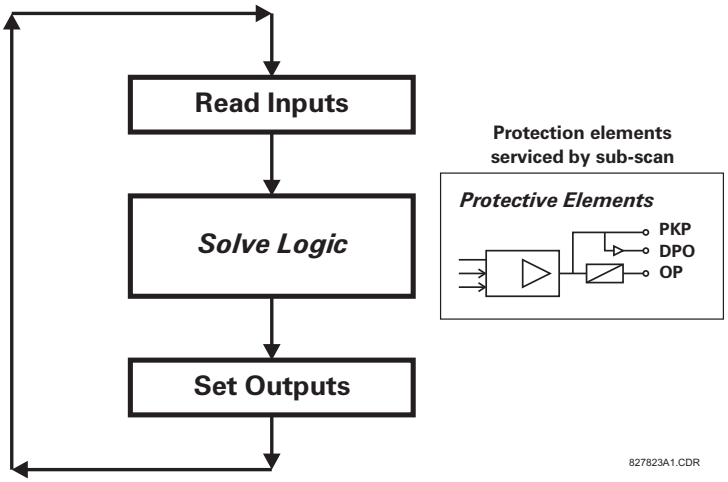


Figure 1–3: UR-SERIES SCAN OPERATION

1.2.3 SOFTWARE ARCHITECTURE

The firmware (software embedded in the relay) is designed in functional modules which can be installed in any relay as required. This is achieved with Object-Oriented Design and Programming (OOD/OOP) techniques.

Object-Oriented techniques involve the use of ‘objects’ and ‘classes’. An ‘object’ is defined as “a logical entity that contains both data and code that manipulates that data”. A ‘class’ is the generalized form of similar objects. By using this concept, one can create a Protection Class with the Protection Elements as objects of the class such as Time Overcurrent, Instantaneous Overcurrent, Current Differential, Undervoltage, Overvoltage, Underfrequency, and Distance. These objects represent completely self-contained software modules. The same object-class concept can be used for Metering, Input/Output Control, HMI, Communications, or any functional entity in the system.

Employing OOD/OOP in the software architecture of the Universal Relay achieves the same features as the hardware architecture: modularity, scalability, and flexibility. The application software for any Universal Relay (e.g. Feeder Protection, Transformer Protection, Distance Protection) is constructed by combining objects from the various functionality classes. This results in a ’common look and feel’ across the entire family of UR-series platform-based applications.

1.2.4 IMPORTANT CONCEPTS

As described above, the architecture of the UR-series relays differ from previous devices. To achieve a general understanding of this device, some sections of Chapter 5 are quite helpful. The most important functions of the relay are contained in “elements”. A description of the UR-series elements can be found in the *Introduction to Elements* section in Chapter 5. An example of a simple element, and some of the organization of this manual, can be found in the *Digital Elements* section. An explanation of the use of inputs from CTs and VTs is in the *Introduction to AC Sources* section in Chapter 5. A description of how digital signals are used and routed within the relay is contained in the *Introduction to FlexLogic*™ section in Chapter 5.

1.3.1 PC REQUIREMENTS

The faceplate keypad and display or the EnerVista UR Setup software interface can be used to communicate with the relay. The EnerVista UR Setup software interface is the preferred method to edit settings and view actual values because the PC monitor can display more information in a simple comprehensible format.

The following minimum requirements must be met for the EnerVista UR Setup software to properly operate on a PC.

- Pentium class or higher processor (Pentium II 300 MHz or higher recommended)
- Windows 95, 98, 98SE, ME, NT 4.0 (Service Pack 4 or higher), 2000, XP
- Internet Explorer 4.0 or higher
- 128 MB of RAM (256 MB recommended)
- 200 MB of available space on system drive and 200 MB of available space on installation drive
- Video capable of displaying 800 x 600 or higher in high-color mode (16-bit color)
- RS232 and/or Ethernet port for communications to the relay

The following qualified modems have been tested to be compliant with the L60 and the EnerVista UR Setup software.

- US Robotics external 56K FaxModem 5686
- US Robotics external Sportster 56K X2
- PCTEL 2304WT V.92 MDC internal modem

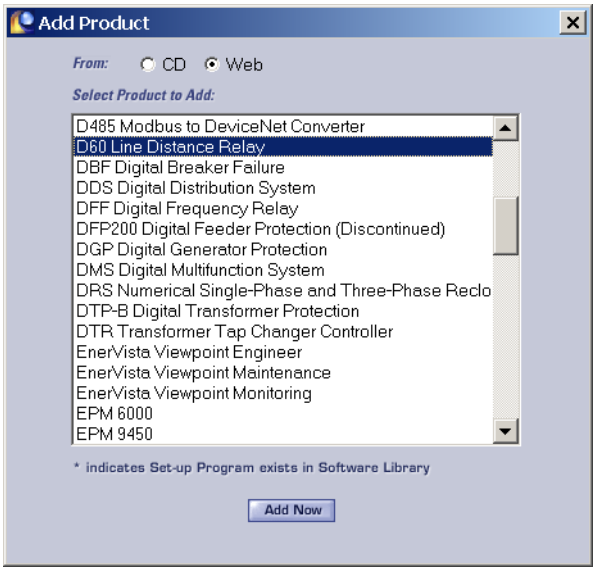
1.3.2 INSTALLATION

After ensuring the minimum requirements for using EnerVista UR Setup are met (see previous section), use the following procedure to install the EnerVista UR Setup from the enclosed GE EnerVista CD.

1. Insert the GE EnerVista CD into your CD-ROM drive.
2. Click the **Install Now** button and follow the installation instructions to install the no-charge EnerVista software.
3. When installation is complete, start the EnerVista Launchpad application.
4. Click the **IED Setup** section of the **Launch Pad** window.

5. In the EnerVista Launch Pad window, click the **Add Product** button and select the “L60 Line Phase Comparison System” from the Install Software window as shown below. Select the “Web” option to ensure the most recent software

release, or select “CD” if you do not have a web connection, then click the **Add Now** button to list software items for the L60.



6. EnerVista Launchpad will obtain the software from the Web or CD and automatically start the installation program.
7. Select the complete path, including the new directory name, where the EnerVista UR Setup will be installed.
8. Click on **Next** to begin the installation. The files will be installed in the directory indicated and the installation program will automatically create icons and add EnerVista UR Setup to the Windows start menu.
9. Click **Finish** to end the installation. The UR-series device will be added to the list of installed IEDs in the EnerVista Launchpad window, as shown below.

1.3.3 CONFIGURING THE L60 FOR SOFTWARE ACCESS

a) OVERVIEW

The user can connect remotely to the L60 through the rear RS485 port or the rear Ethernet port with a PC running the EnerVista UR Setup software. The L60 can also be accessed locally with a laptop computer through the front panel RS232 port or the rear Ethernet port using the *Quick Connect* feature.

- To configure the L60 for remote access via the rear RS485 port(s), refer to the *Configuring Serial Communications* section.
- To configure the L60 for remote access via the rear Ethernet port, refer to the *Configuring Ethernet Communications* section. An Ethernet module must be specified at the time of ordering.
- To configure the L60 for local access with a laptop through either the front RS232 port or rear Ethernet port, refer to the *Using the Quick Connect Feature* section. An Ethernet module must be specified at the time of ordering for Ethernet communications.

b) CONFIGURING SERIAL COMMUNICATIONS

Before starting, verify that the serial cable is properly connected to the RS485 terminals on the back of the device. The faceplate RS232 port is intended for local use and is not described in this section; see the *Using the Quick Connect Feature* section for details on configuring the RS232 port.

A GE Multilin F485 converter (or compatible RS232-to-RS485 converter) is will be required. Refer to the F485 instruction manual for additional details.

1. Verify that the latest version of the EnerVista UR Setup software is installed (available from the GE EnerVista CD or online from http://www.GEmultilin.com). See the *Software Installation* section for installation details.
2. Select the "UR" device from the EnerVista Launchpad to start EnerVista UR Setup.
3. Click the **Device Setup** button to open the Device Setup window and click the **Add Site** button to define a new site.
4. Enter the desired site name in the "Site Name" field. If desired, a short description of site can also be entered along with the display order of devices defined for the site. In this example, we will use "Location 1" as the site name. Click the **OK** button when complete.
5. The new site will appear in the upper-left list in the EnerVista UR Setup window. Click the **Device Setup** button then select the new site to re-open the Device Setup window.
6. Click the **Add Device** button to define the new device.
7. Enter the desired name in the "Device Name" field and a description (optional) of the site.
8. Select "Serial" from the **Interface** drop-down list. This will display a number of interface parameters that must be entered for proper serial communications.

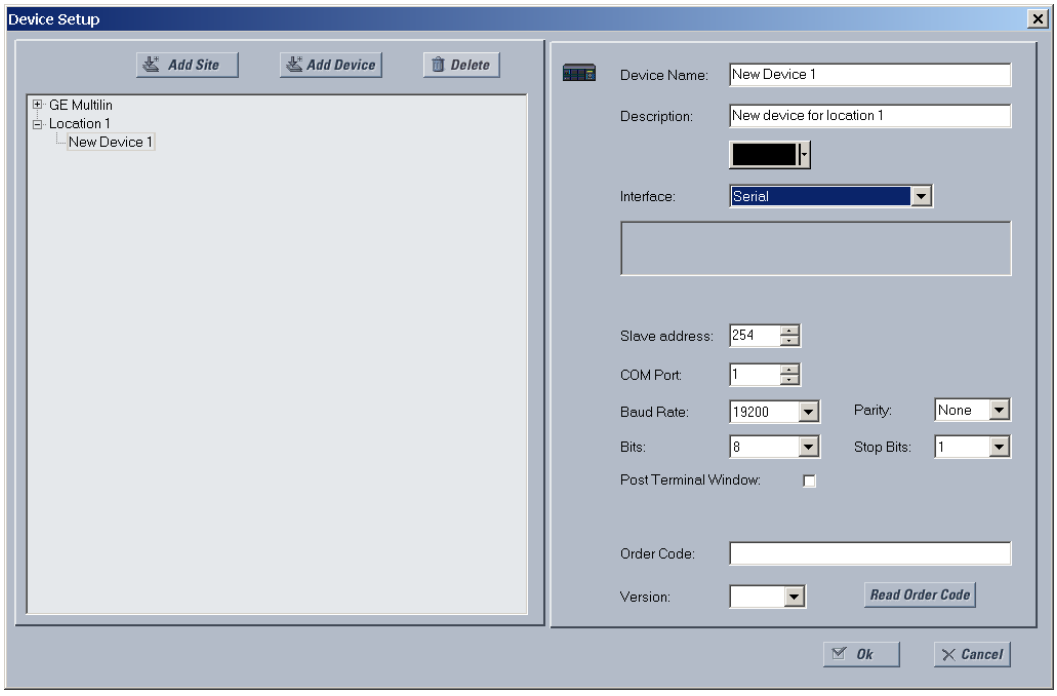


Figure 1–4: CONFIGURING SERIAL COMMUNICATIONS

9. Enter the relay slave address, COM port, baud rate, and parity settings from the SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ SERIAL PORTS menu in their respective fields.
10. Click the **Read Order Code** button to connect to the L60 device and upload the order code. If an communications error occurs, ensure that the EnerVista UR Setup serial communications values entered in the previous step correspond to the relay setting values.
11. Click "OK" when the relay order code has been received. The new device will be added to the Site List window (or Online window) located in the top left corner of the main EnerVista UR Setup window.

The Site Device has now been configured for RS232 communications. Proceed to the *Connecting to the L60* section to begin communications.

c) CONFIGURING ETHERNET COMMUNICATIONS

Before starting, verify that the Ethernet network cable is properly connected to the Ethernet port on the back of the relay. To setup the relay for Ethernet communications, it will be necessary to define a Site, then add the relay as a Device at that site.

1. Verify that the latest version of the EnerVista UR Setup software is installed (available from the GE EnerVista CD or online from http://www.GEmultilin.com). See the *Software Installation* section for installation details.
2. Select the "UR" device from the EnerVista Launchpad to start EnerVista UR Setup.
3. Click the **Device Setup** button to open the Device Setup window, then click the **Add Site** button to define a new site.
4. Enter the desired site name in the "Site Name" field. If desired, a short description of site can also be entered along with the display order of devices defined for the site. In this example, we will use "Location 2" as the site name. Click the **OK** button when complete.
5. The new site will appear in the upper-left list in the EnerVista UR Setup window. Click the **Device Setup** button then select the new site to re-open the Device Setup window.
6. Click the **Add Device** button to define the new device.
7. Enter the desired name in the "Device Name" field and a description (optional) of the site.
8. Select "Ethernet" from the **Interface** drop-down list. This will display a number of interface parameters that must be entered for proper Ethernet functionality.

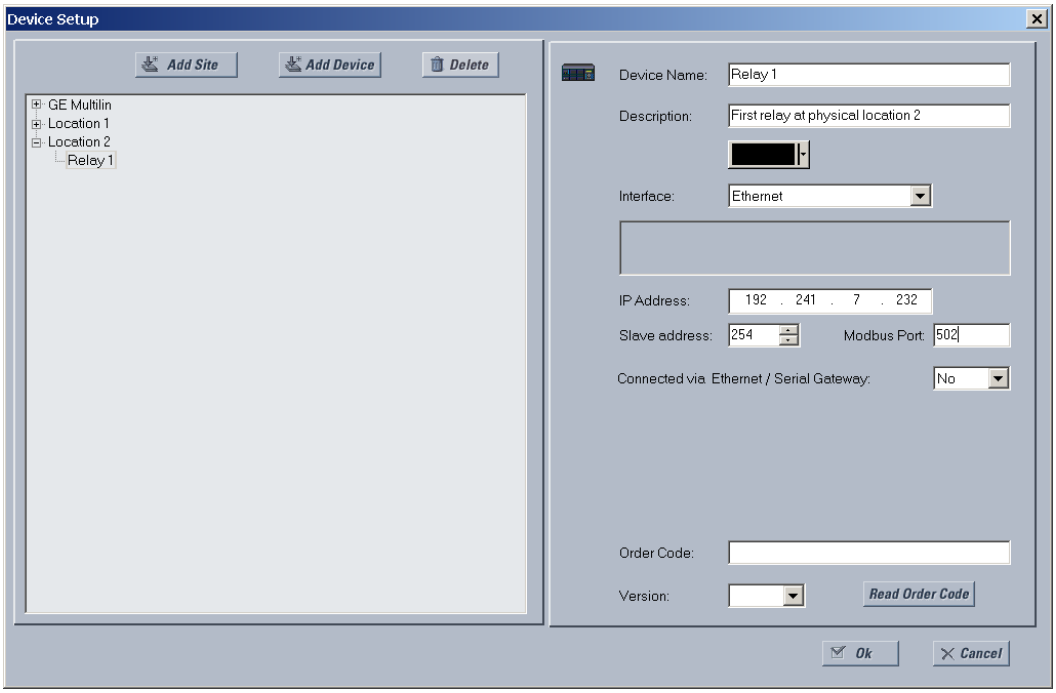


Figure 1–5: CONFIGURING ETHERNET COMMUNICATIONS

9. Enter the relay IP address specified in the **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ NETWORK ⇨ IP ADDRESS**) in the "IP Address" field.
10. Enter the relay slave address and Modbus port address values from the respective settings in the **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ MODBUS PROTOCOL** menu.
11. Click the **Read Order Code** button to connect to the L60 device and upload the order code. If an communications error occurs, ensure that the three EnerVista UR Setup values entered in the previous steps correspond to the relay setting values.
12. Click **OK** when the relay order code has been received. The new device will be added to the Site List window (or Online window) located in the top left corner of the main EnerVista UR Setup window.

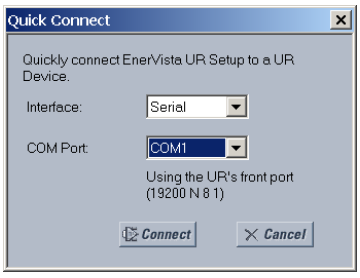
The Site Device has now been configured for Ethernet communications. Proceed to the *Connecting to the L60* section to begin communications.

1.3.4 USING THE QUICK CONNECT FEATURE

a) USING QUICK CONNECT VIA THE FRONT PANEL RS232 PORT

Before starting, verify that the serial cable is properly connected from the laptop computer to the front panel RS232 port with a straight-through 9-pin to 9-pin RS232 cable.

1. Verify that the latest version of the EnerVista UR Setup software is installed (available from the GE EnerVista CD or online from http://www.GEmultilin.com). See the *Software Installation* section for installation details.
2. Select the "UR" device from the EnerVista Launchpad to start EnerVista UR Setup.
3. Click the **Quick Connect** button to open the Quick Connect dialog box.



4. Select the **Serial** interface and the correct COM Port, then click **Connect**.
5. The EnerVista UR Setup software will create a site named "Quick Connect" with a corresponding device also named "Quick Connect" and display them on the upper-left corner of the screen. Expand the sections to view data directly from the L60 device.

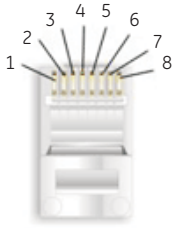
Each time the EnerVista UR Setup software is initialized, click the **Quick Connect** button to establish direct communications to the L60. This ensures that configuration of the EnerVista UR Setup software matches the L60 model number.

b) USING QUICK CONNECT VIA THE REAR ETHERNET PORTS

To use the Quick Connect feature to access the L60 from a laptop through Ethernet, first assign an IP address to the relay from the front panel keyboard.

1. Press the MENU key until the SETTINGS menu is displayed.
2. Navigate to the **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ NETWORK ⇨ IP ADDRESS** setting.
3. Enter an IP address of "1.1.1.1" and select the ENTER key to save the value.
4. In the same menu, select the **SUBNET IP MASK** setting.
5. Enter a subnet IP address of "255.0.0.0" and press the ENTER key to save the value.

Next, use an Ethernet cross-over cable to connect the laptop to the rear Ethernet port. The pinout for an Ethernet cross-over cable is shown below.



END 1		
Pin	Wire color	Diagram
1	White/orange	
2	Orange	
3	White/green	
4	Blue	
5	White/blue	
6	Green	
7	White/brown	
8	Brown	

END 2		
Pin	Wire color	Diagram
1	White/green	
2	Green	
3	White/orange	
4	Blue	
5	White/blue	
6	Orange	
7	White/brown	
8	Brown	

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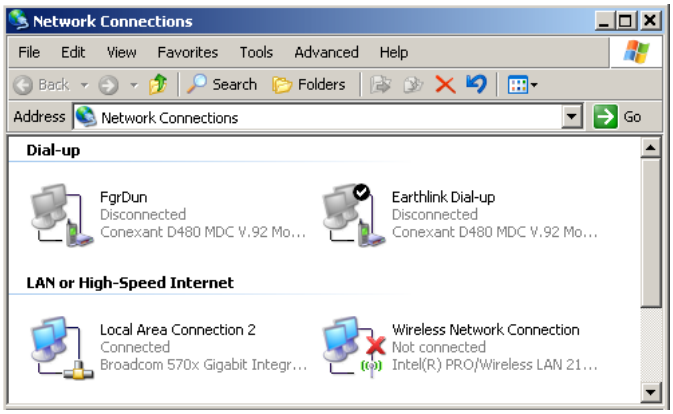
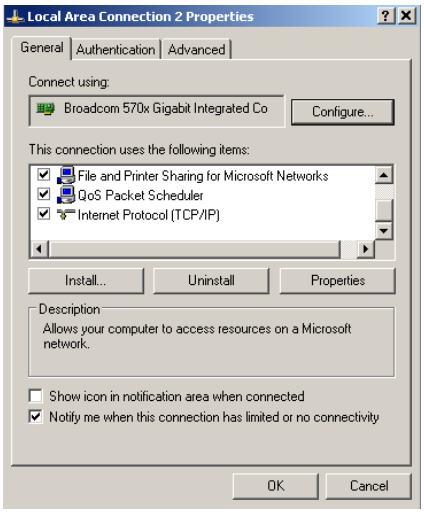
Figure 1–6: ETHERNET CROSS-OVER CABLE PIN LAYOUT

Now, assign the laptop computer an IP address compatible with the relay's IP address.

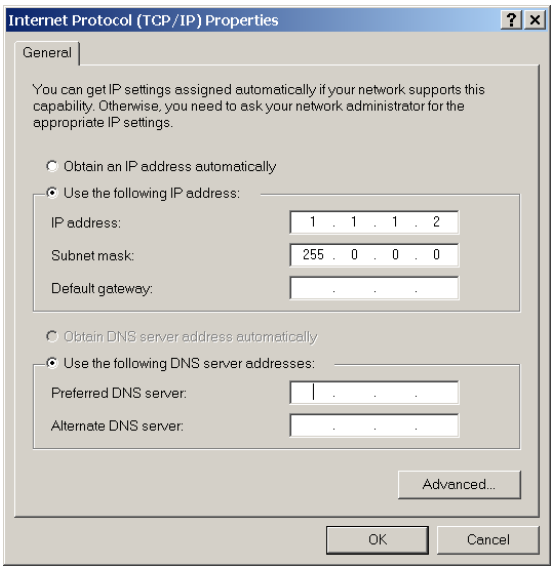
1. From the Windows desktop, right-click the **My Network Places** icon and select **Properties** to open the network connections window.



2. Right-click the **Local Area Connection** icon and select **Properties**.



3. Select the **Internet Protocol (TCP/IP)** item from the list provided and click the **Properties** button.



4. Click on the “Use the following IP address” box.
5. Enter an **IP address** with the first three numbers the same as the IP address of the L60 relay and the last number different (in this example, 1.1.1.2).
6. Enter a subnet mask equal to the one set in the L60 (in this example, 255.0.0.0).
7. Click OK to save the values.

Before continuing, it will be necessary to test the Ethernet connection.

1. Open a Windows console window by selecting **Start > Run** from the Windows Start menu and typing “cmd”.
2. Type the following command:

```
C:\WINNT>ping 1.1.1.1
```

3. If the connection is successful, the system will return four replies as follows:

```
Pinging 1.1.1.1 with 32 bytes of data:

Reply from 1.1.1.1: bytes=32 time<10ms TTL=255
Reply from 1.1.1.1: bytes=32 time<10ms TTL=255
Reply from 1.1.1.1: bytes=32 time<10ms TTL=255
Reply from 1.1.1.1: bytes=32 time<10ms TTL=255

Ping statistics for 1.1.1.1:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip time in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0 ms
```

4. Note that the values for `time` and `TTL` will vary depending on local network configuration.

If the following sequence of messages appears when entering the `C:\WINNT>ping 1.1.1.1` command:

```
Pinging 1.1.1.1 with 32 bytes of data:

Request timed out.
Request timed out.
Request timed out.
Request timed out.

Ping statistics for 1.1.1.1:
    Packets: Sent = 4, Received = 0, Lost = 4 (100% loss),
Approximate round trip time in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0 ms

Pinging 1.1.1.1 with 32 bytes of data:
```

Verify the physical connection between the L60 and the laptop computer, and double-check the programmed IP address in the **PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ NETWORK ⇨ IP ADDRESS** setting, then repeat step 2 in the above procedure.

If the following sequence of messages appears when entering the `C:\WINNT>ping 1.1.1.1` command:

```
Pinging 1.1.1.1 with 32 bytes of data:

Hardware error.
Hardware error.
Hardware error.
Hardware error.

Ping statistics for 1.1.1.1:
    Packets: Sent = 4, Received = 0, Lost = 4 (100% loss),
Approximate round trip time in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0 ms

Pinging 1.1.1.1 with 32 bytes of data:
```

Verify the physical connection between the L60 and the laptop computer, and double-check the programmed IP address in the **PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ NETWORK ⇨ IP ADDRESS** setting, then repeat step 2 in the above procedure.

If the following sequence of messages appears when entering the `C:\WINNT>ping 1.1.1.1` command:

```
Pinging 1.1.1.1 with 32 bytes of data:

Destination host unreachable.
Destination host unreachable.
Destination host unreachable.
Destination host unreachable.

Ping statistics for 1.1.1.1:
    Packets: Sent = 4, Received = 0, Lost = 4 (100% loss),
Approximate round trip time in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0 ms

Pinging 1.1.1.1 with 32 bytes of data:
```

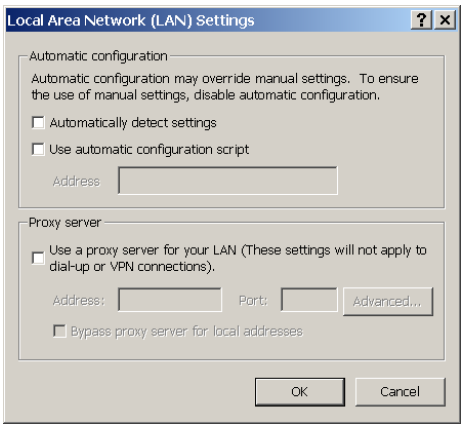
Verify the IP address is programmed in the local PC by entering the ipconfig command in the command window.

```
C:\WINNT>ipconfig

Windows 2000 IP Configuration

Ethernet adapter <F4FE223E-5EB6-4BFB-9E34-1BD7BE7F59FF>:

        Connection-specific DNS suffix. . :
        IP Address. . . . . . . . . . . . : 0.0.0.0
        Subnet Mask . . . . . . . . . . . : 0.0.0.0
        Default Gateway . . . . . . . . . :

Ethernet adapter Local Area Connection:

        Connection-specific DNS suffix  . :
        IP Address. . . . . . . . . . . . : 1.1.1.2
        Subnet Mask . . . . . . . . . . . : 255.0.0.0
        Default Gateway . . . . . . . . . :

C:\WINNT>
```

It may be necessary to restart the laptop for the change in IP address to take effect (Windows 98 or NT).

Before using the Quick Connect feature through the Ethernet port, it is necessary to disable any configured proxy settings in Internet Explorer.

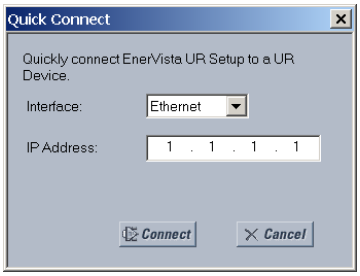
1. Start the Internet Explorer software.
2. Select the **Tools > Internet Options** menu item and click on **Connections** tab.
3. Click on the **LAN Settings** button to open the following window.



4. Ensure that the “Use a proxy server for your LAN” box is not checked.

If this computer is used to connect to the Internet, re-enable any proxy server settings after the laptop has been disconnected from the L60 relay.

1. Verify that the latest version of the EnerVista UR Setup software is installed (available from the GE enerVista CD or online from http://www.GEmultilin.com). See the *Software Installation* section for installation details.
2. Start the Internet Explorer software.
3. Select the “UR” device from the EnerVista Launchpad to start EnerVista UR Setup.
4. Click the **Quick Connect** button to open the Quick Connect dialog box.



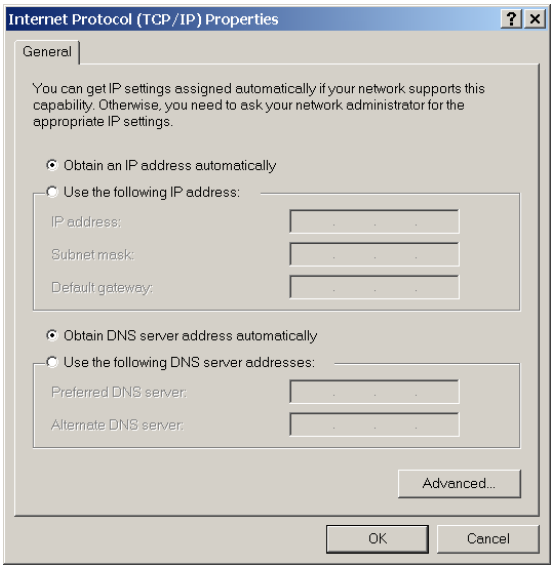
5. Select the **Ethernet** interface and enter the IP address assigned to the L60, then click **Connect**.
6. The EnerVista UR Setup software will create a site named “Quick Connect” with a corresponding device also named “Quick Connect” and display them on the upper-left corner of the screen. Expand the sections to view data directly from the L60 device.

Each time the EnerVista UR Setup software is initialized, click the **Quick Connect** button to establish direct communications to the L60. This ensures that configuration of the EnerVista UR Setup software matches the L60 model number.

When direct communications with the L60 via Ethernet is complete, make the following changes:

1. From the Windows desktop, right-click the **My Network Places** icon and select **Properties** to open the network connections window.
2. Right-click the **Local Area Connection** icon and select the **Properties** item.
3. Select the **Internet Protocol (TCP/IP)** item from the list provided and click the **Properties** button.

4. Set the computer to “Obtain a relay address automatically” as shown below.



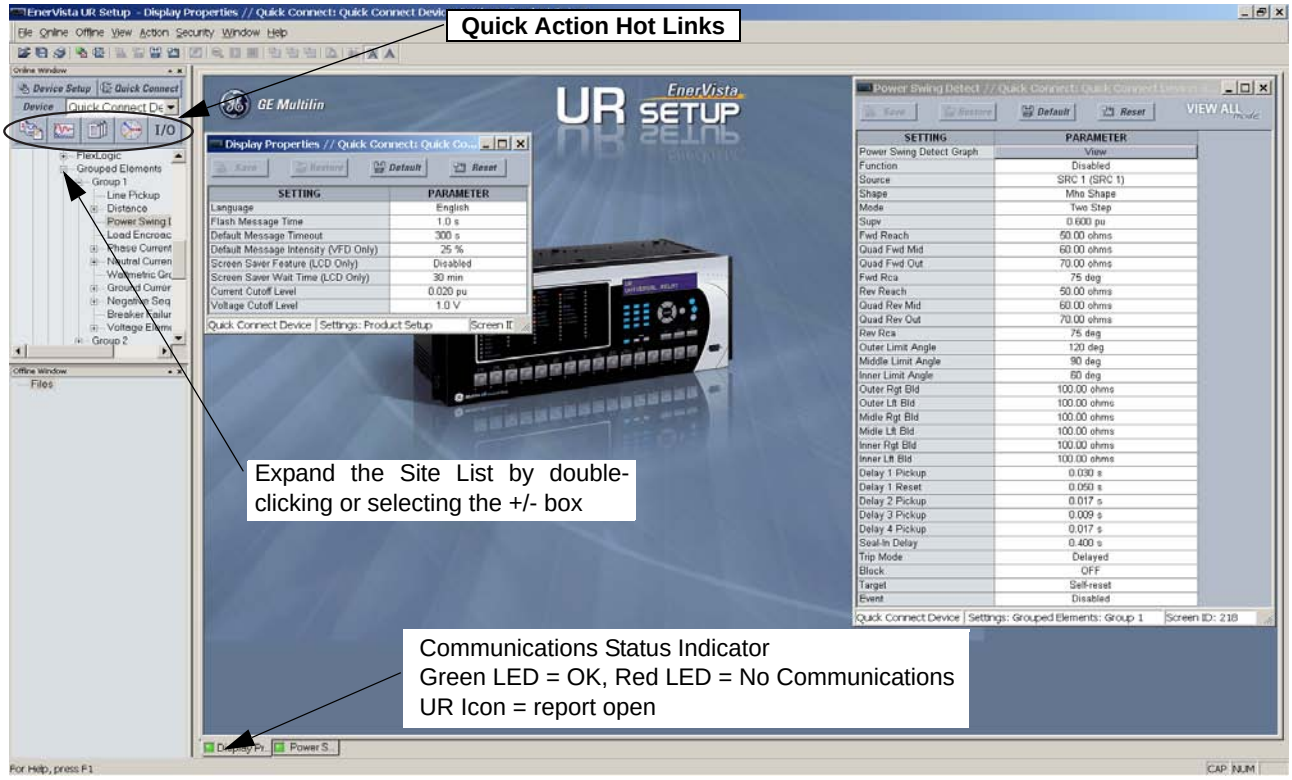
If this computer is used to connect to the Internet, re-enable any proxy server settings after the laptop has been disconnected from the L60 relay.

AUTOMATIC DISCOVERY OF ETHERNET DEVICES

The UR Setup Software now has the ability to automatically discover and communicate to all of the URs that are located on an Ethernet Network.

Using the Quick Connect Feature, a single click of the mouse will trigger the software to automatically detect any UR relays located on the Ethernet network. The Setup Software will then proceed to configure all settings and order code options in the Device Setup menu, for the purpose of communicating to multiple relays. Using this feature will allow you to identify and interrogate in seconds, all UR devices found in a particular location.

1. Open the Display Properties window through the Site List tree as shown below:



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2. The Display Properties window will open with a status indicator on the lower left of the EnerVista UR Setup window.
3. If the status indicator is red, verify that the Ethernet network cable is properly connected to the Ethernet port on the back of the relay and that the relay has been properly setup for communications (steps A and B earlier).

   If a relay icon appears in place of the status indicator, than a report (such as an oscillography or event record) is open. Close the report to re-display the green status indicator.
4. The Display Properties settings can now be edited, printed, or changed according to user specifications.

NOTE **Refer to Chapter 4 in this manual and the EnerVista UR Setup Help File for more information about the using the EnerVista UR Setup software interface.**

QUICK ACTION HOT LINKS

The UR Setup Software has several new Quick Action buttons that provide users with instant access to several functions that are often performed when using UR relays. In the Online Window, users can select which relay they wish to interrogate from a pull-down window, then click on the button for the action they wish to perform. The Quick Action functions available are:

- View device's Event Record
- View device's last recorded Oscillography Record
- View status of all device Inputs and Outputs
- View all of the device Metering values
- View the device's Protection Summary

1.4.1 MOUNTING AND WIRING

Please refer to Chapter 3: Hardware for detailed mounting and wiring instructions. Review all **WARNINGS** and **CAUTIONS** carefully.

1.4.2 COMMUNICATIONS

The EnerVista UR Setup software communicates to the relay via the faceplate RS232 port or the rear panel RS485 / Ethernet ports. To communicate via the faceplate RS232 port, a standard "straight-through" serial cable is used. The DB-9 male end is connected to the relay and the DB-9 or DB-25 female end is connected to the PC COM1 or COM2 port as described in the *CPU Communications Ports* section of Chapter 3.

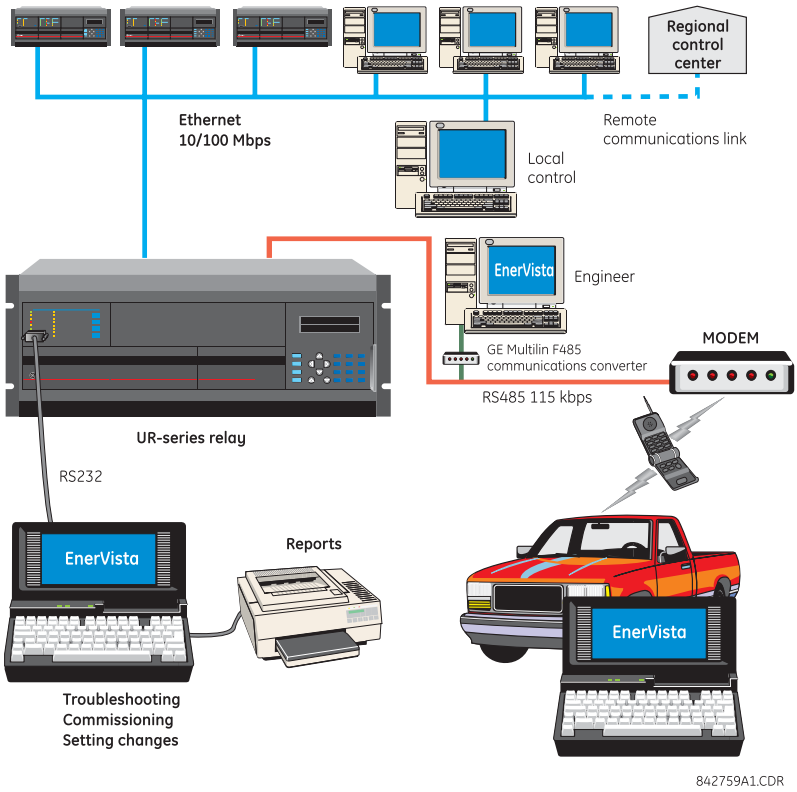


Figure 1–7: RELAY COMMUNICATIONS OPTIONS

To communicate through the L60 rear RS485 port from a PC RS232 port, the GE Multilin RS232/RS485 converter box is required. This device (catalog number F485) connects to the computer using a "straight-through" serial cable. A shielded twisted-pair (20, 22, or 24 AWG) connects the F485 converter to the L60 rear communications port. The converter terminals (+, –, GND) are connected to the L60 communication module (+, –, COM) terminals. Refer to the *CPU Communications Ports* section in chapter 3 for option details. The line should be terminated with an R-C network (i.e. 120 Ω, 1 nF) as described in the chapter 3.

1.4.3 FACEPLATE DISPLAY

All messages are displayed on a 2 × 20 backlit liquid crystal display (LCD) to make them visible under poor lighting conditions. Messages are descriptive and should not require the aid of an instruction manual for deciphering. While the keypad and display are not actively being used, the display will default to user-defined messages. Any high priority event driven message will automatically override the default message and appear on the display.

1.5.1 FACEPLATE KEYPAD

Display messages are organized into 'pages' under the following headings: Actual Values, Settings, Commands, and Targets. The MENU key navigates through these pages. Each heading page is broken down further into logical subgroups.

The MESSAGE keys navigate through the subgroups. The VALUE keys scroll increment or decrement numerical setting values when in programming mode. These keys also scroll through alphanumeric values in the text edit mode. Alternatively, values may also be entered with the numeric keypad.

The decimal key initiates and advance to the next character in text edit mode or enters a decimal point. The HELP key may be pressed at any time for context sensitive help messages. The ENTER key stores altered setting values.

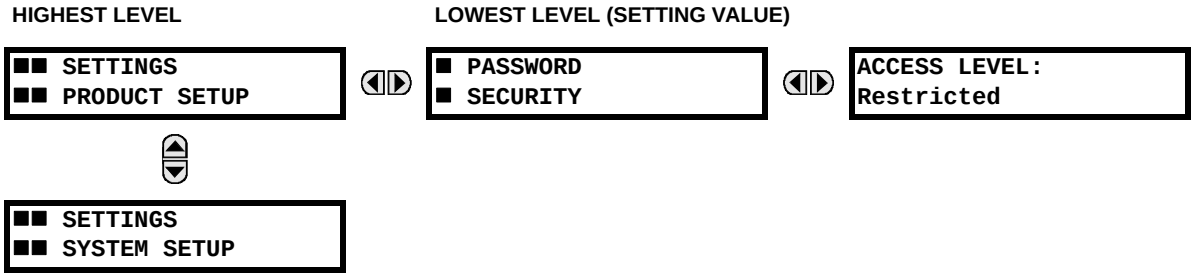
1.5.2 MENU NAVIGATION

Press the MENU key to select the desired header display page (top-level menu). The header title appears momentarily followed by a header display page menu item. Each press of the MENU key advances through the following main heading pages:

- Actual values
- Settings
- Commands
- Targets
- User displays (when enabled)

1.5.3 MENU HIERARCHY

The setting and actual value messages are arranged hierarchically. The header display pages are indicated by double scroll bar characters (■■), while sub-header pages are indicated by single scroll bar characters (■). The header display pages represent the highest level of the hierarchy and the sub-header display pages fall below this level. The MESSAGE UP and DOWN keys move within a group of headers, sub-headers, setting values, or actual values. Continually pressing the MESSAGE RIGHT key from a header display displays specific information for the header category. Conversely, continually pressing the MESSAGE LEFT key from a setting value or actual value display returns to the header display.



1.5.4 RELAY ACTIVATION

The relay is defaulted to the "Not Programmed" state when it leaves the factory. This safeguards against the installation of a relay whose settings have not been entered. When powered up successfully, the Trouble LED will be on and the In Service LED off. The relay in the "Not Programmed" state will block signaling of any output relay. These conditions will remain until the relay is explicitly put in the "Programmed" state.

Select the menu message **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ INSTALLATION ⇨ RELAY SETTINGS**

```
RELAY SETTINGS:
Not Programmed
```

To put the relay in the “Programmed” state, press either of the VALUE keys once and then press ENTER. The faceplate Trouble LED will turn off and the In Service LED will turn on. The settings for the relay can be programmed manually (refer to *Chapter 5*) via the faceplate keypad or remotely (refer to the EnerVista UR Setup help file) via the EnerVista UR Setup software interface.

1.5.5 BATTERY TAB

The battery tab is installed in the power supply module before the L60 shipped from the factory. The battery tab prolongs battery life in the event the relay is powered down for long periods of time before installation. The battery is responsible for backing up event records, oscillography, data logger, and real-time clock information when the relay is powered off. The battery failure self-test error generated by the relay is a minor and should not affect the relay functionality. When the relay is installed and ready for commissioning, the tab should be removed. The battery tab should be re-inserted if the relay is powered off for an extended period of time. If required, contact the factory for a replacement battery or battery tab.

1.5.6 RELAY PASSWORDS

It is recommended that passwords be set up for each security level and assigned to specific personnel. There are two user password security access levels, COMMAND and SETTING:

1. COMMAND

The COMMAND access level restricts the user from making any settings changes, but allows the user to perform the following operations:

- operate breakers via faceplate keypad
- change state of virtual inputs
- clear event records
- clear oscillography records
- operate user-programmable pushbuttons

2. SETTING

The SETTING access level allows the user to make any changes to any of the setting values.

NOTE

Refer to the *Changing Settings* section in Chapter 4 for complete instructions on setting up security level passwords.

1.5.7 FLEXLOGIC™ CUSTOMIZATION

FlexLogic™ equation editing is required for setting up user-defined logic for customizing the relay operations. See the *FlexLogic™* section in Chapter 5 for additional details.

1.5.8 COMMISSIONING

Tables for recording settings before entering them via the keypad are available from the GE Multilin website at http://www.GEmultilin.com.

The L60 requires a minimum amount of maintenance when it is commissioned into service. Since the L60 is a microprocessor-based relay, its characteristics do not change over time. As such, no further functional tests are required.

Furthermore, the L60 performs a number of continual self-tests and takes the necessary action in case of any major errors (see the *Relay Self-Test* section in Chapter 7 for details). However, it is recommended that L60 maintenance be scheduled with other system maintenance. This maintenance may involve the in-service, out-of-service, or unscheduled maintenance.

In-service maintenance:

1. Visual verification of the analog values integrity such as voltage and current (in comparison to other devices on the corresponding system).
2. Visual verification of active alarms, relay display messages, and LED indications.
3. LED test.
4. Visual inspection for any damage, corrosion, dust, or loose wires.
5. Event recorder file download with further events analysis.

Out-of-service maintenance:

1. Check wiring connections for firmness.
2. Analog values (currents, voltages, RTDs, analog inputs) injection test and metering accuracy verification. Calibrated test equipment is required.
3. Protection elements setting verification (analog values injection or visual verification of setting file entries against relay settings schedule).
4. Contact inputs and outputs verification. This test can be conducted by direct change of state forcing or as part of the system functional testing.
5. Visual inspection for any damage, corrosion, or dust.
6. Event recorder file download with further events analysis.
7. LED Test and pushbutton continuity check.

Unscheduled maintenance such as during a disturbance causing system interruption:

1. View the event recorder and oscillography or fault report for correct operation of inputs, outputs, and elements.

If it is concluded that the relay or one of its modules is of concern, contact GE Multilin for prompt service.

2.1.1 OVERVIEW

The L60 Line Phase Comparison System provides a simple phase-comparison principle successfully employed by analog and static relays for many years along with the significant advantages of a modern microprocessor based relay. The phase comparison element performs the following calculations:

- Samples and filters three-phase AC currents at a rate of 64 samples per cycle.
- Computes sequence components of the current.
- If two CT/VT modules are employed for breaker-and-a-half applications, the relay sums up two currents and performs the breaker-and-the-half logic calculations.
- Forms a composite signal from current components according to a user-defined setting.
- Forms local positive and negative squares from the composite signal sent to remote terminal and used locally along with the channel delay value.
- Samples received from remote terminal squares 64 samples per cycle measuring magnitude of the pulse voltage.
- Processes received samples to compensate for asymmetry and distortions in the signal.
- Detects fault condition with the fault detector.
- Compares coincidence of local and remote squares which indicate the presence of internal or external faults.
- Detects transient conditions to block the phase comparison function.

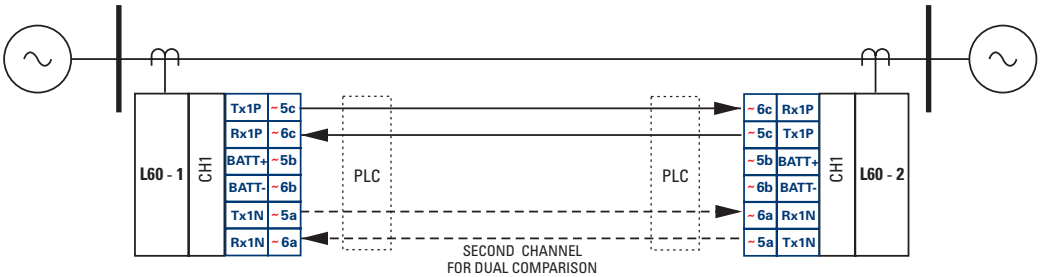
All processed signals, including transmitted and received pulses, are available in oscillography for commissioning, maintenance, and analysis. The L60 integrates received pulses on a sample-per-sample base, similar to the analog phase-comparison principle, making the relay exceptionally robust on noisy channels. All permissive and blocking schemes, as well as single and dual phase comparison, are incorporated into a single protection element and can be selected with a relay setting. The L60 supports two and three-terminal applications, can be used for single- and three-pole tripping applications, and supports breaker-and-a-half applications. Multiple backup functions include three-zone phase and ground distance, directional overcurrent, pilot schemes, and current and voltage elements.

Control features include synchrocheck, autoreclosure, and control for two breakers. Monitoring features include CT failure detector, VT fuse failure detector, breaker arcing current, disturbance detector and continuous monitor.

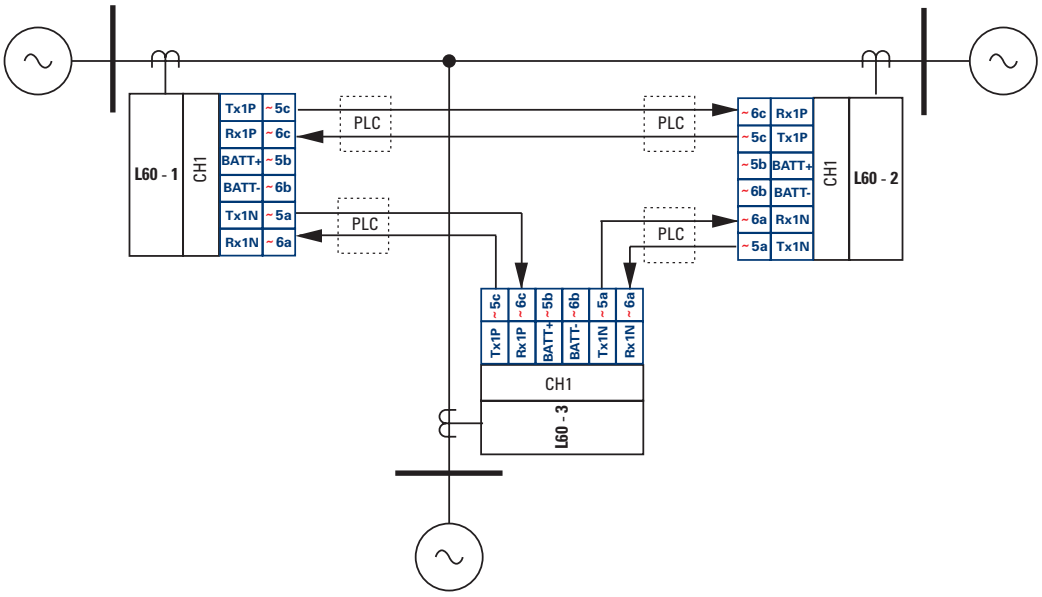
Diagnostic features include an event recorder capable of storing 1024 time-tagged events, oscillography capable of storing up to 64 records with programmable trigger, content and sampling rate, and data logger acquisition of up to 16 channels, with programmable content and sampling rate. The internal clock used for time-tagging can be synchronized with an IRIG-B signal or via the SNTP protocol over the Ethernet port. This precise time stamping allows the sequence of events to be determined throughout the system. Events can also be programmed (via FlexLogic™ equations) to trigger oscillography data capture which may be set to record the measured parameters before and after the event for viewing on a personal computer (PC). These tools significantly reduce troubleshooting time and simplify report generation in the event of a system fault.

A faceplate RS232 port may be used to connect to a PC for the programming of settings and the monitoring of actual values. A variety of communications modules are available. Two rear RS485 ports allow independent access by operating and engineering staff. All serial ports use the Modbus® RTU protocol. The RS485 ports may be connected to system computers with baud rates up to 115.2 kbps. The RS232 port has a fixed baud rate of 19.2 kbps. Optional communications modules include a 10Base-F Ethernet interface which can be used to provide fast, reliable communications in noisy environments. Another option provides two 10Base-F fiber optic ports for redundancy. The Ethernet port supports IEC 61850, Modbus®/TCP, and TFTP protocols, and allows access to the relay via any standard web browser (L60 web pages). The IEC 60870-5-104 protocol is supported on the Ethernet port. DNP 3.0 and IEC 60870-5-104 cannot be enabled at the same time.

Typical two and three-terminal applications are shown below.



TYPICAL 2-TERMINAL APPLICATION



TYPICAL 3-TERMINAL APPLICATION

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Figure 2–1: 87PC COMMUNICATIONS

The L60 IEDs use flash memory technology which allows field upgrading as new features are added. The following single line diagram illustrates the relay functionality using ANSI (American National Standards Institute) device numbers.

Table 2–1: ANSI DEVICE NUMBERS AND FUNCTIONS

DEVICE NUMBER	FUNCTION
21G	Ground distance
21P	Phase distance
25	Synchrocheck
27P	Phase undervoltage
27X	Auxiliary undervoltage
32N	Wattmetric zero-sequence directional
50BF	Breaker failure
50DD	Disturbance detector
50G	Ground instantaneous overcurrent
50N	Neutral instantaneous overcurrent
50P	Phase instantaneous overcurrent
50_2	Negative-sequence instantaneous overcurrent
51G	Ground time overcurrent
51N	Neutral time overcurrent

DEVICE NUMBER	FUNCTION
51P	Phase time overcurrent
51_2	Negative-sequence time overcurrent
52	AC circuit breaker
59N	Neutral overvoltage
59P	Phase overvoltage
59X	Auxiliary overvoltage
59_2	Negative-sequence overvoltage
67N	Neutral directional overcurrent
67P	Phase directional overcurrent
67_2	Negative-sequence directional overcurrent
68	Power swing blocking
78	Out-of-step tripping
79	Automatic recloser
87PC	Phase comparison

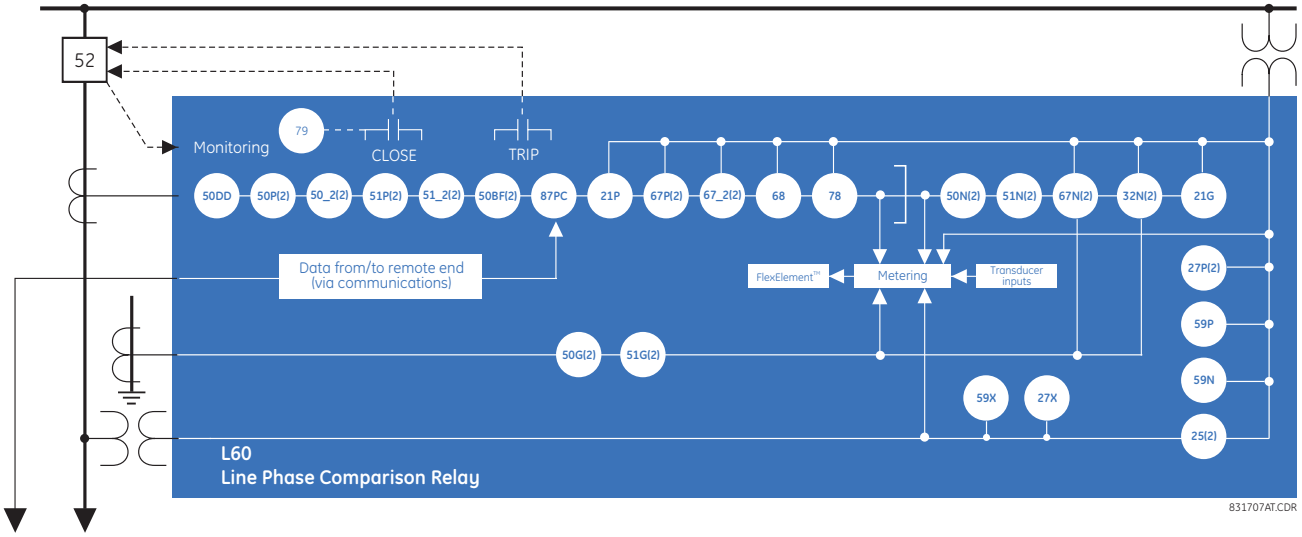


Figure 2–2: SINGLE LINE DIAGRAM

Table 2–2: OTHER DEVICE FUNCTIONS

FUNCTION	FUNCTION
Breaker Arcing Current (I^2t)	IEC 61850 Communications (optional)
Breaker Control	Modbus Communications
Contact Inputs (up to 96)	Modbus User Map
Contact Outputs (up to 64)	Non-Volatile Latches
Control Pushbuttons	Non-Volatile Selector Switch
CT Failure Detector	Open Breaker Echo
Data Logger	Oscillography
Digital Counters (8)	Pilot Scheme (POTT)
Digital Elements (48)	Setting Groups (6)
DNP 3.0 or IEC 60870-5-104 Communications	Time Synchronization over SNTP
Event Recorder	Transducer Inputs/Outputs
Fault Location	User Definable Display
Fault Reporting	User Programmable LEDs
FlexElements™ (8)	User Programmable Pushbuttons
FlexLogic™ Equations	User Programmable Self-Tests
Line Pickup	Virtual Inputs (64)
Load Encroachment	Virtual Outputs (96)
Metering: Current, Voltage, Power, Frequency	VT Fuse Failure

2.1.2 ORDERING

The L60 is available as a 19-inch rack horizontal mount unit or a reduced size (¾) vertical mount unit, and consists of the following modules: CPU, faceplate, power supply, CPU, CT/VT, digital input/outputs, and inter-relay communications. Each of these modules can be supplied in a number of configurations specified at the time of ordering. The information required to completely specify the relay is provided in the following tables (see chapter 3 for full details of relay modules).

The L60 is specified with two CT/VT modules (8F and 8P). When the L60 is applied in two-breaker configurations (such as breaker-and-a-half or ring configurations), the currents from the two CTs are summed internally within the relay or externally. If the voltage is not supplies to the relay, some functions (such as distance, undervoltage, and synchrocheck) will not be available.

NOTE

Order codes are subject to change without notice. Refer to the GE Multilin ordering page at http://www.GEindustrial.com/multilin/order.htm for the latest details concerning L60 ordering options.

The order codes for the horizontal mount units are shown below.

Table 2–3: L60 ORDER CODES (HORIZONTAL UNITS)

	L60	-	*	**	-	*	*	-	F	**	-	H	**	-	L	**	-	N	**	-	S	**	-	U	**	-	W/X	**	For Full Sized Horizontal Mount
BASE UNIT	L60																												Base Unit
CPU			E																										RS485 and RS485
			G																										RS485 and multi-mode ST 10Base-F
			H																										RS485 and multi-mode ST redundant 10Base-F
			J																										RS485 and multi-mode ST 100Base-FX
			K																										RS485 and multi-mode ST redundant 100Base-FX
			L																										RS485 and single mode SC 100Base-FX
			M																										RS485 and single mode SC redundant 100Base-FX
			N																										RS485 and 10/100Base-T
			P																										RS485 and single mode ST 100Base-FX
			R																										RS485 and single mode ST redundant 100Base-FX
SOFTWARE				00																									No software options
				02																									Breaker-and-a-Half software
				03																									IEC 61850; not available for Type E CPUs
				05																									Breaker-and-a-Half software and IEC 61850; not available for Type E CPUs
MOUNT/COATING					H																								Horizontal (19" rack)
					A																								Horizontal (19" rack) with harsh environmental coating
FACEPLATE/ DISPLAY						C																							English display
						D																							French display
						R																							Russian display
						A																							Chinese display
						P																							English display with 4 small and 12 large programmable pushbuttons
						G																							French display with 4 small and 12 large programmable pushbuttons
						S																							Russian display with 4 small and 12 large programmable pushbuttons
						B																							Chinese display with 4 small and 12 large programmable pushbuttons
						K																							Enhanced front panel with English display
						M																							Enhanced front panel with French display
						Q																							Enhanced front panel with Russian display
						U																							Enhanced front panel with Chinese display
						L																							Enhanced front panel with English display and user-programmable pushbuttons
						N																							Enhanced front panel with French display and user-programmable pushbuttons
						T																							Enhanced front panel with Russian display and user-programmable pushbuttons
						V																							Enhanced front panel with Chinese display and user-programmable pushbuttons
POWER SUPPLY							H																						125 / 250 V AC/DC power supply
(redundant supply must							H																					RH	125 / 250 V AC/DC with redundant 125 / 250 V AC/DC power supply
be same type as main supply)							L																						24 to 48 V (DC only) power supply
							L																					RL	24 to 48 V (DC only) with redundant 24 to 48 V DC power supply
CT/VT MODULES									8P						8F														4CT, 2 communications channels, standard 4CT/4VT (breaker-and-a-half)
DIGITAL INPUTS/OUTPUTS													XX		XX			XX			XX			XX			XX		No Module
													4A		4A			4A			4A			4A					4 Solid-State (no monitoring) MOSFET outputs
													4B		4B			4B			4B			4B					4 Solid-State (voltage with optional current) MOSFET outputs
													4C		4C			4C			4C			4C					4 Solid-State (current with optional voltage) MOSFET outputs
													4D		4D			4D			4D			4D					16 digital inputs with Auto-Burnishing
													4L		4L			4L			4L			4L					14 Form-A (no monitoring) Latching outputs
													67		67			67			67			67					8 Form-A (no monitoring) outputs
													6A		6A			6A			6A			6A					2 Form-A (voltage with optional current) and 2 Form-C outputs, 8 digital inputs
													6B		6B			6B			6B			6B					2 Form-A (voltage with optional current) and 4 Form-C outputs, 4 digital inputs
													6C		6C			6C			6C			6C					8 Form-C outputs
													6D		6D			6D			6D			6D					16 digital inputs
													6E		6E			6E			6E			6E					4 Form-C outputs, 8 digital inputs
													6F		6F			6F			6F			6F					8 Fast Form-C outputs
													6G		6G			6G			6G			6G					4 Form-A (voltage with optional current) outputs, 8 digital inputs
													6H		6H			6H			6H			6H					6 Form-A (voltage with optional current) outputs, 4 digital inputs
													6K		6K			6K			6K			6K					4 Form-C and 4 Fast Form-C outputs
													6L		6L			6L			6L			6L					2 Form-A (current with optional voltage) and 2 Form-C outputs, 8 digital inputs
													6M		6M			6M			6M			6M					2 Form-A (current with optional voltage) and 4 Form-C outputs, 4 digital inputs
													6N		6N			6N			6N			6N					4 Form-A (current with optional voltage) outputs, 8 digital inputs
													6P		6P			6P			6P			6P					6 Form-A (current with optional voltage) outputs, 4 digital inputs
													6R		6R			6R			6R			6R					2 Form-A (no monitoring) and 2 Form-C outputs, 8 digital inputs
													6S		6S			6S			6S			6S					2 Form-A (no monitoring) and 4 Form-C outputs, 4 digital inputs
													6T		6T			6T			6T			6T					4 Form-A (no monitoring) outputs, 8 digital inputs
													6U		6U			6U			6U			6U					6 Form-A (no monitoring) outputs, 4 digital inputs
TRANSDUCER													5A		5A			5A			5A			5A					4 dcmA inputs, 4 dcmA outputs (only one 5A module is allowed)
INPUTS/OUTPUTS													5C		5C			5C			5C			5C					8 RTD inputs
(select a maximum of 3 per unit)													5D		5D			5D			5D			5D					4 RTD inputs, 4 dcmA outputs (only one 5D module is allowed)
													5E		5E			5E			5E			5E					4 RTD inputs, 4 dcmA inputs
													5F		5F			5F			5F			5F					8 dcmA inputs
INTER-RELAY																								2A		2A			C37.94SM, 1300nm single-mode, ELED, 1 channel single-mode
COMMUNICATIONS																								2B		2B			C37.94SM, 1300nm single-mode, ELED, 2 channel single-mode
(select a maximum of 1 per unit)																								2E		2E			Bi-phase, single channel
																								2F		2F			Bi-phase, dual channel
																								72		72			1550 nm, single-mode, LASER, 1 Channel
																								73		73			1550 nm, single-mode, LASER, 2 Channel
																								74		74			Channel 1 - RS422; Channel 2 - 1550 nm, single-mode, LASER
																								75		75			Channel 1 - G.703; Channel 2 - 1550 nm, Single-mode LASER
																								76		76			IEEE C37.94, 820 nm, multimode, LED, 1 Channel
																								77		77			IEEE C37.94, 820 nm, multimode, LED, 2 Channels
																								7A		7A			820 nm, multi-mode, LED, 1 Channel
																								7B		7B			1300 nm, multi-mode, LED, 1 Channel
																								7C		7C			1300 nm, single-mode, ELED, 1 Channel
																								7D		7D			1300 nm, single-mode, LASER, 1 Channel
																								7E		7E			Channel 1 - G.703; Channel 2 - 820 nm, multi-mode
																								7F		7F			Channel 1 - G.703; Channel 2 - 1300 nm, multi-mode
																								7G		7G			Channel 1 - G.703; Channel 2 - 1300 nm, single-mode ELED
																								7H		7H			820 nm, multi-mode, LED, 2 Channels
																								7I		7I			1300 nm, multi-mode, LED, 2 Channels
																								7J		7J			1300 nm, single-mode, ELED, 2 Channels
																								7K		7K			1300 nm, single-mode, LASER, 2 Channels
																								7L		7L			Channel 1 - RS422; Channel 2 - 820 nm, multi-mode, LED
																								7M		7M			Channel 1 - RS422; Channel 2 - 1300 nm, multi-mode, LED
																								7P		7P			Channel 1 - RS422; Channel 2 - 1300 nm, single-mode, LASER
																								7Q		7Q			Channel 1 - G.703; Channel 2 - 1300 nm, single-mode LASER
																								7R		7R			G.703, 1 Channel
																								7S		7S			G.703, 2 Channels
																								7T		7T			RS422, 1 Channel
																								7W		7W			RS422, 2 Channels

The order codes for the reduced size vertical mount units are shown below.

Table 2–4: L60 ORDER CODES (REDUCED SIZE VERTICAL UNITS)

	L60 - * ** - * * * - F ** - H ** - L ** - N ** - R **	Reduced Size Vertical Mount
BASE UNIT	L60	Base Unit
CPU	E	RS485 and RS485
	G	RS485 and multi-mode ST 10Base-F
	H	RS485 and multi-mode ST redundant 10Base-F
	J	RS485 and multi-mode ST 100Base-FX
	K	RS485 and multi-mode ST redundant 100Base-FX
	L	RS485 and single mode SC 100Base-FX
	M	RS485 and single mode SC redundant 100Base-FX
	N	RS485 and 10/100Base-T
	P	RS485 and single mode ST 100Base-FX
	R	RS485 and single mode ST redundant 100Base-FX
SOFTWARE	00	No software options
	02	Breaker-and-a-Half software
	03	IEC 61850; not available for Type E CPUs
	05	Breaker-and-a-Half software and IEC 61850; not available for Type E CPUs
MOUNT/COATING	V	Vertical (3/4 rack)
	B	Vertical (3/4 rack) with harsh environmental coating
FACEPLATE/ DISPLAY	F	English display
	D	French display
	R	Russian display
	K	Chinese display
POWER SUPPLY	H	125 / 250 V AC/DC power supply
	L	24 to 48 V (DC only) power supply
CT/VT MODULES	8P	4CT, 2 communications channels, standard 4CT/4VT (breaker-and-a-half)
DIGITAL INPUTS/OUTPUTS	XX	No Module
	4A	4 Solid-State (no monitoring) MOSFET outputs
	4B	4 Solid-State (voltage with optional current) MOSFET outputs
	4C	4 Solid-State (current with optional voltage) MOSFET outputs
	4D	16 digital inputs with Auto-Burnishing
	4L	14 Form-A (no monitoring) Latching outputs
	67	8 Form-A (no monitoring) outputs
	6A	2 Form-A (voltage with optional current) and 2 Form-C outputs, 8 digital inputs
	6B	2 Form-A (voltage with optional current) and 4 Form-C outputs, 4 digital inputs
	6C	8 Form-C outputs
	6D	16 digital inputs
	6E	4 Form-C outputs, 8 digital inputs
	6F	8 Fast Form-C outputs
	6G	4 Form-A (voltage with optional current) outputs, 8 digital inputs
	6H	6 Form-A (voltage with optional current) outputs, 4 digital inputs
	6K	4 Form-C and 4 Fast Form-C outputs
	6L	2 Form-A (current with optional voltage) and 2 Form-C outputs, 8 digital inputs
	6M	2 Form-A (current with optional voltage) and 4 Form-C outputs, 4 digital inputs
	6N	4 Form-A (current with optional voltage) outputs, 8 digital inputs
	6P	6 Form-A (current with optional voltage) outputs, 4 digital inputs
	6R	2 Form-A (no monitoring) and 2 Form-C outputs, 8 digital inputs
	6S	2 Form-A (no monitoring) and 4 Form-C outputs, 4 digital inputs
	6T	4 Form-A (no monitoring) outputs, 8 digital inputs
	6U	6 Form-A (no monitoring) outputs, 4 digital inputs
TRANSDUCER INPUTS/OUTPUTS (select a maximum of 3 per unit)	5A	4 dcmA inputs, 4 dcmA outputs (only one 5A module is allowed)
	5C	8 RTD inputs
	5D	4 RTD inputs, 4 dcmA outputs (only one 5D module is allowed)
	5E	4 RTD inputs, 4 dcmA inputs
	5F	8 dcmA inputs
INTER-RELAY COMMUNICATIONS (select a maximum of 1 per unit)	2A	C37.94SM, 1300nm single-mode, ELED, 1 channel single-mode
	2B	C37.94SM, 1300nm single-mode, ELED, 2 channel single-mode
	2E	Bi-phase, single channel
	2F	Bi-phase, dual channel
	72	1550 nm, single-mode, LASER, 1 Channel
	73	1550 nm, single-mode, LASER, 2 Channel
	74	Channel 1 - RS422; Channel 2 - 1550 nm, single-mode, LASER
	75	Channel 1 - G.703; Channel 2 - 1550 nm, Single-mode LASER
	76	IEEE C37.94, 820 nm, multimode, LED, 1 Channel
	77	IEEE C37.94, 820 nm, multimode, LED, 2 Channels
	7A	820 nm, multi-mode, LED, 1 Channel
	7B	1300 nm, multi-mode, LED, 1 Channel
	7C	1300 nm, single-mode, ELED, 1 Channel
	7D	1300 nm, single-mode, LASER, 1 Channel
	7E	Channel 1 - G.703; Channel 2 - 820 nm, multi-mode
	7F	Channel 1 - G.703; Channel 2 - 1300 nm, multi-mode
	7G	Channel 1 - G.703; Channel 2 - 1300 nm, single-mode ELED
	7H	820 nm, multi-mode, LED, 2 Channels
	7I	1300 nm, multi-mode, LED, 2 Channels
	7J	1300 nm, single-mode, ELED, 2 Channels
	7K	1300 nm, single-mode, LASER, 2 Channels
	7L	Channel 1 - RS422; Channel 2 - 820 nm, multi-mode, LED
	7M	Channel 1 - RS422; Channel 2 - 1300 nm, multi-mode, LED
	7P	Channel 1 - RS422; Channel 2 - 1300 nm, single-mode, LASER
	7Q	Channel 1 - G.703; Channel 2 - 1300 nm, single-mode LASER
	7R	G.703, 1 Channel
	7S	G.703, 2 Channels
	7T	RS422, 1 Channel
	7W	RS422, 2 Channels

2.1.3 REPLACEMENT MODULES

Replacement modules can be ordered separately as shown below. When ordering a replacement CPU module or faceplate, please provide the serial number of your existing unit.

NOTE

Not all replacement modules may be applicable to the L60 relay. Only the modules specified in the order codes are available as replacement modules.

NOTE

Replacement module codes are subject to change without notice. Refer to the GE Multilin ordering page at http://www.GEindustrial.com/multilin/order.htm for the latest details concerning L60 ordering options.

The replacement module order codes for the horizontal mount units are shown below.

Table 2–5: ORDER CODES FOR REPLACEMENT MODULES, HORIZONTAL UNITS

UR - ** - *	
POWER SUPPLY	1H — 125 / 250 V AC/DC
(redundant supply only	1L — 24 to 48 V (DC only)
available in horizontal units; must	RH — redundant 125 / 250 V AC/DC
be same type as main supply)	RH — redundant 24 to 48 V (DC only)
CPU	9E — RS485 and RS485 (Modbus RTU, DNP 3.0)
	9G — RS485 and 10Base-F (Ethernet, Modbus TCP/IP, DNP 3.0)
	9H — RS485 and Redundant 10Base-F (Ethernet, Modbus TCP/IP, DNP 3.0)
	9J — RS485 and multi-mode ST 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9K — RS485 and multi-mode ST redundant 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9L — RS485 and single mode SC 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9M — RS485 and single mode SC redundant 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9N — RS485 and 10/100Base-T (Ethernet, Modbus TCP/IP, DNP 3.0)
	9P — RS485 and single mode ST 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9R — RS485 and single mode ST redundant 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
FACEPLATE/DISPLAY	3C — Horizontal faceplate with keypad and English display
	3D — Horizontal faceplate with keypad and French display
	3R — Horizontal faceplate with keypad and Russian display
	3A — Horizontal faceplate with keypad and Chinese display
	3P — Horizontal faceplate with keypad, user-programmable pushbuttons, and English display
	3G — Horizontal faceplate with keypad, user-programmable pushbuttons, and French display
	3S — Horizontal faceplate with keypad, user-programmable pushbuttons, and Russian display
	3B — Horizontal faceplate with keypad, user-programmable pushbuttons, and Chinese display
	3K — Enhanced front panel with English display
	3M — Enhanced front panel with French display
	3Q — Enhanced front panel with Russian display
	3U — Enhanced front panel with Chinese display
	3L — Enhanced front panel with English display and user-programmable pushbuttons
	3N — Enhanced front panel with French display and user-programmable pushbuttons
	3T — Enhanced front panel with Russian display and user-programmable pushbuttons
	3V — Enhanced front panel with Chinese display and user-programmable pushbuttons
DIGITAL INPUTS AND OUTPUTS	4A — 4 Solid-State (no monitoring) MOSFET outputs
	4B — 4 Solid-State (voltage with optional current) MOSFET outputs
	4C — 4 Solid-State (current with optional voltage) MOSFET outputs
	4D — 16 digital inputs with Auto-Burnishing
	4L — 14 Form-A (no monitoring) Latching outputs
	67 — 8 Form-A (no monitoring) outputs
	6A — 2 Form-A (voltage with optional current) and 2 Form-C outputs, 8 digital inputs
	6B — 2 Form-A (voltage with optional current) and 4 Form-C outputs, 4 digital inputs
	6C — 8 Form-C outputs
	6D — 16 digital inputs
	6E — 4 Form-C outputs, 8 digital inputs
	6F — 8 Fast Form-C outputs
	6G — 4 Form-A (voltage with optional current) outputs, 8 digital inputs
	6H — 6 Form-A (voltage with optional current) outputs, 4 digital inputs
	6K — 4 Form-C and 4 Fast Form-C outputs
	6L — 2 Form-A (current with optional voltage) and 2 Form-C outputs, 8 digital inputs
	6M — 2 Form-A (current with optional voltage) and 4 Form-C outputs, 4 digital inputs
	6N — 4 Form-A (current with optional voltage) outputs, 8 digital inputs
	6P — 6 Form-A (current with optional voltage) outputs, 4 digital inputs
	6R — 2 Form-A (no monitoring) and 2 Form-C outputs, 8 digital inputs
	6S — 2 Form-A (no monitoring) and 4 Form-C outputs, 4 digital inputs
	6T — 4 Form-A (no monitoring) outputs, 8 digital inputs
	6U — 6 Form-A (no monitoring) outputs, 4 digital inputs
CT/VT	8F — Standard 4CT/4VT
MODULES	8G — Sensitive Ground 4CT/4VT
(NOT AVAILABLE FOR THE C30)	8H — Standard 8CT
	8J — Sensitive Ground 8CT
	8L — Standard 4CT/4VT with enhanced diagnostics
	8M — Sensitive Ground 4CT/4VT with enhanced diagnostics
	8N — Standard 8CT with enhanced diagnostics
	8R — Sensitive Ground 8CT with enhanced diagnostics
	8P — 4CT and 2 communications channels
INTER-RELAY COMMUNICATIONS	2A — C37.94SM, 1300nm single-mode, ELED, 1 channel single-mode
	2B — C37.94SM, 1300nm single-mode, ELED, 2 channel single-mode
	2E — Bi-phase, single channel
	2F — Bi-phase, dual channel
	72 — 1550 nm, single-mode, LASER, 1 Channel
	73 — 1550 nm, single-mode, LASER, 2 Channel
	74 — Channel 1 - RS422; Channel 2 - 1550 nm, single-mode, LASER
	75 — Channel 1 - G.703; Channel 2 - 1550 nm, Single-mode LASER
	76 — IEEE C37.94, 820 nm, multimode, LED, 1 Channel
	77 — IEEE C37.94, 820 nm, multimode, LED, 2 Channels
	7A — 820 nm, multi-mode, LED, 1 Channel
	7B — 1300 nm, multi-mode, LED, 1 Channel
	7C — 1300 nm, single-mode, ELED, 1 Channel
	7D — 1300 nm, single-mode, LASER, 1 Channel
	7E — Channel 1 - G.703; Channel 2 - 820 nm, multi-mode
	7F — Channel 1 - G.703; Channel 2 - 1300 nm, multi-mode
	7G — Channel 1 - G.703; Channel 2 - 1300 nm, single-mode ELED
	7H — 820 nm, multi-mode, LED, 2 Channels
	7I — 1300 nm, multi-mode, LED, 2 Channels
	7J — 1300 nm, single-mode, ELED, 2 Channels
	7K — 1300 nm, single-mode, LASER, 2 Channels
	7L — Channel 1 - RS422; Channel 2 - 820 nm, multi-mode, LED
	7M — Channel 1 - RS422; Channel 2 - 1300 nm, multi-mode, LED
	7P — Channel 1 - RS422; Channel 2 - 1300 nm, single-mode, LASER
	7Q — Channel 1 - G.703; Channel 2 - 1300 nm, single-mode LASER
	7R — G.703, 1 Channel
	7S — G.703, 2 Channels
	7T — RS422, 1 Channel
	7V — RS422, 2 Channels, 2 Clock Inputs
	7W — RS422, 2 Channels
TRANSDUCER	5A — 4 dcmA inputs, 4 dcmA outputs (only one 5A module is allowed)
INPUTS/OUTPUTS	5C — 8 RTD inputs
	5D — 4 RTD inputs, 4 dcmA outputs (only one 5D module is allowed)
	5E — 4 dcmA inputs, 4 RTD inputs
	5F — 8 dcmA inputs

The replacement module order codes for the reduced-size vertical mount units are shown below.

Table 2–6: ORDER CODES FOR REPLACEMENT MODULES, VERTICAL UNITS

	UR - ** - *	
POWER SUPPLY	1H	125 / 250 V AC/DC
	1L	24 to 48 V (DC only)
CPU	9E	RS485 and RS485 (Modbus RTU, DNP 3.0)
	9G	RS485 and 10Base-F (Ethernet, Modbus TCP/IP, DNP 3.0)
	9H	RS485 and Redundant 10Base-F (Ethernet, Modbus TCP/IP, DNP 3.0)
	9J	RS485 and multi-mode ST 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9K	RS485 and multi-mode ST redundant 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9L	RS485 and single mode SC 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9M	RS485 and single mode SC redundant 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9N	RS485 and 10/100Base-T (Ethernet, Modbus TCP/IP, DNP 3.0)
	9P	RS485 and single mode ST 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
	9R	RS485 and single mode ST redundant 100Base-FX (Ethernet, Modbus TCP/IP, DNP 3.0)
FACEPLATE/DISPLAY	3F	Vertical faceplate with keypad and English display
	3D	Vertical faceplate with keypad and French display
	3R	Vertical faceplate with keypad and Russian display
	3K	Vertical faceplate with keypad and Chinese display
DIGITAL	4A	4 Solid-State (no monitoring) MOSFET outputs
INPUTS/OUTPUTS	4B	4 Solid-State (voltage with optional current) MOSFET outputs
	4C	4 Solid-State (current with optional voltage) MOSFET outputs
	4D	16 digital inputs with Auto-Burnishing
	4L	14 Form-A (no monitoring) Latching outputs
	67	8 Form-A (no monitoring) outputs
	6A	2 Form-A (voltage with optional current) and 2 Form-C outputs, 8 digital inputs
	6B	2 Form-A (voltage with optional current) and 4 Form-C outputs, 4 digital inputs
	6C	8 Form-C outputs
	6D	16 digital inputs
	6E	4 Form-C outputs, 8 digital inputs
	6F	8 Fast Form-C outputs
	6G	4 Form-A (voltage with optional current) outputs, 8 digital inputs
	6H	6 Form-A (voltage with optional current) outputs, 4 digital inputs
	6K	4 Form-C and 4 Fast Form-C outputs
	6L	2 Form-A (current with optional voltage) and 2 Form-C outputs, 8 digital inputs
	6M	2 Form-A (current with optional voltage) and 4 Form-C outputs, 4 digital inputs
	6N	4 Form-A (current with optional voltage) outputs, 8 digital inputs
	6P	6 Form-A (current with optional voltage) outputs, 4 digital inputs
	6R	2 Form-A (no monitoring) and 2 Form-C outputs, 8 digital inputs
	6S	2 Form-A (no monitoring) and 4 Form-C outputs, 4 digital inputs
	6T	4 Form-A (no monitoring) outputs, 8 digital inputs
	6U	6 Form-A (no monitoring) outputs, 4 digital inputs
CT/VT	8F	Standard 4CT/4VT
MODULES	8G	Sensitive Ground 4CT/4VT
(NOT AVAILABLE FOR THE C30)	8H	Standard 8CT
	8J	Sensitive Ground 8CT
	8L	Standard 4CT/4VT with enhanced diagnostics
	8M	Sensitive Ground 4CT/4VT with enhanced diagnostics
	8N	Standard 8CT with enhanced diagnostics
	8R	Sensitive Ground 8CT with enhanced diagnostics
	8P	4CT and 2 communications channels
INTER-RELAY COMMUNICATIONS	2A	C37.94SM, 1300nm single-mode, ELED, 1 channel single-mode
	2B	C37.94SM, 1300nm single-mode, ELED, 2 channel single-mode
	2E	Bi-phase, single channel
	2F	Bi-phase, dual channel
	72	1550 nm, single-mode, LASER, 1 Channel
	73	1550 nm, single-mode, LASER, 2 Channel
	74	Channel 1 - RS422; Channel 2 - 1550 nm, single-mode, LASER
	75	Channel 1 - G.703; Channel 2 - 1550 nm, Single-mode LASER
	76	IEEE C37.94, 820 nm, multimode, LED, 1 Channel
	77	IEEE C37.94, 820 nm, multimode, LED, 2 Channels
	7A	820 nm, multi-mode, LED, 1 Channel
	7B	1300 nm, multi-mode, LED, 1 Channel
	7C	1300 nm, single-mode, ELED, 1 Channel
	7D	1300 nm, single-mode, LASER, 1 Channel
	7E	Channel 1 - G.703; Channel 2 - 820 nm, multi-mode
	7F	Channel 1 - G.703; Channel 2 - 1300 nm, multi-mode
	7G	Channel 1 - G.703; Channel 2 - 1300 nm, single-mode ELED
	7H	820 nm, multi-mode, LED, 2 Channels
	7I	1300 nm, multi-mode, LED, 2 Channels
	7J	1300 nm, single-mode, ELED, 2 Channels
	7K	1300 nm, single-mode, LASER, 2 Channels
	7L	Channel 1 - RS422; Channel 2 - 820 nm, multi-mode, LED
	7M	Channel 1 - RS422; Channel 2 - 1300 nm, multi-mode, LED
	7P	Channel 1 - RS422; Channel 2 - 1300 nm, single-mode, LASER
	7Q	Channel 1 - G.703; Channel 2 - 1300 nm, single-mode LASER
	7R	G.703, 1 Channel
	7S	G.703, 2 Channels
	7T	RS422, 1 Channel
	7V	RS422, 2 Channels, 2 Clock Inputs
	7W	RS422, 2 Channels
TRANSDUCER	5A	4 dcmA inputs, 4 dcmA outputs (only one 5A module is allowed)
INPUTS/OUTPUTS	5C	8 RTD inputs
	5D	4 RTD inputs, 4 dcmA outputs (only one 5D module is allowed)
	5E	4 dcmA inputs, 4 RTD inputs
	5F	8 dcmA inputs

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

2.2.1 PROTECTION ELEMENTS

NOTE

The operating times below include the activation time of a trip rated form-A output contact unless otherwise indicated. FlexLogic™ operands of a given element are 4 ms faster. This should be taken into account when using FlexLogic™ to interconnect with other protection or control elements of the relay, building FlexLogic™ equations, or interfacing with other IEDs or power system devices via communications or different output contacts.

87PC SCHEME

Signal selection: mixed I_2 – K × I_1 (K = 0.00 to 0.25 in steps of 0.01), or 3I_0
Angle reference: 0 to 360° leading in steps of 1
Fault detector low:
  Instantaneous overcurrent: 0.02 to 15.00 pu in steps of 0.01
  $I_2 \times Z - V_2$: 0.005 to 15.000 pu in steps of 0.001
  dI_2 / dt: 0.01 to 5.00 pu in steps of 0.01
  dI_1 / dt: 0.01 to 5.00 pu in steps of 0.01
Fault detector high:
  Instantaneous overcurrent: 0.10 to 15.00 pu in steps of 0.01
  $I_2 \times Z - V_2$: 0.005 to 15.000 pu in steps of 0.001
  dI_2 / dt: 0.01 to 5.00 pu in steps of 0.01
  dI_1 / dt: 0.01 to 5.00 pu in steps of 0.01
Signal symmetry adjustment: –5.0 to 5.0 ms in steps of 0.1
Channel delay adjustment: 0.000 to 30.00 ms in steps of 0.001
Channel adjustments: channel delay and signal symmetry compensation
Operate time (typical): ¾ cycle for single phase comparison
½ cycle for dual phase comparison
Trip security: first coincidence or enhanced
Second coincidence timer: 10 to 200 ms in steps of 1
Enhanced stability angle: 40 to 180° in steps of 1

PHASE DISTANCE

Characteristic: mho (memory polarized or offset) or quad (memory polarized or non-directional), selectable individually per zone
Number of zones: 3
Directionality: forward, reverse, or non-directional
Reach (secondary Ω): 0.02 to 500.00 Ω in steps of 0.01
Reach accuracy: ±5% including the effect of CVT transients up to an SIR of 30
Distance:
  Characteristic angle: 30 to 90° in steps of 1
  Comparator limit angle: 30 to 90° in steps of 1
Directional supervision:
  Characteristic angle: 30 to 90° in steps of 1
  Limit angle: 30 to 90° in steps of 1
Right blinder (Quad only):
  Reach: 0.02 to 500 Ω in steps of 0.01
  Characteristic angle: 60 to 90° in steps of 1
Left Blinder (Quad only):
  Reach: 0.02 to 500 Ω in steps of 0.01
  Characteristic angle: 60 to 90° in steps of 1
Time delay: 0.000 to 65.535 s in steps of 0.001
Timing accuracy: ±3% or 4 ms, whichever is greater
Current supervision:
  Level: line-to-line current
  Pickup: 0.050 to 30.000 pu in steps of 0.001
  Dropout: 97 to 98%
Memory duration: 5 to 25 cycles in steps of 1
VT location: all delta-wye and wye-delta transformers
CT location: all delta-wye and wye-delta transformers
Voltage supervision pickup (series compensation applications): 0 to 5.000 pu in steps of 0.001
Operation time: 1 to 1.5 cycles (typical)
Reset time: 1 power cycle (typical)

GROUND DISTANCE

Characteristic: Mho (memory polarized or offset) or Quad (memory polarized or non-directional)
Reactance polarization: negative-sequence or zero-sequence current
Non-homogeneity angle: –40 to 40° in steps of 1
Number of zones: 3
Directionality: forward, reverse, or non-directional
Reach (secondary Ω): 0.02 to 500.00 Ω in steps of 0.01
Reach accuracy: ±5% including the effect of CVT transients up to an SIR of 30
Distance characteristic angle: 30 to 90° in steps of 1
Distance comparator limit angle: 30 to 90° in steps of 1
Directional supervision:
  Characteristic angle: 30 to 90° in steps of 1
  Limit angle: 30 to 90° in steps of 1
Zero-sequence compensation
  Z0/Z1 magnitude: 0.00 to 10.00 in steps of 0.01
  Z0/Z1 angle: –90 to 90° in steps of 1
Zero-sequence mutual compensation
  Z0M/Z1 magnitude: 0.00 to 7.00 in steps of 0.01
  Z0M/Z1 angle: –90 to 90° in steps of 1
Right blinder (Quad only):
  Reach: 0.02 to 500 Ω in steps of 0.01
  Characteristic angle: 60 to 90° in steps of 1
Left blinder (Quad only):
  Reach: 0.02 to 500 Ω in steps of 0.01
  Characteristic angle: 60 to 90° in steps of 1
Time delay: 0.000 to 65.535 s in steps of 0.001
Timing accuracy: ±3% or 4 ms, whichever is greater
Current supervision:
  Level: neutral current (3I_0)
  Pickup: 0.050 to 30.000 pu in steps of 0.001
  Dropout: 97 to 98%
Memory duration: 5 to 25 cycles in steps of 1
Voltage supervision pickup (series compensation applications): 0 to 5.000 pu in steps of 0.001
Operation time: 1 to 1.5 cycles (typical)
Reset time: 1 power cycle (typical)

LINE PICKUP

Phase instantaneous overcurrent: 0.000 to 30.000 pu
Undervoltage pickup: 0.000 to 3.000 pu
Overvoltage delay: 0.000 to 65.535 s

PHASE/NEUTRAL/GROUND TOC

Current: Phasor or RMS
Pickup level: 0.000 to 30.000 pu in steps of 0.001
Dropout level: 97% to 98% of pickup
Level accuracy:
  for 0.1 to 2.0 × CT: ±0.5% of reading or ±0.4% of rated (whichever is greater)
  for > 2.0 × CT: ±1.5% of reading > 2.0 × CT rating
Curve shapes: IEEE Moderately/Very/Extremely Inverse; IEC (and BS) A/B/C and Short Inverse; GE IAC Inverse, Short/Very/Extremely Inverse; I^2t; FlexCurves™ (programmable); Definite Time (0.01 s base curve)
Curve multiplier: Time Dial = 0.00 to 600.00 in steps of 0.01
Reset type: Instantaneous/Timed (per IEEE)
Timing accuracy: Operate at > 1.03 × actual pickup ±3.5% of operate time or ±½ cycle (whichever is greater)

PHASE/NEUTRAL/GROUND IOC

Pickup level: 0.000 to 30.000 pu in steps of 0.001
Dropout level: 97 to 98% of pickup
Level accuracy:
  0.1 to 2.0 × CT rating: ±0.5% of reading or ±0.4% of rated (whichever is greater)
  > 2.0 × CT rating ±1.5% of reading
Overreach: <2%
Pickup delay: 0.00 to 600.00 s in steps of 0.01
Reset delay: 0.00 to 600.00 s in steps of 0.01
Operate time: <16 ms at 3 × pickup at 60 Hz (Phase/Ground IOC)
<20 ms at 3 × pickup at 60 Hz (Neutral IOC)
Timing accuracy: Operate at 1.5 × pickup ±3% or ±4 ms (whichever is greater)

NEGATIVE SEQUENCE TOC

Current: Phasor
Pickup level: 0.000 to 30.000 pu in steps of 0.001
Dropout level: 97% to 98% of pickup
Level accuracy: ±0.5% of reading or ±0.4% of rated (whichever is greater)
from 0.1 to 2.0 x CT rating
±1.5% of reading > 2.0 x CT rating
Curve shapes: IEEE Moderately/Very/Extremely Inverse; IEC (and BS) A/B/C and Short Inverse; GE IAC Inverse, Short/Very/Extremely Inverse; I^2t; FlexCurves™ (programmable); Definite Time (0.01 s base curve)
Curve multiplier (Time dial): 0.00 to 600.00 in steps of 0.01
Reset type: Instantaneous/Timed (per IEEE) and Linear
Timing accuracy: Operate at > 1.03 × actual pickup ±3.5% of operate time or ±½ cycle (whichever is greater)

NEGATIVE SEQUENCE IOC

Current:	Phasor
Pickup level:	0.000 to 30.000 pu in steps of 0.001
Dropout level:	97 to 98% of pickup
Level accuracy:	0.1 to 2.0 × CT rating: ±0.5% of reading or ±0.4% of rated (whichever is greater) > 2.0 × CT rating: ±1.5% of reading
Overreach:	< 2%
Pickup delay:	0.00 to 600.00 s in steps of 0.01
Reset delay:	0.00 to 600.00 s in steps of 0.01
Operate time:	< 20 ms at 3 × pickup at 60 Hz
Timing accuracy:	Operate at 1.5 × pickup ±3% or ±4 ms (whichever is greater)

PHASE DIRECTIONAL OVERCURRENT

Relay connection:	90° (quadrature)
Quadrature voltage:	ABC phase seq.: phase A (V_{BC}), phase B (V_{CA}), phase C (V_{AB}) ACB phase seq.: phase A (V_{CB}), phase B (V_{AC}), phase C (V_{BA})
Polarizing voltage threshold:	0.000 to 3.000 pu in steps of 0.001
Current sensitivity threshold:	0.05 pu
Characteristic angle:	0 to 359° in steps of 1
Angle accuracy:	±2°
Operation time (FlexLogic™ operands):	Tripping (reverse load, forward fault):< 12 ms, typically Blocking (forward load, reverse fault):< 8 ms, typically

NEUTRAL DIRECTIONAL OVERCURRENT

Directionality:	Co-existing forward and reverse
Polarizing:	Voltage, Current, Dual
Polarizing voltage:	V_0 or VX
Polarizing current:	IG
Operating current:	I_0
Level sensing:	3 × (|I_0| – *K* × |I_1|), IG
Restraint, *K*:	0.000 to 0.500 in steps of 0.001
Characteristic angle:	–90 to 90° in steps of 1
Limit angle:	40 to 90° in steps of 1, independent for forward and reverse
Angle accuracy:	±2°
Offset impedance:	0.00 to 250.00 Ω in steps of 0.01
Pickup level:	0.002 to 30.000 pu in steps of 0.01
Dropout level:	97 to 98%
Operation time:	< 16 ms at 3 × pickup at 60 Hz

NEGATIVE SEQUENCE DIRECTIONAL OC

Directionality:	Co-existing forward and reverse
Polarizing:	Voltage
Polarizing voltage:	V_2
Operating current:	I_2
Level sensing:	Zero-sequence:|I_0| – *K* × |I_1| Negative-sequence:|I_2| – *K* × |I_1|
Restraint, *K*:	0.000 to 0.500 in steps of 0.001
Characteristic angle:	0 to 90° in steps of 1
Limit angle:	40 to 90° in steps of 1, independent for forward and reverse
Angle accuracy:	±2°
Offset impedance:	0.00 to 250.00 Ω in steps of 0.01
Pickup level:	0.05 to 30.00 pu in steps of 0.01
Dropout level:	97 to 98%
Operation time:	< 16 ms at 3 × pickup at 60 Hz

WATTMETRIC ZERO-SEQUENCE DIRECTIONAL

Measured power:	zero-sequence
Number of elements:	2
Characteristic angle:	0 to 360° in steps of 1
Minimum power:	0.001 to 1.200 pu in steps of 0.001
Pickup level accuracy:	±1% or ±0.0025 pu, whichever is greater
Hysteresis:	3% or 0.001 pu, whichever is greater
Pickup delay:	definite time (0 to 600.00 s in steps of 0.01), inverse time, or FlexCurve
Inverse time multiplier:	0.01 to 2.00 s in steps of 0.01
Time accuracy:	±3% or ±20 ms, whichever is greater
Operate time:	<30 ms at 60 Hz

PHASE UNDERVOLTAGE

Voltage:	Phasor only
Pickup level:	0.000 to 3.000 pu in steps of 0.001
Dropout level:	102 to 103% of pickup
Level accuracy:	±0.5% of reading from 10 to 208 V
Curve shapes:	GE IAV Inverse; Definite Time (0.1s base curve)
Curve multiplier:	Time dial = 0.00 to 600.00 in steps of 0.01
Timing accuracy:	Operate at < 0.90 × pickup ±3.5% of operate time or ±4 ms (whichever is greater)

AUXILIARY UNDERVOLTAGE

Pickup level:	0.000 to 3.000 pu in steps of 0.001
Dropout level:	102 to 103% of pickup
Level accuracy:	±0.5% of reading from 10 to 208 V
Curve shapes:	GE IAV Inverse, Definite Time
Curve multiplier:	Time Dial = 0 to 600.00 in steps of 0.01
Timing accuracy:	±3% of operate time or ±4 ms (whichever is greater)

PHASE OVERVOLTAGE

Voltage: Phasor only
Pickup level: 0.000 to 3.000 pu in steps of 0.001
Dropout level: 97 to 98% of pickup
Level accuracy: ±0.5% of reading from 10 to 208 V
Pickup delay: 0.00 to 600.00 in steps of 0.01 s
Operate time: < 30 ms at 1.10 × pickup at 60 Hz
Timing accuracy: ±3% or ±4 ms (whichever is greater)

NEUTRAL OVERVOLTAGE

Pickup level: 0.000 to 3.000 pu in steps of 0.001
Dropout level: 97 to 98% of pickup
Level accuracy: ±0.5% of reading from 10 to 208 V
Pickup delay: 0.00 to 600.00 s in steps of 0.01 (definite time) or user-defined curve
Reset delay: 0.00 to 600.00 s in steps of 0.01
Timing accuracy: ±3% or ±20 ms (whichever is greater)
Operate time: < 30 ms at 1.10 × pickup at 60 Hz

AUXILIARY OVERVOLTAGE

Pickup level: 0.000 to 3.000 pu in steps of 0.001
Dropout level: 97 to 98% of pickup
Level accuracy: ±0.5% of reading from 10 to 208 V
Pickup delay: 0 to 600.00 s in steps of 0.01
Reset delay: 0 to 600.00 s in steps of 0.01
Timing accuracy: ±3% of operate time or ±4 ms (whichever is greater)
Operate time: < 30 ms at 1.10 × pickup at 60 Hz

NEGATIVE SEQUENCE OVERVOLTAGE

Pickup level: 0.000 to 1.250 pu in steps of 0.001
Dropout level: 97 to 98% of pickup
Level accuracy: ±0.5% of reading from 10 to 208 V
Pickup delay: 0 to 600.00 s in steps of 0.01
Reset delay: 0 to 600.00 s in steps of 0.01
Time accuracy: ±3% or ±20 ms, whichever is greater
Operate time: < 30 ms at 1.10 × pickup at 60 Hz

BREAKER FAILURE

Mode: 1-pole, 3-pole
Current supervision: phase, neutral current
Current supv. pickup: 0.001 to 30.000 pu in steps of 0.001
Current supv. dropout: 97 to 98% of pickup
Current supv. accuracy:
  0.1 to 2.0 × CT rating: ±0.75% of reading or ±2% of rated (whichever is greater)
  above 2 × CT rating: ±2.5% of reading

BREAKER ARCING CURRENT

Principle: accumulates breaker duty (I^2t) and measures fault duration
Initiation: programmable per phase from any FlexLogic™ operand
Compensation for auxiliary relays: 0 to 65.535 s in steps of 0.001
Alarm threshold: 0 to 50000 kA2-cycle in steps of 1
Fault duration accuracy: 0.25 of a power cycle
Availability: 1 per CT bank with a minimum of 2

BREAKER FLASHOVER

Operating quantity: phase current, voltage and voltage difference
Pickup level voltage: 0 to 1.500 pu in steps of 0.001
Dropout level voltage: 97 to 98% of pickup
Pickup level current: 0 to 1.500 pu in steps of 0.001
Dropout level current: 97 to 98% of pickup
Level accuracy: ±0.5% or ±0.1% of rated, whichever is greater
Pickup delay: 0 to 65.535 s in steps of 0.001
Time accuracy: ±3% or ±42 ms, whichever is greater
Operate time: <42 ms at 1.10 × pickup at 60 Hz

OPEN BREAKER ECHO

Keying of the transmitter in case one end of the line is open or weak-infeed at the terminal.

SYNCHROCHECK

Max voltage difference: 0 to 400000 V in steps of 1
Max angle difference: 0 to 100° in steps of 1
Max freq. difference: 0.00 to 2.00 Hz in steps of 0.01
Hysteresis for max. freq. diff.: 0.00 to 0.10 Hz in steps of 0.01
Dead source function: None, LV1 & DV2, DV1 & LV2, DV1 or DV2, DV1 xor DV2, DV1 & DV2 (L = Live, D = Dead)

AUTORECLOSURE

Two breakers applications
Single- and three-pole tripping schemes
Up to 4 reclose attempts before lockout
Selectable reclosing mode and breaker sequence

PILOT-AIDED SCHEMES

Permissive Overreaching Transfer Trip (POTT)

TRIP OUTPUT

Collects trip and reclose input requests and issues outputs to control tripping and reclosing.
Communications timer delay: 0 to 65535 s in steps of 0.001
Evolving fault timer: 0.000 to 65.535 s in steps of 0.001
Timing accuracy: ±3% or 4 ms, whichever is greater

POWER SWING DETECT

Functions: Power swing block, Out-of-step trip
Characteristic: Mho or Quad
Measured impedance: Positive-sequence
Blocking / tripping modes: 2-step or 3-step
Tripping mode: Early or Delayed
Current supervision:
  Pickup level: 0.050 to 30.000 pu in steps of 0.001
  Dropout level: 97 to 98% of pickup
Fwd / reverse reach (sec. Ω): 0.10 to 500.00 Ω in steps of 0.01
Left and right blinders (sec. Ω): 0.10 to 500.00 Ω in steps of 0.01
Impedance accuracy: ±5%
Fwd / reverse angle impedances: 40 to 90° in steps of 1
Angle accuracy: ±2°
Characteristic limit angles: 40 to 140° in steps of 1
Timers: 0.000 to 65.535 s in steps of 0.001
Timing accuracy: ±3% or 4 ms, whichever is greater

LOAD ENCROACHMENT

Responds to:	Positive-sequence quantities
Minimum voltage:	0.000 to 3.000 pu in steps of 0.001
Reach (sec. Ω):	0.02 to 250.00 Ω in steps of 0.01
Impedance accuracy:	±5%
Angle:	5 to 50° in steps of 1
Angle accuracy:	±2°
Pickup delay:	0 to 65.535 s in steps of 0.001
Reset delay:	0 to 65.535 s in steps of 0.001
Time accuracy:	±3% or ±4 ms, whichever is greater
Operate time:	< 30 ms at 60 Hz

OPEN POLE DETECTOR

Functionality:	Detects an open pole condition, monitoring breaker auxiliary contacts, the current in each phase and optional voltages on the line
Current pickup level:	0.000 to 30.000 pu in steps of 0.001

Line capacitive reactances (X_{C1}, X_{C0}): 300.0 to 9999.9 sec. Ω in steps of 0.1

Remote current pickup level: 0.000 to 30.000 pu in steps of 0.001

Current dropout level:	pickup + 3%, not less than 0.05 pu

TRIP BUS (TRIP WITHOUT FLEXLOGIC™)

Number of elements:	6
Number of inputs:	16
Operate time:	<2 ms at 60 Hz
Time accuracy:	±3% or 10 ms, whichever is greater

2.2.2 USER-PROGRAMMABLE ELEMENTS

FLEXLOGIC™

Programming language:	Reverse Polish Notation with graphical visualization (keypad programmable)
Lines of code:	512
Internal variables:	64
Supported operations:	NOT, XOR, OR (2 to 16 inputs), AND (2 to 16 inputs), NOR (2 to 16 inputs), NAND (2 to 16 inputs), latch (reset-dominant), edge detectors, timers
Inputs:	any logical variable, contact, or virtual input
Number of timers:	32
Pickup delay:	0 to 60000 (ms, sec., min.) in steps of 1
Dropout delay:	0 to 60000 (ms, sec., min.) in steps of 1

FLEXCURVES™

Number:	4 (A through D)
Reset points:	40 (0 through 1 of pickup)
Operate points:	80 (1 through 20 of pickup)
Time delay:	0 to 65535 ms in steps of 1

FLEX STATES

Number:	up to 256 logical variables grouped under 16 Modbus addresses
Programmability:	any logical variable, contact, or virtual input

FLEXELEMENTS™

Number of elements:	8
Operating signal:	any analog actual value, or two values in differential mode
Operating signal mode:	signed or absolute value
Operating mode:	level, delta
Comparator direction:	over, under
Pickup Level:	–90.000 to 90.000 pu in steps of 0.001
Hysteresis:	0.1 to 50.0% in steps of 0.1
Delta dt:	20 ms to 60 days
Pickup & dropout delay:	0.000 to 65.535 s in steps of 0.001

NON-VOLATILE LATCHES

Type:	set-dominant or reset-dominant
Number:	16 (individually programmed)
Output:	stored in non-volatile memory
Execution sequence:	as input prior to protection, control, and FlexLogic™

USER-PROGRAMMABLE LEDs

Number:	48 plus trip and alarm
Programmability:	from any logical variable, contact, or virtual input
Reset mode:	self-reset or latched

LED TEST

Initiation:	from any digital input or user-programmable condition
Number of tests:	3, interruptible at any time
Duration of full test:	approximately 3 minutes
Test sequence 1:	all LEDs on
Test sequence 2:	all LEDs off, one LED at a time on for 1 s
Test sequence 3:	all LEDs on, one LED at a time off for 1 s

USER-DEFINABLE DISPLAYS

Number of displays:	16
Lines of display:	2 × 20 alphanumeric characters
Parameters:	up to 5, any Modbus register addresses
Invoking and scrolling:	keypad, or any user-programmable condition, including pushbuttons

CONTROL PUSHBUTTONS

Number of pushbuttons:	7
Operation:	drive FlexLogic™ operands

USER-PROGRAMMABLE PUSHBUTTONS (OPTIONAL)

Number of pushbuttons:	12 (standard faceplate); 16 (enhanced faceplate)
Mode:	self-reset, latched
Display message:	2 lines of 20 characters each
Drop-out timer:	0.00 to 60.00 s in steps of 0.05
Autoreset timer:	0.00 to 600.0 s in steps of 0.1

SELECTOR SWITCH

Number of elements:	2
Upper position limit:	1 to 7 in steps of 1
Selecting mode:	time-out or acknowledge
Time-out timer:	3.0 to 60.0 s in steps of 0.1
Control inputs:	step-up and 3-bit
Power-up mode:	restore from non-volatile memory or synchronize to a 3-bit control input or synch/restore mode

2.2.3 MONITORING

OSCILLOGRAPHY

Maximum records:	64
Sampling rate:	64 samples per power cycle
Triggers:	Any element pickup, dropout or operate Digital input change of state Digital output change of state FlexLogic™ equation
Data:	AC input channels Element state Digital input state Digital output state
Data storage:	In non-volatile memory

EVENT RECORDER

Capacity:	1024 events
Time-tag:	to 1 microsecond
Triggers:	Any element pickup, dropout or operate Digital input change of state Digital output change of state Self-test events
Data storage:	In non-volatile memory

DATA LOGGER

Number of channels:	1 to 16
Parameters:	Any available analog actual value
Sampling rate:	15 to 3600000 ms in steps of 1
Trigger:	any FlexLogic™ operand
Mode:	continuous or triggered
Storage capacity:	(NN is dependent on memory) 1-second rate: 01 channel for NN days 16 channels for NN days ↓ 60-minute rate: 01 channel for NN days 16 channels for NN days

FAULT LOCATOR

Method:	single-ended
Voltage source:	wye-connected VTs, delta-connected VTs and neutral voltage, delta-connected VTs and zero-sequence current (approximation)
Maximum accuracy if:	fault resistance is zero or fault currents from all line terminals are in phase
Relay accuracy:	±1.5% (V > 10 V, I > 0.1 pu)
Worst-case accuracy:	
$VT_{\%error}$ +	(user data)
$CT_{\%error}$ +	(user data)
$Z_{Line\%error}$ +	(user data)
$METHOD_{\%error}$ +	(see chapter 6)
$RELAY\ ACCURACY_{\%error}$ +	(1.5%)

2.2.4 METERING

RMS CURRENT: PHASE, NEUTRAL, AND GROUND

Accuracy at

0.1 to 2.0 × CT rating:	±0.25% of reading or ±0.1% of rated (whichever is greater)
> 2.0 × CT rating:	±1.0% of reading

RMS VOLTAGE

Accuracy:	±0.5% of reading from 10 to 208 V

REAL POWER (WATTS)

Accuracy:	±1.0% of reading at $-0.8 < PF \le -1.0$ and $0.8 < PF \le 1.0$

REACTIVE POWER (VARS)

Accuracy:	±1.0% of reading at $-0.2 \le PF \le 0.2$

APPARENT POWER (VA)

Accuracy:	±1.0% of reading

WATT-HOURS (POSITIVE AND NEGATIVE)

Accuracy:	±2.0% of reading
Range:	±0 to 2×10^9 MWh
Parameters:	3-phase only
Update rate:	50 ms

VAR-HOURS (POSITIVE AND NEGATIVE)

Accuracy: ±2.0% of reading
Range: ±0 to 2×10^9 Mvarh
Parameters: 3-phase only
Update rate: 50 ms

FREQUENCY

Accuracy at
V = 0.8 to 1.2 pu: ±0.001 Hz (when voltage signal is used for frequency measurement)
I = 0.1 to 0.25 pu: ±0.05 Hz
I > 0.25 pu: ±0.001 Hz (when current signal is used for frequency measurement)

2.2.5 INPUTS

AC CURRENT

CT rated primary: 1 to 50000 A
CT rated secondary: 1 A or 5 A by connection
Nominal frequency: 20 to 65 Hz
Relay burden: < 0.2 VA at rated secondary
Conversion range:
  Standard CT: 0.02 to 46 × CT rating RMS symmetrical
  Sensitive Ground CT module: 0.002 to 4.6 × CT rating RMS symmetrical
Current withstand: 20 ms at 250 times rated
1 sec. at 100 times rated
continuous at 3 times rated

AC VOLTAGE

VT rated secondary: 50.0 to 240.0 V
VT ratio: 1.00 to 24000.00
Nominal frequency: 20 to 65 Hz
Relay burden: < 0.25 VA at 120 V
Conversion range: 1 to 275 V
Voltage withstand: continuous at 260 V to neutral
1 min./hr at 420 V to neutral

CONTACT INPUTS

Dry contacts: 1000 Ω maximum
Wet contacts: 300 V DC maximum
Selectable thresholds: 17 V, 33 V, 84 V, 166 V
Tolerance: ±10%
Contacts per common return: 4
Recognition time: < 1 ms
Debounce time: 0.0 to 16.0 ms in steps of 0.5
Continuous current draw: 3 mA (when energized)

CONTACT INPUTS WITH AUTO-BURNISHING

Dry contacts: 1000 Ω maximum
Wet contacts: 300 V DC maximum
Selectable thresholds: 17 V, 33 V, 84 V, 166 V
Tolerance: ±10%
Contacts per common return: 2
Recognition time: < 1 ms
Debounce time: 0.0 to 16.0 ms in steps of 0.5
Continuous current draw: 3 mA (when energized)
Auto-burnish impulse current: 50 to 70 mA
Duration of auto-burnish impulse: 25 to 50 ms

DCMA INPUTS

Current input (mA DC): 0 to –1, 0 to +1, –1 to +1, 0 to 5, 0 to 10, 0 to 20, 4 to 20 (programmable)
Input impedance: 379 Ω ±10%
Conversion range: –1 to + 20 mA DC
Accuracy: ±0.2% of full scale
Type: Passive

RTD INPUTS

Types (3-wire): 100 Ω Platinum, 100 & 120 Ω Nickel, 10 Ω Copper
Sensing current: 5 mA
Range: –50 to +250°C
Accuracy: ±2°C
Isolation: 36 V pk-pk

IRIG-B INPUT

Amplitude modulation: 1 to 10 V pk-pk
DC shift: TTL
Input impedance: 22 kΩ
Isolation: 2 kV

REMOTE INPUTS (IEC 61850 GSSE/GOOSE)

Number of input points: 32, configured from 64 incoming bit pairs
Number of remote devices: 16
Default states on loss of comms.: On, Off, Latest/Off, Latest/On

TELEPROTECTION

Number of input points: 16
No. of remote devices: 3
Default states on loss of comms.: On, Off, Latest/Off, Latest/On
Ring configuration: No
Data rate: 64 or 128 kbps
CRC: 32-bit

2.2.6 POWER SUPPLY

LOW RANGE

Nominal DC voltage: 24 to 48 V
Min/max DC voltage: 20 / 60 V
Voltage loss hold-up: 20 ms duration at nominal
NOTE: Low range is DC only.

HIGH RANGE

Nominal DC voltage: 125 to 250 V
Min/max DC voltage: 88 / 300 V
Nominal AC voltage: 100 to 240 V at 50/60 Hz
Min/max AC voltage: 88 / 265 V at 25 to 100 Hz
Voltage loss hold-up: 200 ms duration at nominal

ALL RANGES

Volt withstand: 2 × Highest Nominal Voltage for 10 ms
Power consumption: typical = 15 to 20 W/VA
maximum = 50 W/VA
contact factory for exact order code consumption

INTERNAL FUSE

RATINGS
Low range power supply: 8 A / 250 V
High range power supply: 4 A / 250 V
INTERRUPTING CAPACITY
AC: 100 000 A RMS symmetrical
DC: 10 000 A

2.2.7 OUTPUTS

FORM-A RELAY

Make and carry for 0.2 s: 30 A as per ANSI C37.90
Carry continuous: 6 A
Break (DC inductive, L/R = 40 ms):

VOLTAGE	CURRENT
24 V	1 A
48 V	0.5 A
125 V	0.3 A
250 V	0.2 A

Operate time: < 4 ms
Contact material: silver alloy

LATCHING RELAY

Make and carry for 0.2 s: 30 A as per ANSI C37.90
Carry continuous: 6 A
Break at L/R of 40 ms: 0.25 A DC max.
Operate time: < 4 ms
Contact material: silver alloy
Control: separate operate and reset inputs
Control mode: operate-dominant or reset-dominant

FORM-A VOLTAGE MONITOR

Applicable voltage: approx. 15 to 250 V DC
Trickle current: approx. 1 to 2.5 mA

FORM-A CURRENT MONITOR

Threshold current: approx. 80 to 100 mA

FORM-C AND CRITICAL FAILURE RELAY

Make and carry for 0.2 s: 30 A as per ANSI C37.90
Carry continuous: 8 A
Break (DC inductive, L/R = 40 ms):

VOLTAGE	CURRENT
24 V	1 A
48 V	0.5 A
125 V	0.3 A
250 V	0.2 A

Operate time: < 8 ms
Contact material: silver alloy

FAST FORM-C RELAY

Make and carry: 0.1 A max. (resistive load)
Minimum load impedance:

INPUT VOLTAGE	IMPEDANCE	
	2 W RESISTOR	1 W RESISTOR
250 V DC	20 KΩ	50 KΩ
120 V DC	5 KΩ	2 KΩ
48 V DC	2 KΩ	2 KΩ
24 V DC	2 KΩ	2 KΩ

Note: values for 24 V and 48 V are the same due to a required 95% voltage drop across the load impedance.

Operate time: < 0.6 ms
Internal Limiting Resistor: 100 Ω, 2 W

SOLID-STATE OUTPUT RELAY

Operate and release time: <100 μs

Maximum voltage: 265 V DC

Maximum continuous current: 5 A at 45°C; 4 A at 65°C

Make and carry:

for 0.2 s: 30 A as per ANSI C37.90

for 0.03 s 300 A

Breaking capacity:

	UL508	Utility application (autoreclose scheme)	Industrial application
Operations/ interval	5000 ops / 1 s-On, 9 s-Off	5 ops / 0.2 s-On, 0.2 s-Off within 1 minute	10000 ops / 0.2 s-On, 30 s-Off
	1000 ops / 0.5 s-On, 0.5 s-Off		
Break capability (0 to 250 V DC)	3.2 A L/R = 10 ms	10 A L/R = 40 ms	10 A L/R = 40 ms
	1.6 A L/R = 20 ms		
	0.8 A L/R = 40 ms		

IRIG-B OUTPUT

Amplitude: 10 V peak-peak RS485 level

Maximum load: 100 ohms

Time delay: 1 ms for AM input
40 μs for DC-shift input

Isolation: 2 kV

CONTROL POWER EXTERNAL OUTPUT (FOR DRY CONTACT INPUT)

Capacity: 100 mA DC at 48 V DC

Isolation: ±300 Vpk

REMOTE OUTPUTS (IEC 61850 GSSE/GOOSE)

Standard output points: 32

User output points: 32

DCMA OUTPUTS

Range: –1 to 1 mA, 0 to 1 mA, 4 to 20 mA

Max. load resistance: 12 kΩ for –1 to 1 mA range
12 kΩ for 0 to 1 mA range
600 Ω for 4 to 20 mA range

Accuracy: ±0.75% of full-scale for 0 to 1 mA range
±0.5% of full-scale for –1 to 1 mA range
±0.75% of full-scale for 0 to 20 mA range

99% Settling time to a step change: 100 ms

Isolation: 1.5 kV

Driving signal: any FlexAnalog quantity

Upper and lower limit for the driving signal: –90 to 90 pu in steps of 0.001

2.2.8 COMMUNICATIONS

RS232

Front port: 19.2 kbps, Modbus® RTU

RS485

1 or 2 rear ports: Up to 115 kbps, Modbus® RTU, isolated together at 36 Vpk

Typical distance: 1200 m

Isolation: 2 kV

ETHERNET (FIBER)

PARAMETER	FIBER TYPE		
	10MB MULTI-MODE	100MB MULTI-MODE	100MB SINGLE-MODE
Wavelength	820 nm	1310 nm	1310 nm
Connector	ST	ST	SC
Transmit power	–20 dBm	–20 dBm	–15 dBm
Receiver sensitivity	–30 dBm	–30 dBm	–30 dBm
Power budget	10 dB	10 dB	15 dB
Maximum input power	–7.6 dBm	–14 dBm	–7 dBm
Typical distance	1.65 km	2 km	15 km
Duplex	full/half	full/half	full/half
Redundancy	yes	yes	yes

ETHERNET (COPPER)

Modes: 10 MB, 10/100 MB (auto-detect)

Connector: RJ45

SNTP clock synchronization error: <10 ms (typical)

2.2.9 INTER-RELAY COMMUNICATIONS

SHIELDED TWISTED-PAIR INTERFACE OPTIONS

INTERFACE TYPE	TYPICAL DISTANCE
RS422	1200 m
G.703	100 m

NOTE **RS422 distance is based on transmitter power and does not take into consideration the clock source provided by the user.**

LINK POWER BUDGET

EMITTER, FIBER TYPE	TRANSMIT POWER	RECEIVED SENSITIVITY	POWER BUDGET
820 nm LED, Multimode	–20 dBm	–30 dBm	10 dB
1300 nm LED, Multimode	–21 dBm	–30 dBm	9 dB
1300 nm ELED, Singlemode	–23 dBm	–30 dBm	9 dB
1300 nm Laser, Singlemode	–1 dBm	–30 dBm	29 dB
1550 nm Laser, Singlemode	+5 dBm	–30 dBm	35 dB

NOTE **These Power Budgets are calculated from the manufacturer's worst-case transmitter power and worst case receiver sensitivity.**

MAXIMUM OPTICAL INPUT POWER

EMITTER, FIBER TYPE	MAX. OPTICAL INPUT POWER
820 nm LED, Multimode	–7.6 dBm
1300 nm LED, Multimode	–11 dBm
1300 nm ELED, Singlemode	–14 dBm
1300 nm Laser, Singlemode	–14 dBm
1550 nm Laser, Singlemode	–14 dBm

TYPICAL LINK DISTANCE

EMITTER TYPE	FIBER TYPE	CONNECTOR TYPE	TYPICAL DISTANCE
820 nm LED	Multimode	ST	1.65 km
1300 nm LED	Multimode	ST	3.8 km
1300 nm ELED	Singlemode	ST	11.4 km
1300 nm Laser	Singlemode	ST	64 km
1550 nm Laser	Singlemode	ST	105 km

NOTE **Typical distances listed are based on the following assumptions for system loss. As actual losses will vary from one installation to another, the distance covered by your system may vary.**

CONNECTOR LOSSES (TOTAL OF BOTH ENDS)

ST connector 2 dB

FIBER LOSSES

820 nm multimode 3 dB/km
1300 nm multimode 1 dB/km
1300 nm singlemode 0.35 dB/km
1550 nm singlemode 0.25 dB/km
Splice losses: One splice every 2 km, at 0.05 dB loss per splice.

SYSTEM MARGIN

3 dB additional loss added to calculations to compensate for all other losses.

Compensated difference in transmitting and receiving (channel asymmetry) channel delays using GPS satellite clock: 10 ms

2.2.10 ENVIRONMENTAL

AMBIENT TEMPERATURES

Storage: –40 to 80°C

OPERATING TEMPERATURES

Cold: IEC 60068-2-1, 16 h at –40°C
Dry Heat: IEC 60068-2-2, 16 h at +85°C

NOTE The LCD contrast may be impaired at temperatures less than –20°C.

OTHER

Humidity (non-condensing): IEC 60068-2-30, 95%, Variant 1, 6 days
Altitude: Up to 2000 m
Installation Category: II

2.2.11 TYPE TESTS

Electrical fast transient: ANSI/IEEE C37.90.1
IEC 61000-4-4
IEC 60255-22-4

Oscillatory transient: ANSI/IEEE C37.90.1
IEC 61000-4-12

Insulation resistance: IEC 60255-5

Dielectric strength: IEC 60255-6
ANSI/IEEE C37.90

Electrostatic discharge: EN 61000-4-2

Surge immunity: EN 61000-4-5

RFI susceptibility: ANSI/IEEE C37.90.2
IEC 61000-4-3
IEC 60255-22-3
Ontario Hydro C-5047-77

Conducted RFI: IEC 61000-4-6

Voltage dips/interruptions/variations:
IEC 61000-4-11
IEC 60255-11

Power frequency magnetic field immunity:
IEC 61000-4-8

Pulse magnetic field immunity: IEC 61000-4-9

Vibration test (sinusoidal): IEC 60255-21-1

Shock and bump: IEC 60255-21-2

Seismic: IEC 60255-21-3
IEEE C37.98

Cold: IEC 60028-2-1, 16 h at –40°C

Dry heat: IEC 60028-2-2, 16 h at 85°C

NOTE **Type test report available upon request.**

2.2.12 PRODUCTION TESTS

THERMAL

Products go through an environmental test based upon an Accepted Quality Level (AQL) sampling process.

2.2.13 APPROVALS

APPROVALS

UL Listed for the USA and Canada

CE:

LVD 73/23/EEC: IEC 1010-1

EMC 81/336/EEC: EN 50081-2, EN 50082-2

2.2.14 MAINTENANCE

MOUNTING

Attach mounting brackets using 20 inch-pounds (±2 inch-pounds) of torque.

CLEANING

Normally, cleaning is not required; but for situations where dust has accumulated on the faceplate display, a dry cloth can be used.

NOTE Units that are stored in a de-energized state should be powered up once per year, for one hour continuously, to avoid deterioration of electrolytic capacitors.

a) HORIZONTAL UNITS

The L60 Line Phase Comparison System is available as a 19-inch rack horizontal mount unit with a removable faceplate. The faceplate can be specified as either standard or enhanced at the time of ordering. The enhanced faceplate contains additional user-programmable pushbuttons and LED indicators.

The modular design allows the relay to be easily upgraded or repaired by a qualified service person. The faceplate is hinged to allow easy access to the removable modules, and is itself removable to allow mounting on doors with limited rear depth. There is also a removable dust cover that fits over the faceplate, which must be removed when attempting to access the keypad or RS232 communications port.

The case dimensions are shown below, along with panel cutout details for panel mounting. When planning the location of your panel cutout, ensure that provision is made for the faceplate to swing open without interference to or from adjacent equipment.

The relay must be mounted such that the faceplate sits semi-flush with the panel or switchgear door, allowing the operator access to the keypad and the RS232 communications port. The relay is secured to the panel with the use of four screws supplied with the relay.

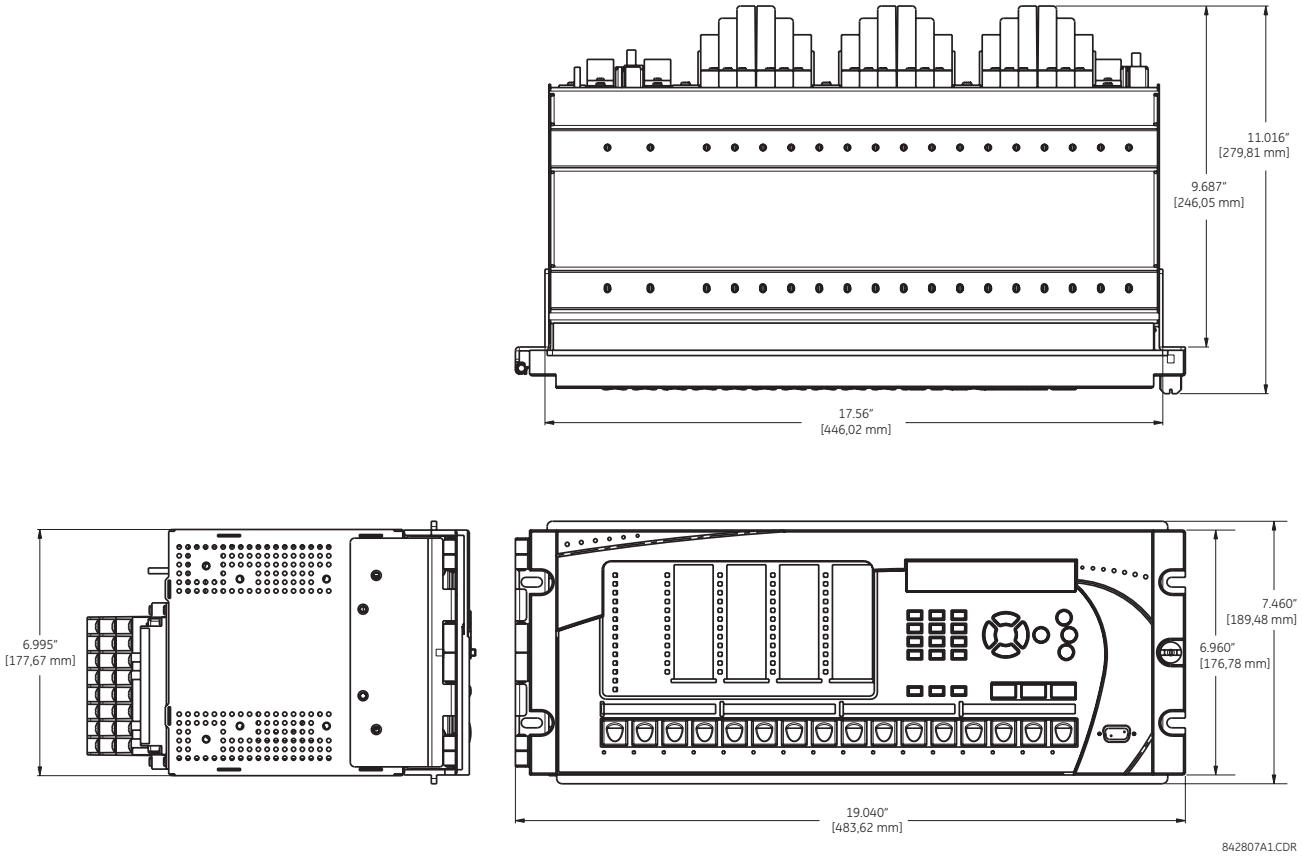


Figure 3–1: L60 HORIZONTAL DIMENSIONS (ENHANCED PANEL)

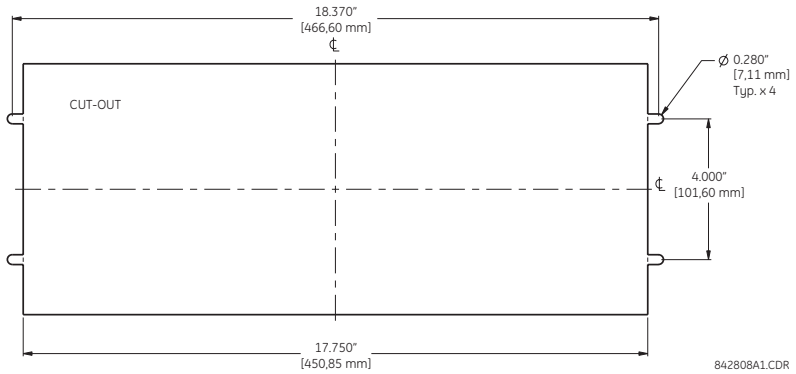


Figure 3–2: L60 HORIZONTAL MOUNTING (ENHANCED PANEL)

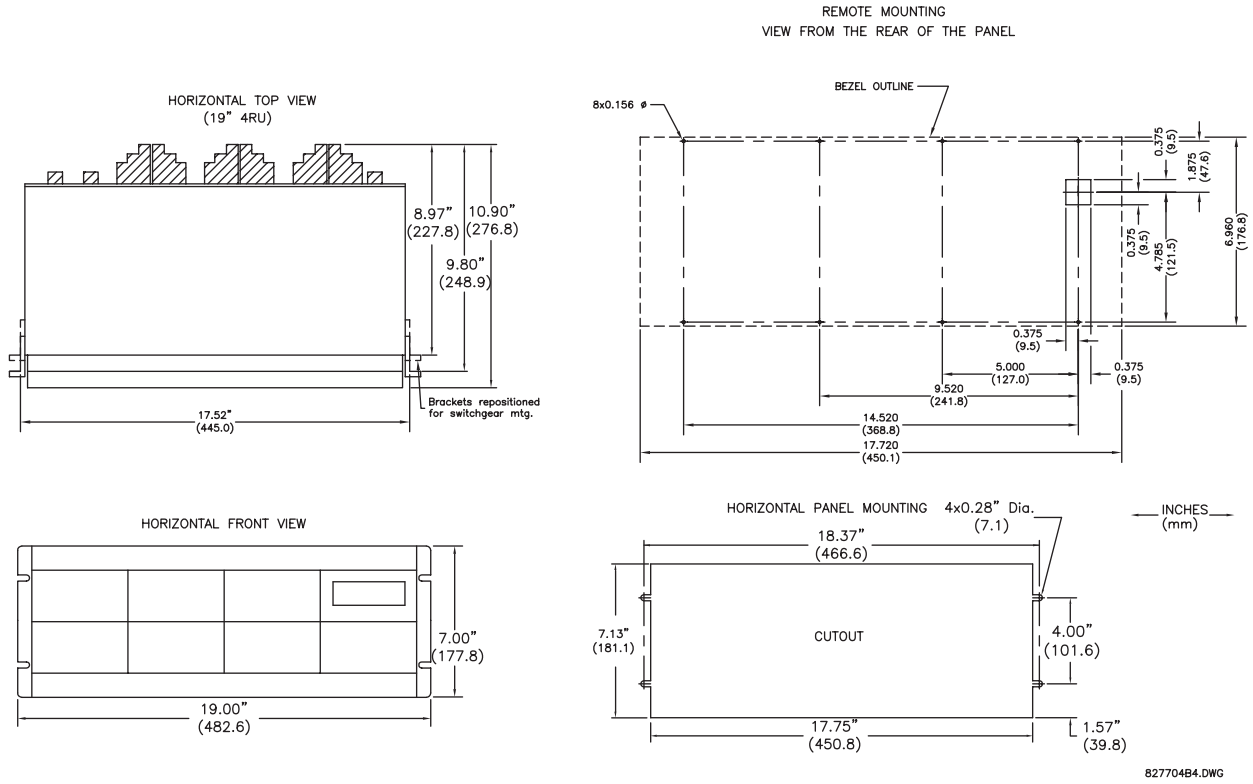


Figure 3–3: L60 HORIZONTAL MOUNTING AND DIMENSIONS (STANDARD PANEL)

b) VERTICAL UNITS

The L60 Line Phase Comparison System is available as a reduced size (¾) vertical mount unit, with a removable faceplate. The modular design allows the relay to be easily upgraded or repaired by a qualified service person. The faceplate is hinged to allow easy access to the removable modules, and is itself removable to allow mounting on doors with limited rear depth. There is also a removable dust cover that fits over the faceplate, which must be removed when attempting to access the keypad or RS232 communications port.

The case dimensions are shown below, along with panel cutout details for panel mounting. When planning the location of your panel cutout, ensure that provision is made for the faceplate to swing open without interference to or from adjacent equipment.

The relay must be mounted such that the faceplate sits semi-flush with the panel or switchgear door, allowing the operator access to the keypad and the RS232 communications port. The relay is secured to the panel with the use of four screws supplied with the relay.

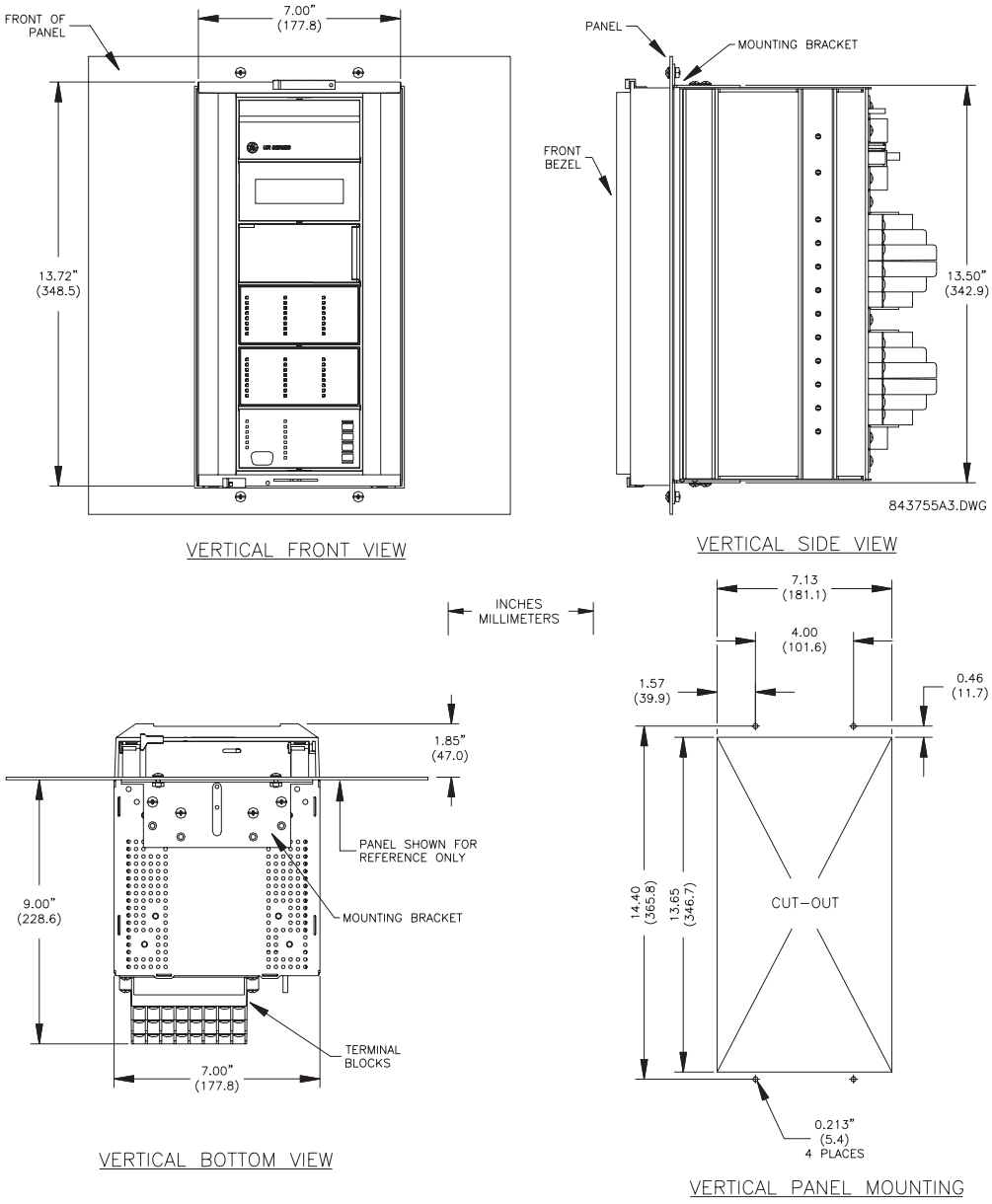


Figure 3–4: L60 VERTICAL MOUNTING AND DIMENSIONS

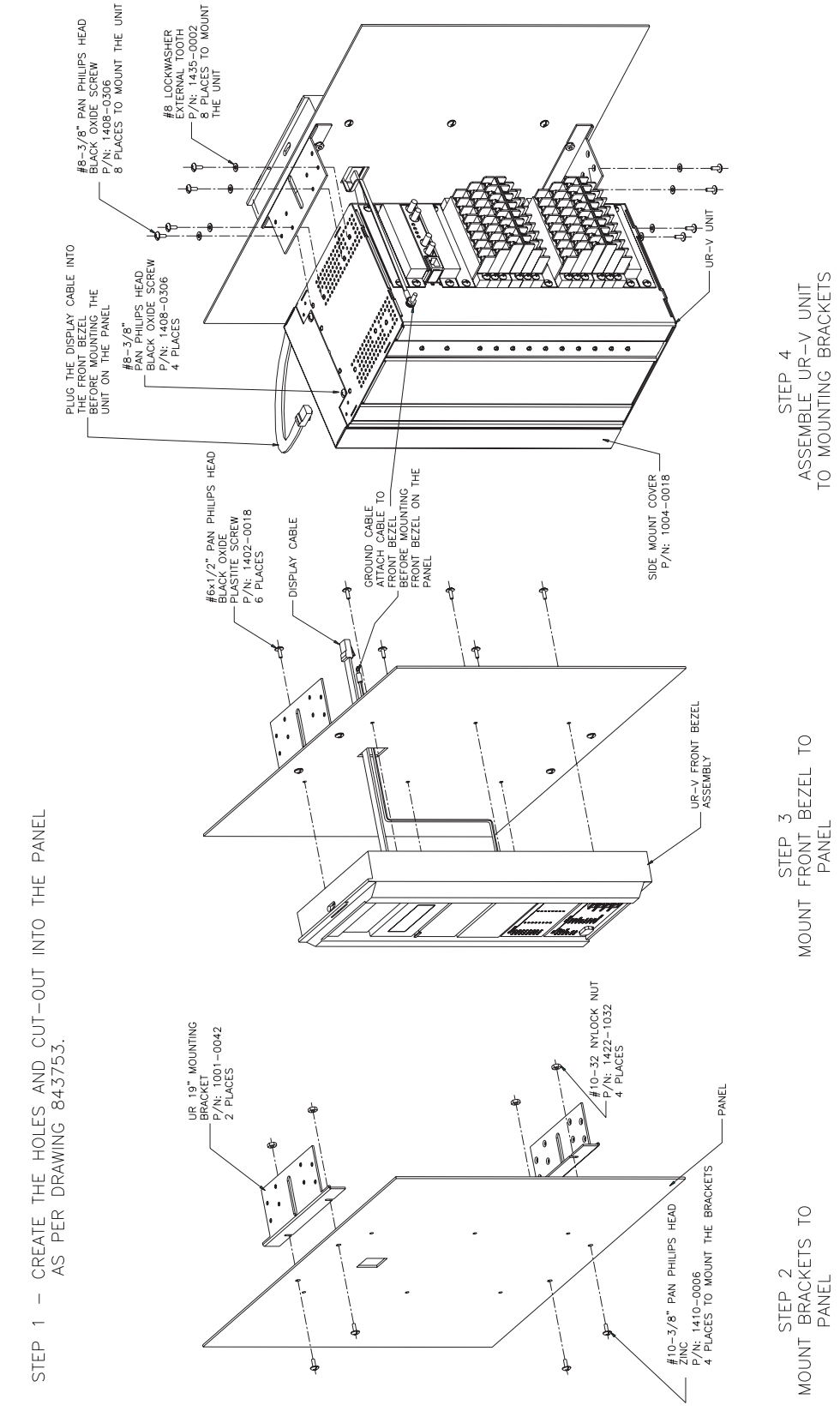


Figure 3–5: L60 VERTICAL SIDE MOUNTING INSTALLATION

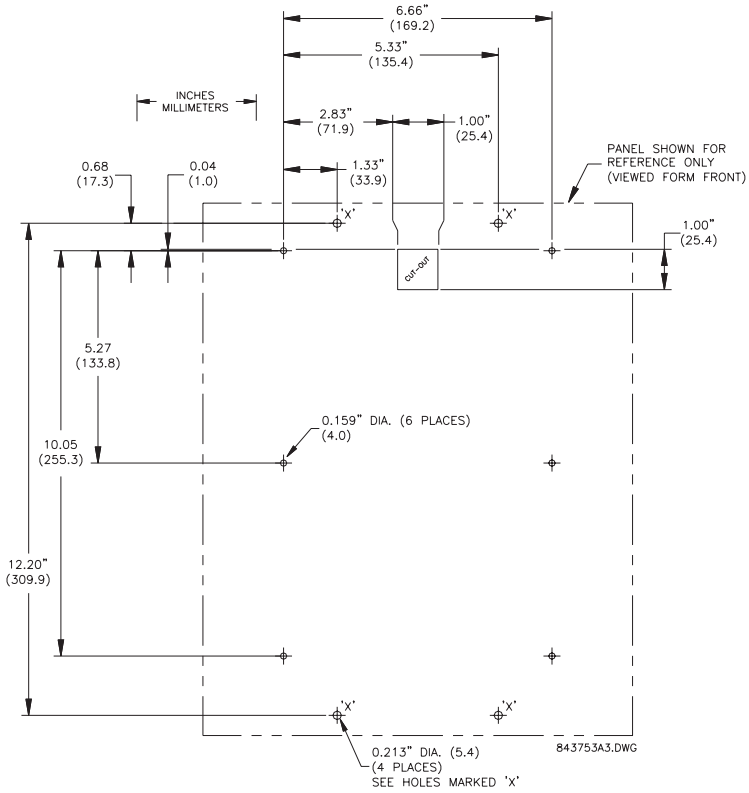


Figure 3–6: L60 VERTICAL SIDE MOUNTING REAR DIMENSIONS

3.1.2 MODULE WITHDRAWAL AND INSERTION

Module withdrawal and insertion may only be performed when control power has been removed from the unit. Inserting an incorrect module type into a slot may result in personal injury, damage to the unit or connected equipment, or undesired operation!

Proper electrostatic discharge protection (for example, a static strap) must be used when coming in contact with modules while the relay is energized!

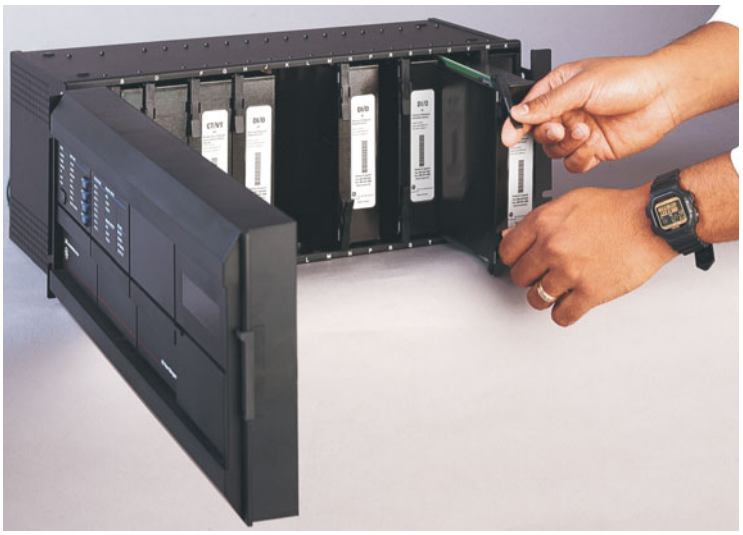
The relay, being modular in design, allows for the withdrawal and insertion of modules. Modules must only be replaced with like modules in their original factory configured slots.

The enhanced faceplate can be opened to the left, once thumb screw has been removed, as shown below. This allows for easy accessibility of the modules for withdrawal. The new wide-angle hinge assembly in the enhanced front panel opens completely and allows easy access to all modules in the L60.

842812A1.CDR

Figure 3–7: UR MODULE WITHDRAWAL AND INSERTION (ENHANCED FACEPLATE)

The standard faceplate can be opened to the left, once the sliding latch on the right side has been pushed up, as shown below. This allows for easy accessibility of the modules for withdrawal.



842760A1.CDR

Figure 3–8: UR MODULE WITHDRAWAL AND INSERTION (STANDARD FACEPLATE)

To properly remove a module, the ejector/inserter clips, located at the top and bottom of each module, must be pulled simultaneously. Before performing this action, **control power must be removed from the relay**. Record the original location of the module to ensure that the same or replacement module is inserted into the correct slot. Modules with current input provide automatic shorting of external CT circuits.

To properly insert a module, ensure that the **correct** module type is inserted into the **correct** slot position. The ejector/inserter clips located at the top and at the bottom of each module must be in the disengaged position as the module is smoothly inserted into the slot. Once the clips have cleared the raised edge of the chassis, engage the clips simultaneously. When the clips have locked into position, the module will be fully inserted.

NOTE

All CPU modules except the 9E are equipped with 10Base-T or 10Base-F Ethernet connectors. These connectors must be individually disconnected from the module before it can be removed from the chassis.

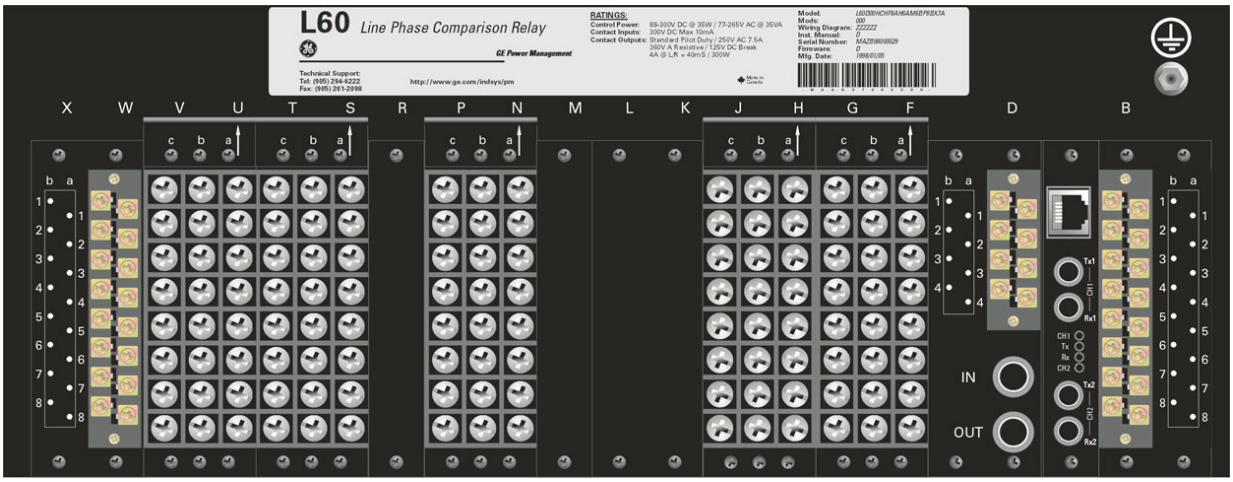
NOTE

The 4.0x release of the L60 relay includes new hardware modules.The new CPU modules are specified with codes 9E and higher. The new CT/VT modules are specified with the codes 8F and higher.

The new CT/VT modules can only be used with new CPUs; similarly, old CT/VT modules can only be used with old CPUs. To prevent hardware mismatches, the new modules have blue labels and a warning sticker stating **"Attn.: Ensure CPU and DSP module label colors are the same!"**. In the event that there is a mismatch between the CPU and CT/VT module, the relay will not function and a **DSP ERROR** or **HARDWARE MISMATCH** error will be displayed.

All other input/output modules are compatible with the new hardware. Firmware versions 4.0x and higher are only compatible with the new hardware modules. Previous versions of the firmware (3.4x and earlier) are only compatible with the older hardware modules.

3.1.3 REAR TERMINAL LAYOUT



831710AK.CDR

Figure 3–9: REAR TERMINAL VIEW

WARNING

Do not touch any rear terminals while the relay is energized!

The relay follows a convention with respect to terminal number assignments which are three characters long assigned in order by module slot position, row number, and column letter. Two-slot wide modules take their slot designation from the first slot position (nearest to CPU module) which is indicated by an arrow marker on the terminal block. See the following figure for an example of rear terminal assignments.

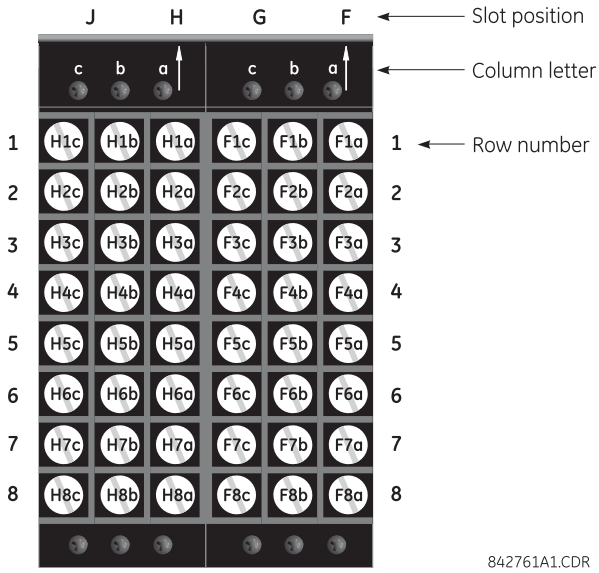


Figure 3–10: EXAMPLE OF MODULES IN F AND H SLOTS

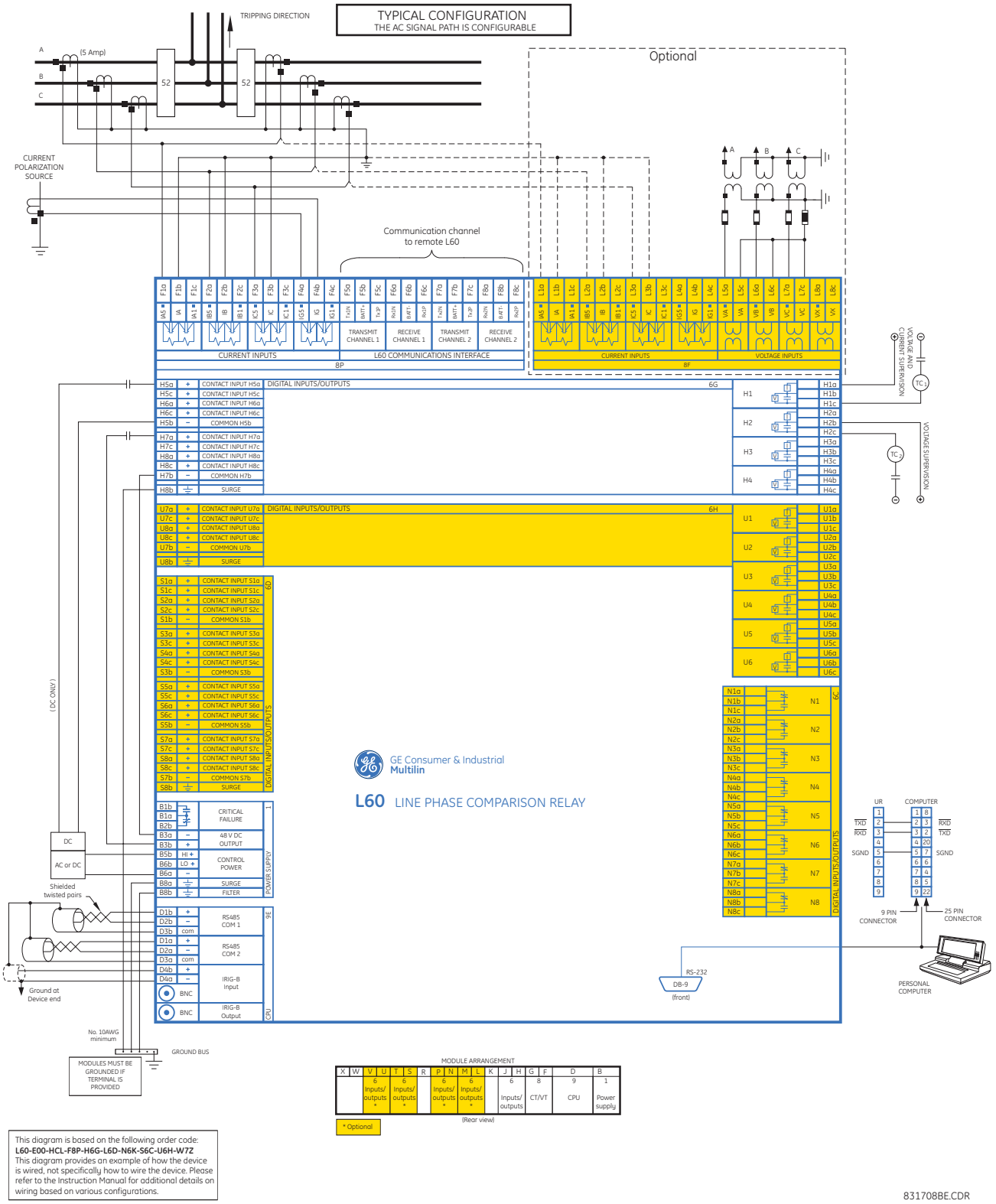


Figure 3–11: TYPICAL WIRING DIAGRAM

3.2.2 DIELECTRIC STRENGTH

The dielectric strength of the UR-series module hardware is shown in the following table:

Table 3–1: DIELECTRIC STRENGTH OF UR-SERIES MODULE HARDWARE

MODULE TYPE	MODULE FUNCTION	TERMINALS		DIELECTRIC STRENGTH (AC)
		FROM	TO	
1	Power supply	High (+); Low (+); (–)	Chassis	2000 V AC for 1 minute
1	Power supply	48 V DC (+) and (–)	Chassis	2000 V AC for 1 minute
1	Power supply	Relay terminals	Chassis	2000 V AC for 1 minute
2	Reserved	N/A	N/A	N/A
3	Reserved	N/A	N/A	N/A
4	Reserved	N/A	N/A	N/A
5	Analog inputs/outputs	All except 8b	Chassis	< 50 V DC
6	Digital inputs/outputs	All	Chassis	2000 V AC for 1 minute
7	G.703	All except 2b, 3a, 7b, 8a	Chassis	2000 V AC for 1 minute
	RS422	All except 6a, 7b, 8a	Chassis	< 50 V DC
8	CT/VT	All	Chassis	2000 V AC for 1 minute
9	CPU	All	Chassis	2000 V AC for 1 minute

Filter networks and transient protection clamps are used in the hardware to prevent damage caused by high peak voltage transients, radio frequency interference (RFI), and electromagnetic interference (EMI). These protective components **can be damaged** by application of the ANSI/IEEE C37.90 specified test voltage for a period longer than the specified one minute.

3.2.3 CONTROL POWER

CONTROL POWER SUPPLIED TO THE RELAY MUST BE CONNECTED TO THE MATCHING POWER SUPPLY RANGE OF THE RELAY. IF THE VOLTAGE IS APPLIED TO THE WRONG TERMINALS, DAMAGE MAY OCCUR!

The L60 relay, like almost all electronic relays, contains electrolytic capacitors. These capacitors are well known to be subject to deterioration over time if voltage is not applied periodically. Deterioration can be avoided by powering the relays up once a year.

The power supply module can be ordered for two possible voltage ranges, with or without a redundant power option. Each range has a dedicated input connection for proper operation. The ranges are as shown below (see the *Technical Specifications* section of chapter 2 for additional details):

LO range: 24 to 48 V (DC only) nominal
HI range: 125 to 250 V nominal

The power supply module provides power to the relay and supplies power for dry contact input connections.

The power supply module provides 48 V DC power for dry contact input connections and a critical failure relay (see the *Typical Wiring Diagram* earlier). The critical failure relay is a form-C that will be energized once control power is applied and the relay has successfully booted up with no critical self-test failures. If on-going self-test diagnostic checks detect a critical failure (see the *Self-Test Errors* table in chapter 7) or control power is lost, the relay will de-energize.

For high reliability systems, the L60 has a redundant option in which two L60 power supplies are placed in parallel on the bus. If one of the power supplies become faulted, the second power supply will assume the full load of the relay without any interruptions. Each power supply has a green LED on the front of the module to indicate it is functional. The critical fail relay of the module will also indicate a faulted power supply.

An LED on the front of the module shows the status of the power supply:

LED INDICATION	POWER SUPPLY
ON	OK
ON / OFF CYCLING	Failure
OFF	Failure

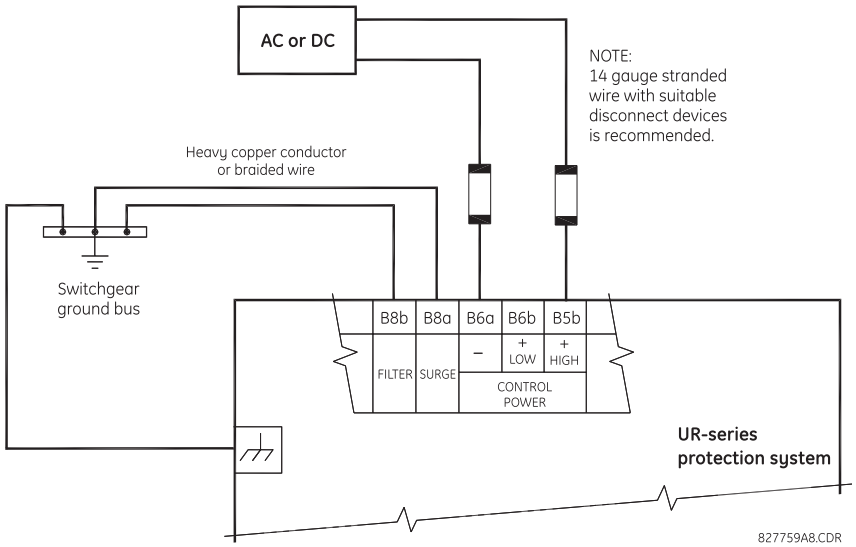


Figure 3–12: CONTROL POWER CONNECTION

3.2.4 CT/VT MODULES

A CT/VT module may have voltage inputs on channels 1 through 4 inclusive, or channels 5 through 8 inclusive. Channels 1 and 5 are intended for connection to phase A, and are labeled as such in the relay. Likewise, channels 2 and 6 are intended for connection to phase B, and channels 3 and 7 are intended for connection to phase C.

Channels 4 and 8 are intended for connection to a single-phase source. For voltage inputs, these channel are labelled as auxiliary voltage (VX). For current inputs, these channels are intended for connection to a CT between system neutral and ground, and are labelled as ground current (IG).

CAUTION

Verify that the connection made to the relay nominal current of 1 A or 5 A matches the secondary rating of the connected CTs. Unmatched CTs may result in equipment damage or inadequate protection.

CT/VT modules may be ordered with a standard ground current input that is the same as the phase current input. Each AC current input has an isolating transformer and an automatic shorting mechanism that shorts the input when the module is withdrawn from the chassis. There are no internal ground connections on the current inputs. Current transformers with 1 to 50000 A primaries and 1 A or 5 A secondaries may be used.

The above modules are available with enhanced diagnostics. These modules can automatically detect CT/VT hardware failure and take the relay out of service.

CT connections for both ABC and ACB phase rotations are identical as shown in the *Typical wiring diagram*.

The phase voltage channels are used for most metering and protection purposes. The auxiliary voltage channel is used as input for the synchrocheck and volts-per-hertz features.

The L60 uses a special CT/VT module not available on other UR-series relays. This type 8P module has four current inputs and special communications inputs/outputs for interfacing with PLCs. The communications interface requires an external DC source (station battery) to drive inputs/outputs as shown in the *L60 channel communications* section in this chapter.

NOTE

Substitute the tilde "~" symbol with the slot position of the module in the following figure.

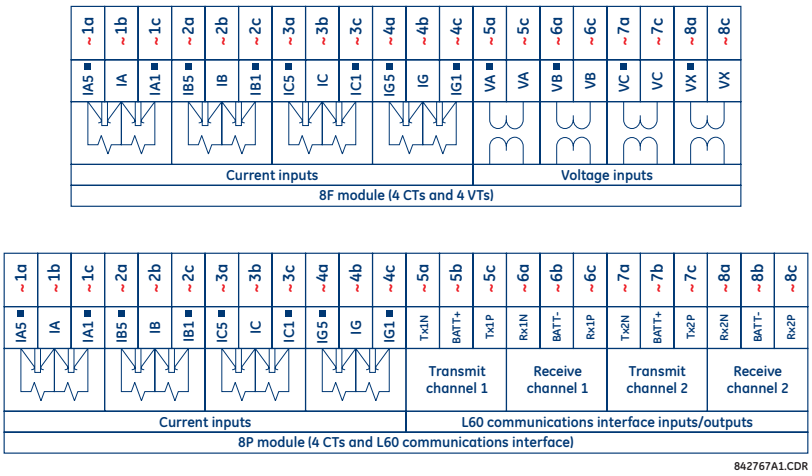


Figure 3–13: CT/VT MODULE WIRING

3.2.5 CONTACT INPUTS/OUTPUTS

Every digital input/output module has 24 terminal connections. They are arranged as three terminals per row, with eight rows in total. A given row of three terminals may be used for the outputs of one relay. For example, for form-C relay outputs, the terminals connect to the normally open (NO), normally closed (NC), and common contacts of the relay. For a form-A output, there are options of using current or voltage detection for feature supervision, depending on the module ordered. The terminal configuration for contact inputs is different for the two applications.

The digital inputs are grouped with a common return. The L60 has two versions of grouping: four inputs per common return and two inputs per common return. When a digital input/output module is ordered, four inputs per common is used. The four inputs per common allows for high-density inputs in combination with outputs, with a compromise of four inputs sharing one common. If the inputs must be isolated per row, then two inputs per common return should be selected (4D module).

The tables and diagrams on the following pages illustrate the module types (6A, etc.) and contact arrangements that may be ordered for the relay. Since an entire row is used for a single contact output, the name is assigned using the module slot position and row number. However, since there are two contact inputs per row, these names are assigned by module slot position, row number, and column position.

Some form-A / solid-state relay outputs include circuits to monitor the DC voltage across the output contact when it is open, and the DC current through the output contact when it is closed. Each of the monitors contains a level detector whose output is set to logic “On = 1” when the current in the circuit is above the threshold setting. The voltage monitor is set to “On = 1” when the current is above about 1 to 2.5 mA, and the current monitor is set to “On = 1” when the current exceeds about 80 to 100 mA. The voltage monitor is intended to check the health of the overall trip circuit, and the current monitor can be used to seal-in the output contact until an external contact has interrupted current flow.

Block diagrams are shown below for form-A and form-A / solid-state relay outputs with optional voltage monitor, optional current monitor, and with no monitoring

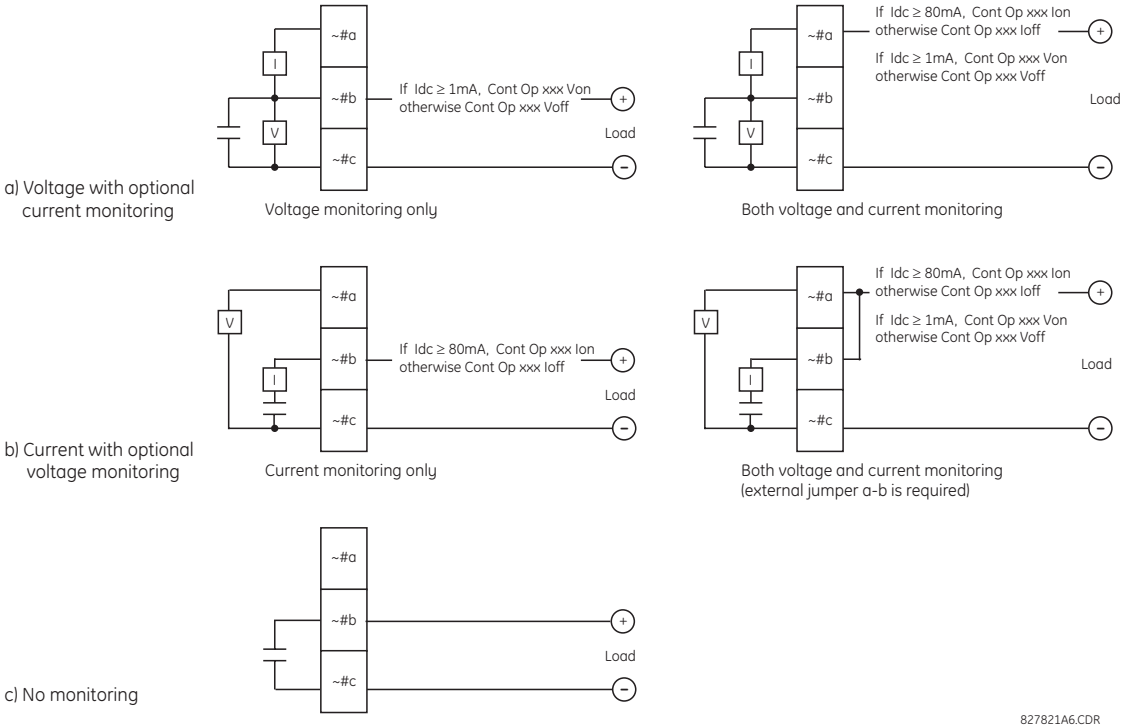


Figure 3–14: FORM-A CONTACT FUNCTIONS

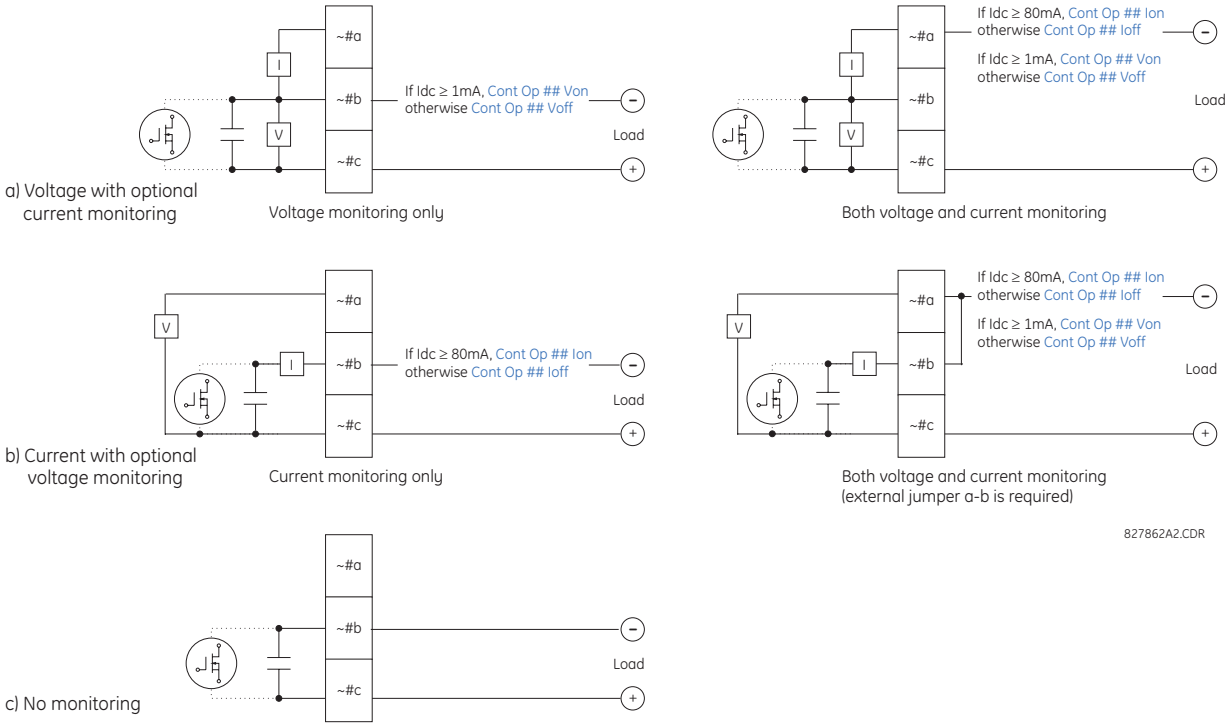


Figure 3–15: FORM-A / SOLID STATE CONTACT FUNCTIONS

The operation of voltage and current monitors is reflected with the corresponding FlexLogic™ operands (Cont Op # Von, Cont Op # Voff, Cont Op # Ion, and Cont Op # Ioff) which can be used in protection, control and alarm logic. The typical application of the voltage monitor is breaker trip circuit integrity monitoring; a typical application of the current monitor is seal-in of the control command. Refer to the *Digital elements* section of chapter 5 for an example of how Form-A/SSR contacts can be applied for breaker trip circuit integrity monitoring.

WARNING

Relay contacts must be considered unsafe to touch when the unit is energized! If the relay contacts need to be used for low voltage accessible applications, it is the customer's responsibility to ensure proper insulation levels!

NOTE

USE OF FORM-A/SSR OUTPUTS IN HIGH IMPEDANCE CIRCUITS

For Form-A/SSR output contacts internally equipped with a voltage measuring cIrcuit across the contact, the circuit has an impedance that can cause a problem when used in conjunction with external high input impedance monitoring equipment such as modern relay test set trigger circuits. These monitoring circuits may continue to read the Form-A contact as being closed after it has closed and subsequently opened, when measured as an impedance.

The solution to this problem is to use the voltage measuring trigger input of the relay test set, and connect the Form-A contact through a voltage-dropping resistor to a DC voltage source. If the 48 V DC output of the power supply is used as a source, a 500 Ω, 10 W resistor is appropriate. In this configuration, the voltage across either the Form-A contact or the resistor can be used to monitor the state of the output.

NOTE

Wherever a tilde "~" symbol appears, substitute with the slot position of the module; wherever a number sign "#" appears, substitute the contact number

NOTE

When current monitoring is used to seal-in the Form-A/SSR contact outputs, the FlexLogic™ operand driving the contact output should be given a reset delay of 10 ms to prevent damage of the output contact (in situations when the element initiating the contact output is bouncing, at values in the region of the pickup value).

Table 3–2: DIGITAL INPUT/OUTPUT MODULE ASSIGNMENTS

~6A MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6B MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5	Form-C
~6	Form-C
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6C MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Form-C
~2	Form-C
~3	Form-C
~4	Form-C
~5	Form-C
~6	Form-C
~7	Form-C
~8	Form-C

~6D MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1a, ~1c	2 Inputs
~2a, ~2c	2 Inputs
~3a, ~3c	2 Inputs
~4a, ~4c	2 Inputs
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6E MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-C
~2	Form-C
~3	Form-C
~4	Form-C
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6F MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Fast Form-C
~2	Fast Form-C
~3	Fast Form-C
~4	Fast Form-C
~5	Fast Form-C
~6	Fast Form-C
~7	Fast Form-C
~8	Fast Form-C

~6G MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6H MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5	Form-A
~6	Form-A
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6K MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Form-C
~2	Form-C
~3	Form-C
~4	Form-C
~5	Fast Form-C
~6	Fast Form-C
~7	Fast Form-C
~8	Fast Form-C

~6L MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6M MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5	Form-C
~6	Form-C
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6N MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6P MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5	Form-A
~6	Form-A
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6R MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6S MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5	Form-C
~6	Form-C
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6T MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6U MODULE	
TERMINAL ASSIGNMENT	OUTPUT OR INPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5	Form-A
~6	Form-A
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~67 MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5	Form-A
~6	Form-A
~7	Form-A
~8	Form-A

~4A MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Not Used
~2	Solid-State
~3	Not Used
~4	Solid-State
~5	Not Used
~6	Solid-State
~7	Not Used
~8	Solid-State

~4B MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Not Used
~2	Solid-State
~3	Not Used
~4	Solid-State
~5	Not Used
~6	Solid-State
~7	Not Used
~8	Solid-State

~4C MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	Not Used
~2	Solid-State
~3	Not Used
~4	Solid-State
~5	Not Used
~6	Solid-State
~7	Not Used
~8	Solid-State

~4D MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1a, ~1c	2 Inputs
~2a, ~2c	2 Inputs
~3a, ~3c	2 Inputs
~4a, ~4c	2 Inputs
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~4L MODULE	
TERMINAL ASSIGNMENT	OUTPUT
~1	2 Outputs
~2	2 Outputs
~3	2 Outputs
~4	2 Outputs
~5	2 Outputs
~6	2 Outputs
~7	2 Outputs
~8	Not Used

Figure 3–16: DIGITAL INPUT/OUTPUT MODULE WIRING (1 of 2)

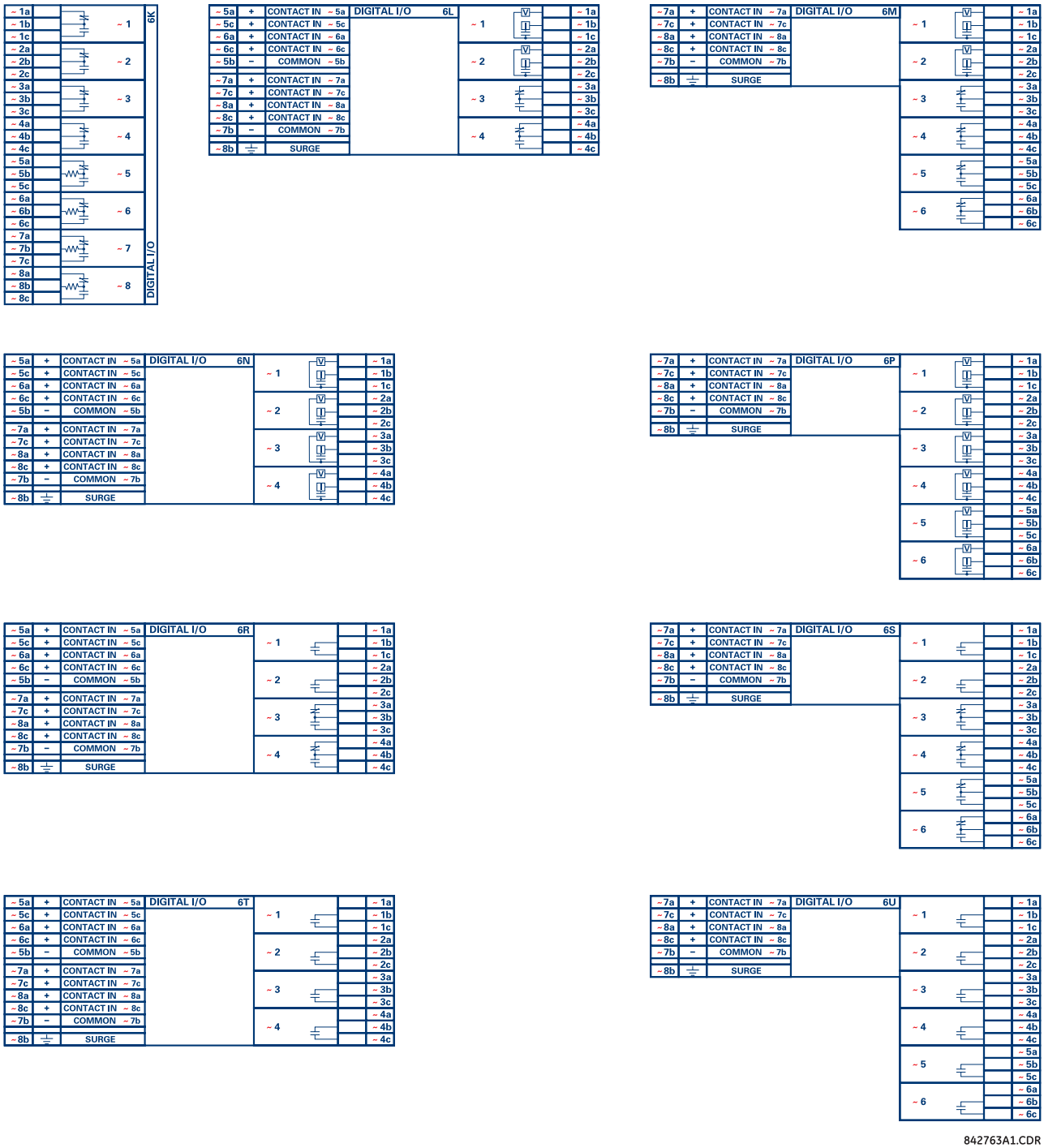


Figure 3–17: DIGITAL INPUT/OUTPUT MODULE WIRING (2 of 2)

CAUTION

CORRECT POLARITY MUST BE OBSERVED FOR ALL CONTACT INPUT AND SOLID STATE OUTPUT CONNECTIONS FOR PROPER FUNCTIONALITY.

CONTACT INPUTS:

A dry contact has one side connected to terminal B3b. This is the positive 48 V DC voltage rail supplied by the power supply module. The other side of the dry contact is connected to the required contact input terminal. Each contact input group has its own common (negative) terminal which must be connected to the DC negative terminal (B3a) of the power supply module. When a dry contact closes, a current of 1 to 3 mA will flow through the associated circuit.

A wet contact has one side connected to the positive terminal of an external DC power supply. The other side of this contact is connected to the required contact input terminal. If a wet contact is used, then the negative side of the external source must be connected to the relay common (negative) terminal of each contact group. The maximum external source voltage for this arrangement is 300 V DC.

The voltage threshold at which each group of four contact inputs will detect a closed contact input is programmable as 17 V DC for 24 V sources, 33 V DC for 48 V sources, 84 V DC for 110 to 125 V sources, and 166 V DC for 250 V sources.

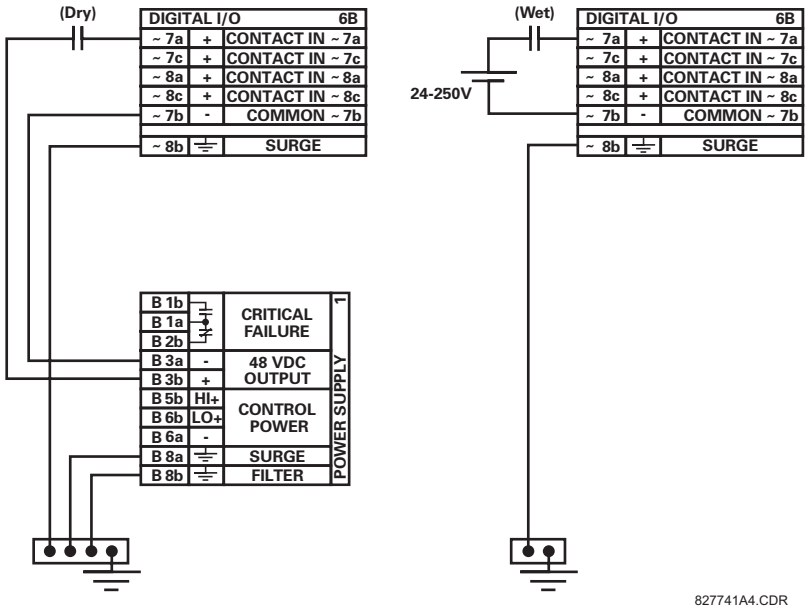


Figure 3–18: DRY AND WET CONTACT INPUT CONNECTIONS

NOTE

Wherever a tilde "~" symbol appears, substitute with the Slot Position of the module.

CONTACT OUTPUTS:

Contact outputs may be ordered as Form-A or Form-C. The Form A contacts may be connected for external circuit supervision. These contacts are provided with voltage and current monitoring circuits used to detect the loss of DC voltage in the circuit, and the presence of DC current flowing through the contacts when the Form-A contact closes. If enabled, the current monitoring can be used as a seal-in signal to ensure that the Form-A contact does not attempt to break the energized inductive coil circuit and weld the output contacts.

NOTE

There is no provision in the relay to detect a DC ground fault on 48 V DC control power external output. We recommend using an external DC supply.

USE OF CONTACT INPUTS WITH AUTO-BURNISHING:

The contact inputs sense a change of the state of the external device contact based on the measured current. When external devices are located in a harsh industrial environment (either outdoor or indoor), their contacts can be exposed to various types of contamination. Normally, there is a thin film of insulating sulfidation, oxidation, or contaminates on the surface of the contacts, sometimes making it difficult or impossible to detect a change of the state. This film must be removed to establish circuit continuity – an impulse of higher than normal current can accomplish this.

The contact inputs with auto-burnish create a high current impulse when the threshold is reached to burn off this oxidation layer as a maintenance to the contacts. Afterwards the contact input current is reduced to a steady-state current. The impulse will have a 5 second delay after a contact input changes state.

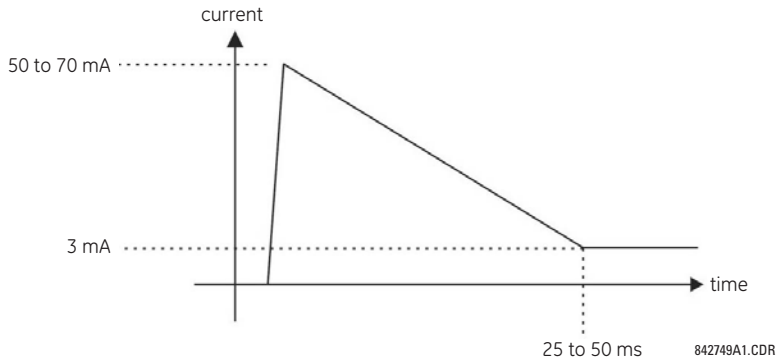


Figure 3–19: CURRENT THROUGH CONTACT INPUTS WITH AUTO-BURNISHING

Regular contact inputs limit current to less than 3 mA to reduce station battery burden. In contrast, contact inputs with auto-burnishing allow currents up to 50 to 70 mA at the first instance when the change of state was sensed. Then, within 25 to 50 ms, this current is slowly reduced to 3 mA as indicated above. The 50 to 70 mA peak current burns any film on the contacts, allowing for proper sensing of state changes. If the external device contact is bouncing, the auto-burnishing starts when external device contact bouncing is over.

Another important difference between the auto-burnishing input module and the regular input modules is that only two contact inputs have common ground, as opposed to four contact inputs sharing one common ground (refer to the *Digital Input/Output Module Wiring* diagrams). This is beneficial when connecting contact inputs to separate voltage sources. Consequently, the threshold voltage setting is also defined per group of two contact inputs.

The auto-burnish feature can be disabled or enabled using the DIP switches found on each daughter card. There is a DIP switch for each contact, for a total of 16 inputs.

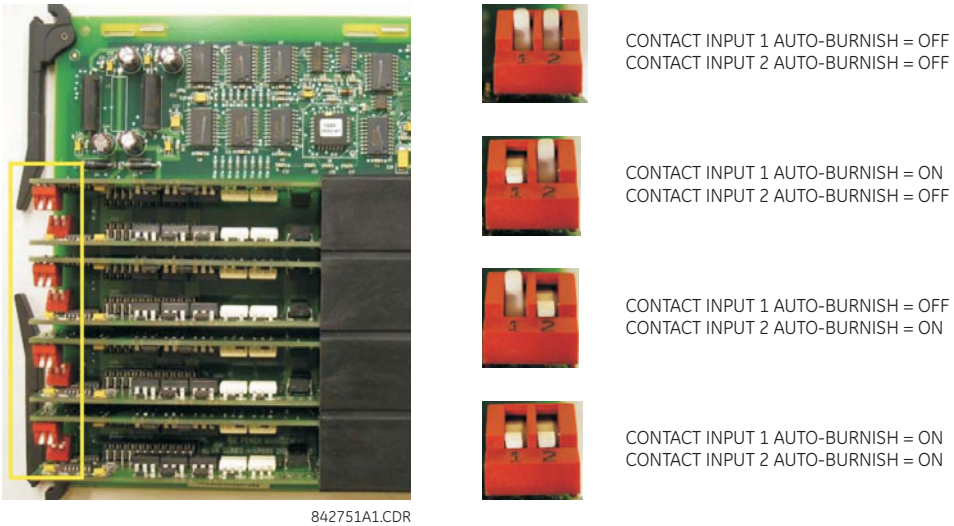


Figure 3–20: AUTO-BURNISH DIP SWITCHES

NOTE

The auto-burnish circuitry has an internal fuse for safety purposes. During regular maintenance, the auto-burnish functionality can be checked using an oscilloscope.

3.2.6 TRANSDUCER INPUTS/OUTPUTS

Transducer input modules can receive input signals from external dcmA output transducers (dcmA In) or resistance temperature detectors (RTD). Hardware and software is provided to receive signals from these external transducers and convert these signals into a digital format for use as required.

Transducer output modules provide DC current outputs in several standard dcmA ranges. Software is provided to configure virtually any analog quantity used in the relay to drive the analog outputs.

Every transducer input/output module has a total of 24 terminal connections. These connections are arranged as three terminals per row with a total of eight rows. A given row may be used for either inputs or outputs, with terminals in column "a" having positive polarity and terminals in column "c" having negative polarity. Since an entire row is used for a single input/output channel, the name of the channel is assigned using the module slot position and row number.

Each module also requires that a connection from an external ground bus be made to Terminal 8b. The current outputs require a twisted-pair shielded cable, where the shield is grounded at one end only. The figure below illustrates the transducer module types (5A, 5C, 5D, 5E, and 5F) and channel arrangements that may be ordered for the relay.

NOTE **Wherever a tilde "~" symbol appears, substitute with the Slot Position of the module.**

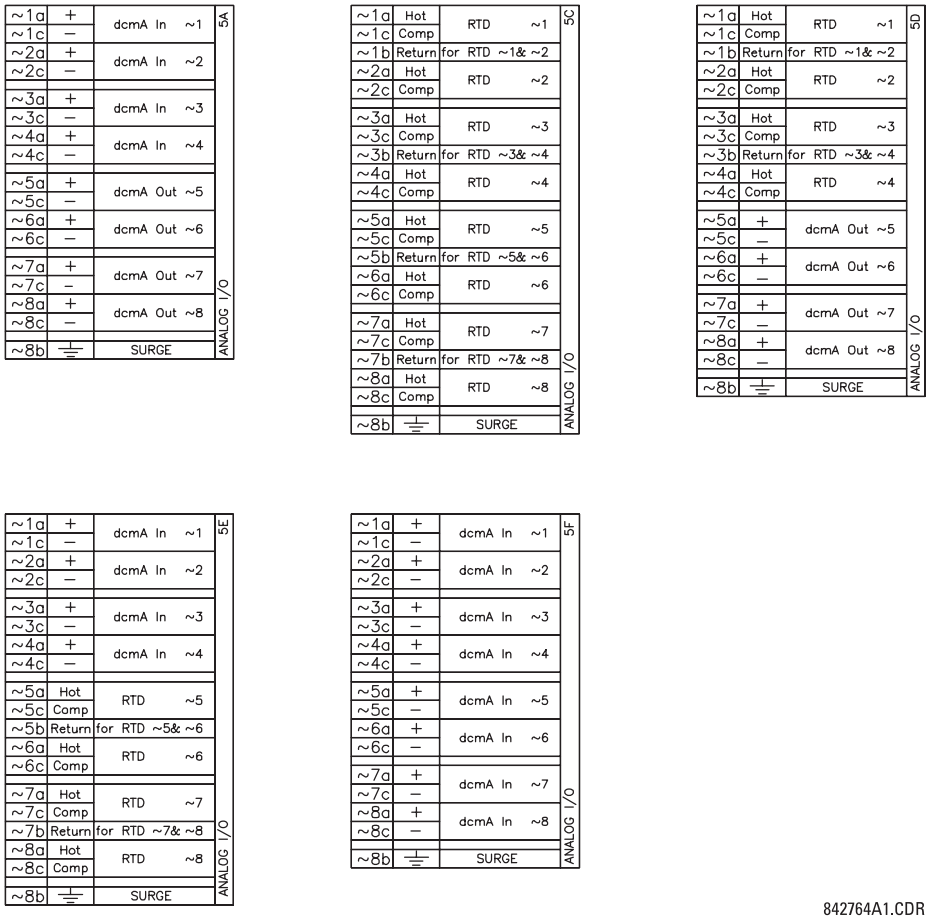


Figure 3–21: TRANSDUCER INPUT/OUTPUT MODULE WIRING

3.2.7 RS232 FACEPLATE PORT

A 9-pin RS232C serial port is located on the relay's faceplate for programming with a portable (personal) computer. All that is required to use this interface is a personal computer running the EnerVista UR Setup software provided with the relay. Cabling for the RS232 port is shown in the following figure for both 9 pin and 25 pin connectors.

NOTE

The baud rate for this port is fixed at **19200 bps**.

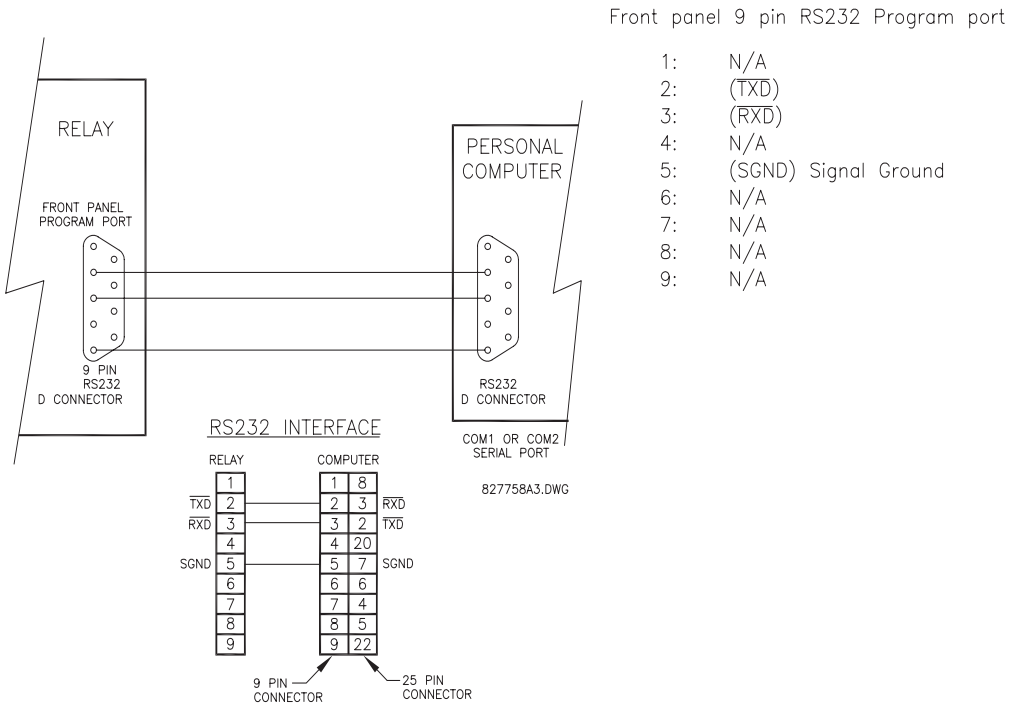


Figure 3–22: RS232 FACEPLATE PORT CONNECTION

3.2.8 CPU COMMUNICATION PORTS

a) OPTIONS

In addition to the RS232 port on the faceplate, the relay provides the user with two additional communication port(s) depending on the CPU module installed.

NOTE

The CPU modules do not require a surge ground connection.

CPU TYPE	COM1	COM2
9E	RS485	RS485
9G	10Base-F and 10Base-T	RS485
9H	Redundant 10Base-F	RS485
9J	100Base-FX	RS485
9K	Redundant 100Base-FX	RS485
9L	100Base-FX	RS485
9M	Redundant 100Base-FX	RS485
9N	10/100Base-T	RS485
9P	100Base-FX	RS485
9R	Redundant 100Base-FX	RS485

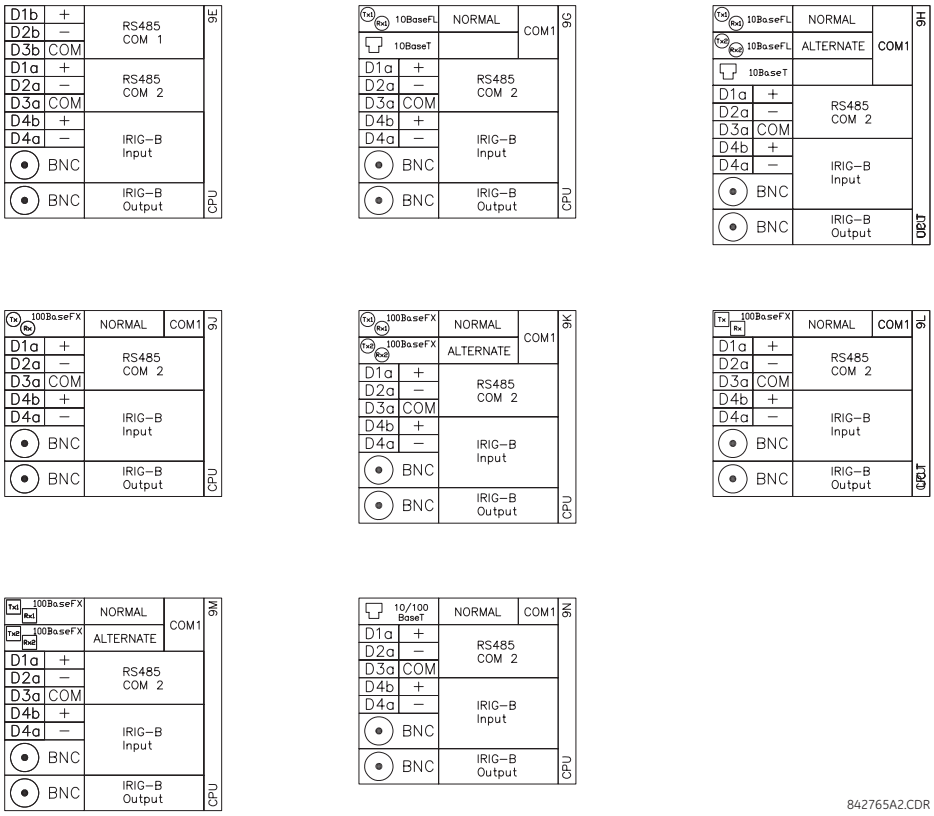


Figure 3–23: CPU MODULE COMMUNICATIONS WIRING

b) RS485 PORTS

RS485 data transmission and reception are accomplished over a single twisted pair with transmit and receive data alternating over the same two wires. Through the use of these port(s), continuous monitoring and control from a remote computer, SCADA system or PLC is possible.

To minimize errors from noise, the use of shielded twisted pair wire is recommended. Correct polarity must also be observed. For instance, the relays must be connected with all RS485 "+" terminals connected together, and all RS485 "–" terminals connected together. The COM terminal should be connected to the common wire inside the shield, when provided. To avoid loop currents, the shield should be grounded at one point only. Each relay should also be daisy chained to the next one in the link. A maximum of 32 relays can be connected in this manner without exceeding driver capability. For larger systems, additional serial channels must be added. It is also possible to use commercially available repeaters to increase the number of relays on a single channel to more than 32. Star or stub connections should be avoided entirely.

Lightning strikes and ground surge currents can cause large momentary voltage differences between remote ends of the communication link. For this reason, surge protection devices are internally provided at both communication ports. An isolated power supply with an optocoupled data interface also acts to reduce noise coupling. To ensure maximum reliability, all equipment should have similar transient protection devices installed.

Both ends of the RS485 circuit should also be terminated with an impedance as shown below.

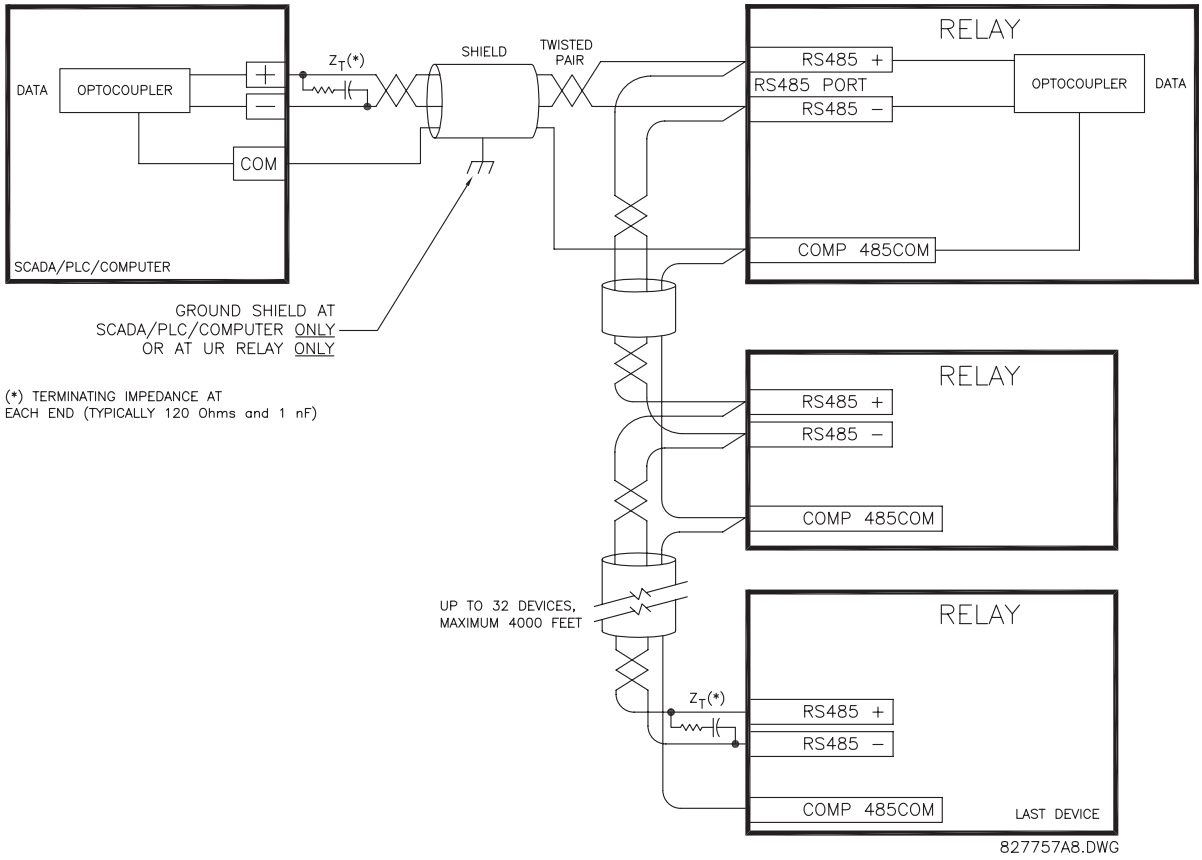


Figure 3–24: RS485 SERIAL CONNECTION

c) 10BASE-FL AND 100BASE-FX FIBER OPTIC PORTS

CAUTION

ENSURE THE DUST COVERS ARE INSTALLED WHEN THE FIBER IS NOT IN USE. DIRTY OR SCRATCHED CONNECTORS CAN LEAD TO HIGH LOSSES ON A FIBER LINK.

CAUTION

OBSERVING ANY FIBER TRANSMITTER OUTPUT MAY CAUSE INJURY TO THE EYE.

The fiber optic communication ports allow for fast and efficient communications between relays at 10 or 100Mbps. Optical fiber may be connected to the relay supporting a wavelength of 820 nm in multi-mode or 1310 nm in multi-mode and single-mode. The 10 Mbps rate is available for CPU modules 9G and 9H; 100Mbps is available for modules 9J, 9K, 9L, and 9M. The 9H, 9K and 9M modules have a second pair of identical optical fiber transmitter and receiver for redundancy.

The optical fiber sizes supported include 50/125 µm, 62.5/125 µm and 100/140 µm for 10 Mbps. The fiber optic port is designed such that the response times will not vary for any core that is 100 µm or less in diameter, 62.5 µm for 100 Mbps. For optical power budgeting, splices are required every 1 km for the transmitter/receiver pair. When splicing optical fibers, the diameter and numerical aperture of each fiber must be the same. In order to engage or disengage the ST type connector, only a quarter turn of the coupling is required.

3.2.9 IRIG-B

IRIG-B is a standard time code format that allows stamping of events to be synchronized among connected devices within 1 millisecond. The IRIG time code formats are serial, width-modulated codes which can be either DC level shifted or amplitude modulated (AM). Third party equipment is available for generating the IRIG-B signal; this equipment may use a GPS satellite system to obtain the time reference so that devices at different geographic locations can also be synchronized.

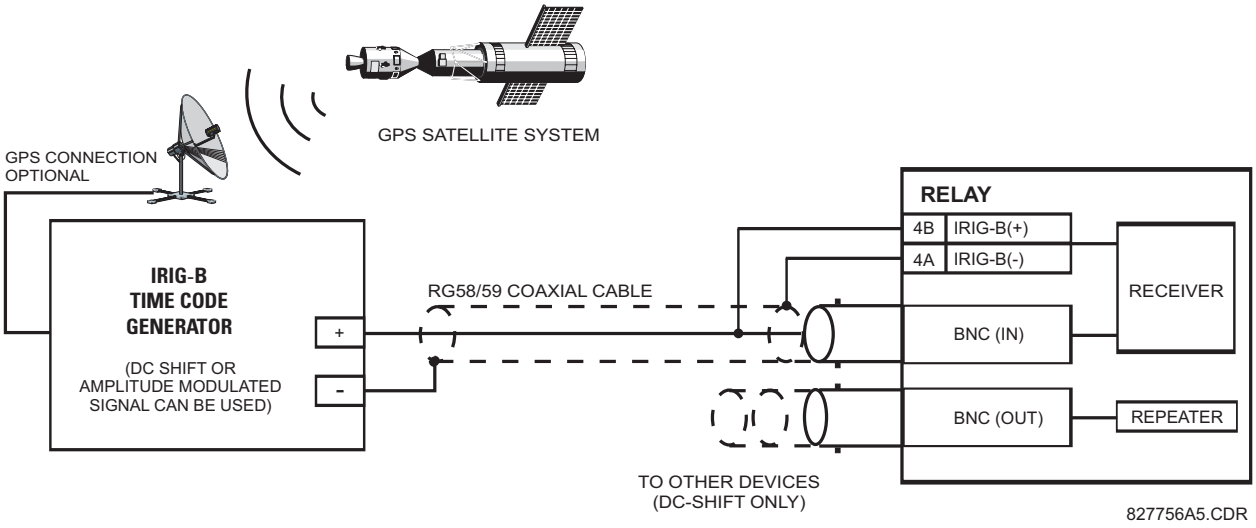


Figure 3–25: IRIG-B CONNECTION

The IRIG-B repeater provides an amplified DC-shift IRIG-B signal to other equipment. By using one IRIG-B serial connection, several UR-series relays can be synchronized. The IRIG-B repeater has a bypass function to maintain the time signal even when a relay in the series is powered down.

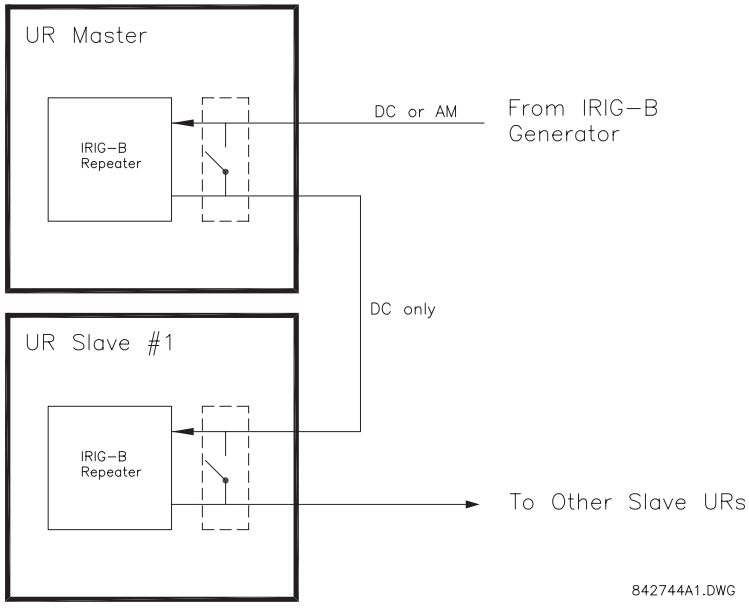


Figure 3–26: IRIG-B REPEATER

NOTE

Using an amplitude modulated receiver will cause errors in event time-stamping.

3.2.10 L60 CHANNEL COMMUNICATIONS

As described earlier in this chapter, L60 communications channels reside on the special CT/VT module (type 8P). This module allows for all possible 87PC scheme combinations (such as dual phase comparison or single-phase comparison, two-terminal or three-terminal applications) in one module. The customer can upgrade or change the scheme at any time. The L60 channel interface requires an external battery to drive inputs and outputs. The module can be used with any battery voltage. However, the battery voltage must be reflected in the **CONTROL ELEMENTS ⇨⇩ PHASE COMPARISON ELEMENTS ⇨ 87PC SCHEME ⇨⇩ 87PC CH1(2) RX VOLT** settings, which define the acceptable voltage threshold received from the PLC. The L60 communications outputs are MOSFETs and inputs are implemented with optocouplers, excluding any galvanic connection between PLC connections and the relay boards.

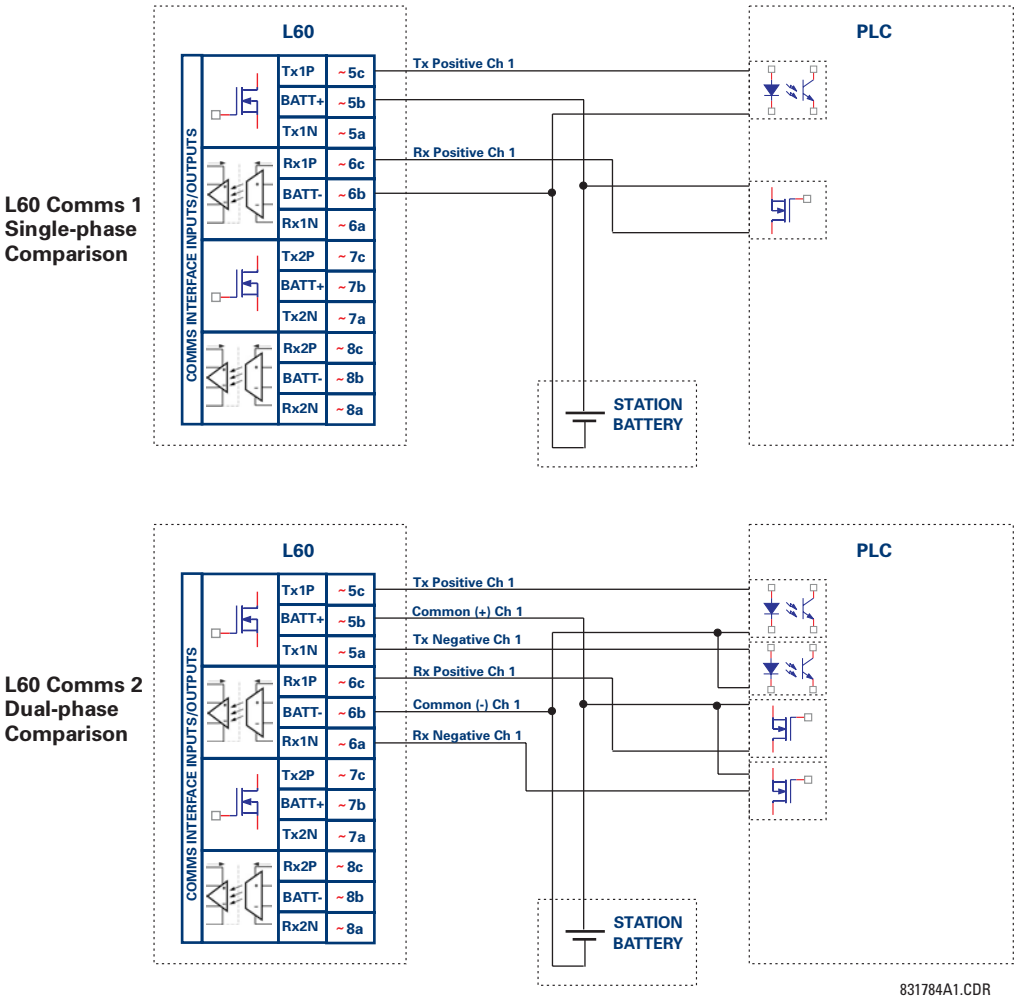


Figure 3–27: L60 TO PLC CONNECTIONS FOR A TWO-TERMINAL LINE

The communications circuitry has the following characteristics for the transmitter and receiver.

Transmitter characteristics:

Operating voltage range: 0 to 300 V DC (typical points: 15 V, 48 V, 125 V, 250 V)
Output current limitation: 100 mA (maximum), 30 mA (nominal)

Receiver characteristics:

Input voltage range: 0 to 300 V DC
Input impedance: 25 kΩ
Input current: 10 mA at 250 V, 5 mA at 125 V, 2 mA at 48 V

3.3.1 DESCRIPTION

The L60 direct inputs/outputs feature makes use of the type 7 series of communications modules. These modules are also used by the L90 Line Differential Relay for inter-relay communications. The direct input/output feature uses the communications channel(s) provided by these modules to exchange digital state information between relays. This feature is available on all UR-series relay models except for the L90 Line Differential relay.

The communications channels are normally connected in a ring configuration as shown below. The transmitter of one module is connected to the receiver of the next module. The transmitter of this second module is then connected to the receiver of the next module in the ring. This is continued to form a communications ring. The figure below illustrates a ring of four UR-series relays with the following connections: UR1-Tx to UR2-Rx, UR2-Tx to UR3-Rx, UR3-Tx to UR4-Rx, and UR4-Tx to UR1-Rx. A maximum of sixteen (16) UR-series relays can be connected in a single ring

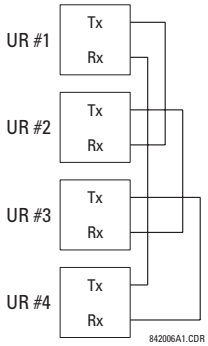


Figure 3–28: DIRECT INPUT/OUTPUT SINGLE CHANNEL CONNECTION

The interconnection for dual-channel Type 7 communications modules is shown below. Two channel modules allow for a redundant ring configuration. That is, two rings can be created to provide an additional independent data path. The required connections are: UR1-Tx1 to UR2-Rx1, UR2-Tx1 to UR3-Rx1, UR3-Tx1 to UR4-Rx1, and UR4-Tx1 to UR1-Rx1 for the first ring; and UR1-Tx2 to UR4-Rx2, UR4-Tx2 to UR3-Rx2, UR3-Tx2 to UR2-Rx2, and UR2-Tx2 to UR1-Rx2 for the second ring.

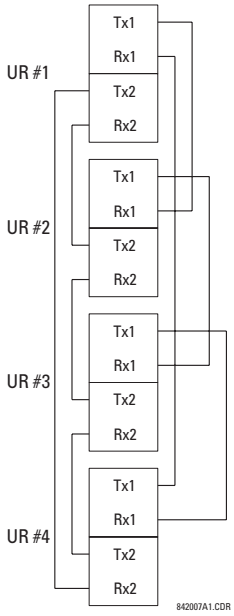


Figure 3–29: DIRECT INPUT/OUTPUT DUAL CHANNEL CONNECTION

The following diagram shows the connection for three UR-series relays using two independent communication channels. UR1 and UR3 have single Type 7 communication modules; UR2 has a dual-channel module. The two communication channels can be of different types, depending on the Type 7 modules used. To allow the direct input/output data to 'crossover' from Channel 1 to Channel 2 on UR2, the **DIRECT I/O CHANNEL CROSSOVER** setting should be "Enabled" on UR2. This forces UR2 to forward messages received on Rx1 out Tx2, and messages received on Rx2 out Tx1.

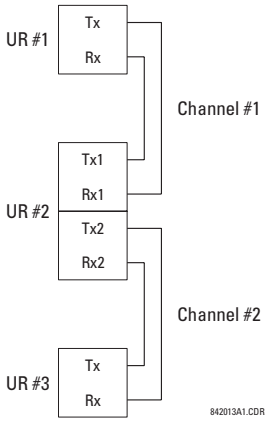


Figure 3–30: DIRECT INPUT/OUTPUT SINGLE/DUAL CHANNEL COMBINATION CONNECTION

The interconnection requirements are described in further detail in this section for each specific variation of Type 7 communications module. These modules are listed in the following table. All fiber modules use ST type connectors.

Table 3–3: CHANNEL COMMUNICATION OPTIONS

MODULE	SPECIFICATION
2A	C37.94SM, 1300 nm, single-mode, ELED, 1 channel single-mode
2B	C37.94SM, 1300 nm, single-mode, ELED, 2 channel single-mode
7A	820 nm, multi-mode, LED, 1 channel
7B	1300 nm, multi-mode, LED, 1 channel
7C	1300 nm, single-mode, ELED, 1 channel
7D	1300 nm, single-mode, LASER, 1 channel
7E	Channel 1: G.703, Channel 2: 820 nm, multi-mode
7F	Channel 1: G.703, Channel 2: 1300 nm, multi-mode
7G	Channel 1: G.703, Channel 2: 1300 nm, single-mode ELED
7H	820 nm, multi-mode, LED, 2 channels
7I	1300 nm, multi-mode, LED, 2 channels
7J	1300 nm, single-mode, ELED, 2 channels
7K	1300 nm, single-mode, LASER, 2 channels
7L	Channel 1: RS422, Channel 2: 820 nm, multi-mode, LED
7M	Channel 1: RS422, Channel 2: 1300 nm, multi-mode, LED
7N	Channel 1: RS422, Channel 2: 1300 nm, single-mode, ELED
7P	Channel 1: RS422, Channel 2: 1300 nm, single-mode, LASER
7Q	Channel 1: G.703, Channel 2: 1300 nm, single-mode, LASER
7R	G.703, 1 channel
7S	G.703, 2 channels
7T	RS422, 1 channel
7V	RS422, 2 channels, 2 clock inputs
7W	RS422, 2 channels
72	1550 nm, single-mode, LASER, 1 channel
73	1550 nm, single-mode, LASER, 2 channels
74	Channel 1 - RS422; Channel 2 - 1550 nm, single-mode, LASER
75	Channel 1 - G.703; Channel 2 - 1550 nm, single-mode, LASER
76	IEEE C37.94, 820 nm, multi-mode, LED, 1 channel
77	IEEE C37.94, 820 nm, multi-mode, LED, 2 channels

CAUTION

OBSERVING ANY FIBER TRANSMITTER OUTPUT MAY CAUSE INJURY TO THE EYE.

3.3.2 FIBER: LED AND ELED TRANSMITTERS

The following figure shows the configuration for the 7A, 7B, 7C, 7H, 7I, and 7J fiber-only modules.

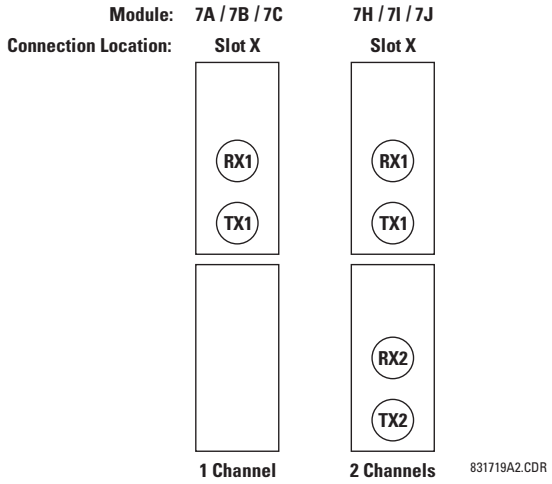


Figure 3–31: LED AND ELED FIBER MODULES

3.3.3 FIBER-LASER TRANSMITTERS

The following figure shows the configuration for the 72, 73, 7D, and 7K fiber-laser module.

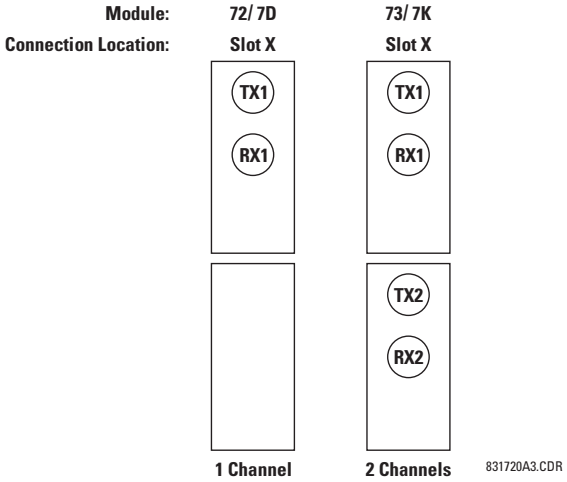


Figure 3–32: LASER FIBER MODULES

WARNING

When using a LASER Interface, attenuators may be necessary to ensure that you do not exceed Maximum Optical Input Power to the receiver.

a) DESCRIPTION

The following figure shows the 64K ITU G.703 co-directional interface configuration.

NOTE

The G.703 module is fixed at 64 kbps. The SETTINGS ⇨ PRODUCT SETUP ⇨⇩ DIRECT I/O ⇨⇩ DIRECT I/O DATA RATE setting is not applicable to this module.

AWG 24 twisted shielded pair is recommended for external connections, with the shield grounded only at one end. Connecting the shield to pin X1a or X6a grounds the shield since these pins are internally connected to ground. Thus, if pin X1a or X6a is used, do not ground at the other end. This interface module is protected by surge suppression devices.

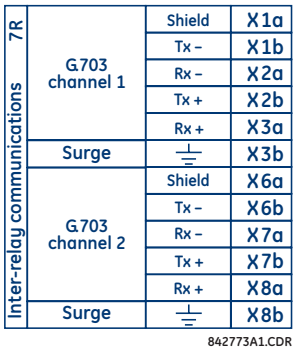


Figure 3–33: G.703 INTERFACE CONFIGURATION

The following figure shows the typical pin interconnection between two G.703 interfaces. For the actual physical arrangement of these pins, see the *Rear terminal assignments* section earlier in this chapter. All pin interconnections are to be maintained for a connection to a multiplexer.

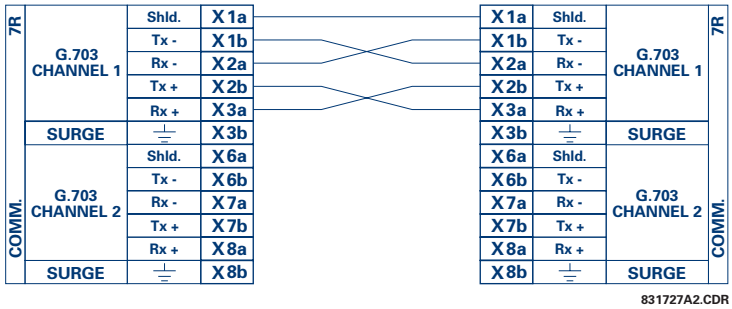


Figure 3–34: TYPICAL PIN INTERCONNECTION BETWEEN TWO G.703 INTERFACES

NOTE

Pin nomenclature may differ from one manufacturer to another. Therefore, it is not uncommon to see pinouts numbered TxA, TxB, RxA and RxB. In such cases, it can be assumed that "A" is equivalent to "+" and "B" is equivalent to "–".

b) G.703 SELECTION SWITCH PROCEDURES

1. Remove the G.703 module (7R or 7S). The ejector/inserter clips located at the top and at the bottom of each module, must be pulled simultaneously in order to release the module for removal. Before performing this action, **control power must be removed from the relay**. The original location of the module should be recorded to help ensure that the same or replacement module is inserted into the correct slot.
2. Remove the module cover screw.
3. Remove the top cover by sliding it towards the rear and then lift it upwards.
4. Set the timing selection switches (channel 1, channel 2) to the desired timing modes.
5. Replace the top cover and the cover screw.

6. Re-insert the G.703 module. Take care to ensure that the **correct** module type is inserted into the **correct** slot position. The ejector/inserter clips located at the top and at the bottom of each module must be in the disengaged position as the module is smoothly inserted into the slot. Once the clips have cleared the raised edge of the chassis, engage the clips simultaneously. When the clips have locked into position, the module will be fully inserted.

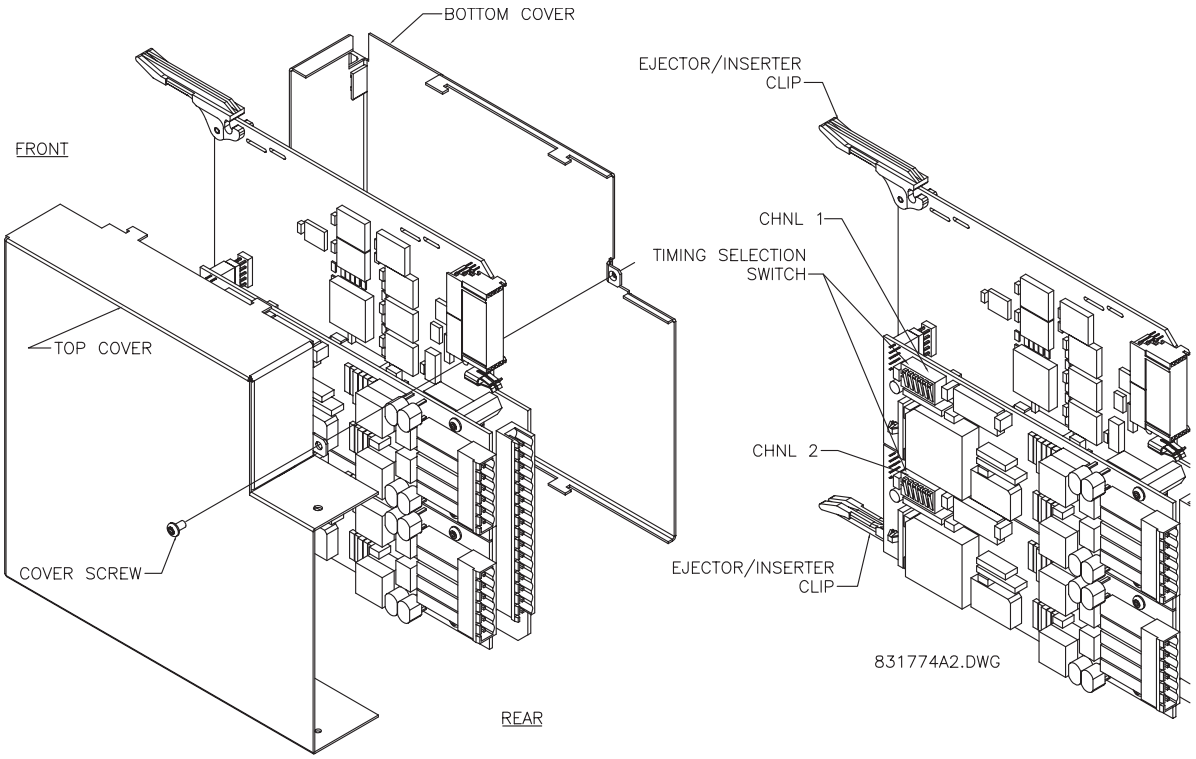


Figure 3–35: G.703 TIMING SELECTION SWITCH SETTING

Table 3–4: G.703 TIMING SELECTIONS

SWITCHES	FUNCTION
S1	OFF → octet timing disabled ON → octet timing 8 kHz
S5 and S6	S5 = OFF and S6 = OFF → loop timing mode S5 = ON and S6 = OFF → internal timing mode S5 = OFF and S6 = ON → minimum remote loopback mode S5 = ON and S6 = ON → dual loopback mode

c) G.703 OCTET TIMING

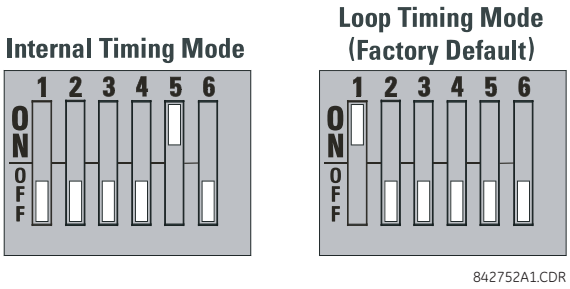
If octet timing is enabled (on), this 8 kHz signal will be asserted during the violation of bit 8 (LSB) necessary for connecting to higher order systems. When L60s are connected back to back, octet timing should be disabled (off).

d) G.703 TIMING MODES

There are two timing modes for the G.703 module: internal timing mode and loop timing mode (default).

- **Internal Timing Mode:** The system clock is generated internally. Therefore, the G.703 timing selection should be in the internal timing mode for back-to-back (UR-to-UR) connections. For back-to-back connections, set for octet timing (S1 = OFF) and timing mode to internal timing (S5 = ON and S6 = OFF).
- **Loop Timing Mode:** The system clock is derived from the received line signal. Therefore, the G.703 timing selection should be in loop timing mode for connections to higher order systems. For connection to a higher order system (UR-to-multiplexer, factory defaults), set to octet timing (S1 = ON) and set timing mode to loop timing (S5 = OFF and S6 = OFF).

The switch settings for the internal and loop timing modes are shown below:



e) G.703 TEST MODES

In *minimum remote loopback* mode, the multiplexer is enabled to return the data from the external interface without any processing to assist in diagnosing G.703 line-side problems irrespective of clock rate. Data enters from the G.703 inputs, passes through the data stabilization latch which also restores the proper signal polarity, passes through the multiplexer and then returns to the transmitter. The differential received data is processed and passed to the G.703 transmitter module after which point the data is discarded. The G.703 receiver module is fully functional and continues to process data and passes it to the differential Manchester transmitter module. Since timing is returned as it is received, the timing source is expected to be from the G.703 line side of the interface.

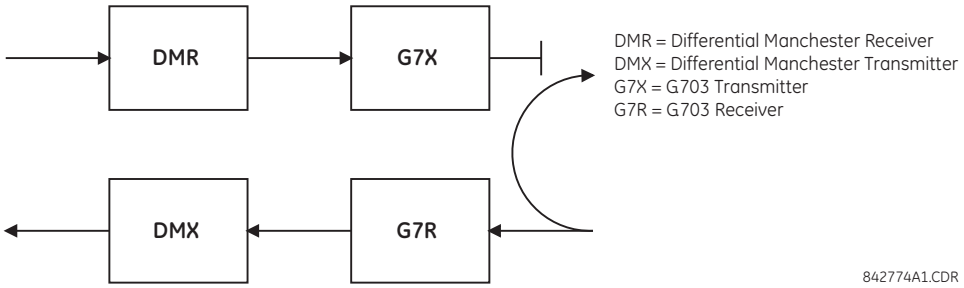


Figure 3–36: G.703 MINIMUM REMOTE LOOPBACK MODE

In *dual loopback mode*, the multiplexers are active and the functions of the circuit are divided into two with each receiver/transmitter pair linked together to deconstruct and then reconstruct their respective signals. Differential Manchester data enters the Differential Manchester receiver module and then is returned to the differential Manchester transmitter module. Likewise, G.703 data enters the G.703 receiver module and is passed through to the G.703 transmitter module to be returned as G.703 data. Because of the complete split in the communications path and because, in each case, the clocks are extracted and reconstructed with the outgoing data, in this mode there must be two independent sources of timing. One source lies on the G.703 line side of the interface while the other lies on the differential Manchester side of the interface.

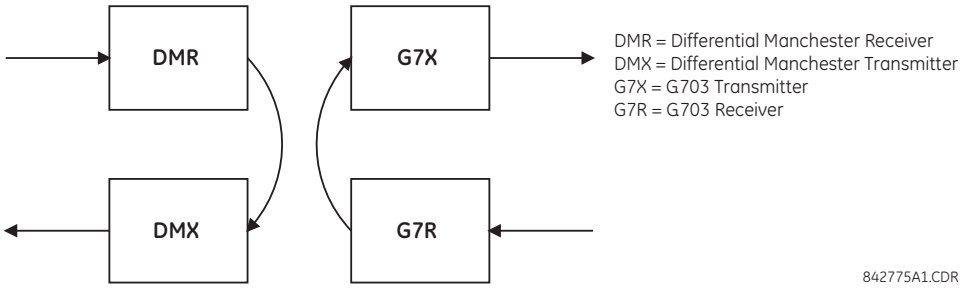


Figure 3–37: G.703 DUAL LOOPBACK MODE

a) DESCRIPTION

There are two RS422 inter-relay communications modules available: single-channel RS422 (module 7T) and dual-channel RS422 (module 7W). The modules can be configured to run at 64 or 128 kbps. AWG 24 twisted shielded pair cable is recommended for external connections. These modules are protected by optically-isolated surge suppression devices.

The shield pins (6a and 7b) are internally connected to the ground pin (8a). Proper shield termination is as follows:

- Site 1: Terminate shield to pins 6a and/or 7b.
- Site 2: Terminate shield to COM pin 2b.

The clock terminating impedance should match the impedance of the line.

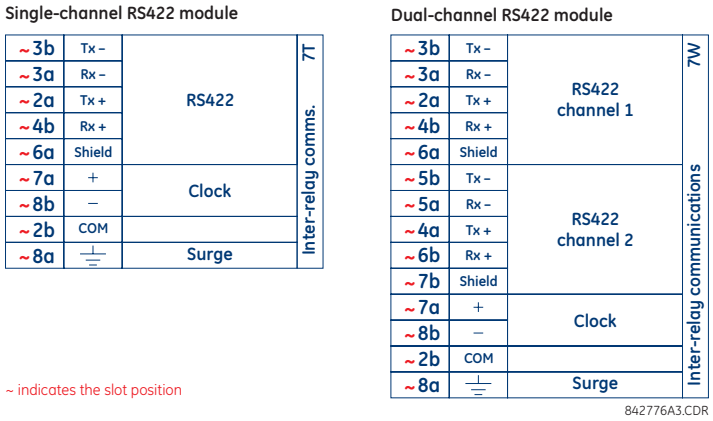


Figure 3–38: RS422 INTERFACE CONNECTIONS

The following figure shows the typical pin interconnection between two single-channel RS422 interfaces installed in slot W. All pin interconnections are to be maintained for a connection to a multiplexer.

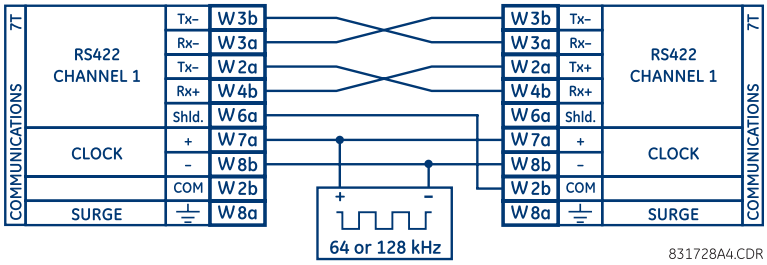


Figure 3–39: TYPICAL PIN INTERCONNECTION BETWEEN TWO RS422 INTERFACES

b) TWO-CHANNEL APPLICATION VIA MULTIPLEXERS

The RS422 interface may be used for single or two channel applications over SONET/SDH and/or multiplexed systems. When used in single-channel applications, the RS422 interface links to higher order systems in a typical fashion observing transmit (Tx), receive (Rx), and send timing (ST) connections. However, when used in two-channel applications, certain criteria must be followed since there is one clock input for the two RS422 channels. The system will function correctly if the following connections are observed and your data module has a terminal timing feature. Terminal timing is a common feature to most synchronous data units that allows the module to accept timing from an external source. Using the terminal timing feature, two channel applications can be achieved if these connections are followed: The send timing outputs from the multiplexer (data module 1), will connect to the clock inputs of the UR–RS422 interface in the usual fashion. In addition, the send timing outputs of data module 1 will also be paralleled to the terminal timing inputs of data module 2. By using this configuration, the timing for both data modules and both UR–RS422 channels will be derived from a single clock source. As a result, data sampling for both of the UR–RS422 channels will be synchronized via the send timing leads on data module 1 as shown below. If the terminal timing feature is not available or this type of connection is not desired, the G.703 interface is a viable option that does not impose timing restrictions.

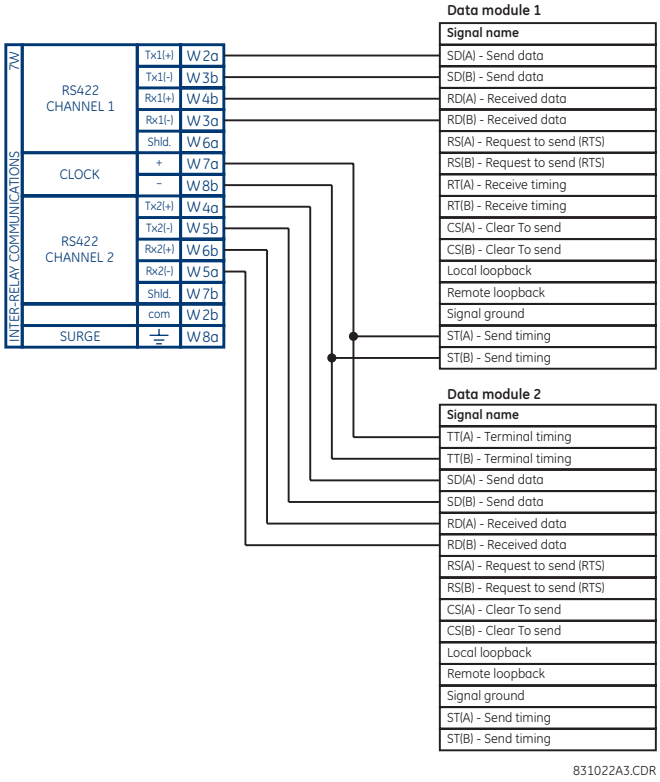


Figure 3–40: TIMING CONFIGURATION FOR RS422 TWO-CHANNEL, 3-TERMINAL APPLICATION

Data module 1 provides timing to the L60 RS422 interface via the ST(A) and ST(B) outputs. Data module 1 also provides timing to data module 2 TT(A) and TT(B) inputs via the ST(A) and AT(B) outputs. The data module pin numbers have been omitted in the figure above since they may vary depending on the manufacturer.

c) TRANSMIT TIMING

The RS422 interface accepts one clock input for transmit timing. It is important that the rising edge of the 64 kHz transmit timing clock of the multiplexer interface is sampling the data in the center of the transmit data window. Therefore, it is important to confirm clock and data transitions to ensure proper system operation. For example, the following figure shows the positive edge of the Tx clock in the center of the Tx data bit.

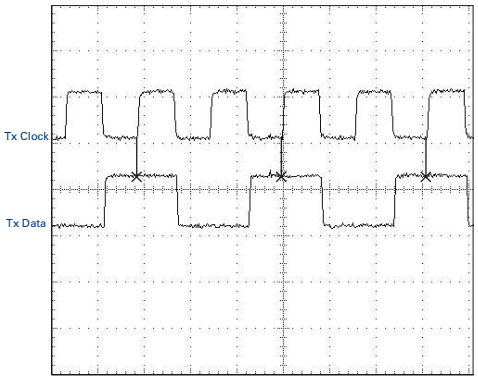


Figure 3–41: CLOCK AND DATA TRANSITIONS

d) RECEIVE TIMING

The RS422 interface utilizes NRZI-MARK modulation code and; therefore, does not rely on an Rx clock to recapture data. NRZI-MARK is an edge-type, invertible, self-clocking code.

To recover the Rx clock from the data-stream, an integrated DPLL (digital phase lock loop) circuit is utilized. The DPLL is driven by an internal clock, which is 16-times over-sampled, and uses this clock along with the data-stream to generate a data clock that can be used as the SCC (serial communication controller) receive clock.

3.3.6 RS422 AND FIBER INTERFACE

The following figure shows the combined RS422 plus Fiber interface configuration at 64K baud. The 7L, 7M, 7N, 7P, and 74 modules are used in two-terminal with a redundant channel or three-terminal configurations where channel 1 is employed via the RS422 interface (possibly with a multiplexer) and channel 2 via direct fiber.

AWG 24 twisted shielded pair is recommended for external RS422 connections and the shield should be grounded only at one end. For the direct fiber channel, power budget issues should be addressed properly.

WARNING

When using a LASER Interface, attenuators may be necessary to ensure that you do not exceed maximum optical input power to the receiver.

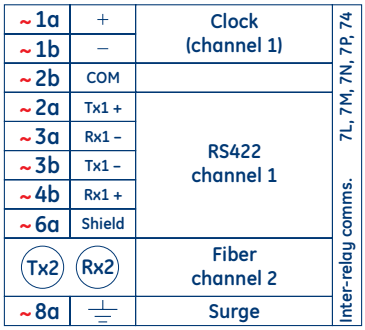


Figure 3–42: RS422 AND FIBER INTERFACE CONNECTION

Connections shown above are for multiplexers configured as DCE (data communications equipment) units.

3.3.7 G.703 AND FIBER INTERFACE

The figure below shows the combined G.703 plus Fiber interface configuration at 64K baud. The 7E, 7F, 7G, 7Q, and 75 modules are used in configurations where Channel 1 is employed via the G.703 interface (possibly with a multiplexer) and Channel 2 via direct fiber. AWG 24 twisted shielded pair is recommended for external G.703 connections connecting the shield to Pin 1A at one end only. For the direct fiber channel, power budget issues should be addressed properly. See previous sections for more details on the G.703 and Fiber interfaces.

WARNING

When using a LASER Interface, attenuators may be necessary to ensure that you do <u>not</u> exceed Maximum Optical Input Power to the receiver.

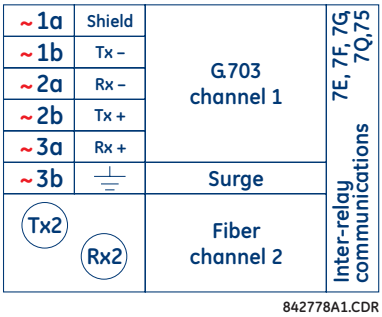


Figure 3–43: G.703 AND FIBER INTERFACE CONNECTION

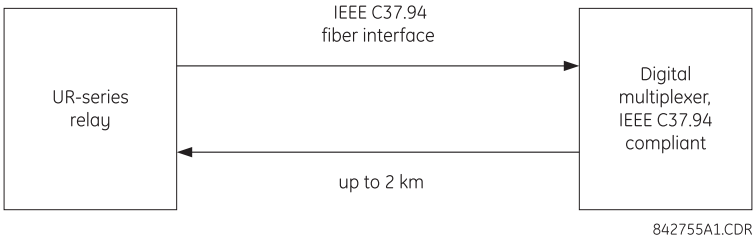
3.3.8 IEEE C37.94 INTERFACE

The UR-series IEEE C37.94 communication modules (76 and 77) are designed to interface with IEEE C37.94 compliant digital multiplexers and/or an IEEE C37.94 compliant interface converter for use with L90 and L90 direct inputs/outputs on version 3.20 and direct input/output applications for firmware revisions 3.30 and higher. The IEEE C37.94 standard defines a point-to-point optical link for synchronous data between a multiplexer and a teleprotection device. This data is typically 64 kbps, but the standard provides for speeds up to 64*n* kbps, where *n* = 1, 2,…, 12. The UR-series C37.94 communication module is 64 kbps only with *n* fixed at 1. The frame is a valid International Telecommunications Union (ITU-T) recommended G.704 pattern from the standpoint of framing and data rate. The frame is 256 bits and is repeated at a frame rate of 8000 Hz, with a resultant bit rate of 2048 kbps.

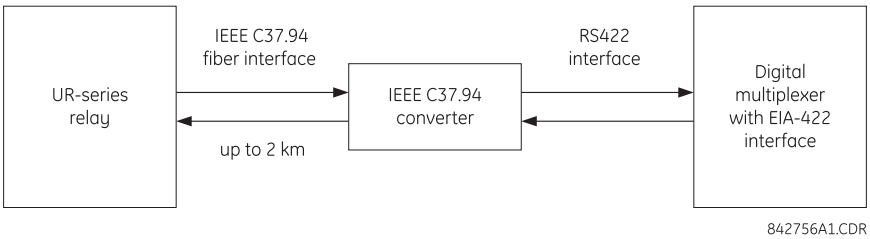
The specifications for the module are as follows:

IEEE standard: C37.94 for 1 × 64 kbps optical fiber interface
Fiber optic cable type: 50 mm or 62.5 mm core diameter optical fiber
Fiber optic mode: multi-mode
Fiber optic cable length: up to 2 km
Fiber optic connector: type ST
Wavelength: 830 ±40 nm
Connection: as per all fiber optic connections, a Tx to Rx connection is required.

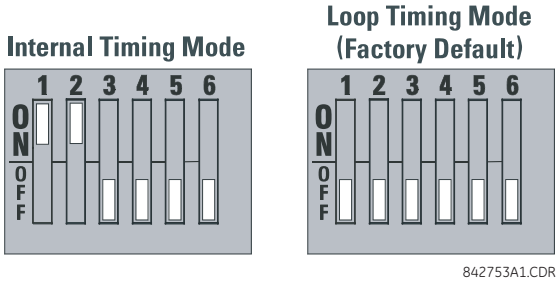
The UR-series C37.94 communication module can be connected directly to any compliant digital multiplexer that supports the IEEE C37.94 standard as shown below.



The UR-series C37.94 communication module can be connected to the electrical interface (G.703, RS422, or X.21) of a non-compliant digital multiplexer via an optical-to-electrical interface converter that supports the IEEE C37.94 standard, as shown below.



The UR-series C37.94 communication module has six (6) switches that are used to set the clock configuration. The functions of these control switches is shown below.



For the Internal Timing Mode, the system clock is generated internally. Therefore, the timing switch selection should be Internal Timing for Relay 1 and Loop Timed for Relay 2. There must be only one timing source configured.

For the Looped Timing Mode, the system clock is derived from the received line signal. Therefore, the timing selection should be in Loop Timing Mode for connections to higher order systems.

The C37.94 communications module cover removal procedure is as follows:

1. Remove the C37.94 module (76 or 77):

   The ejector/inserter clips located at the top and at the bottom of each module, must be pulled simultaneously in order to release the module for removal. Before performing this action, **control power must be removed from the relay**. The original location of the module should be recorded to help ensure that the same or replacement module is inserted into the correct slot.

2. Remove the module cover screw.
3. Remove the top cover by sliding it towards the rear and then lift it upwards.
4. Set the Timing Selection Switches (Channel 1, Channel 2) to the desired timing modes (see description above).
5. Replace the top cover and the cover screw.
6. Re-insert the C37.94 module Take care to ensure that the **correct** module type is inserted into the **correct** slot position. The ejector/inserter clips located at the top and at the bottom of each module must be in the disengaged position as the module is smoothly inserted into the slot. Once the clips have cleared the raised edge of the chassis, engage the clips simultaneously. When the clips have locked into position, the module will be fully inserted.

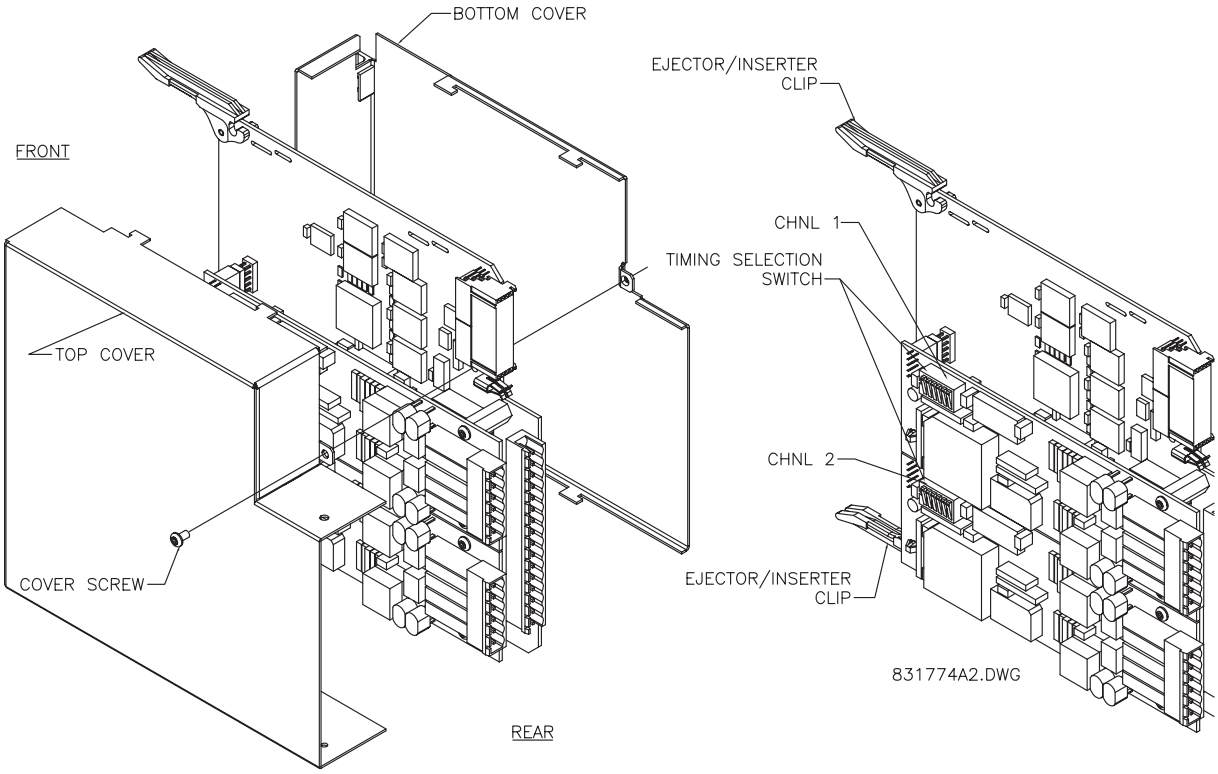


Figure 3–44: IEEE C37.94 TIMING SELECTION SWITCH SETTING

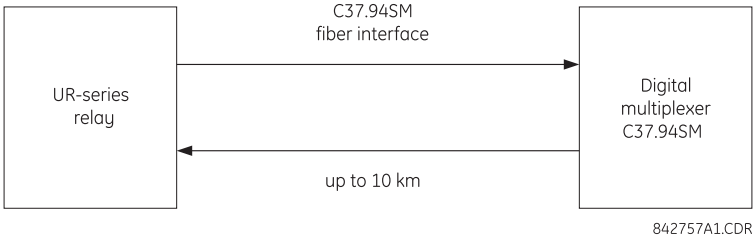
3.3.9 C37.94SM INTERFACE

The UR-series C37.94SM communication modules (2A and 2B) are designed to interface with modified IEEE C37.94 compliant digital multiplexers and/or IEEE C37.94 compliant interface converters that have been converted from 820 nm multimode fiber optics to 1300 nm ELED single-mode fiber optics. The IEEE C37.94 standard defines a point-to-point optical link for synchronous data between a multiplexer and a teleprotection device. This data is typically 64 kbps, but the standard provides for speeds up to 64*n* kbps, where *n* = 1, 2,…, 12. The UR-series C37.94SM communication module is 64 kbps only with *n* fixed at 1. The frame is a valid International Telecommunications Union (ITU-T) recommended G.704 pattern from the standpoint of framing and data rate. The frame is 256 bits and is repeated at a frame rate of 8000 Hz, with a resultant bit rate of 2048 kbps.

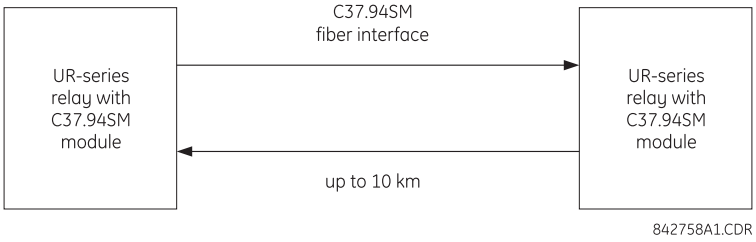
The specifications for the module are as follows:

Emulated IEEE standard: emulates C37.94 for 1 × 64 kbps optical fiber interface (modules set to *n* = 1 or 64 kbps)
Fiber optic cable type: 9/125 μm core diameter optical fiber
Fiber optic mode: single-mode, ELED compatible with HP HFBR-1315T transmitter and HP HFBR-2316T receiver
Fiber optic cable length: up to 10 km
Fiber optic connector: type ST
Wavelength: 1300 ±40 nm
Connection: as per all fiber optic connections, a Tx to Rx connection is required.

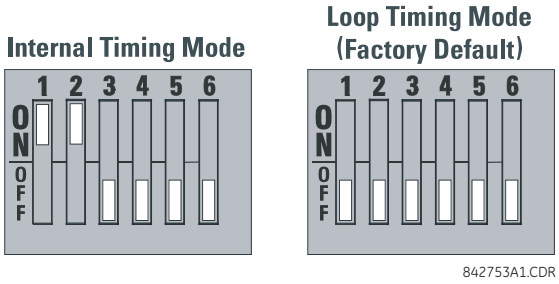
The UR-series C37.94SM communication module can be connected **directly** to any compliant digital multiplexer that supports C37.94SM as shown below.



It can also can be connected **directly** to any other UR-series relay with a C37.94SM module as shown below.



The UR-series C37.94SM communication module has six (6) switches that are used to set the clock configuration. The functions of these control switches is shown below.



For the Internal Timing Mode, the system clock is generated internally. Therefore, the timing switch selection should be Internal Timing for Relay 1 and Loop Timed for Relay 2. There must be only one timing source configured.

For the Looped Timing Mode, the system clock is derived from the received line signal. Therefore, the timing selection should be in Loop Timing Mode for connections to higher order systems.

The C37.94SM communications module cover removal procedure is as follows:

1. Remove the C37.94SM module (modules 2A or 2B):

   The ejector/inserter clips located at the top and at the bottom of each module, must be pulled simultaneously in order to release the module for removal. Before performing this action, **control power must be removed from the relay**. The original location of the module should be recorded to help ensure that the same or replacement module is inserted into the correct slot.

2. Remove the module cover screw.
3. Remove the top cover by sliding it towards the rear and then lift it upwards.
4. Set the Timing Selection Switches (Channel 1, Channel 2) to the desired timing modes (see description above).
5. Replace the top cover and the cover screw.
6. Re-insert the C37.94SM module. Take care to ensure that the **correct** module type is inserted into the **correct** slot position. The ejector/inserter clips located at the top and at the bottom of each module must be in the disengaged position as the module is smoothly inserted into the slot. Once the clips have cleared the raised edge of the chassis, engage the clips simultaneously. When the clips have locked into position, the module will be fully inserted.

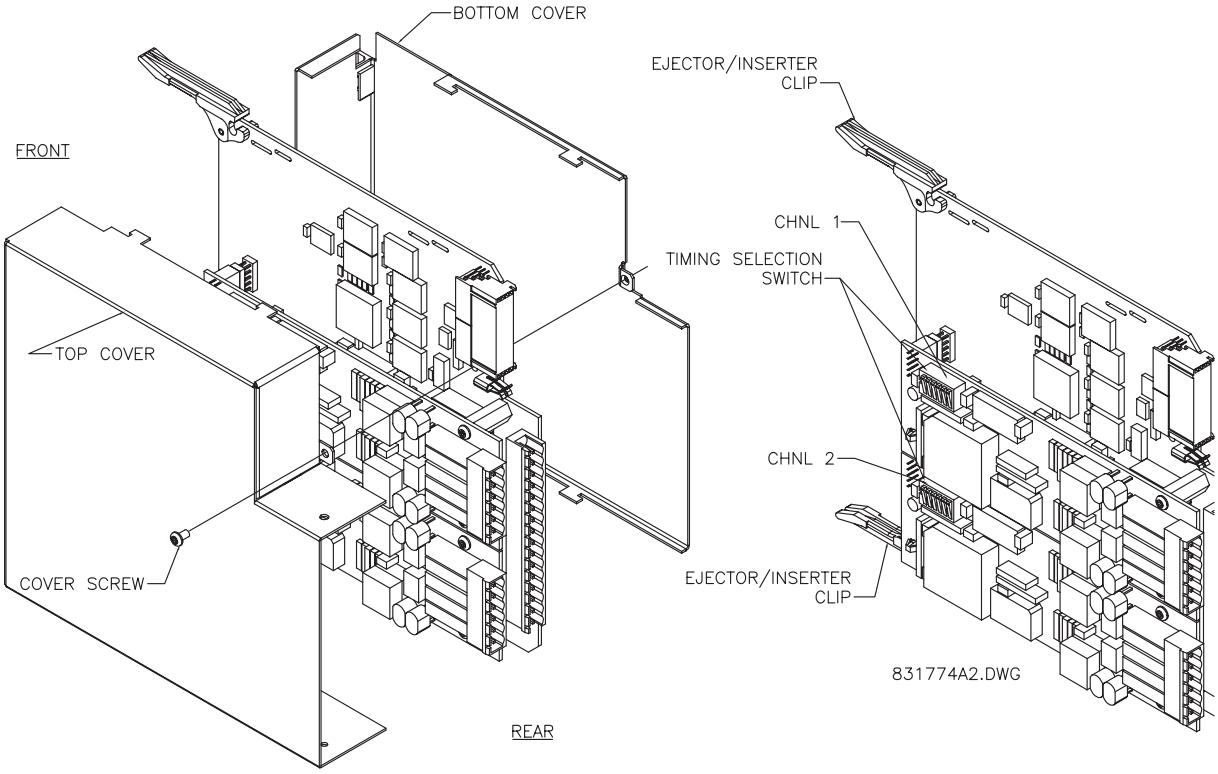


Figure 3–45: C37.94SM TIMING SELECTION SWITCH SETTING

4.1.1 INTRODUCTION

The EnerVista UR Setup software provides a graphical user interface (GUI) as one of two human interfaces to a UR device. The alternate human interface is implemented via the device's faceplate keypad and display (refer to the *Faceplate interface* section in this chapter).

The EnerVista UR Setup software provides a single facility to configure, monitor, maintain, and trouble-shoot the operation of relay functions, connected over local or wide area communication networks. It can be used while disconnected (off-line) or connected (on-line) to a UR device. In off-line mode, settings files can be created for eventual downloading to the device. In on-line mode, you can communicate with the device in real-time.

The EnerVista UR Setup software, provided with every L60 relay, can be run from any computer supporting Microsoft Windows® 95, 98, NT, 2000, ME, and XP. This chapter provides a summary of the basic EnerVista UR Setup software interface features. The EnerVista UR Setup Help File provides details for getting started and using the EnerVista UR Setup software interface.

4.1.2 CREATING A SITE LIST

To start using the EnerVista UR Setup software, a site definition and device definition must first be created. See the EnerVista UR Setup Help File or refer to the *Connecting EnerVista UR Setup with the L60* section in Chapter 1 for details.

4.1.3 ENERVISTA UR SETUP OVERVIEW

a) ENGAGING A DEVICE

The EnerVista UR Setup software may be used in on-line mode (relay connected) to directly communicate with the L60 relay. Communicating relays are organized and grouped by communication interfaces and into sites. Sites may contain any number of relays selected from the UR-series of relays.

b) USING SETTINGS FILES

The EnerVista UR Setup software interface supports three ways of handling changes to relay settings:

- In off-line mode (relay disconnected) to create or edit relay settings files for later download to communicating relays.
- While connected to a communicating relay to directly modify any relay settings via relay data view windows, and then save the settings to the relay.
- You can create/edit settings files and then write them to the relay while the interface is connected to the relay.

Settings files are organized on the basis of file names assigned by the user. A settings file contains data pertaining to the following types of relay settings:

- Device definition
- Product setup
- System setup
- FlexLogic™
- Grouped elements
- Control elements
- Inputs/outputs
- Testing

Factory default values are supplied and can be restored after any changes.

c) CREATING AND EDITING FLEXLOGIC™

You can create or edit a FlexLogic™ equation in order to customize the relay. You can subsequently view the automatically generated logic diagram.

d) VIEWING ACTUAL VALUES

You can view real-time relay data such as input/output status and measured parameters.

e) VIEWING TRIGGERED EVENTS

While the interface is in either on-line or off-line mode, you can view and analyze data generated by triggered specified parameters, via one of the following:

- **Event Recorder facility:** The event recorder captures contextual data associated with the last 1024 events, listed in chronological order from most recent to oldest.
- **Oscillography facility:** The oscillography waveform traces and digital states are used to provide a visual display of power system and relay operation data captured during specific triggered events.

f) FILE SUPPORT

- **Execution:** Any EnerVista UR Setup file which is double clicked or opened will launch the application, or provide focus to the already opened application. If the file was a settings file (has a URS extension) which had been removed from the Settings List tree menu, it will be added back to the Settings List tree menu.
- **Drag and Drop:** The Site List and Settings List control bar windows are each mutually a drag source and a drop target for device-order-code-compatible files or individual menu items. Also, the Settings List control bar window and any Windows Explorer directory folder are each mutually a file drag source and drop target.

  New files which are dropped into the Settings List window are added to the tree which is automatically sorted alphabetically with respect to settings file names. Files or individual menu items which are dropped in the selected device menu in the Site List window will automatically be sent to the on-line communicating device.

g) FIRMWARE UPGRADES

The firmware of a L60 device can be upgraded, locally or remotely, via the EnerVista UR Setup software. The corresponding instructions are provided by the EnerVista UR Setup Help file under the topic “Upgrading Firmware”.

NOTE

Modbus addresses assigned to firmware modules, features, settings, and corresponding data items (i.e. default values, minimum/maximum values, data type, and item size) may change slightly from version to version of firmware. The addresses are rearranged when new features are added or existing features are enhanced or modified. The **EEPROM DATA ERROR** message displayed after upgrading/downgrading the firmware is a resettable, self-test message intended to inform users that the Modbus addresses have changed with the upgraded firmware. This message does not signal any problems when appearing after firmware upgrades.

4.1.4 ENERVISTA UR SETUP MAIN WINDOW

The EnerVista UR Setup software main window supports the following primary display components:

1. Title bar which shows the pathname of the active data view.
2. Main window menu bar.
3. Main window tool bar.
4. Site list control bar window.
5. Settings list control bar window.
6. Device data view windows, with common tool bar.
7. Settings file data view windows, with common tool bar.
8. Workspace area with data view tabs.
9. Status bar.
10. Quick Action Hot Links

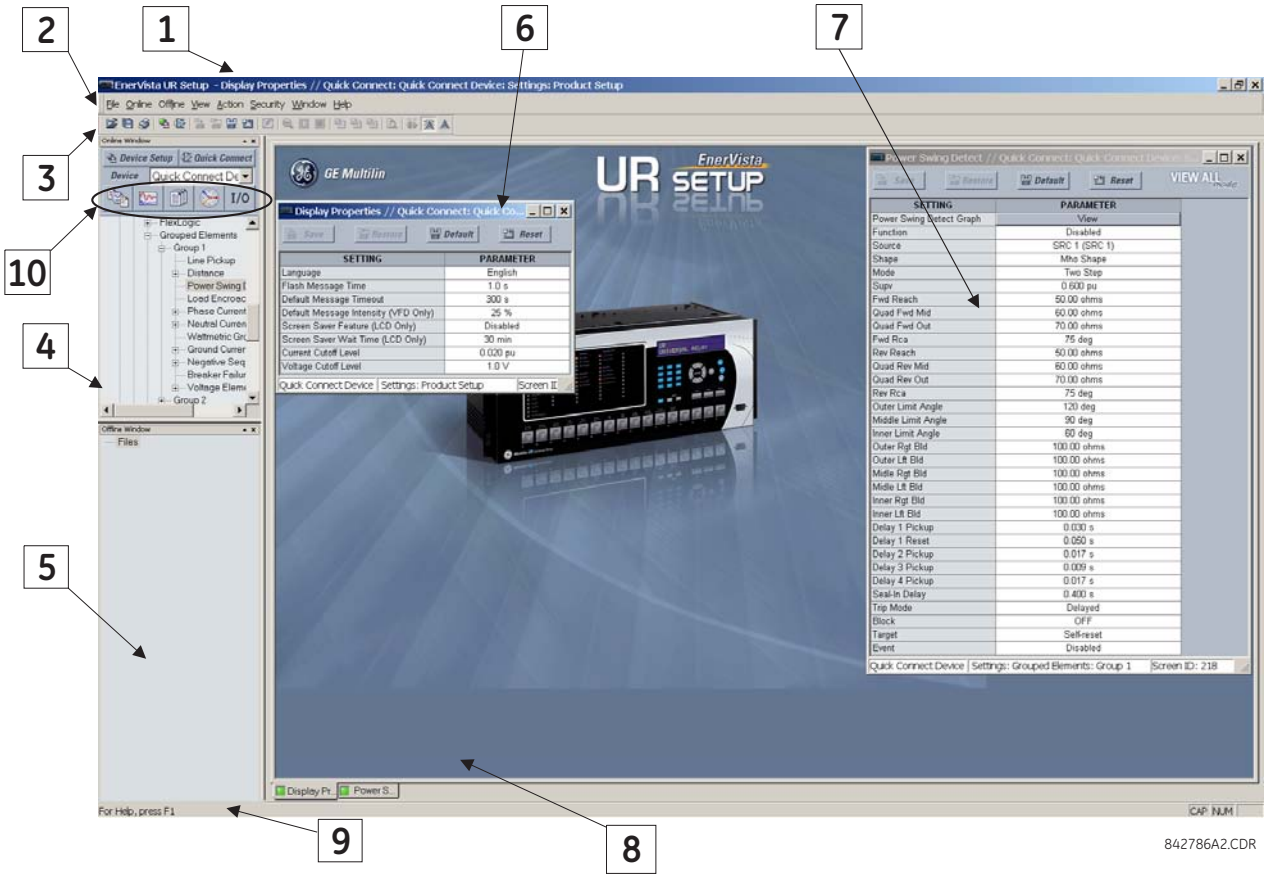


Figure 4–1: ENERVISTA UR SETUP SOFTWARE MAIN WINDOW

a) ENHANCED FACEPLATE

The front panel interface is one of two supported interfaces, the other interface being EnerVista UR Setup software. The front panel interface consists of LED panels, an RS232 port, keypad, LCD display, control pushbuttons, and optional user-programmable pushbuttons.

The faceplate is hinged to allow easy access to the removable modules.

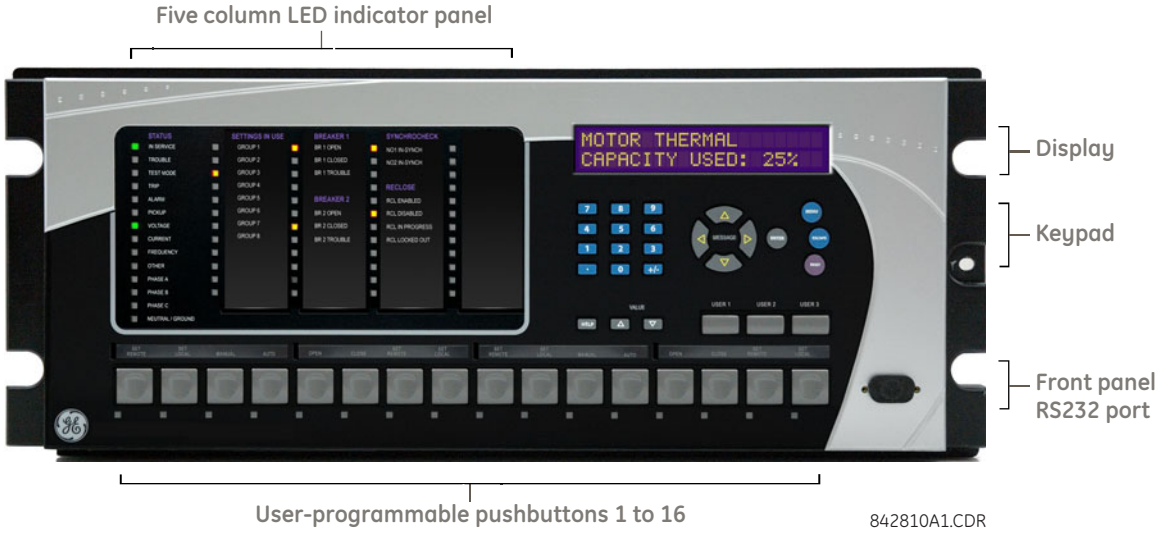


Figure 4–2: UR-SERIES ENHANCED FACEPLATE

b) STANDARD FACEPLATE

The front panel interface is one of two supported interfaces, the other interface being EnerVista UR Setup software. The front panel interface consists of LED panels, an RS232 port, keypad, LCD display, control pushbuttons, and optional user-programmable pushbuttons.

The faceplate is hinged to allow easy access to the removable modules. There is also a removable dust cover that fits over the faceplate which must be removed in order to access the keypad panel. The following figure shows the horizontal arrangement of the faceplate panels.

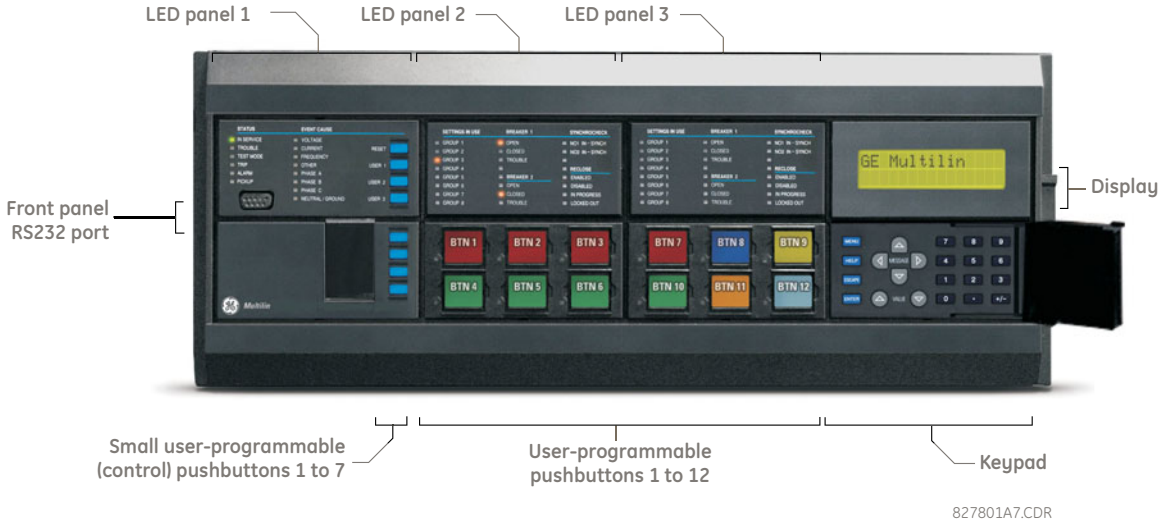


Figure 4–3: UR-SERIES STANDARD HORIZONTAL FACEPLATE PANELS

The following figure shows the vertical arrangement of the faceplate panels for relays ordered with the vertical option.

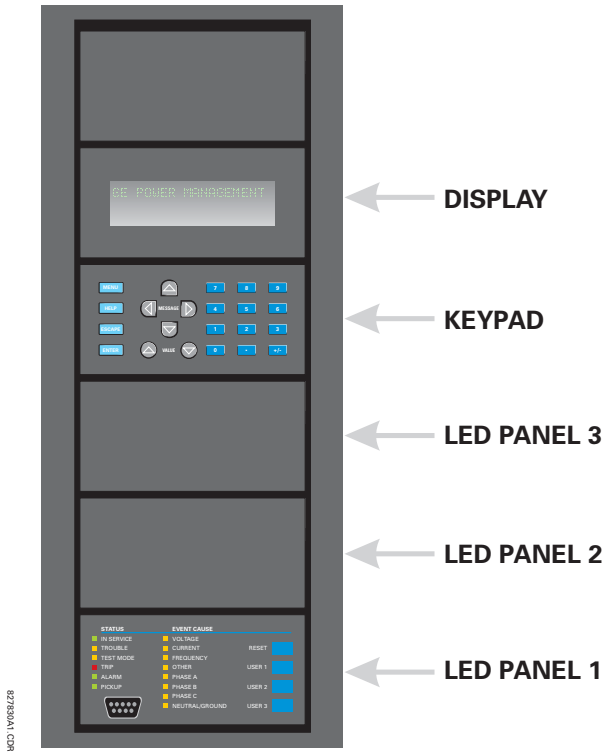


Figure 4–4: UR-SERIES STANDARD VERTICAL FACEPLATE PANELS

4.2.2 LED INDICATORS

a) ENHANCED FACEPLATE

The enhanced front panel display provides five columns of LED indicators. The first column contains 14 status and event cause LEDs, and the next four columns contain the 48 user-programmable LEDs.

The RESET key is used to reset any latched LED indicator or target message, once the condition has been cleared (these latched conditions can also be reset via the **SETTINGS** ⇨⇩ **INPUT/OUTPUTS** ⇨⇩ **RESETTING** menu). The USER keys are used by the Breaker Control feature. The RS232 port is intended for connection to a portable PC.

Figure 4–5: TYPICAL LED INDICATOR PANEL FOR ENHANCED FACEPLATE

The status indicators in the first column are described below.

- **IN SERVICE**: This LED indicates that control power is applied, all monitored inputs, outputs, and internal systems are OK, and that the device has been programmed.
- **TROUBLE**: This LED indicates that the relay has detected an internal problem.

- **TEST MODE**: This LED indicates that the relay is in test mode.
- **TRIP**: This LED indicates that the FlexLogic™ operand serving as a trip switch has operated. This indicator always latches; as such, a reset command must be initiated to allow the latch to be reset.
- **ALARM**: This LED indicates that the FlexLogic™ operand serving as an alarm switch has operated. This indicator is never latched.
- **PICKUP**: This LED indicates that an element is picked up. This indicator is never latched.

The event cause indicators in the first column are described below. These indicate the input type that was involved in a condition detected by an element that is operated or has a latched flag waiting to be reset.

- **VOLTAGE**: This LED indicates voltage was involved.
- **CURRENT**: This LED indicates current was involved.
- **FREQUENCY**: This LED indicates frequency was involved.
- **OTHER**: This LED indicates a composite function was involved.
- **PHASE A**: This LED indicates phase A was involved.
- **PHASE B**: This LED indicates phase B was involved.
- **PHASE C**: This LED indicates phase C was involved.
- **NEUTRAL/GROUND**: This LED indicates that neutral or ground was involved.

The user-programmable LEDs consist of 48 amber LED indicators in four columns. The operation of these LEDs is user-defined. Support for applying a customized label beside every LED is provided. The L60 is shipped with the default label for several user-programmable pushbuttons. However, the LEDs are not pre-programmed to reflect these labels. To match the pre-printed label, the LED settings must be programmed as described in the *User-programmable LEDs* section of chapter 5. The default labels can be replaced by user-printed labels.

User customization of LED operation is of maximum benefit in installations where languages other than English are used to communicate with operators. Refer to the *User-programmable LEDs* section in chapter 5 for the settings used to program the operation of the LEDs on these panels.

b) STANDARD FACEPLATE

The standar faceplate consists of three panels with LED indicators, keys, and a communications port. The RESET key is used to reset any latched LED indicator or target message, once the condition has been cleared (these latched conditions can also be reset via the **SETTINGS** ⇨⇩ **INPUT/OUTPUTS** ⇨⇩ **RESETTING** menu). The USER keys are used by the Breaker Control feature. The RS232 port is intended for connection to a portable PC.

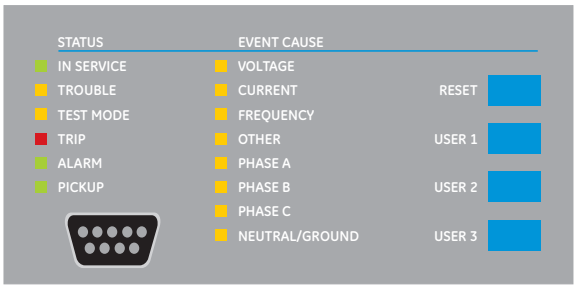


Figure 4–6: LED PANEL 1

STATUS INDICATORS:

- **IN SERVICE**: Indicates that control power is applied; all monitored inputs/outputs and internal systems are OK; the relay has been programmed.
- **TROUBLE**: Indicates that the relay has detected an internal problem.
- **TEST MODE**: Indicates that the relay is in test mode.

- **TRIP**: Indicates that the selected FlexLogic™ operand serving as a Trip switch has operated. This indicator always latches; the RESET command must be initiated to allow the latch to be reset.
- **ALARM**: Indicates that the selected FlexLogic™ operand serving as an Alarm switch has operated. This indicator is never latched.
- **PICKUP**: Indicates that an element is picked up. This indicator is never latched.

EVENT CAUSE INDICATORS:

These indicate the input type that was involved in a condition detected by an element that is operated or has a latched flag waiting to be reset.

- **VOLTAGE**: Indicates voltage was involved.
- **CURRENT**: Indicates current was involved.
- **FREQUENCY**: Indicates frequency was involved.
- **OTHER**: Indicates a composite function was involved.
- **PHASE A**: Indicates phase A was involved.
- **PHASE B**: Indicates phase B was involved.
- **PHASE C**: Indicates phase C was involved.
- **NEUTRAL/GROUND**: Indicates that neutral or ground was involved.

USER-PROGRAMMABLE INDICATORS:

The second and third provide 48 amber LED indicators whose operation is controlled by the user. Support for applying a customized label beside every LED is provided.

User customization of LED operation is of maximum benefit in installations where languages other than English are used to communicate with operators. Refer to the *User-programmable LEDs* section in chapter 5 for the settings used to program the operation of the LEDs on these panels.

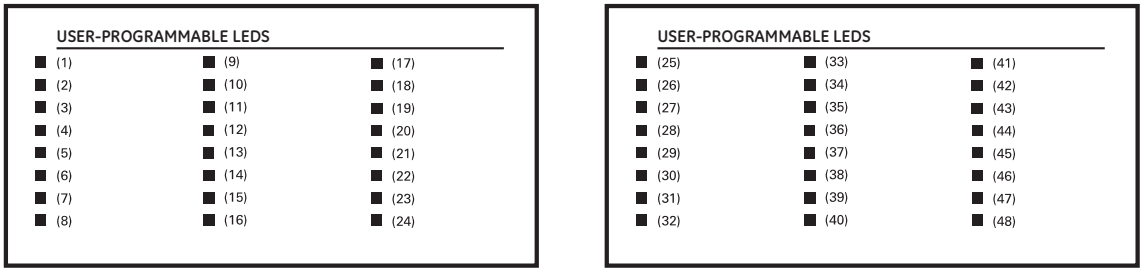


Figure 4–7: LED PANELS 2 AND 3 (INDEX TEMPLATE)

DEFAULT LABELS FOR LED PANEL 2:

The default labels are intended to represent:

- **GROUP 1...6**: The illuminated GROUP is the active settings group.
- **BREAKER 1(2) OPEN**: The breaker is open.
- **BREAKER 1(2) CLOSED**: The breaker is closed.
- **BREAKER 1(2) TROUBLE**: A problem related to the breaker has been detected.
- **SYNCHROCHECK NO1(2) IN-SYNCH**: Voltages have satisfied the synchrocheck element.
- **RECLOSE ENABLED**: The recloser is operational.
- **RECLOSE DISABLED**: The recloser is not operational.
- **RECLOSE IN PROGRESS**: A reclose operation is in progress.
- **RECLOSE LOCKED OUT**: The recloser is not operational and requires a reset.

Firmware revisions 2.9x and earlier support eight user setting groups; revisions 3.0x and higher support six setting groups. For convenience of users using earlier firmware revisions, the relay panel shows eight setting groups. Please note that the LEDs, despite their default labels, are fully user-programmable.

The relay is shipped with the default label for the LED panel 2. The LEDs, however, are not pre-programmed. To match the pre-printed label, the LED settings must be entered as shown in the *User-Programmable LEDs* section of Chapter 5. The LEDs are fully user-programmable. The default labels can be replaced by user-printed labels for both panels as explained in the following section.

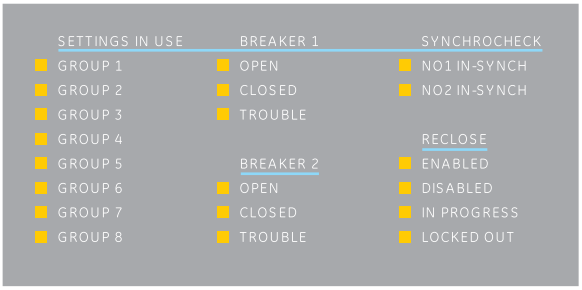


Figure 4–8: LED PANEL 2 (DEFAULT LABELS)

4.2.3 CUSTOM LABELING OF LEDS

a) ENHANCED FACEPLATE

The following procedure requires the pre-requisites listed below.

- EnerVista UR Setup software is installed and operational.
- The L60 settings have been saved to a settings file.
- The L60 front panel label cutout sheet (GE Multilin part number 1006-0047) has been downloaded from http://www.GEindustrial.com/multilin/support/ur and printed.
- Small-bladed knife.

This procedure describes how to create custom LED labels for the enhance front panel display.

1. Start the EnerVista UR Setup software.

2. Select the **Front Panel Report** item at the bottom of the menu tree for the settings file. The front panel report window will be displayed.

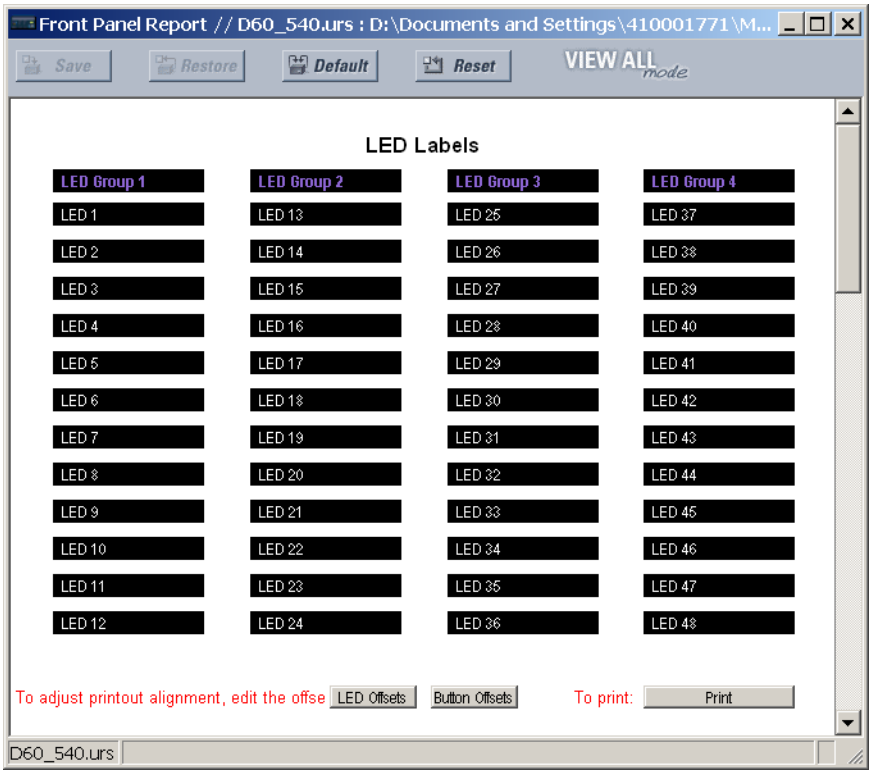


Figure 4–9: FRONT PANEL REPORT WINDOW

3. Enter the text to appear next to each LED and above each user-programmable pushbuttons in the fields provided.
4. Feed the L60 front panel label cutout sheet into a printer and press the **Print** button in the front panel report window.
5. When printing is complete, fold the sheet along the perforated lines and punch out the labels.
6. Remove the L60 label insert tool from the package and bend the tabs as follows.
   - Bend the two tabs towards centre of the tool upwards (towards you when looking from the printed side) - *see figure 4-10 below.*
   - Bend the two tabs towards centre of the tool downwards (away from you when looking from the printed side) - *see figure 4-11below.*
   - Bend the tab at the centre of the tool tail, inward (toward you when looking at the printed side) - s*ee figure 4-12 below.*

   These tabs will be used for insertion and removal of the default and custom LED labels.

NOTE **It is important that the tool be adjusted and used, EXACTLY as shown below, with the printed side containing the GE part number, facing UPWARDS.**

SETTING UP THE LABEL TOOL:

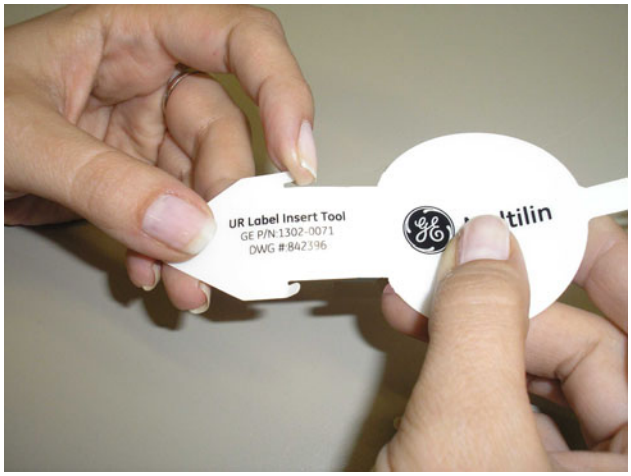


Figure 4–10: *LABEL TOOL* - BENDING THE UPPER TABS UPWARD

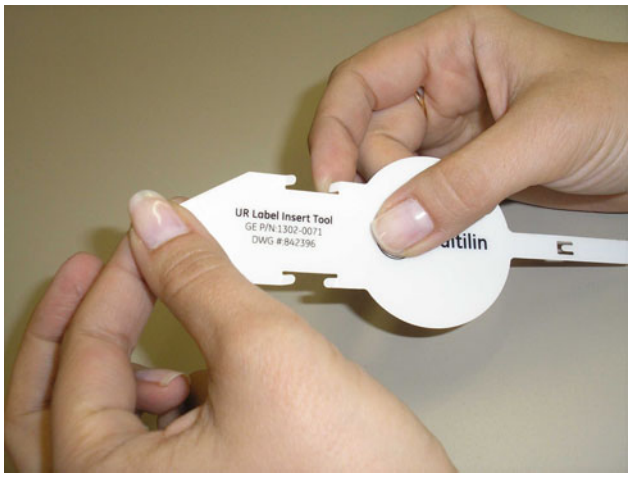


Figure 4–11: *LABEL TOOL* - BENDING THE LOWER TABS DOWNWARD

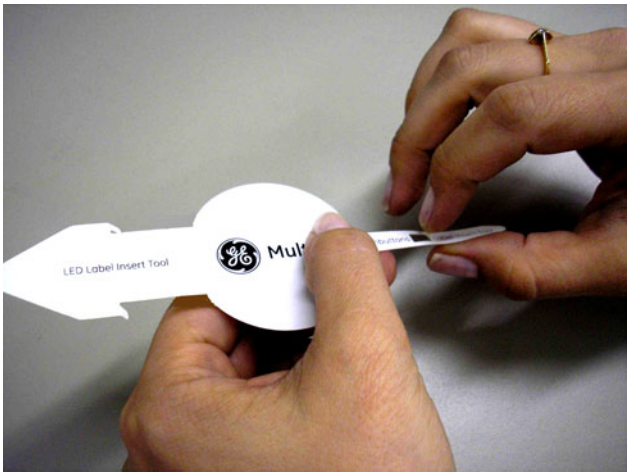


Figure 4–12: *LABEL TOOL* - BENDING THE TAB AT THE CENTRE OF THE TOOL TAIL

INSERTION AND REMOVAL OF LED LABELS:

Figure 4–13: *STEP 1* - USE KNIFE TO LIFT THE LED LABEL AND SLIDE THE LABEL TOOL UNDERNEATH. MAKE SURE THE BENDED UPPER TABS ARE POINTING OUTWARDS (IE - AWAY FROM YOU).

Figure 4–14: ***STEP 2*** - SLIDE THE TOOL IN UNTIL THE TABS SNAP OUT AS SHOWN

Figure 4–15: ***STEP 3*** - PULL THE TOOL OUT ALONG WITH THE LED LABEL

Figure 4–16: *STEP 7* - SLIDE HALF OF THE PRINTED LED LABEL INSIDE THE POCKET

Figure 4–17: *STEP 8* - SLIDE THE LABEL TOOL INSIDE THE POCKET AS SHOWN

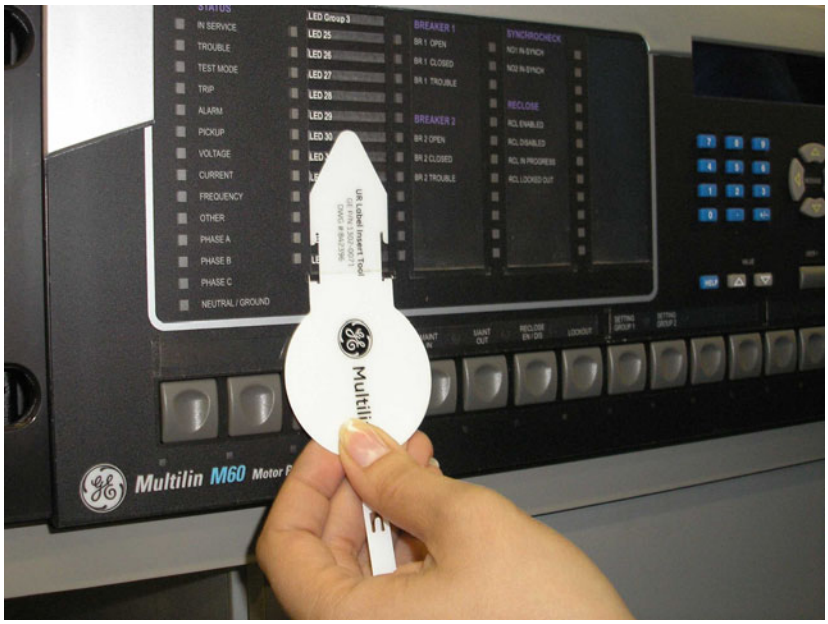


Figure 4–18: *STEP 9* - PUSH THE LABEL IN UNTIL THE TEXT ALIGNS WITH THE LEDS

INSERTION AND REMOVAL OF PUSHBUTTON LABELS:

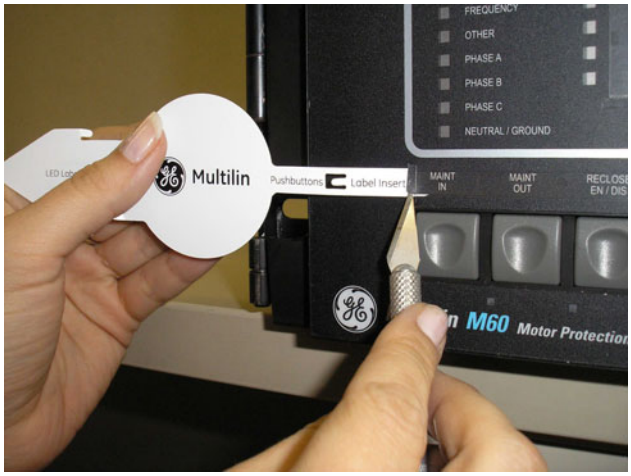


Figure 4–19: *STEP 1* - USE KNIFE TO LIFT THE PUSHBUTTON LABEL AND SLIDE TAIL OF THE LABEL TOOL UNDERNEATH. MAKE SURE THE BENDED TAB IS POINTING OUTWARDS (IE - AWAY FROM YOU).

Figure 4–20: *STEP 2* - SLIDE THE TOOL IN UNTIL THE TAB SNAPS OUT AS SHOWN

Figure 4–21: *STEP 3* - PULL THE TOOL OUT WITH THE PUSHBUTTON LABEL

Figure 4–22: *STEP 4* - SLIDE IN THE CUSTOM BUTTON LABEL AS SHOWN

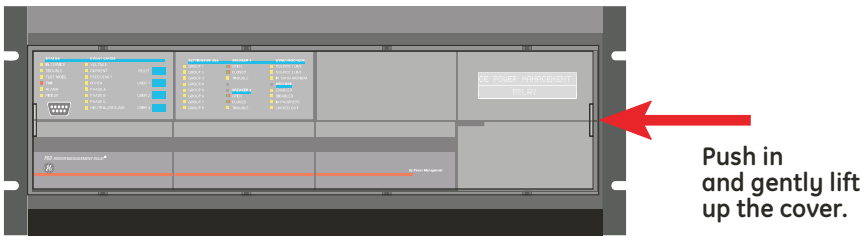
b) STANDARD FACEPLATE

Custom labeling of an LED-only panel is facilitated through a Microsoft Word file available from the following URL:

http://www.GEindustrial.com/multilin/support/ur/

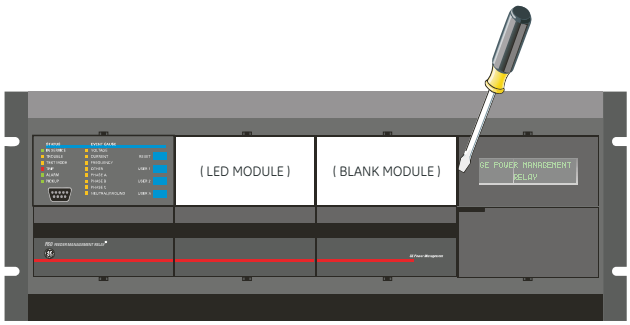
This file provides templates and instructions for creating appropriate labeling for the LED panel. The following procedures are contained in the downloadable file. The panel templates provide relative LED locations and located example text (x) edit boxes. The following procedure demonstrates how to install/uninstall the custom panel labeling.

1. Remove the clear Lexan Front Cover (GE Multilin part number: 1501-0014).



842771A1.CDR

2. Pop out the LED module and/or the blank module with a screwdriver as shown below. Be careful not to damage the plastic covers.



842722A1.CDR

3. Place the left side of the customized module back to the front panel frame, then snap back the right side.

4. Put the clear Lexan front cover back into place.

The following items are required to customize the L60 display module:

- Black and white or color printer (color preferred).
- Microsoft Word 97 or later software for editing the template.
- 1 each of: 8.5" x 11" white paper, exacto knife, ruler, custom display module (GE Multilin Part Number: 1516-0069), and a custom module cover (GE Multilin Part Number: 1502-0015).

The following procedure describes how to customize the L60 display module:

1. Open the LED panel customization template with Microsoft Word. Add text in places of the **LED x** text placeholders on the template(s). Delete unused place holders as required.
2. When complete, save the Word file to your local PC for future use.
3. Print the template(s) to a local printer.
4. From the printout, cut-out the Background Template from the three windows, using the cropmarks as a guide.
5. Put the Background Template on top of the custom display module (GE Multilin Part Number: 1513-0069) and snap the clear custom module cover (GE Multilin Part Number: 1502-0015) over it and the templates.

4.2.4 DISPLAY

All messages are displayed on a 2 × 20 backlit liquid crystal display (LCD) to make them visible under poor lighting conditions. Messages are descriptive and should not require the aid of an instruction manual for deciphering. While the keypad and display are not actively being used, the display will default to user-defined messages. Any high priority event driven message will automatically override the default message and appear on the display.

4.2.5 KEYPAD

Display messages are organized into ‘pages’ under the following headings: Actual Values, Settings, Commands, and Targets. The MENU key navigates through these pages. Each heading page is broken down further into logical subgroups.

The MESSAGE keys navigate through the subgroups. The VALUE keys scroll increment or decrement numerical setting values when in programming mode. These keys also scroll through alphanumeric values in the text edit mode. Alternatively, values may also be entered with the numeric keypad.

The decimal key initiates and advance to the next character in text edit mode or enters a decimal point. The HELP key may be pressed at any time for context sensitive help messages. The ENTER key stores altered setting values.

4.2.6 BREAKER CONTROL

a) INTRODUCTION

The L60 can interface with associated circuit breakers. In many cases the application monitors the state of the breaker, which can be presented on faceplate LEDs, along with a breaker trouble indication. Breaker operations can be manually initiated from faceplate keypad or automatically initiated from a FlexLogic™ operand. A setting is provided to assign names to each breaker; this user-assigned name is used for the display of related flash messages. These features are provided for two breakers; the user may use only those portions of the design relevant to a single breaker, which must be breaker 1.

For the following discussion it is assumed the **SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ BREAKERS ⇨ BREAKER 1(2) ⇨ BREAKER FUNCTION** setting is "Enabled" for each breaker.

b) CONTROL MODE SELECTION AND MONITORING

Installations may require that a breaker is operated in the three-pole only mode (3-pole), or in the one and three-pole (1-pole) mode, selected by setting. If the mode is selected as 3-pole, a single input tracks the breaker open or closed position. If the mode is selected as 1-pole, all three breaker pole states must be input to the relay. These inputs must be in agreement to indicate the position of the breaker.

For the following discussion it is assumed the **SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ BREAKERS ⇨ BREAKER 1(2) ⇨⇩ BREAKER 1(2) PUSH BUTTON CONTROL** setting is “Enabled” for each breaker.

c) FACEPLATE (USER KEY) CONTROL

After the 30 minute interval during which command functions are permitted after a correct command password, the user cannot open or close a breaker via the keypad. The following discussions begin from the not-permitted state.

d) CONTROL OF TWO BREAKERS

For the following example setup, the **(Name)** field represents the user-programmed variable name.

For this application (setup shown below), the relay is connected and programmed for both breaker 1 and breaker 2. The USER 1 key performs the selection of which breaker is to be operated by the USER 2 and USER 3 keys. The USER 2 key is used to manually close the breaker and the USER 3 key is used to manually open the breaker.

`ENTER COMMAND PASSWORD`	This message appears when the USER 1, USER 2, or USER 3 key is pressed and a **COMMAND PASSWORD** is required; i.e. if **COMMAND PASSWORD** is enabled and no commands have been issued within the last 30 minutes.
`Press USER 1 To Select Breaker`	This message appears if the correct password is entered or if none is required. This message will be maintained for 30 seconds or until the USER 1 key is pressed again.
`BKR1-(Name) SELECTED USER 2=CLS/USER 3=OP`	This message is displayed after the USER 1 key is pressed for the second time. Three possible actions can be performed from this state within 30 seconds as per items **(1)**, **(2)** and **(3)** below:
(1)	
`USER 2 OFF/ON To Close BKR1-(Name)`	If the USER 2 key is pressed, this message appears for 20 seconds. If the USER 2 key is pressed again within that time, a signal is created that can be programmed to operate an output relay to close breaker 1.
(2)	
`USER 3 OFF/ON To Open BKR1-(Name)`	If the USER 3 key is pressed, this message appears for 20 seconds. If the USER 3 key is pressed again within that time, a signal is created that can be programmed to operate an output relay to open breaker 1.
(3)	
`BKR2-(Name) SELECTED USER 2=CLS/USER 3=OP`	If the USER 1 key is pressed at this step, this message appears showing that a different breaker is selected. Three possible actions can be performed from this state as per **(1)**, **(2)** and **(3)**. Repeatedly pressing the USER 1 key alternates between available breakers. Pressing keys other than USER 1, 2 or 3 at any time aborts the breaker control function.

e) CONTROL OF ONE BREAKER

For this application the relay is connected and programmed for breaker No only. Operation for this application is identical to that described above for two breakers.

4.2.7 MENUS

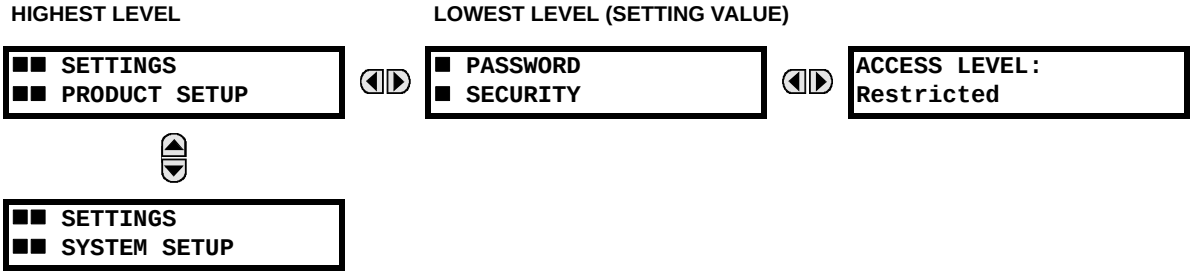
a) NAVIGATION

Press the MENU key to select the desired header display page (top-level menu). The header title appears momentarily followed by a header display page menu item. Each press of the MENU key advances through the following main heading pages:

- Actual values
- Settings
- Commands
- Targets
- User displays (when enabled)

b) HIERARCHY

The setting and actual value messages are arranged hierarchically. The header display pages are indicated by double scroll bar characters (■■), while sub-header pages are indicated by single scroll bar characters (■). The header display pages represent the highest level of the hierarchy and the sub-header display pages fall below this level. The MESSAGE UP and DOWN keys move within a group of headers, sub-headers, setting values, or actual values. Continually pressing the MESSAGE RIGHT key from a header display displays specific information for the header category. Conversely, continually pressing the MESSAGE LEFT key from a setting value or actual value display returns to the header display.



c) EXAMPLE MENU NAVIGATION

■■ ACTUAL VALUES ■■ STATUS	Press the MENU key until the header for the first Actual Values page appears. This page contains system and relay status information. Repeatedly press the MESSAGE keys to display the other actual value headers.
⇩	
■■ SETTINGS ■■ PRODUCT SETUP	Press the MENU key until the header for the first page of Settings appears. This page contains settings to configure the relay.
⇩	
■■ SETTINGS ■■ SYSTEM SETUP	Press the MESSAGE DOWN key to move to the next Settings page. This page contains settings for System Setup. Repeatedly press the MESSAGE UP and DOWN keys to display the other setting headers and then back to the first Settings page header.
⇩	
■ PASSWORD ■ SECURITY	From the Settings page one header (Product Setup), press the MESSAGE RIGHT key once to display the first sub-header (Password Security).
⇩	
ACCESS LEVEL: Restricted	Press the MESSAGE RIGHT key once more and this will display the first setting for Password Security. Pressing the MESSAGE DOWN key repeatedly will display the remaining setting messages for this sub-header.
⇩	
■ PASSWORD ■ SECURITY	Press the MESSAGE LEFT key once to move back to the first sub-header message.
⇩	
■ DISPLAY ■ PROPERTIES	Pressing the MESSAGE DOWN key will display the second setting sub-header associated with the Product Setup header.
⇩	
FLASH MESSAGE TIME: 1.0 s	Press the MESSAGE RIGHT key once more and this will display the first setting for Display Properties.
⇩	
DEFAULT MESSAGE INTENSITY: 25%	To view the remaining settings associated with the Display Properties subheader, repeatedly press the MESSAGE DOWN key. The last message appears as shown.

4.2.8 CHANGING SETTINGS

a) ENTERING NUMERICAL DATA

Each numerical setting has its own minimum, maximum, and increment value associated with it. These parameters define what values are acceptable for a setting.

```
FLASH MESSAGE
TIME:  1.0 s
```
⇩

For example, select the **SETTINGS** ⇨ **PRODUCT SETUP** ⇨⇩ **DISPLAY PROPERTIES** ⇨ **FLASH MESSAGE TIME** setting.

```
MINIMUM:   0.5
MAXIMUM:  10.0
```

Press the HELP key to view the minimum and maximum values. Press the HELP key again to view the next context sensitive help message.

Two methods of editing and storing a numerical setting value are available.

- **0 to 9 and decimal point**: The relay numeric keypad works the same as that of any electronic calculator. A number is entered one digit at a time. The leftmost digit is entered first and the rightmost digit is entered last. Pressing the MESSAGE LEFT key or pressing the ESCAPE key, returns the original value to the display.
- **VALUE keys**: The VALUE UP key increments the displayed value by the step value, up to the maximum value allowed. While at the maximum value, pressing the VALUE UP key again will allow the setting selection to continue upward from the minimum value. The VALUE DOWN key decrements the displayed value by the step value, down to the minimum value. While at the minimum value, pressing the VALUE DOWN key again will allow the setting selection to continue downward from the maximum value.

```
FLASH MESSAGE
TIME:  2.5 s
```
⇩

As an example, set the flash message time setting to 2.5 seconds. Press the appropriate numeric keys in the sequence “2 . 5". The display message will change as the digits are being entered.

```
NEW SETTING
HAS BEEN STORED
```

Until ENTER is pressed, editing changes are not registered by the relay. Therefore, press ENTER to store the new value in memory. This flash message will momentarily appear as confirmation of the storing process. Numerical values which contain decimal places will be rounded-off if more decimal place digits are entered than specified by the step value.

b) ENTERING ENUMERATION DATA

Enumeration settings have data values which are part of a set, whose members are explicitly defined by a name. A set is comprised of two or more members.

```
ACCESS LEVEL:
Restricted
```

For example, the selections available for **ACCESS LEVEL** are "Restricted", "Command", "Setting", and "Factory Service".

Enumeration type values are changed using the VALUE keys. The VALUE UP key displays the next selection while the VALUE DOWN key displays the previous selection.

```
ACCESS LEVEL:
Setting
```
⇩

If the **ACCESS LEVEL** needs to be "Setting", press the VALUE keys until the proper selection is displayed. Press HELP at any time for the context sensitive help messages.

```
NEW SETTING
HAS BEEN STORED
```

Changes are not registered by the relay until the ENTER key is pressed. Pressing ENTER stores the new value in memory. This flash message momentarily appears as confirmation of the storing process.

c) ENTERING ALPHANUMERIC TEXT

Text settings have data values which are fixed in length, but user-defined in character. They may be comprised of upper case letters, lower case letters, numerals, and a selection of special characters.

There are several places where text messages may be programmed to allow the relay to be customized for specific applications. One example is the Message Scratchpad. Use the following procedure to enter alphanumeric text messages.

For example: to enter the text, “Breaker #1”.

1. Press the decimal to enter text edit mode.
2. Press the VALUE keys until the character 'B' appears; press the decimal key to advance the cursor to the next position.
3. Repeat step 2 for the remaining characters: r,e,a,k,e,r, ,#,1.
4. Press ENTER to store the text.
5. If you have any problem, press HELP to view context sensitive help. Flash messages will sequentially appear for several seconds each. For the case of a text setting message, pressing HELP displays how to edit and store new values.

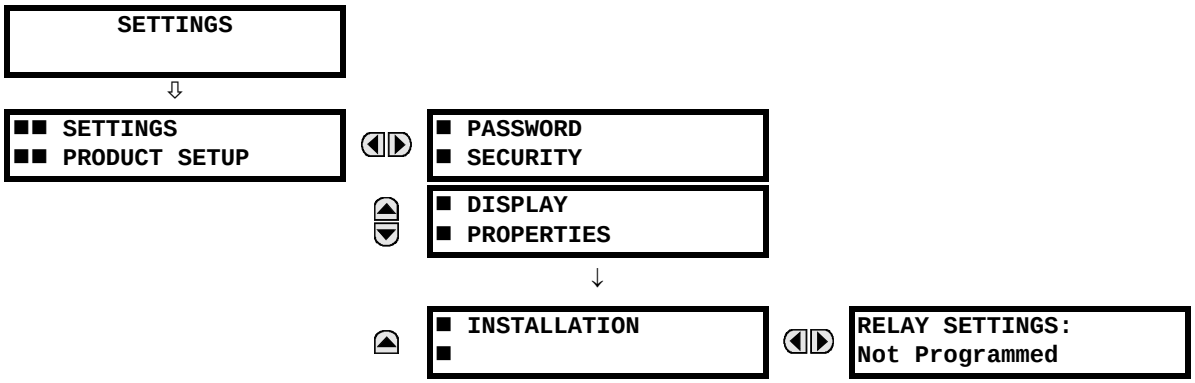
d) ACTIVATING THE RELAY

RELAY SETTINGS: **Not Programmed**

When the relay is powered up, the Trouble LED will be on, the In Service LED off, and this message displayed, indicating the relay is in the "Not Programmed" state and is safeguarding (output relays blocked) against the installation of a relay whose settings have not been entered. This message remains until the relay is explicitly put in the "Programmed" state.

To change the **RELAY SETTINGS**: "Not Programmed" mode to "Programmed", proceed as follows:

1. Press the MENU key until the **SETTINGS** header flashes momentarily and the **PRODUCT SETUP** message appears on the display.
2. Press the MESSAGE RIGHT key until the **PASSWORD SECURITY** message appears on the display.
3. Press the MESSAGE DOWN key until the **INSTALLATION** message appears on the display.
4. Press the MESSAGE RIGHT key until the **RELAY SETTINGS: Not Programmed** message is displayed.



5. After the **RELAY SETTINGS: Not Programmed** message appears on the display, press the VALUE keys change the selection to "Programmed".
6. Press the ENTER key.

RELAY SETTINGS: **Not Programmed**	**RELAY SETTINGS:** **Programmed**	**NEW SETTING** **HAS BEEN STORED**

7. When the "NEW SETTING HAS BEEN STORED" message appears, the relay will be in "Programmed" state and the In Service LED will turn on.

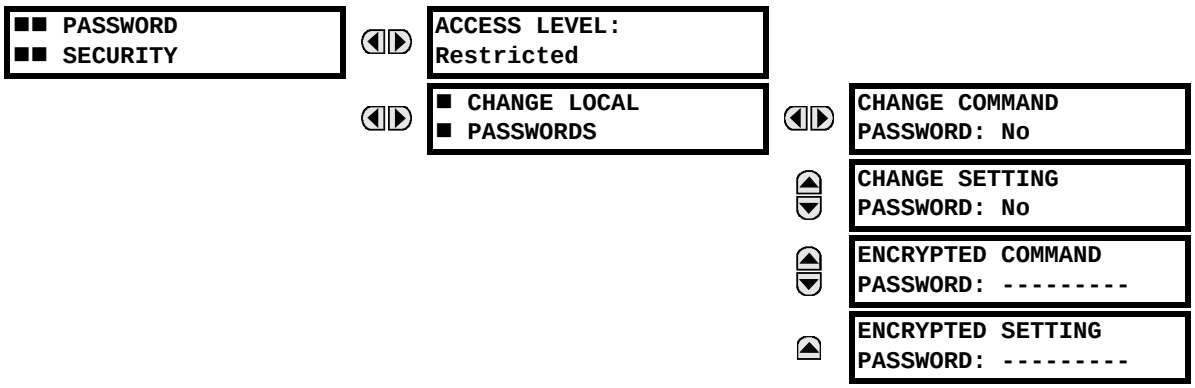
e) ENTERING INITIAL PASSWORDS

The L60 supports password entry from a local or remote connection.

Local access is defined as any access to settings or commands via the faceplate interface. This includes both keypad entry and the faceplate RS232 connection. Remote access is defined as any access to settings or commands via any rear communications port. This includes both Ethernet and RS485 connections. Any changes to the local or remote passwords enables this functionality.

To enter the initial setting (or command) password, proceed as follows:

1. Press the MENU key until the **SETTINGS** header flashes momentarily and the **PRODUCT SETUP** message appears on the display.
2. Press the MESSAGE RIGHT key until the **ACCESS LEVEL** message appears on the display.
3. Press the MESSAGE DOWN key until the **CHANGE LOCAL PASSWORDS** message appears on the display.
4. Press the MESSAGE RIGHT key until the **CHANGE SETTING PASSWORD** (or **CHANGE COMMAND PASSWORD**) message appears on the display.



5. After the **CHANGE...PASSWORD** message appears on the display, press the VALUE UP or DOWN key to change the selection to "Yes".
6. Press the ENTER key and the display will prompt you to **ENTER NEW PASSWORD**.
7. Type in a numerical password (up to 10 characters) and press the ENTER key.
8. When the **VERIFY NEW PASSWORD** is displayed, re-type in the same password and press ENTER.

9. When the **NEW PASSWORD HAS BEEN STORED** message appears, your new Setting (or Command) Password will be active.

f) CHANGING EXISTING PASSWORD

To change an existing password, follow the instructions in the previous section with the following exception. A message will prompt you to type in the existing password (for each security level) before a new password can be entered.

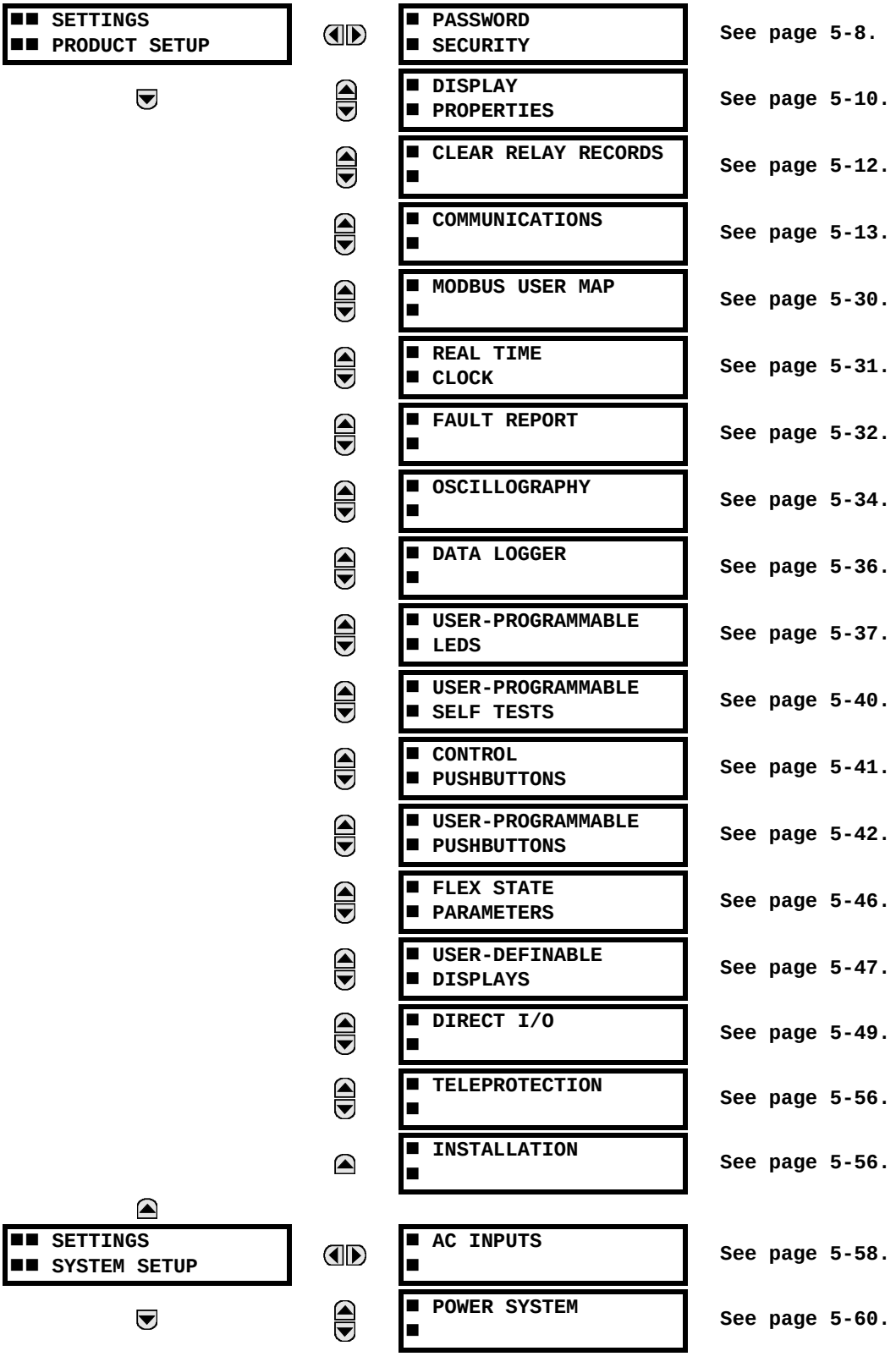
In the event that a password has been lost (forgotten), submit the corresponding encrypted password from the **PASSWORD SECURITY** menu to the Factory for decoding.

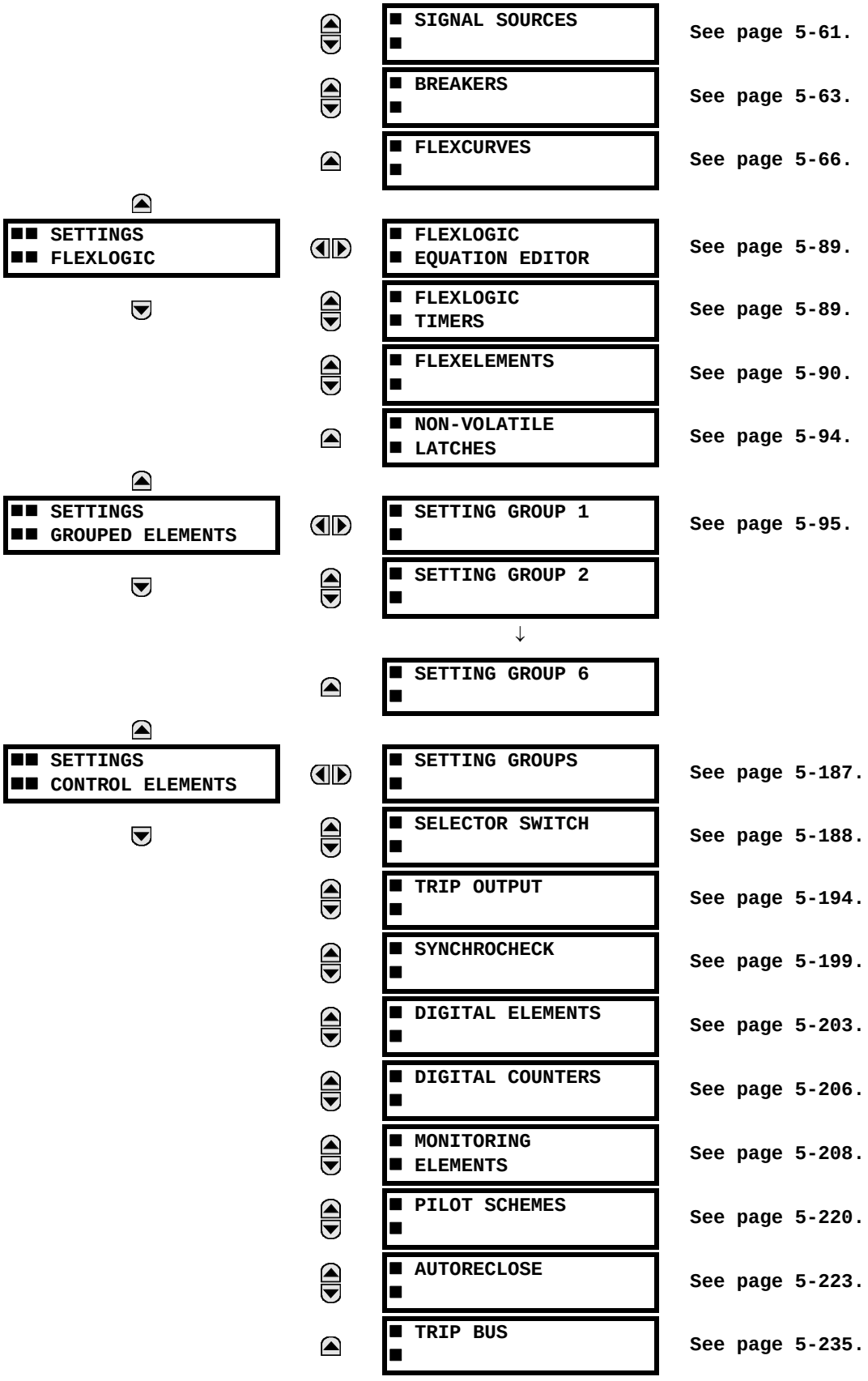
g) INVALID PASSWORD ENTRY

In the event that an incorrect Command or Setting password has been entered via the faceplate interface three times within a three-minute time span, the LOCAL ACCESS DENIED FlexLogic™ operand will be set to "On" and the L60 will not allow Settings or Command access via the faceplate interface for the next ten minutes. The **TOO MANY ATTEMPTS – BLOCKED**

FOR 10 MIN! flash message will appear upon activation of the ten minute timeout or any other time a user attempts any change to the defined tier during the ten minute timeout. The LOCAL ACCESS DENIED FlexLogic™ operand will be set to "Off" after the expiration of the ten-minute timeout.

In the event that an incorrect Command or Setting password has been entered via the any external communications interface three times within a three-minute time span, the REMOTE ACCESS DENIED FlexLogic™ operand will be set to "On" and the L60 will not allow Settings or Command access via the any external communications interface for the next ten minutes. The REMOTE ACCESS DENIED FlexLogic™ operand will be set to "Off" after the expiration of the ten-minute timeout.


SETTINGS
PRODUCT SETUP
PASSWORD
SECURITY
See page 5-8.
DISPLAY
PROPERTIES
See page 5-10.
CLEAR RELAY RECORDS
See page 5-12.
COMMUNICATIONS
See page 5-13.
MODBUS USER MAP
See page 5-30.
REAL TIME
CLOCK
See page 5-31.
FAULT REPORT
See page 5-32.
OSCILLOGRAPHY
See page 5-34.
DATA LOGGER
See page 5-36.
USER-PROGRAMMABLE
LEDS
See page 5-37.
USER-PROGRAMMABLE
SELF TESTS
See page 5-40.
CONTROL
PUSHBUTTONS
See page 5-41.
USER-PROGRAMMABLE
PUSHBUTTONS
See page 5-42.
FLEX STATE
PARAMETERS
See page 5-46.
USER-DEFINABLE
DISPLAYS
See page 5-47.
DIRECT I/O
See page 5-49.
TELEPROTECTION
See page 5-56.
INSTALLATION
See page 5-56.
SETTINGS
SYSTEM SETUP
AC INPUTS
See page 5-58.
POWER SYSTEM
See page 5-60.


SETTINGS
FLEXLOGIC
SETTINGS
GROUPED ELEMENTS
SETTINGS
CONTROL ELEMENTS
SIGNAL SOURCES
See page 5-61.
BREAKERS
See page 5-63.
FLEXCURVES
See page 5-66.
FLEXLOGIC
EQUATION EDITOR
See page 5-89.
FLEXLOGIC
TIMERS
See page 5-89.
FLEXELEMENTS
See page 5-90.
NON-VOLATILE
LATCHES
See page 5-94.
SETTING GROUP 1
See page 5-95.
SETTING GROUP 2
SETTING GROUP 6
SETTING GROUPS
See page 5-187.
SELECTOR SWITCH
See page 5-188.
TRIP OUTPUT
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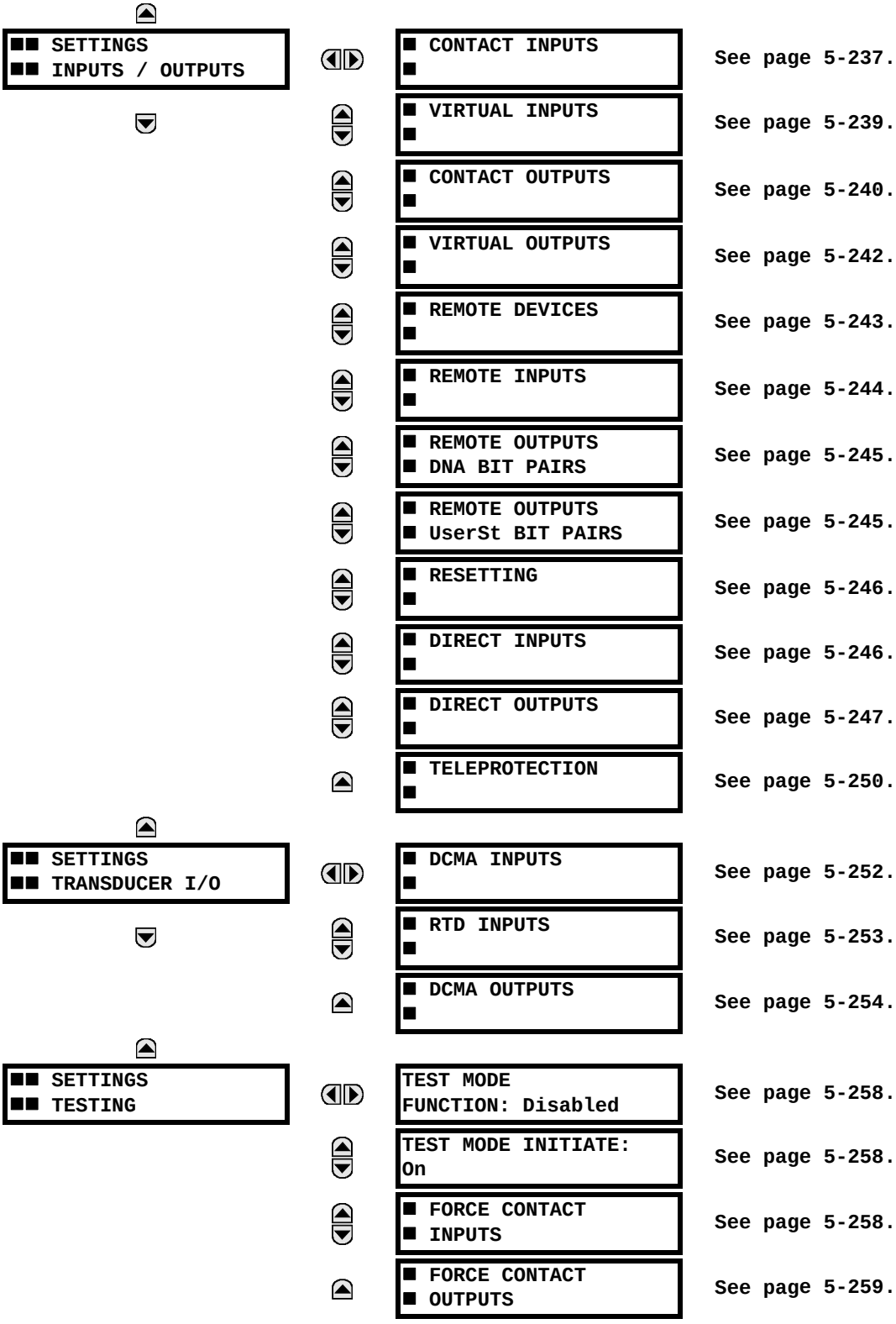
SYNCHROCHECK
See page 5-199.
DIGITAL ELEMENTS
See page 5-203.
DIGITAL COUNTERS
See page 5-206.
MONITORING
ELEMENTS
See page 5-208.
PILOT SCHEMES
See page 5-220.
AUTORECLOSE
See page 5-223.
TRIP BUS
See page 5-235.


SETTINGS
INPUTS / OUTPUTS
CONTACT INPUTS
See page 5-237.
VIRTUAL INPUTS
See page 5-239.
CONTACT OUTPUTS
See page 5-240.
VIRTUAL OUTPUTS
See page 5-242.
REMOTE DEVICES
See page 5-243.
REMOTE INPUTS
See page 5-244.
REMOTE OUTPUTS
DNA BIT PAIRS
See page 5-245.
REMOTE OUTPUTS
UserSt BIT PAIRS
See page 5-245.
RESETTING
See page 5-246.
DIRECT INPUTS
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DIRECT OUTPUTS
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TELEPROTECTION
See page 5-250.
SETTINGS
TRANSDUCER I/O
DCMA INPUTS
See page 5-252.
RTD INPUTS
See page 5-253.
DCMA OUTPUTS
See page 5-254.
SETTINGS
TESTING
TEST MODE
FUNCTION: Disabled
See page 5-258.
TEST MODE INITIATE:
On
See page 5-258.
FORCE CONTACT
INPUTS
See page 5-258.
FORCE CONTACT
OUTPUTS
See page 5-259.

5.1.2 INTRODUCTION TO ELEMENTS

In the design of UR relays, the term “element” is used to describe a feature that is based around a comparator. The comparator is provided with an input (or set of inputs) that is tested against a programmed setting (or group of settings) to determine if the input is within the defined range that will set the output to logic 1, also referred to as “setting the flag”. A single comparator may make multiple tests and provide multiple outputs; for example, the time overcurrent comparator sets a pickup flag when the current input is above the setting and sets an operate flag when the input current has been at a level above the pickup setting for the time specified by the time-current curve settings. All comparators, except the digital element which uses a logic state as the input, use analog parameter actual values as the input.

Elements are arranged into two classes, *grouped* and *control*. Each element classed as a grouped element is provided with six alternate sets of settings, in setting groups numbered 1 through 6. The performance of a grouped element is defined by the setting group that is active at a given time. The performance of a control element is independent of the selected active setting group.

The main characteristics of an element are shown on the element logic diagram. This includes the inputs, settings, fixed logic, and the output operands generated (abbreviations used on scheme logic diagrams are defined in Appendix F).

Some settings for current and voltage elements are specified in per-unit (pu) calculated quantities:

pu quantity = (actual quantity) / (base quantity)

For current elements, the ‘base quantity’ is the nominal secondary or primary current of the CT.

Where the current source is the sum of two CTs with different ratios, the ‘base quantity’ will be the common secondary or primary current to which the sum is scaled (that is, normalized to the larger of the two rated CT inputs). For example, if CT1 = 300 / 5 A and CT2 = 100 / 5 A, then in order to sum these, CT2 is scaled to the CT1 ratio. In this case, the base quantity will be 5 A secondary or 300 A primary.

For voltage elements the ‘base quantity’ is the nominal primary voltage of the protected system which corresponds (based on VT ratio and connection) to secondary VT voltage applied to the relay.

For example, on a system with a 13.8 kV nominal primary voltage and with 14400:120 V Delta-connected VTs, the secondary nominal voltage (1 pu) would be:

$$\frac{13800}{14400} \times 120 = 115 \text{ V} \quad \textbf{(EQ 5.1)}$$

For Wye-connected VTs, the secondary nominal voltage (1 pu) would be:

$$\frac{13800}{14400} \times \frac{120}{\sqrt{3}} = 66.4 \text{ V} \quad \textbf{(EQ 5.2)}$$

Many settings are common to most elements and are discussed below:

- **FUNCTION setting:** This setting programs the element to be operational when selected as “Enabled”. The factory default is “Disabled”. Once programmed to “Enabled”, any element associated with the Function becomes active and all options become available.
- **NAME setting:** This setting is used to uniquely identify the element.
- **SOURCE setting:** This setting is used to select the parameter or set of parameters to be monitored.
- **PICKUP setting:** For simple elements, this setting is used to program the level of the measured parameter above or below which the pickup state is established. In more complex elements, a set of settings may be provided to define the range of the measured parameters which will cause the element to pickup.
- **PICKUP DELAY setting:** This setting sets a time-delay-on-pickup, or on-delay, for the duration between the Pickup and Operate output states.
- **RESET DELAY setting:** This setting is used to set a time-delay-on-dropout, or off-delay, for the duration between the Operate output state and the return to logic 0 after the input transits outside the defined pickup range.
- **BLOCK setting:** The default output operand state of all comparators is a logic 0 or “flag not set”. The comparator remains in this default state until a logic 1 is asserted at the RUN input, allowing the test to be performed. If the RUN input changes to logic 0 at any time, the comparator returns to the default state. The RUN input is used to supervise the comparator. The BLOCK input is used as one of the inputs to RUN control.

- **TARGET setting:** This setting is used to define the operation of an element target message. When set to Disabled, no target message or illumination of a faceplate LED indicator is issued upon operation of the element. When set to Self-Reset, the target message and LED indication follow the Operate state of the element, and self-resets once the operate element condition clears. When set to Latched, the target message and LED indication will remain visible after the element output returns to logic 0 - until a RESET command is received by the relay.
- **EVENTS setting:** This setting is used to control whether the Pickup, Dropout or Operate states are recorded by the event recorder. When set to Disabled, element pickup, dropout or operate are not recorded as events. When set to Enabled, events are created for:

  (Element) PKP (pickup)
  (Element) DPO (dropout)
  (Element) OP (operate)

  The DPO event is created when the measure and decide comparator output transits from the pickup state (logic 1) to the dropout state (logic 0). This could happen when the element is in the operate state if the reset delay time is not '0'.

5.1.3 INTRODUCTION TO AC SOURCES

a) BACKGROUND

The L60 can be ordered with one or two CT/VT modules. With one module, the L60 will support complete phase comparison functionality as well as backup current functions. Only one three-phase CT input is available for line currents with one CT/VT module. If two breakers are involved in an application, the current must be summed externally. With two CT/VT modules, the L60 allows the connection of two breaker CTs directly to the relay, processing the currents individually for some functions and summing them for other functions by employing the 'sources' mechanism. Two CT/VT modules are generally required on systems with breaker-and-a-half or ring bus configurations.

In these applications, each of the two three-phase sets of individual phase currents (one associated with each breaker) can be used as an input to a breaker failure element. The sum of both breaker phase currents and 3I_0 residual currents may be required for the circuit relaying and metering functions. Two separate synchrocheck elements can be programmed to check synchronization between two different buses VT and the line VT. These requirements can be satisfied with a single L60, equipped with sufficient CT and VT input channels, by selecting proper parameter to measure. A mechanism is provided to specify the AC parameter (or group of parameters) used as the input to protection/control comparators and some metering elements. Selection of the measured parameter(s) is partially performed by the design of a measuring element or protection/control comparator by identifying the measured parameter type (fundamental frequency phasor, harmonic phasor, symmetrical component, total waveform RMS magnitude, phase-phase or phase-ground voltage, etc.). The user completes the process by selecting the instrument transformer input channels to use and some parameters calculated from these channels. The input parameters available include the summation of currents from multiple input channels. For the summed currents of phase, 3I_0, and ground current, current from CTs with different ratios are adjusted to a single ratio before summation. A mechanism called a "Source" configures the routing of CT and VT input channels to measurement sub-systems.

Sources, in the context of L60 series relays, refer to the logical grouping of current and voltage signals such that one source contains all the signals required to measure the load or fault in a particular power apparatus. A given source may contain all or some of the following signals: three-phase currents, single-phase ground current, three-phase voltages and an auxiliary voltages from a single-phase VT for checking for synchronism.

To illustrate the concept of sources, as applied to current inputs only, consider the breaker-and-a-half scheme below. Some protection elements, like breaker failure, require individual CT current as an input. Other elements, like distance, require the sum of both current as an input. The phase comparison function requires the CT currents to be processed individually to cope with a possible CT saturation of one CT during an external fault on the upper bus. The current into protected line is the phasor sum (or difference) of the currents in CT1 and CT2, depending on the current distribution on the upper bus.

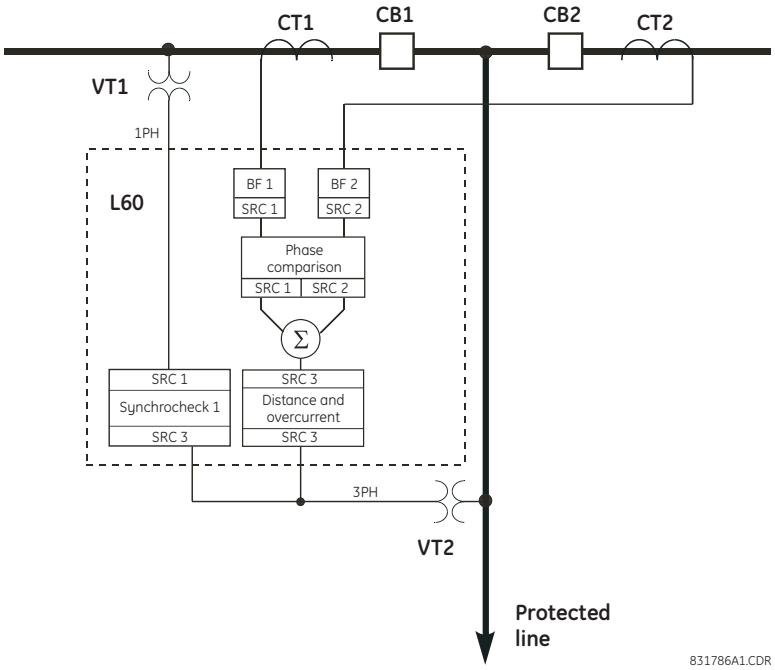


Figure 5–1: BREAKER-AND-A-HALF SCHEME

If the relay contains one CT/VT module, then only SRC1 is available and this will be used by 87PC function. If the relay contains two CT/VT modules, the following table explains how to configure the sources for full functionality.

Table 5–1: SOURCE CONFIGURATION FOR PHASE COMPARISON

FUNCTION	CT/VT MODULE 1 (TYPE 8P)		CT/VT MODULE 1 (TYPE 8F)	
	SRC 1	SRC 2	SRC 3	SRC 4
Phase current	F1 to F3 CT channels (used for 87PC first current and Breaker Failure 1)	Not available	L1 to L3 CT channels (used for 87PC second current and Breaker Failure 2). This source is configurable only if a second CT/VT module is ordered.	Sum of F1:F3 and L1:L3 (used for distance and overcurrent)
Ground current	F1 (Ground overcurrent)	Not available	---	---
Phase voltage	Not available	Not available	---	Three-phase line VT for distance and synchrocheck
Auxiliary voltage	Not available	Not available	Single-phase bus VT for synchrocheck	---

b) CT/VT MODULE CONFIGURATION

CT and VT input channels are contained in CT/VT modules. The type of input channel can be phase/neutral/other voltage, phase/ground current, or sensitive ground current. The CT/VT modules calculate total waveform RMS levels, fundamental frequency phasors, symmetrical components and harmonics for voltage or current, as allowed by the hardware in each channel. These modules may calculate other parameters as directed by the CPU module.

A CT/VT module contains up to eight input channels, numbered 1 through 8. The channel numbering corresponds to the module terminal numbering 1 through 8 and is arranged as follows: Channels 1, 2, 3 and 4 are always provided as a group, hereafter called a "bank," and all four are either current or voltage, as are channels 5, 6, 7 and 8. Channels 1, 2, 3 and 5, 6, 7 are arranged as phase A, B and C respectively. Channels 4 and 8 are either another current or voltage.

Banks are ordered sequentially from the block of lower-numbered channels to the block of higher-numbered channels, and from the CT/VT module with the lowest slot position letter to the module with the highest slot position letter, as follows:

INCREASING SLOT POSITION LETTER -->		
CT/VT MODULE 1	**CT/VT MODULE 2**	**CT/VT MODULE 3**
< bank 1 >	< bank 3 >	< bank 5 >
< bank 2 >	< bank 4 >	< bank 6 >

The UR platform allows for a maximum of three sets of three-phase voltages and six sets of three-phase currents. The result of these restrictions leads to the maximum number of CT/VT modules in a chassis to three. The maximum number of sources is six. A summary of CT/VT module configurations is shown below.

ITEM	MAXIMUM NUMBER
CT/VT Module	1
CT Bank (3 phase channels, 1 ground channel)	2
VT Bank (3 phase channels, 1 auxiliary channel)	1

c) CT/VT INPUT CHANNEL CONFIGURATION

Upon relay startup, configuration settings for every bank of current or voltage input channels in the relay are automatically generated from the order code. Within each bank, a channel identification label is automatically assigned to each bank of channels in a given product. The 'bank' naming convention is based on the physical location of the channels, required by the user to know how to connect the relay to external circuits. Bank identification consists of the letter designation of the slot in which the CT/VT module is mounted as the first character, followed by numbers indicating the channel, either 1 or 5.

For three-phase channel sets, the number of the lowest numbered channel identifies the set. For example, F1 represents the three-phase channel set of F1/F2/F3, where F is the slot letter and 1 is the first channel of the set of three channels.

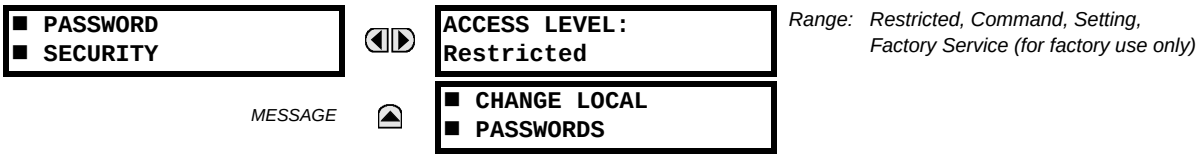
Upon startup, the CPU configures the settings required to characterize the current and voltage inputs, and will display them in the appropriate section in the sequence of the banks (as described above) as follows for a maximum configuration: F1, F5, L1, L5, S1, and S5.

The above section explains how the input channels are identified and configured to the specific application instrument transformers and the connections of these transformers. The specific parameters to be used by each measuring element and comparator, and some actual values are controlled by selecting a specific source. The source is a group of current and voltage input channels selected by the user to facilitate this selection. With this mechanism, a user does not have to make multiple selections of voltage and current for those elements that need both parameters, such as a distance element or a watt calculation. It also gathers associated parameters for display purposes.

The basic idea of arranging a source is to select a point on the power system where information is of interest. An application example of the grouping of parameters in a source is a transformer winding, on which a three phase voltage is measured, and the sum of the currents from CTs on each of two breakers is required to measure the winding current flow.

5.2.1 PASSWORD SECURITY

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨ PASSWORD SECURITY



Two levels of password security are provided: command and setting.

The following operations are under command password supervision:

- Operating the breakers via faceplate keypad.
- Changing the state of virtual inputs
- Clearing the event records.
- Clearing the oscillography records.
- Clearing fault reports.
- Changing the date and time.
- Clearing the breaker arcing current.
- Clearing energy records.
- Clearing the data logger.
- Clearing the user-programmable pushbuttons.

The following operations are under setting password supervision:

- Changing any setting.
- Test mode operation.

The command and setting passwords are defaulted to “Null” when the relay is shipped from the factory. When a password is set to “Null”, the password security feature is disabled.

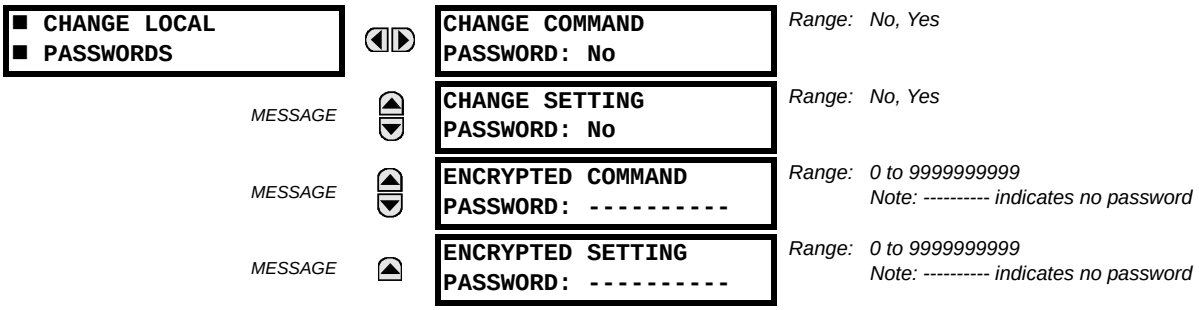
The L60 supports password entry from a local or remote connection.

Local access is defined as any access to settings or commands via the faceplate interface. This includes both keypad entry and the faceplate RS232 connection. Remote access is defined as any access to settings or commands via any rear communications port. This includes both Ethernet and RS485 connections. Any changes to the local or remote passwords enables this functionality.

When entering a settings or command password via EnerVista or any serial interface, the user must enter the corresponding connection password. If the connection is to the back of the L60, the remote password must be used. If the connection is to the RS232 port of the faceplate, the local password must be used.

The local password settings are shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨ PASSWORD SECURITY ⇨ CHANGE LOCAL PASSWORDS



Programming a password code is required to enable each access level. A password consists of 1 to 10 numerical characters. When a **CHANGE ... PASSWORD** setting is set to "Yes", the following message sequence is invoked:

1. ENTER NEW PASSWORD: _____
2. VERIFY NEW PASSWORD: _____
3. NEW PASSWORD HAS BEEN STORED

To gain write access to a "Restricted" setting, set **ACCESS LEVEL** to "Setting" and then change the setting, or attempt to change the setting and follow the prompt to enter the programmed password. If the password is correctly entered, access will be allowed. If no keys are pressed for longer than 30 minutes or control power is cycled, accessibility will automatically revert to the "Restricted" level.

If an entered password is lost (or forgotten), consult the factory with the corresponding **ENCRYPTED PASSWORD**.

In the event that an incorrect Command or Setting password has been entered via the faceplate interface three times within a three-minute time span, the LOCAL ACCESS DENIED FlexLogic™ operand will be set to “On” and the L60 will not allow Settings or Command access via the faceplate interface for the next ten minutes. The **TOO MANY ATTEMPTS – BLOCKED FOR 10 MIN!** flash message will appear upon activation of the ten minute timeout or any other time a user attempts any change to the defined tier during the ten minute timeout. The LOCAL ACCESS DENIED FlexLogic™ operand will be set to “Off” after the expiration of the ten-minute timeout.

In the event that an incorrect Command or Setting password has been entered via the any external communications interface three times within a three-minute time span, the REMOTE ACCESS DENIED FlexLogic™ operand will be set to “On” and the L60 will not allow Settings or Command access via the any external communications interface for the next ten minutes. The REMOTE ACCESS DENIED FlexLogic™ operand will be set to “Off” after the expiration of the ten-minute timeout.

The L60 provides a means to raise an alarm upon failed password entry. Should password verification fail while accessing a password-protected level of the relay (either settings or commands), the UNAUTHORIZED ACCESS FlexLogic™ operand is asserted. The operand can be programmed to raise an alarm via contact outputs or communications. This feature can be used to protect against both unauthorized and accidental access attempts.

The UNAUTHORIZED ACCESS operand is reset with the **COMMANDS ⇨⇩ CLEAR RECORDS ⇨⇩ RESET UNAUTHORIZED ALARMS** command. Therefore, to apply this feature with security, the command level should be password-protected.

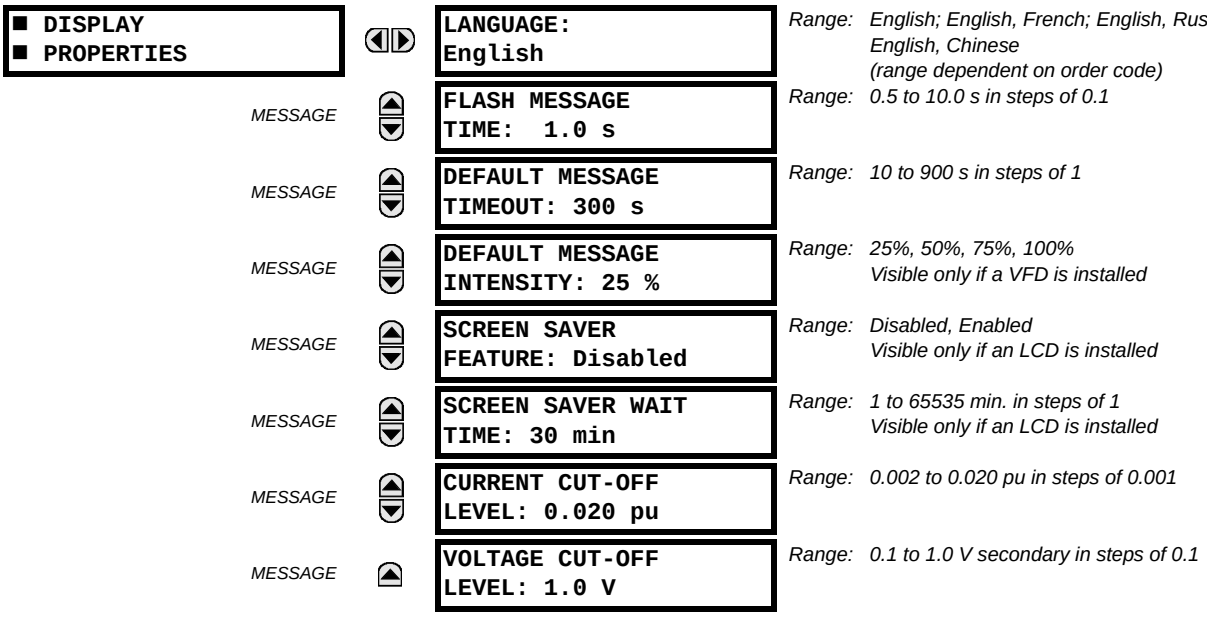
The operand does not generate events or targets. If these are required, the operand can be assigned to a digital element programmed with event logs and/or targets enabled.

If the SETTING and COMMAND passwords are identical, this one password allows access to both commands and settings.

When EnerVista UR Setup is used to access a particular level, the user will continue to have access to that level as long as there are open windows in the EnerVista UR Setup software. To re-establish the Password Security feature, all windows must be closed for at least 30 minutes.

5.2.2 DISPLAY PROPERTIES

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ DISPLAY PROPERTIES



5

Some relay messaging characteristics can be modified to suit different situations using the display properties settings.

- **LANGUAGE**: This setting selects the language used to display settings, actual values, and targets. The range is dependent on the order code of the relay.
- **FLASH MESSAGE TIME**: Flash messages are status, warning, error, or information messages displayed for several seconds in response to certain key presses during setting programming. These messages override any normal messages. The duration of a flash message on the display can be changed to accommodate different reading rates.
- **DEFAULT MESSAGE TIMEOUT**: If the keypad is inactive for a period of time, the relay automatically reverts to a default message. The inactivity time is modified via this setting to ensure messages remain on the screen long enough during programming or reading of actual values.
- **DEFAULT MESSAGE INTENSITY**: To extend phosphor life in the vacuum fluorescent display, the brightness can be attenuated during default message display. During keypad interrogation, the display always operates at full brightness.
- **SCREEN SAVER FEATURE** and **SCREEN SAVER WAIT TIME**: These settings are only visible if the L60 has a liquid crystal display (LCD) and control its backlighting. When the **SCREEN SAVER FEATURE** is "Enabled", the LCD backlighting is turned off after the **DEFAULT MESSAGE TIMEOUT** followed by the **SCREEN SAVER WAIT TIME**, providing that no keys have been pressed and no target messages are active. When a keypress occurs or a target becomes active, the LCD backlighting is turned on.
- **CURRENT CUT-OFF LEVEL**: This setting modifies the current cut-off threshold. Very low currents (1 to 2% of the rated value) are very susceptible to noise. Some customers prefer very low currents to display as zero, while others prefer the current be displayed even when the value reflects noise rather than the actual signal. The L60 applies a cut-off value to the magnitudes and angles of the measured currents. If the magnitude is below the cut-off level, it is substituted with zero. This applies to phase and ground current phasors as well as true RMS values and symmetrical components. The cut-off operation applies to quantities used for metering, protection, and control, as well as those used by communications protocols. Note that the cut-off level for the sensitive ground input is 10 times lower that the **CURRENT CUT-OFF LEVEL** setting value. Raw current samples available via oscillography are not subject to cut-off.
- **VOLTAGE CUT-OFF LEVEL**: This setting modifies the voltage cut-off threshold. Very low secondary voltage measurements (at the fractional volt level) can be affected by noise. Some customers prefer these low voltages to be displayed as zero, while others prefer the voltage to be displayed even when the value reflects noise rather than the actual signal. The L60 applies a cut-off value to the magnitudes and angles of the measured voltages. If the magnitude is below the cut-off level, it is substituted with zero. This operation applies to phase and auxiliary voltages, and symmetrical

components. The cut-off operation applies to quantities used for metering, protection, and control, as well as those used by communications protocols. Raw samples of the voltages available via oscillography are not subject cut-off.

The **CURRENT CUT-OFF LEVEL** and the **VOLTAGE CUT-OFF LEVEL** are used to determine the metered power cut-off levels. The power cut-off level is calculated as shown below. For Delta connections:

$$\text{3-phase power cut-off} = \frac{\sqrt{3} \times \textbf{CURRENT CUT-OFF LEVEL} \times \textbf{VOLTAGE CUT-OFF LEVEL} \times \text{VT primary} \times \text{CT primary}}{\text{VT secondary}} \quad \textbf{(EQ 5.3)}$$

For Wye connections:

$$\text{3-phase power cut-off} = \frac{3 \times \textbf{CURRENT CUT-OFF LEVEL} \times \textbf{VOLTAGE CUT-OFF LEVEL} \times \text{VT primary} \times \text{CT primary}}{\text{VT secondary}} \quad \textbf{(EQ 5.4)}$$

$$\text{per-phase power cut-off} = \frac{\textbf{CURRENT CUT-OFF LEVEL} \times \textbf{VOLTAGE CUT-OFF LEVEL} \times \text{VT primary} \times \text{CT primary}}{\text{VT secondary}} \quad \textbf{(EQ 5.5)}$$

where VT primary = VT secondary × VT ratio and CT primary = CT secondary × CT ratio.

For example, given the following settings:

CURRENT CUT-OFF LEVEL: “0.02 pu”
VOLTAGE CUT-OFF LEVEL: “1.0 V”
PHASE CT PRIMARY: “100 A”
PHASE VT SECONDARY: “66.4 V”
PHASE VT RATIO: “208.00 : 1"
PHASE VT CONNECTION: “Delta”.

We have:

CT primary = “100 A”, and
VT primary = **PHASE VT SECONDARY** x **PHASE VT RATIO** = 66.4 V x 208 = 13811.2 V

The power cut-off is therefore:

power cut-off = (**CURRENT CUT-OFF LEVEL** × **VOLTAGE CUT-OFF LEVEL** × CT primary × VT primary)/VT secondary
= ($\sqrt{3}$ × 0.02 pu × 1.0 V × 100 A × 13811.2 V) / 66.4 V
= 720.5 watts

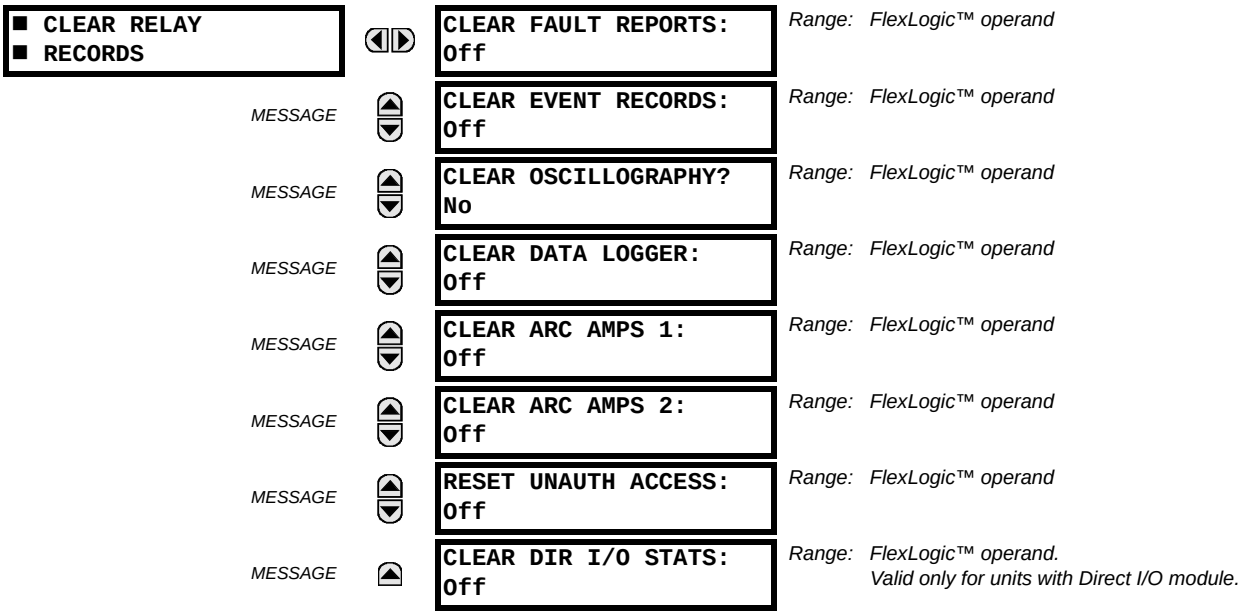
Any calculated power value below this cut-off will not be displayed. As well, the three-phase energy data will not accumulate if the total power from all three phases does not exceed the power cut-off.

NOTE

Lower the VOLTAGE CUT-OFF LEVEL and CURRENT CUT-OFF LEVEL with care as the relay accepts lower signals as valid measurements. Unless dictated otherwise by a specific application, the default settings of “0.02 pu” for CURRENT CUT-OFF LEVEL and “1.0 V” for VOLTAGE CUT-OFF LEVEL are recommended.

5.2.3 CLEAR RELAY RECORDS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ CLEAR RELAY RECORDS



Selected records can be cleared from user-programmable conditions with FlexLogic™ operands. Assigning user-programmable pushbuttons to clear specific records are typical applications for these commands. Since the L60 responds to rising edges of the configured FlexLogic™ operands, they must be asserted for at least 50 ms to take effect.

Clearing records with user-programmable operands is not protected by the command password. However, user-programmable pushbuttons are protected by the command password. Thus, if they are used to clear records, the user-programmable pushbuttons can provide extra security if required.

For example, to assign User-Programmable Pushbutton 1 to clear demand records, the following settings should be applied.

1. Assign the clear demand function to Pushbutton 1 by making the following change in the SETTINGS ⇨ PRODUCT SETUP ⇨⇩ CLEAR RELAY RECORDS menu:

   CLEAR DEMAND: "PUSHBUTTON 1 ON"

2. Set the properties for User-Programmable Pushbutton 1 by making the following changes in the SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE PUSHBUTTONS ⇨ USER PUSHBUTTON 1 menu:

   PUSHBUTTON 1 FUNCTION: "Self-reset"
   PUSHBTN 1 DROP-OUT TIME: "0.20 s"

a) MAIN MENU

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS

■ COMMUNICATIONS ■		■ SERIAL PORTS ■	See below.
	MESSAGE	■ NETWORK ■	See page 5–14.
	MESSAGE	■ MODBUS PROTOCOL ■	See page 5–14.
	MESSAGE	■ DNP PROTOCOL ■	See page 5–15.
	MESSAGE	■ DNP / IEC104 ■ POINT LISTS	See page 5–18.
	MESSAGE	■ IEC 61850 PROTOCOL ■	See page 5–19.
	MESSAGE	■ WEB SERVER ■ HTTP PROTOCOL	See page 5–28.
	MESSAGE	■ TFTP PROTOCOL ■	See page 5–28.
	MESSAGE	■ IEC 60870-5-104 ■ PROTOCOL	See page 5–29.
	MESSAGE	■ SNTP PROTOCOL ■	See page 5–29.

b) SERIAL PORTS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨ SERIAL PORTS

■ SERIAL PORTS ■		RS485 COM1 BAUD RATE: 19200	Range: 300, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 57600, 115200. Only active if CPU Type E is ordered.
	MESSAGE	RS485 COM1 PARITY: None	Range: None, Odd, Even Only active if CPU Type E is ordered
	MESSAGE	RS485 COM1 RESPONSE MIN TIME: 0 ms	Range: 0 to 1000 ms in steps of 10 Only active if CPU Type E is ordered
	MESSAGE	RS485 COM2 BAUD RATE: 19200	Range: 300, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 57600, 115200
	MESSAGE	RS485 COM2 PARITY: None	Range: None, Odd, Even
	MESSAGE	RS485 COM2 RESPONSE MIN TIME: 0 ms	Range: 0 to 1000 ms in steps of 10

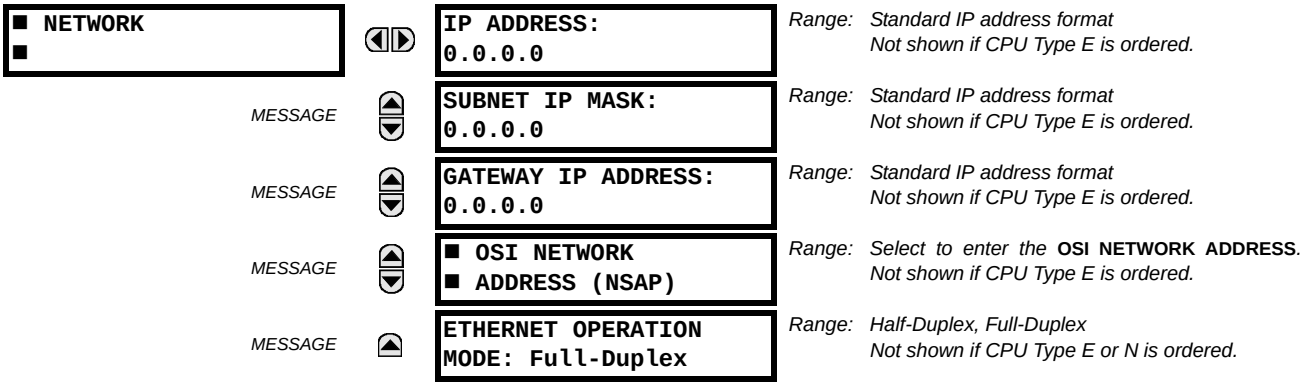
The L60 is equipped with up to three independent serial communication ports. The faceplate RS232 port is intended for local use and is fixed at 19200 baud and no parity. The rear COM1 port type is selected when ordering: either an Ethernet or RS485 port. The rear COM2 port is RS485. The RS485 ports have settings for baud rate and parity. It is important that these parameters agree with the settings used on the computer or other equipment that is connected to these ports. Any of these ports may be connected to a computer running EnerVista UR Setup. This software can download and upload setting files, view measured parameters, and upgrade the relay firmware. A maximum of 32 relays can be daisy-chained and connected to a DCS, PLC or PC using the RS485 ports.

NOTE

For each RS485 port, the minimum time before the port will transmit after receiving data from a host can be set. This feature allows operation with hosts which hold the RS485 transmitter active for some time after each transmission.

c) NETWORK

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ NETWORK



These messages appear only if the L60 is ordered with an Ethernet card.

The IP addresses are used with the DNP, Modbus/TCP, IEC 61580, IEC 60870-5-104, TFTP, and HTTP protocols. The NSAP address is used with the IEC 61850 protocol over the OSI (CLNP/TP4) stack only. Each network protocol has a setting for the TCP/UDP port number. These settings are used only in advanced network configurations and should normally be left at their default values, but may be changed if required (for example, to allow access to multiple UR-series relays behind a router). By setting a different **TCP/UDP PORT NUMBER** for a given protocol on each UR-series relay, the router can map the relays to the same external IP address. The client software (EnerVista UR Setup, for example) must be configured to use the correct port number if these settings are used.

NOTE

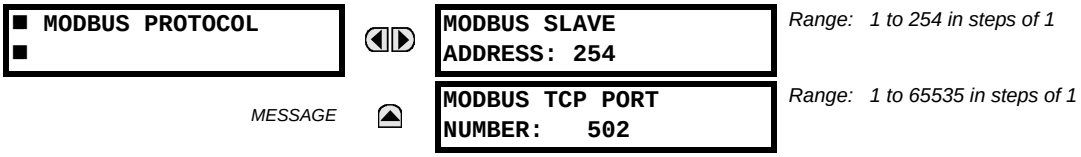
When the NSAP address, any TCP/UDP port number, or any user map setting (when used with DNP) is changed, it will not become active until power to the relay has been cycled (off-on).

WARNING

Do not set more than one protocol to the same TCP/UDP PORT NUMBER, as this will result in unreliable operation of those protocols.

d) MODBUS PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ MODBUS PROTOCOL



The serial communication ports utilize the Modbus protocol, unless configured for DNP or IEC 60870-5-104 operation (see descriptions below). This allows the EnerVista UR Setup software to be used. The UR operates as a Modbus slave device only. When using Modbus protocol on the RS232 port, the L60 will respond regardless of the **MODBUS SLAVE ADDRESS** programmed. For the RS485 ports each L60 must have a unique address from 1 to 254. Address 0 is the broadcast address which all Modbus slave devices listen to. Addresses do not have to be sequential, but no two devices can have the same address or conflicts resulting in errors will occur. Generally, each device added to the link should use the next higher address starting at 1. Refer to Appendix B for more information on the Modbus protocol.

NOTE

Changes to the MODBUS TCP PORT NUMBER setting will not take effect until the L60 is restarted.

e) DNP PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ DNP PROTOCOL

■ DNP PROTOCOL ■	■ DNP CHANNELS ■	Range: see sub-menu below
MESSAGE	DNP ADDRESS: 65519	Range: 0 to 65519 in steps of 1
MESSAGE	■ DNP NETWORK ■ CLIENT ADDRESSES	Range: see sub-menu below
MESSAGE	DNP TCP/UDP PORT NUMBER: 20000	Range: 1 to 65535 in steps of 1
MESSAGE	DNP UNSOL RESPONSE FUNCTION: Disabled	Range: Enabled, Disabled
MESSAGE	DNP UNSOL RESPONSE TIMEOUT: 5 s	Range: 0 to 60 s in steps of 1
MESSAGE	DNP UNSOL RESPONSE MAX RETRIES: 10	Range: 1 to 255 in steps of 1
MESSAGE	DNP UNSOL RESPONSE DEST ADDRESS: 1	Range: 0 to 65519 in steps of 1
MESSAGE	DNP CURRENT SCALE FACTOR: 1	Range: 0.001, 0.01. 0.1, 1, 10, 100, 1000, 10000, 100000
MESSAGE	DNP VOLTAGE SCALE FACTOR: 1	Range: 0.001, 0.01. 0.1, 1, 10, 100, 1000, 10000, 100000
MESSAGE	DNP POWER SCALE FACTOR: 1	Range: 0.001, 0.01. 0.1, 1, 10, 100, 1000, 10000, 100000
MESSAGE	DNP ENERGY SCALE FACTOR: 1	Range: 0.001, 0.01. 0.1, 1, 10, 100, 1000, 10000, 100000
MESSAGE	DNP PF SCALE FACTOR: 1	Range: 0.001, 0.01. 0.1, 1, 10, 100, 1000, 10000, 100000
MESSAGE	DNP OTHER SCALE FACTOR: 1	Range: 0.001, 0.01. 0.1, 1, 10, 100, 1000, 10000, 100000
MESSAGE	DNP CURRENT DEFAULT DEADBAND: 30000	Range: 0 to 100000000 in steps of 1
MESSAGE	DNP VOLTAGE DEFAULT DEADBAND: 30000	Range: 0 to 100000000 in steps of 1
MESSAGE	DNP POWER DEFAULT DEADBAND: 30000	Range: 0 to 100000000 in steps of 1
MESSAGE	DNP ENERGY DEFAULT DEADBAND: 30000	Range: 0 to 100000000 in steps of 1
MESSAGE	DNP PF DEFAULT DEADBAND: 30000	Range: 0 to 100000000 in steps of 1
MESSAGE	DNP OTHER DEFAULT DEADBAND: 30000	Range: 0 to 100000000 in steps of 1
MESSAGE	DNP TIME SYNC IIN PERIOD: 1440 min	Range: 1 to 10080 min. in steps of 1

MESSAGE

DNP MESSAGE FRAGMENT SIZE: 240 — Range: 30 to 2048 in steps of 1

MESSAGE

DNP OBJECT 1 DEFAULT VARIATION: 2 — Range: 1, 2

MESSAGE

DNP OBJECT 2 DEFAULT VARIATION: 2 — Range: 1, 2

MESSAGE

DNP OBJECT 20 DEFAULT VARIATION: 1 — Range: 1, 2, 5, 6

MESSAGE

DNP OBJECT 21 DEFAULT VARIATION: 1 — Range: 1, 2, 9, 10

MESSAGE

DNP OBJECT 22 DEFAULT VARIATION: 1 — Range: 1, 2, 5, 6

MESSAGE

DNP OBJECT 23 DEFAULT VARIATION: 2 — Range: 1, 2, 5, 6

MESSAGE

DNP OBJECT 30 DEFAULT VARIATION: 1 — Range: 1, 2, 3, 4, 5

MESSAGE

DNP OBJECT 32 DEFAULT VARIATION: 1 — Range: 1, 2, 3, 4, 5, 7

MESSAGE

DNP NUMBER OF PAIRED CONTROL POINTS: 0 — Range: 0 to 32 in steps of 1

MESSAGE

DNP TCP CONNECTION TIMEOUT: 120 s — Range: 10 to 300 s in steps of 1

The L60 supports the Distributed Network Protocol (DNP) version 3.0. The L60 can be used as a DNP slave device connected to multiple DNP masters (usually an RTU or a SCADA master station). Since the L60 maintains two sets of DNP data change buffers and connection information, two DNP masters can actively communicate with the L60 at one time.

NOTE

The IEC 60870-5-104 and DNP protocols cannot be simultaneously. When the IEC 60870-5-104 FUNCTION setting is set to "Enabled", the DNP protocol will not be operational. When this setting is changed it will not become active until power to the relay has been cycled (off-to-on).

The DNP Channels sub-menu is shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ DNP PROTOCOL ⇨ DNP CHANNELS

■ DNP CHANNELS ■

DNP CHANNEL 1 PORT: NETWORK — Range: NONE, COM1 - RS485, COM2 - RS485, FRONT PANEL - RS232, NETWORK - TCP, NETWORK - UDP

MESSAGE

DNP CHANNEL 2 PORT: COM2 - RS485 — Range: NONE, COM1 - RS485, COM2 - RS485, FRONT PANEL - RS232, NETWORK - TCP, NETWORK - UDP

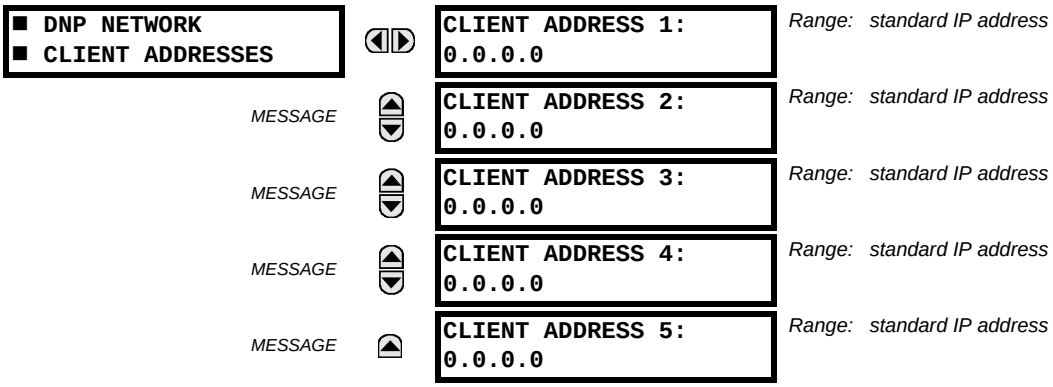
The **DNP CHANNEL 1(2) PORT** settings select the communications port assigned to the DNP protocol for each channel. Once DNP is assigned to a serial port, the Modbus protocol is disabled on that port. Note that COM1 can be used only in non-Ethernet UR relays. When this setting is set to "Network - TCP", the DNP protocol can be used over TCP/IP on channels 1 or 2. When this value is set to "Network - UDP", the DNP protocol can be used over UDP/IP on channel 1 only. Refer to *Appendix E* for additional information on the DNP protocol.

NOTE

Changes to the DNP CHANNEL 1(2) PORT settings will take effect only after power has been cycled to the relay.

The **DNP NETWORK CLIENT ADDRESS** settings can force the L60 to respond to a maximum of five specific DNP masters. The settings in this sub-menu are shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ DNP PROTOCOL ⇨ DNP NETWORK CLIENT ADDRESSES



The **DNP UNSOL RESPONSE FUNCTION** should be "Disabled" for RS485 applications since there is no collision avoidance mechanism. The **DNP UNSOL RESPONSE TIMEOUT** sets the time the L60 waits for a DNP master to confirm an unsolicited response. The **DNP UNSOL RESPONSE MAX RETRIES** setting determines the number of times the L60 retransmits an unsolicited response without receiving confirmation from the master; a value of "255" allows infinite re-tries. The **DNP UNSOL RESPONSE DEST ADDRESS** is the DNP address to which all unsolicited responses are sent. The IP address to which unsolicited responses are sent is determined by the L60 from the current TCP connection or the most recent UDP message.

The DNP scale factor settings are numbers used to scale analog input point values. These settings group the L60 analog input data into the following types: current, voltage, power, energy, power factor, and other. Each setting represents the scale factor for all analog input points of that type. For example, if the **DNP VOLTAGE SCALE FACTOR** setting is set to "1000", all DNP analog input points that are voltages will be returned with values 1000 times smaller (for example, a value of 72000 V on the L60 will be returned as 72). These settings are useful when analog input values must be adjusted to fit within certain ranges in DNP masters. Note that a scale factor of 0.1 is equivalent to a multiplier of 10 (that is, the value will be 10 times larger).

The **DNP DEFAULT DEADBAND** settings determine when to trigger unsolicited responses containing analog input data. These settings group the L60 analog input data into the following types: current, voltage, power, energy, power factor, and other. Each setting represents the default deadband value for all analog input points of that type. For example, to trigger unsolicited responses from the L60 when any current values change by 15 A, the **DNP CURRENT DEFAULT DEADBAND** setting should be set to "15". Note that these settings are the deadband default values. DNP object 34 points can be used to change deadband values, from the default, for each individual DNP analog input point. Whenever power is removed and re-applied to the L60, the default deadbands will be in effect.

NOTE

The L60 relay does not support energy metering. As such, the **DNP ENERGY SCALE FACTOR** and **DNP ENERGY DEFAULT DEADBAND** settings are not applicable.

The **DNP TIME SYNC IIN PERIOD** setting determines how often the Need Time Internal Indication (IIN) bit is set by the L60. Changing this time allows the DNP master to send time synchronization commands more or less often, as required.

The **DNP MESSAGE FRAGMENT SIZE** setting determines the size, in bytes, at which message fragmentation occurs. Large fragment sizes allow for more efficient throughput; smaller fragment sizes cause more application layer confirmations to be necessary which can provide for more robust data transfer over noisy communication channels.

NOTE

When the DNP data points (analog inputs and/or binary inputs) are configured for Ethernet-enabled relays, check the "DNP Points Lists" L60 web page to view the points lists. This page can be viewed with a web browser by entering the L60 IP address to access the L60 "Main Menu", then by selecting the "Device Information Menu" > "DNP Points Lists" menu item.

The **DNP OBJECT 1(32) DEFAULT VARIATION** settings allow the user to select the DNP default variation number for object types 1, 2, 20, 21, 22, 23, 30, and 32. The default variation refers to the variation response when variation 0 is requested and/or in class 0, 1, 2, or 3 scans. Refer to the *DNP Implementation* section in Appendix E for additional details.

The DNP binary outputs typically map one-to-one to IED data points. That is, each DNP binary output controls a single physical or virtual control point in an IED. In the L60 relay, DNP binary outputs are mapped to virtual inputs. However, some legacy DNP implementations use a mapping of one DNP binary output to two physical or virtual control points to support the concept of trip/close (for circuit breakers) or raise/lower (for tap changers) using a single control point. That is, the DNP master can operate a single point for both trip and close, or raise and lower, operations. The L60 can be configured to sup-

port paired control points, with each paired control point operating two virtual inputs. The **DNP NUMBER OF PAIRED CONTROL POINTS** setting allows configuration of from 0 to 32 binary output paired controls. Points not configured as paired operate on a one-to-one basis.

The **DNP ADDRESS** setting is the DNP slave address. This number identifies the L60 on a DNP communications link. Each DNP slave should be assigned a unique address.

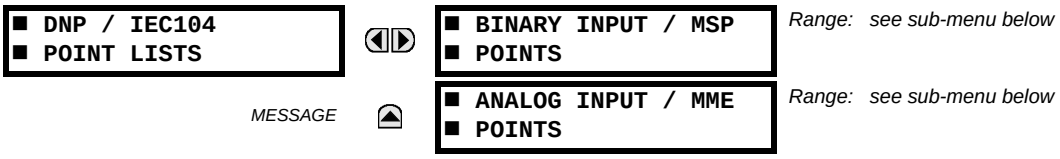
The **DNP TCP CONNECTION TIMEOUT** setting specifies a time delay for the detection of dead network TCP connections. If there is no data traffic on a DNP TCP connection for greater than the time specified by this setting, the connection will be aborted by the L60. This frees up the connection to be re-used by a client.

NOTE

Relay power must be re-cycled after changing the **DNP TCP CONNECTION TIMEOUT** setting for the changes to take effect.

f) DNP / IEC 60870-5-104 POINT LISTS

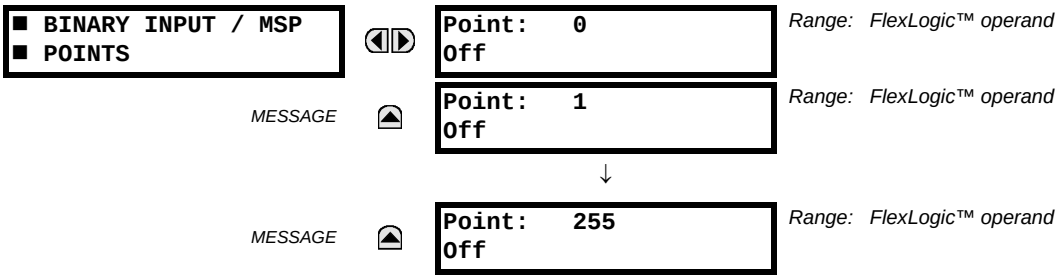
PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ DNP / IEC104 POINT LISTS



The binary and analog inputs points for the DNP protocol, or the MSP and MME points for IEC 60870-5-104 protocol, can configured to a maximum of 256 points. The value for each point is user-programmable and can be configured by assigning FlexLogic™ operands for binary inputs / MSP points or FlexAnalog parameters for analog inputs / MME points.

The menu for the binary input points (DNP) or MSP points (IEC 60870-5-104) is shown below.

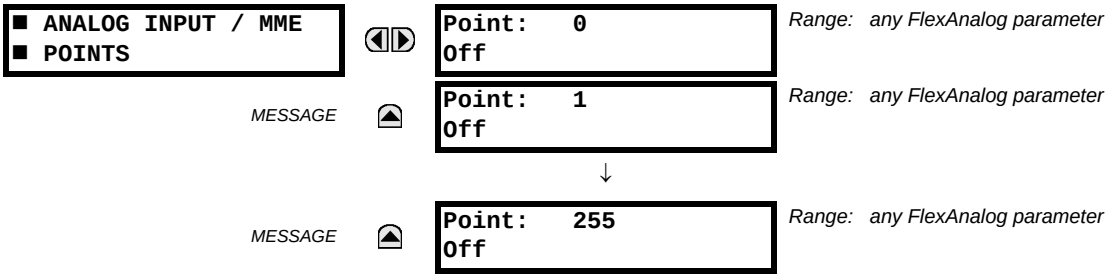
PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ DNP / IEC104 POINT LISTS ⇨ BINARY INPUT / MSP POINTS



Up to 256 binary input points can be configured for the DNP or IEC 60870-5-104 protocols. The points are configured by assigning an appropriate FlexLogic™ operand. Refer to the *Introduction to FlexLogic™* section in this chapter for the full range of assignable operands.

The menu for the analog input points (DNP) or MME points (IEC 60870-5-104) is shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ DNP / IEC104 POINT LISTS ⇨⇩ ANALOG INPUT / MME POINTS



Up to 256 analog input points can be configured for the DNP or IEC 60870-5-104 protocols. The analog point list is configured by assigning an appropriate FlexAnalog parameter to each point. Refer to Appendix A: *FlexAnalog Parameters* for the full range of assignable parameters.

NOTE

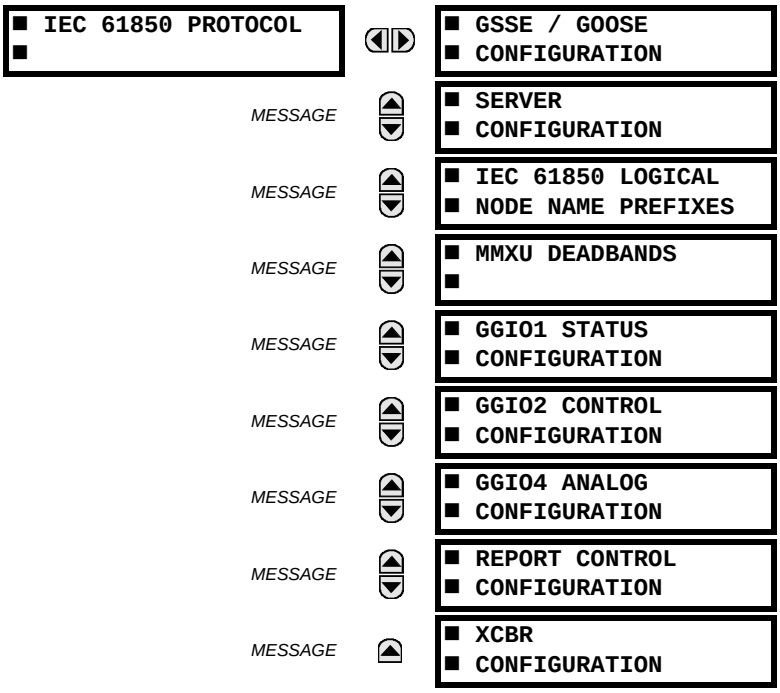
The DNP / IEC 60870-5-104 point lists always begin with point 0 and end at the first "Off" value. Since DNP / IEC 60870-5-104 point lists must be in one continuous block, any points assigned after the first "Off" point are ignored.

NOTE

Changes to the DNP / IEC 60870-5-104 point lists will not take effect until the L60 is restarted.

g) IEC 61850 PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL



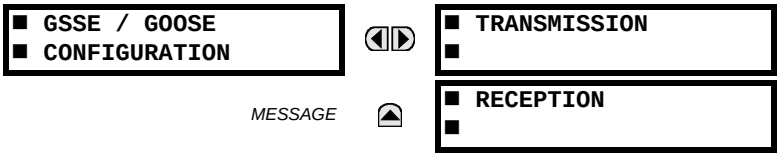
SOFTWARE OPTION

The L60 Line Phase Comparison System is provided with optional IEC 61850 communications capability. This feature is specified as a software option at the time of ordering. Refer to the *Ordering* section of chapter 2 for additional details. The IEC 61850 protocol features are not available if CPU Type E is ordered.

The L60 supports the Manufacturing Message Specification (MMS) protocol as specified by IEC 61850. MMS is supported over two protocol stacks: TCP/IP over ethernet and TP4/CLNP (OSI) over ethernet. The L60 operates as an IEC 61850 server. The *Remote Inputs/Outputs* section in this chapter describe the peer-to-peer GSSE/GOOSE message scheme.

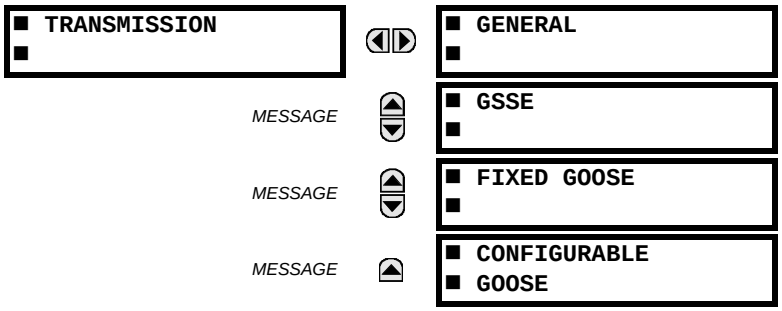
The GSSE/GOOSE configuration main menu is divided into two areas: transmission and reception.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨ GSSE/GOOSE CONFIGURATION



The main transmission menu is shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨ GSSE/GOOSE... ⇨ TRANSMISSION



The general transmission settings are shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨ GSSE/GOOSE... ⇨ TRANSMISSION ⇨ GENERAL

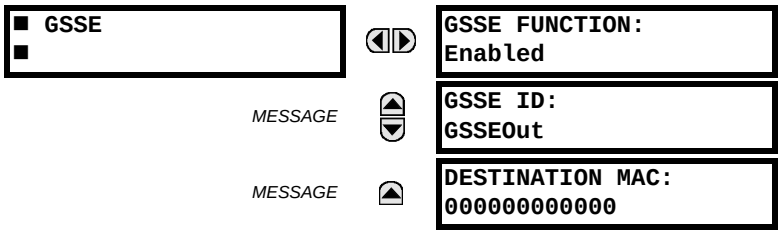
Range: 1 to 60 s in steps of 1

The **DEFAULT GSSE/GOOSE UPDATE TIME** sets the time between GSSE or GOOSE messages when there are no remote output state changes to be sent. When remote output data changes, GSSE or GOOSE messages are sent immediately. This setting controls the steady-state 'heartbeat' time interval.

The **DEFAULT GSSE/GOOSE UPDATE TIME** setting is applicable to GSSE, fixed L60 GOOSE, and configurable GOOSE.

The GSSE settings are shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨ GSSE/GOOSE... ⇨ TRANSMISSION ⇨⇩ GSEE



Range: Enabled, Disabled

Range: 65-character ASCII string

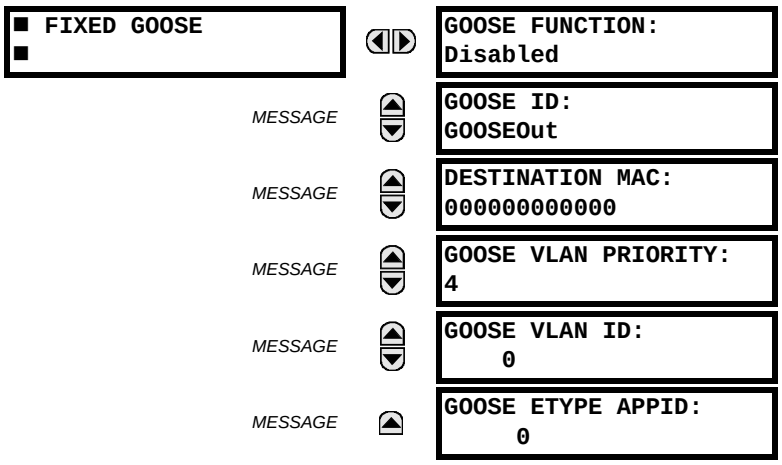
Range: standard MAC address

These settings are applicable to GSSE only. If the fixed GOOSE function is enabled, GSSE messages are not transmitted.

The **GSSE ID** setting represents the IEC 61850 GSSE application ID name string sent as part of each GSSE message. This string identifies the GSSE message to the receiving device. In L60 releases previous to 5.0x, this name string was represented by the **RELAY NAME** setting.

The fixed GOOSE settings are shown below:

PATH: SETTINGS ⇨ PRODUCT... ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨ GSSE/GOOSE... ⇨ TRANSMISSION ⇨⇩ FIXED GOOSE



Range: Enabled, Disabled

Range: 65-character ASCII string

Range: standard MAC address

Range: 0 to 7 in steps of 1

Range: 0 to 4095 in steps of 1

Range: 0 to 16383 in steps of 1

These settings are applicable to fixed (DNA/UserSt) GOOSE only.

The **GOOSE ID** setting represents the IEC 61850 GOOSE application ID (GoID) name string sent as part of each GOOSE message. This string identifies the GOOSE message to the receiving device. In revisions previous to 5.0x, this name string was represented by the **RELAY NAME** setting.

The **DESTINATION MAC** setting allows the destination Ethernet MAC address to be set. This address must be a multicast address; the least significant bit of the first byte must be set. In L60 releases previous to 5.0x, the destination Ethernet MAC address was determined automatically by taking the sending MAC address (that is, the unique, local MAC address of the L60) and setting the multicast bit.

The **GOOSE VLAN PRIORITY** setting indicates the Ethernet priority of GOOSE messages. This allows GOOSE messages to have higher priority than other Ethernet data. The **GOOSE ETYPE APPID** setting allows the selection of a specific application ID for each GOOSE sending device. This value can be left at its default if the feature is not required. Both the **GOOSE VLAN PRIORITY** and **GOOSE ETYPE APPID** settings are required by IEC 61850.

The configurable GOOSE settings are shown below:

PATH: SETTINGS... ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨ GSSE... ⇨ TRANSMISSION ⇨⇩ CONFIGURABLE GOOSE 1(8)

■ CONFIGURABLE ■ GOOSE 1		CONFIG GSE 1 FUNCTION: Enabled	*Range: Enabled, Disabled*
	MESSAGE	CONFIG GSE 1 ID: GOOSEOut_1	*Range: 65-character ASCII string*
	MESSAGE	CONFIG GSE 1 DST MAC: 010CDC010000	*Range: standard MAC address*
	MESSAGE	CONFIG GSE 1 VLAN PRIORITY: 4	*Range: 0 to 7 in steps of 1*
	MESSAGE	CONFIG GSE 1 VLAN ID: 0	*Range: 0 to 4095 in steps of 1*
	MESSAGE	CONFIG GSE 1 ETYPE APPID: 0	*Range: 0 to 16383 in steps of 1*
	MESSAGE	CONFIG GSE 1 CONFREV: 1	*Range: 0 to 4294967295 in steps of 1*
	MESSAGE	■ CONFIG GSE 1 ■ DATASET ITEMS	*Range: 64 data items; each can be set to all valid MMS data item references for transmitted data*

The configurable GOOSE settings allow the L60 to be configured to transmit a number of different datasets within IEC 61850 GOOSE messages. Up to eight different configurable datasets can be configured and transmitted. This is useful for intercommunication between L60 IEDs and devices from other manufacturers that support IEC 61850.

The configurable GOOSE feature allows for the configuration of the datasets to be transmitted or received from the L60. The L60 supports the configuration of eight (8) transmission and reception datasets, allowing for the optimization of data transfer between devices.

Items programmed for dataset 1 will have changes in their status transmitted as soon as the change is detected. Dataset 1 should be used for high-speed transmission of data that is required for applications such as transfer tripping, blocking, and breaker fail initiate. At least one digital status value needs to be configured in dataset 1 to enable transmission of all data configured for dataset 1. Configuring analog data only to dataset 1 will not activate transmission.

Items programmed for datasets 2 through 8 will have changes in their status transmitted at a maximum rate of every 100 ms. Datasets 2 through 8 will regularly analyze each data item configured within them every 100 ms to identify if any changes have been made. If any changes in the data items are detected, these changes will be transmitted through a GOOSE message. If there are no changes detected during this 100 ms period, no GOOSE message will be sent.

For all datasets 1 through 8, the integrity GOOSE message will still continue to be sent at the pre-configured rate even if no changes in the data items are detected.

The GOOSE functionality was enhanced to prevent the relay from flooding a communications network with GOOSE messages due to an oscillation being created that is triggering a message.

The L60 has the ability of detecting if a data item in one of the GOOSE datasets is erroneously oscillating. This can be caused by events such as errors in logic programming, inputs improperly being asserted and de-asserted, or failed station components. If erroneously oscillation is detected, the L60 will stop sending GOOSE messages from the dataset for a minimum period of one second. Should the oscillation persist after the one second time-out period, the L60 will continue to block transmission of the dataset. The L60 will assert the **MAINTENANCE ALERT: GGIO Ind XXX oscill** self-test error message on the front panel display, where **XXX** denotes the data item detected as oscillating.

The configurable GOOSE feature is recommended for applications that require GOOSE data transfer between UR-series IEDs and devices from other manufacturers. Fixed GOOSE is recommended for applications that require GOOSE data transfer between UR-series IEDs.

IEC 61850 GOOSE messaging contains a number of configurable parameters, all of which must be correct to achieve the successful transfer of data. It is critical that the configured datasets at the transmission and reception devices are an exact match in terms of data structure, and that the GOOSE addresses and name strings match exactly. Manual configuration is possible, but third-party substation configuration software may be used to automate the process. The EnerVista UR Setup-software can produce IEC 61850 ICD files and import IEC 61850 SCD files produced by a substation configurator (refer to the *IEC 61850 IED configuration* section later in this appendix).

The following example illustrates the configuration required to transfer IEC 61850 data items between two devices. The general steps required for transmission configuration are:

1. Configure the transmission dataset.
2. Configure the GOOSE service settings.
3. Configure the data.

The general steps required for reception configuration are:

1. Configure the reception dataset.
2. Configure the GOOSE service settings.
3. Configure the data.

This example shows how to configure the transmission and reception of three IEC 61850 data items: a single point status value, its associated quality flags, and a floating point analog value.

The following procedure illustrates the transmission configuration.

1. Configure the transmission dataset by making the following changes in the **PRODUCT SETUP ⇨⇩ COMMUNICATION ⇨⇩ IEC 61850 PROTOCOL ⇨ GSSE/GOOSE CONFIGURATION ⇨ TRANSMISSION ⇨⇩ CONFIGURABLE GOOSE ⇨ CONFIGURABLE GOOSE 1 ⇨⇩ CONFIG GSE 1 DATASET ITEMS** settings menu:
   - Set **ITEM 1** to “GGIO1.ST.Ind1.q” to indicate quality flags for GGIO1 status indication 1.
   - Set **ITEM 2** to “GGIO1.ST.Ind1.stVal” to indicate the status value for GGIO1 status indication 1.

   The transmission dataset now contains a set of quality flags and a single point status Boolean value. The reception dataset on the receiving device must exactly match this structure.
2. Configure the GOOSE service settings by making the following changes in the **PRODUCT SETUP ⇨⇩ COMMUNICATION ⇨⇩ IEC 61850 PROTOCOL ⇨ GSSE/GOOSE CONFIGURATION ⇨ TRANSMISSION ⇨⇩ CONFIGURABLE GOOSE ⇨ CONFIGURABLE GOOSE 1** settings menu:
   - Set **CONFIG GSE 1 FUNCTION** to “Enabled”.
   - Set **CONFIG GSE 1 ID** to an appropriate descriptive string (the default value is “GOOSEOut_1”).
   - Set **CONFIG GSE 1 DST MAC** to a multicast address (for example, 01 00 00 12 34 56).
   - Set the **CONFIG GSE 1 VLAN PRIORITY**; the default value of “4” is OK for this example.
   - Set the **CONFIG GSE 1 VLAN ID** value; the default value is “0”, but some switches may require this value to be “1”.
   - Set the **CONFIG GSE 1 ETYPE APPID** value. This setting represents the Ethertype application ID and must match the configuration on the receiver (the default value is “0”).
   - Set the **CONFIG GSE 1 CONFREV** value. This value changes automatically as described in IEC 61850 part 7-2. For this example it can be left at its default value.

3. Configure the data by making the following changes in the **PRODUCT SETUP ⇨⇩ COMMUNICATION ⇨⇩ IEC 61850 PROTOCOL ⇨ GGIO1 STATUS CONFIGURATION** settings menu:
   – Set **GGIO1 INDICATION 1** to a FlexLogic™ operand used to provide the status of GGIO1.ST.Ind1.stVal (for example, a contact input, virtual input, a protection element status, etc.).

The L60 must be rebooted (control power removed and re-applied) before these settings take effect.

The following procedure illustrates the reception configuration.

1. Configure the reception dataset by making the following changes in the **PRODUCT SETUP ⇨⇩ COMMUNICATION ⇨⇩ IEC 61850 PROTOCOL ⇨ GSSE/GOOSE CONFIGURATION ⇨⇩ RECEPTION ⇨⇩ CONFIGURABLE GOOSE ⇨ CONFIGURABLE GOOSE 1 ⇨⇩ CONFIG GSE 1 DATASET ITEMS** settings menu:
   – Set **ITEM 1** to “GGIO3.ST.Ind1.q” to indicate quality flags for GGIO3 status indication 1.
   – Set **ITEM 2** to “GGIO3.ST.Ind1.stVal” to indicate the status value for GGIO3 status indication 1.

   The reception dataset now contains a set of quality flags, a single point status Boolean value, and a floating point analog value. This matches the transmission dataset configuration above.
2. Configure the GOOSE service settings by making the following changes in the **INPUTS/OUTPUTS ⇨⇩ REMOTE DEVICES ⇨⇩ REMOTE DEVICE 1** settings menu:
   – Set **REMOTE DEVICE 1 ID** to match the GOOSE ID string for the transmitting device. Enter “GOOSEOut_1”.
   – Set **REMOTE DEVICE 1 ETYPE APPID** to match the Ethertype application ID from the transmitting device. This is “0” in the example above.
   – Set the **REMOTE DEVICE 1 DATASET** value. This value represents the dataset number in use. Since we are using configurable GOOSE 1 in this example, program this value as “GOOSEIn 1”.
3. Configure the data by making the following changes in the **INPUTS/OUTPUTS ⇨⇩ REMOTE INPUTS ⇨⇩ REMOTE INPUT 1** settings menu:
   – Set **REMOTE IN 1 DEVICE** to “GOOSEOut_1”.
   – Set **REMOTE IN 1 ITEM** to “Dataset Item 2”. This assigns the value of the GGIO3.ST.Ind1.stVal single point status item to remote input 1.

Remote input 1 can now be used in FlexLogic™ equations or other settings. The L60 must be rebooted (control power removed and re-applied) before these settings take effect.

The value of remote input 1 (Boolean on or off) in the receiving device will be determined by the GGIO1.ST.Ind1.stVal value in the sending device. The above settings will be automatically populated by the EnerVista UR Setup software when a complete SCD file is created by third party substation configurator software.

For intercommunication between L60 IEDs, the fixed (DNA/UserSt) dataset can be used. The DNA/UserSt dataset contains the same DNA and UserSt bit pairs that are included in GSSE messages. All GOOSE messages transmitted by the L60 (DNA/UserSt dataset and configurable datasets) use the IEC 61850 GOOSE messaging services (for example, VLAN support).

NOTE

Set the **CONFIG GSE 1 FUNCTION** function to “Disabled” when configuration changes are required. Once changes are entered, return the **CONFIG GSE 1 FUNCTION** to “Enabled” and restart the unit for changes to take effect.

PATH:...TRANSMISSION ⇨⇩ CONFIGURABLE GOOSE 1(8) ⇨⇩ CONIFIG GSE 1(64) DATA TIMES ⇨ ITEM 1(64)

```
■ CONFIG GSE 1
■ DATASET ITEMS
```

```
ITEM 1:
GGIO1.ST.Ind1.stVal
```

Range: all valid MMS data item references for transmitted data

To create a configurable GOOSE dataset that contains an IEC 61850 Single Point Status indication and its associated quality flags, the following dataset items can be selected: “GGIO1.ST.Ind1.stVal” and “GGIO1.ST.Ind1.q”. The L60 will then create a dataset containing these two data items. The status value for GGIO1.ST.Ind1.stVal is determined by the FlexLogic™ operand assigned to GGIO1 indication 1. Changes to this operand will result in the transmission of GOOSE messages containing the defined dataset.

The main reception menu is applicable to configurable GOOSE only and contains the configurable GOOSE dataset items for reception:

PATH:...RECEPTION ⇨⇩ CONFIGURABLE GOOSE 1(8) ⇨⇩ CONIFIG GSE 1(64) DATA ITEMS

```
■ CONFIG GSE 1
■ DATASET ITEMS
```

```
ITEM 1:
GGIO1.ST.Ind1.stVal
```

Range: all valid MMS data item references for transmitted data

The configurable GOOSE settings allow the L60 to be configured to receive a number of different datasets within IEC 61850 GOOSE messages. Up to eight different configurable datasets can be configured for reception. This is useful for intercommunication between L60 IEDs and devices from other manufacturers that support IEC 61850.

For intercommunication between L60 IEDs, the fixed (DNA/UserSt) dataset can be used. The DNA/UserSt dataset contains the same DNA and UserSt bit pairs that are included in GSSE messages.

To set up a L60 to receive a configurable GOOSE dataset that contains two IEC 61850 single point status indications, the following dataset items can be selected (for example, for configurable GOOSE dataset 1): “GGIO3.ST.Ind1.stVal” and “GGIO3.ST.Ind2.stVal”. The L60 will then create a dataset containing these two data items. The Boolean status values from these data items can be utilized as remote input FlexLogic™ operands. First, the **REMOTE DEVICE 1(16) DATASET** setting must be set to contain dataset “GOOSEIn 1” (that is, the first configurable dataset). Then **REMOTE IN 1(16) ITEM** settings must be set to “Dataset Item 1” and “Dataset Item 2”. These remote input FlexLogic™ operands will then change state in accordance with the status values of the data items in the configured dataset.

Floating point analog values originating from MMXU logical nodes may be included in GOOSE datasets. Deadband (non-instantaneous) values can be transmitted. Received values are used to populate the GGIO3.XM.AnIn1... items. Received values are also available as FlexAnalog parameters (GOOSE Analog In1...).

The main menu for the IEC 61850 server configuration is shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨⇩ SERVER CONFIGURATION

```
■ SERVER
■ CONFIGURATION
```

```
IED NAME: IECDevice
```

Range: up to 32 alphanumeric characters

MESSAGE

```
LD INST: LDInst
```

Range: up to 32 alphanumeric characters

MESSAGE

```
LOCATION: Location
```

Range: up to 80 alphanumeric characters

MESSAGE

```
IEC/MMS TCP PORT
NUMBER:     102
```

Range: 1 to 65535 in steps of 1

MESSAGE

```
INCLUDE NON-IEC
DATA: Enabled
```

Range: Disabled, Enabled

MESSAGE

```
SERVER SCANNING:
Disabled
```

Range: Disabled, Enabled

MESSAGE

```
CLEAR XCBR1 OpCnt:
No
```

Range: No, Yes

MESSAGE

```
CLEAR XCBR2 OpCnt:
No
```

Range: No, Yes

The **IED NAME** and **LD INST** settings represent the MMS domain name (IEC 61850 logical device) where all IEC/MMS logical nodes are located. Valid characters for these values are upper and lowercase letters, numbers, and the underscore (_) character, and the first character in the string must be a letter. This conforms to the IEC 61850 standard. The **LOCATION** is a variable string and can be composed of ASCII characters. This string appears within the PhyName of the LPHD node.

The **IEC/MMS TCP PORT NUMBER** setting allows the user to change the TCP port number for MMS connections. The **INCLUDE NON-IEC DATA** setting determines whether or not the “UR” MMS domain will be available. This domain contains a large number of UR-series specific data items that are not available in the IEC 61850 logical nodes. This data does not follow the IEC 61850 naming conventions. For communications schemes that strictly follow the IEC 61850 standard, this setting should be “Disabled”.

The **SERVER SCANNING** feature should be set to "Disabled" when IEC 61850 client/server functionality is not required. IEC 61850 has two modes of functionality: GOOSE/GSSE inter-device communication and client/server communication. If the GOOSE/GSSE functionality is required without the IEC 61850 client server feature, then server scanning can be disabled to increase CPU resources. When server scanning is disabled, there will be not updated to the IEC 61850 logical node status values in the L60. Clients will still be able to connect to the server (L60 relay), but most data values will not be updated. This setting does not affect GOOSE/GSSE operation.

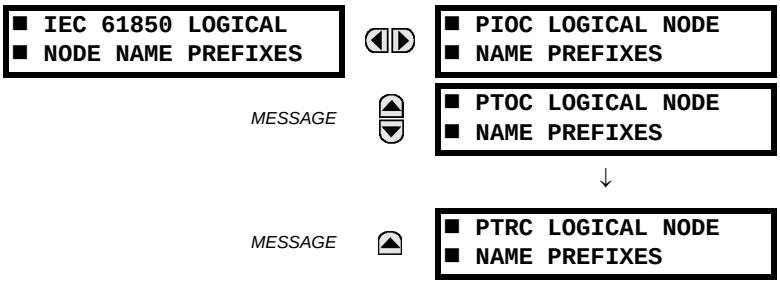
NOTE

Changes to the **IED NAME** setting, **LD INST** setting, and GOOSE dataset will not take effect until the L60 is restarted.

The **CLEAR XCBR1(2) OpCnt** settings represent the breaker operating counters. As breakers operate by opening and closing, the XCBR operating counter status attribute (OpCnt) increments with every operation. Frequent breaker operation may result in very large OpCnt values over time. This setting allows the OpCnt to be reset to "0" for XCBR1 and XCBR2.

The main menu for the IEC 61850 logical node name prefixes is shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨⇩ IEC 61850 LOGICAL NODE NAME PREFIXES

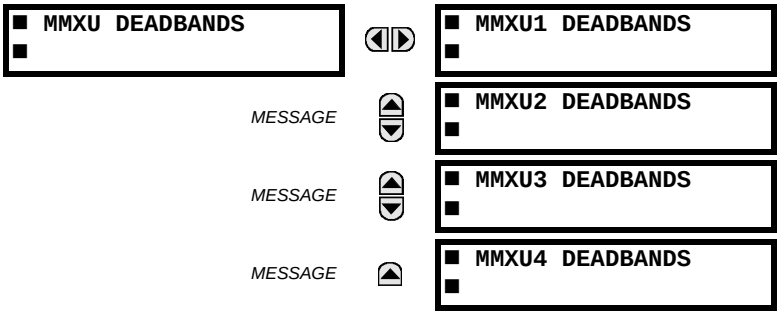


The IEC 61850 logical node name prefix settings are used to create name prefixes to uniquely identify each logical node. For example, the logical node "PTOC1" may have the name prefix "abc". The full logical node name will then be "abcMMXU1". Valid characters for the logical node name prefixes are upper and lowercase letters, numbers, and the underscore (_) character, and the first character in the prefix must be a letter. This conforms to the IEC 61850 standard.

Changes to the logical node prefixes will not take effect until the L60 is restarted.

The main menu for the IEC 61850 MMXU deadbands is shown below.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨⇩ MMXU DEADBANDS



The MMXU deadband settings represent the deadband values used to determine when the update the MMXU "mag" and "cVal" values from the associated "instmag" and "instcVal" values. The "mag" and "cVal" values are used for the IEC 61850 buffered and unbuffered reports. These settings correspond to the associated "db" data items in the CF functional constraint of the MMXU logical node, as per the IEC 61850 standard. According to IEC 61850-7-3, the db value "shall represent the percentage of difference between the maximum and minimum in units of 0.001%". Thus, it is important to know the maximum value for each MMXU measured quantity, since this represents the 100.00% value for the deadband.

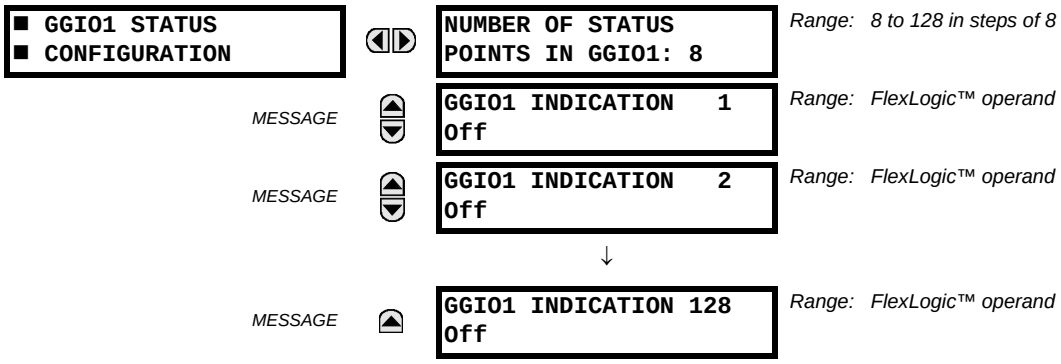
The minimum value for all quantities is 0; the maximum values are as follows:

- phase current: 46 × phase CT primary setting
- neutral current: 46 × ground CT primary setting
- voltage: 275 × VT ratio setting

- power (real, reactive, and apparent): 46 × phase CT primary setting × 275 × VT ratio setting
- frequency: 90 Hz
- power factor: 2

The GGIO1 status configuration points are shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨⇩ GGIO1 STATUS CONFIGURATION



The **NUMBER OF STATUS POINTS IN GGIO1** setting determines the number of "Ind" (single point status indications) that are instantiated in the GGIO1 logical node. Changes to the **NUMBER OF STATUS POINTS IN GGIO1** setting will not take effect until the L60 is restarted.

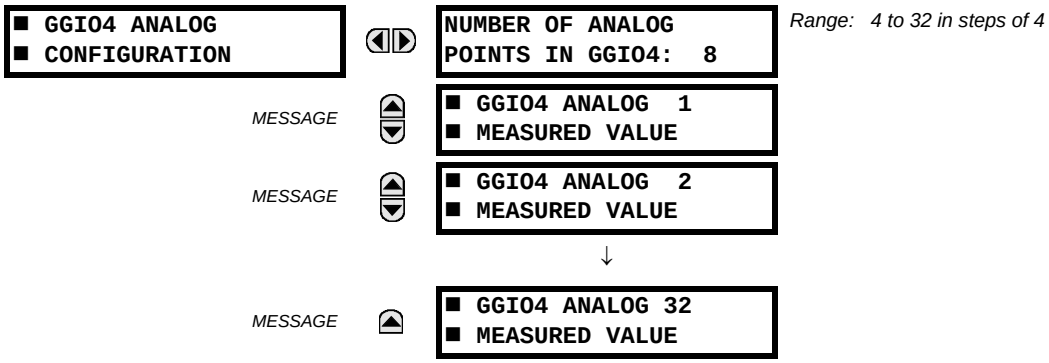
The GGIO2 control configuration points are shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨⇩ GGIO2 CONTROL... ⇨ GGIO2 CF SPSCO 1(64)

The GGIO2 control configuration settings are used to set the control model for each input. The available choices are "0" (status only), "1" (direct control), and "2" (SBO with normal security). The GGIO2 control points are used to control the L60 virtual inputs.

The GGIO4 analog configuration points are shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨⇩ GGIO4 ANALOG CONFIGURATION



The **NUMBER OF ANALOG POINTS** setting determines how many analog data points will exist in GGIO4. When this value is changed, the L60 must be rebooted in order to allow the GGIO4 logical node to be re-instantiated and contain the newly configured number of analog points.

The measured value settings for each of the 32 analog values are shown below.

PATH: SETTINGS ⇨ PRODUCT... ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨⇩ GGIO4... ⇨ GGIO4 ANALOG 1(32) MEASURED VALUE

■ GGIO4 ANALOG 1 ■ MEASURED VALUE		ANALOG IN 1 VALUE: Off	*Range: any FlexAnalog value*
MESSAGE		ANALOG IN 1 DB: 0.000	*Range: 0.000 to 100.000 in steps of 0.001*
MESSAGE		ANALOG IN 1 MIN: 0.000	*Range: –1000000000.000 to 1000000000.000 in steps of 0.001*
MESSAGE		ANALOG IN 1 MAX: 0.000	*Range: –1000000000.000 to 1000000000.000 in steps of 0.001*

These settings are configured as follows.

- **ANALOG IN 1(32) VALUE**: This setting selects the FlexAnalog value to drive the instantaneous value of each GGIO4 analog status value (GGIO4.MX.AnIn1.instMag.f).
- **ANALOG IN 1(32) DB**: This setting specifies the deadband for each analog value. Refer to IEC 61850-7-1 and 61850-7-3 for details. The deadband is used to determine when to update the deadbanded magnitude from the instantaneous magnitude. The deadband is a percentage of the difference between the maximum and minimum values.
- **ANALOG IN 1(32) MIN**: This setting specifies the minimum value for each analog value. Refer to IEC 61850-7-1 and 61850-7-3 for details. This minimum value is used to determine the deadband. The deadband is used in the determination of the deadbanded magnitude from the instantaneous magnitude.
- **ANALOG IN 1(32) MAX**: This setting defines the maximum value for each analog value. Refer to IEC 61850-7-1 and 61850-7-3 for details. This maximum value is used to determine the deadband. The deadband is used in the determination of the deadbanded magnitude from the instantaneous magnitude.

NOTE

Note that the **ANALOG IN 1(32) MIN** and **ANALOG IN 1(32) MAX** settings are stored as IEEE 754 / IEC 60559 floating point numbers. Because of the large range of these settings, not all values can be stored. Some values may be rounded to the closest possible floating point number.

The report control configuration settings are shown below:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850... ⇨⇩ REPORT... ⇨ REPORT 1(6) CONFIGURATION

■ REPORT 1 ■ CONFIGURATION		REPORT 1 RptID:	*Range: up to 66 alphanumeric characters*
MESSAGE		REPORT 1 OptFlds: 0	*Range: 0 to 65535 in steps of 1*
MESSAGE		REPORT 1 BufTm: 0	*Range: 0 to 4294967295 in steps of 1*
MESSAGE		REPORT 1 TrgOps: 0	*Range: 0 to 65535 in steps of 1*
MESSAGE		REPORT 1 IntgPd: 0	*Range: 0 to 4294967295 in steps of 1*

Changes to the report configuration will not take effect until the L60 is restarted.

The breaker configuration settings are shown below. Changes to these values will not take effect until the UR is restarted:

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨⇩ XCBR CONFIGURATION

■ XCBR ■ CONFIGURATION		XCBR1 ST.LOC OPERAND Off	*Range: FlexLogic™ operand*
MESSAGE		XCBR2 ST.LOC OPERAND Off	*Range: FlexLogic™ operand*

NOTE

Since GSSE/GOOSE messages are multicast Ethernet by specification, they will not usually be forwarded by network routers. However, GOOSE messages may be fowarded by routers if the router has been configured for VLAN functionality.

h) WEB SERVER HTTP PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ WEB SERVER HTTP PROTOCOL

```
■ WEB SERVER
■ HTTP PROTOCOL
```

```
HTTP TCP PORT
NUMBER:    80
```

Range: 1 to 65535 in steps of 1

The L60 contains an embedded web server and is capable of transferring web pages to a web browser such as Microsoft Internet Explorer or Netscape Navigator. This feature is available only if the L60 has the ethernet option installed. The web pages are organized as a series of menus that can be accessed starting at the L60 “Main Menu”. Web pages are available showing DNP and IEC 60870-5-104 points lists, Modbus registers, Event Records, Fault Reports, etc. The web pages can be accessed by connecting the UR and a computer to an ethernet network. The Main Menu will be displayed in the web browser on the computer simply by entering the IP address of the L60 into the “Address” box on the web browser.

i) TFTP PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ TFTP PROTOCOL

```
■ TFTP PROTOCOL
■
```

```
TFTP MAIN UDP PORT
NUMBER:    69
```

Range: 1 to 65535 in steps of 1

MESSAGE

```
TFTP DATA UDP PORT 1
NUMBER:    0
```

Range: 0 to 65535 in steps of 1

MESSAGE

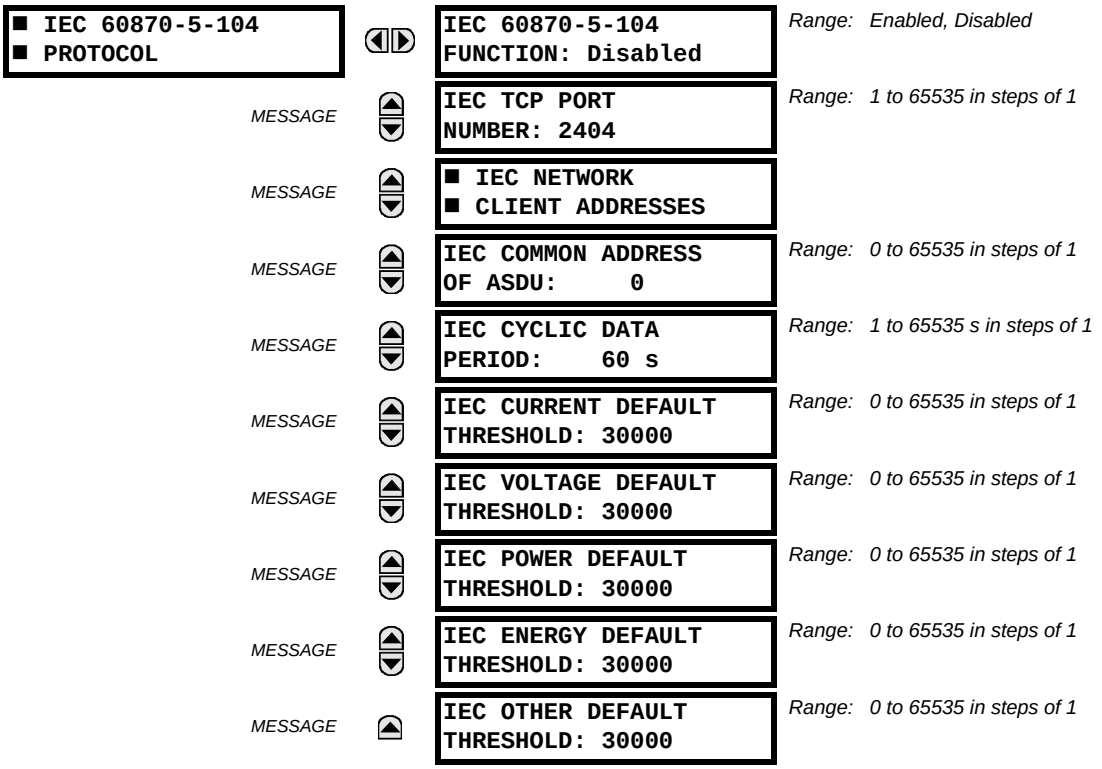
```
TFTP DATA UDP PORT 2
NUMBER:    0
```

Range: 0 to 65535 in steps of 1

The Trivial File Transfer Protocol (TFTP) can be used to transfer files from the L60 over a network. The L60 operates as a TFTP server. TFTP client software is available from various sources, including Microsoft Windows NT. The `dir.txt` file obtained from the L60 contains a list and description of all available files (event records, oscillography, etc.).

j) IEC 60870-5-104 PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 60870-5-104 PROTOCOL



The L60 supports the IEC 60870-5-104 protocol. The L60 can be used as an IEC 60870-5-104 slave device connected to a maximum of two masters (usually either an RTU or a SCADA master station). Since the L60 maintains two sets of IEC 60870-5-104 data change buffers, no more than two masters should actively communicate with the L60 at one time.

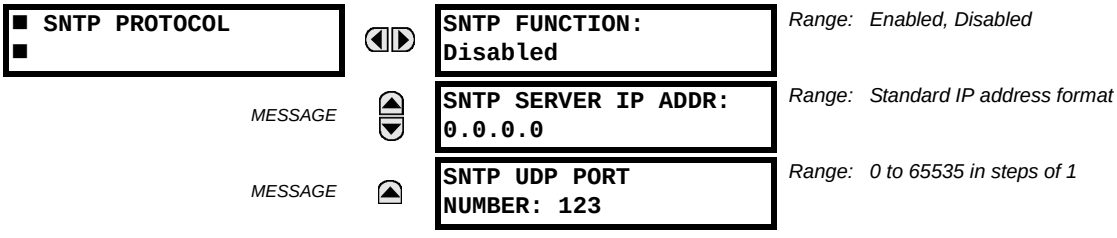
The **IEC ------- DEFAULT THRESHOLD** settings are used to determine when to trigger spontaneous responses containing M_ME_NC_1 analog data. These settings group the L60 analog data into types: current, voltage, power, energy, and other. Each setting represents the default threshold value for all M_ME_NC_1 analog points of that type. For example, to trigger spontaneous responses from the L60 when any current values change by 15 A, the **IEC CURRENT DEFAULT THRESHOLD** setting should be set to 15. Note that these settings are the default values of the deadbands. P_ME_NC_1 (parameter of measured value, short floating point value) points can be used to change threshold values, from the default, for each individual M_ME_NC_1 analog point. Whenever power is removed and re-applied to the L60, the default thresholds will be in effect.

NOTE

The IEC 60870-5-104 and DNP protocols cannot be simultaneously. When the IEC 60870-5-104 FUNCTION setting is set to "Enabled", the DNP protocol will not be operational. When this setting is changed it will not become active until power to the relay has been cycled (off-to-on).

k) SNTP PROTOCOL

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ SNTP PROTOCOL



The L60 supports the Simple Network Time Protocol specified in RFC-2030. With SNTP, the L60 can obtain clock time over an Ethernet network. The L60 acts as an SNTP client to receive time values from an SNTP/NTP server, usually a dedicated product using a GPS receiver to provide an accurate time. Both unicast and broadcast SNTP are supported.

If SNTP functionality is enabled at the same time as IRIG-B, the IRIG-B signal provides the time value to the L60 clock for as long as a valid signal is present. If the IRIG-B signal is removed, the time obtained from the SNTP server is used. If either SNTP or IRIG-B is enabled, the L60 clock value cannot be changed using the front panel keypad.

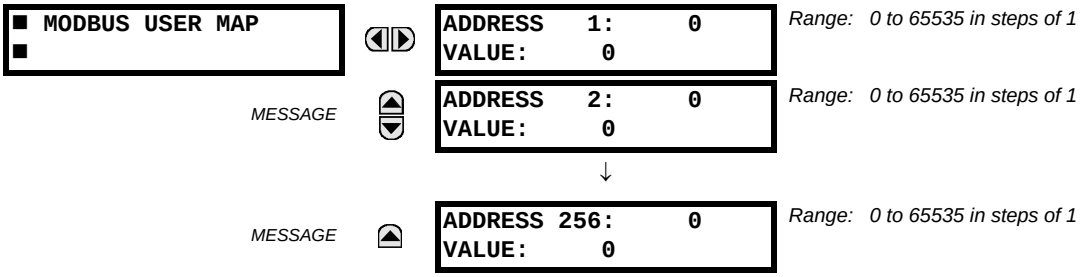
To use SNTP in unicast mode, **SNTP SERVER IP ADDR** must be set to the SNTP/NTP server IP address. Once this address is set and **SNTP FUNCTION** is "Enabled", the L60 attempts to obtain time values from the SNTP/NTP server. Since many time values are obtained and averaged, it generally takes three to four minutes until the L60 clock is closely synchronized with the SNTP/NTP server. It may take up to two minutes for the L60 to signal an SNTP self-test error if the server is offline.

To use SNTP in broadcast mode, set the **SNTP SERVER IP ADDR** setting to "0.0.0.0" and **SNTP FUNCTION** to "Enabled". The L60 then listens to SNTP messages sent to the "all ones" broadcast address for the subnet. The L60 waits up to eighteen minutes (>1024 seconds) without receiving an SNTP broadcast message before signaling an SNTP self-test error.

The UR-series relays do not support the multicast or anycast SNTP functionality.

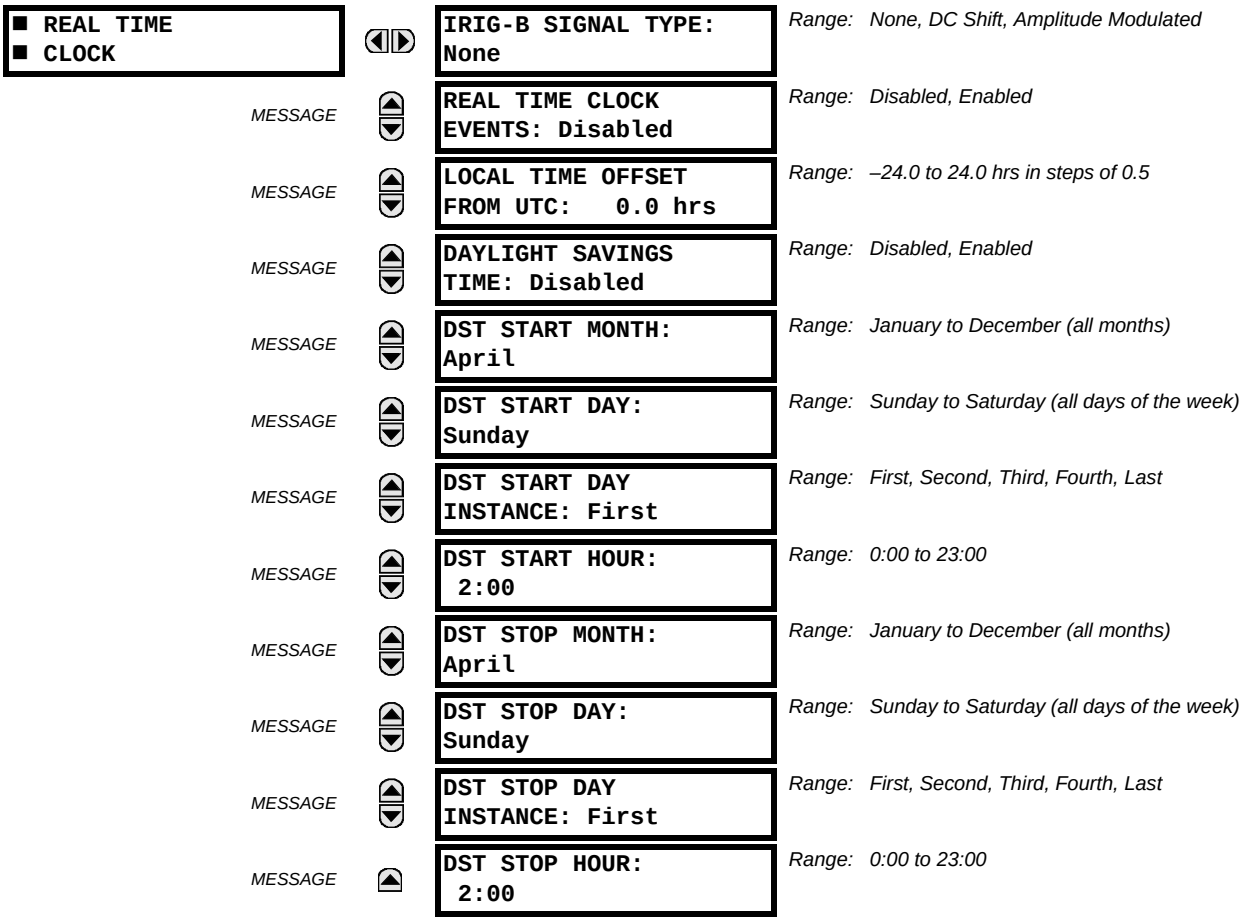
5.2.5 MODBUS USER MAP

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ MODBUS USER MAP



The Modbus User Map provides read-only access for up to 256 registers. To obtain a memory map value, enter the desired address in the **ADDRESS** line (this value must be converted from hex to decimal format). The corresponding value is displayed in the **VALUE** line. A value of "0" in subsequent register **ADDRESS** lines automatically returns values for the previous **ADDRESS** lines incremented by "1". An address value of "0" in the initial register means "none" and values of "0" will be displayed for all registers. Different **ADDRESS** values can be entered as required in any of the register positions.

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ REAL TIME CLOCK



The date and time can be synchronized a known time base and to other relays using an IRIG-B signal. It has the same accuracy as an electronic watch, approximately ±1 minute per month. If an IRIG-B signal is connected to the relay, only the current year needs to be entered. See the COMMANDS ⇨⇩ SET DATE AND TIME menu to manually set the relay clock.

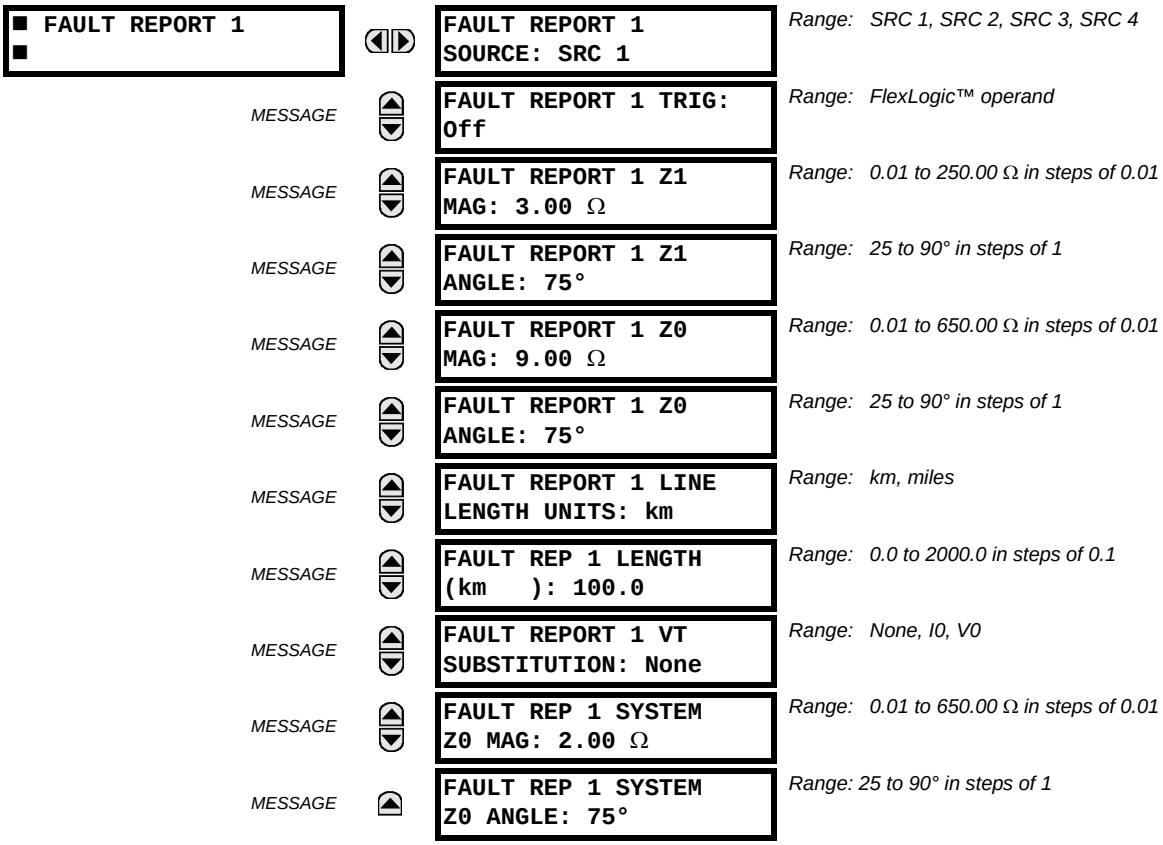
The **REAL TIME CLOCK EVENTS** setting allows changes to the date and/or time to be captured in the event record.

The **LOCAL TIME OFFSET FROM UTC** setting is used to specify the local time zone offset from Universal Coordinated Time (Greenwich Mean Time) in hours. This setting has two uses. When the L60 is time synchronized with IRIG-B, or has no permanent time synchronization, the offset is used to calculate UTC time for IEC 61850 features. When the L60 is time synchronized with SNTP, the offset is used to determine the local time for the L60 clock, since SNTP provides UTC time.

The daylight savings time (DST) settings can be used to allow the L60 clock can follow the DST rules of the local time zone. Note that when IRIG-B time synchronization is active, the DST settings are ignored. The DST settings are used when the L60 is synchronized with SNTP, or when neither SNTP nor IRIG-B is used.

5.2.7 FAULT REPORTS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ FAULT REPORTS ⇨ FAULT REPORT 1



The L60 relay supports one fault report and an associated fault locator. The signal source and trigger condition, as well as the characteristics of the line or feeder, are entered in this menu.

The fault report stores data, in non-volatile memory, pertinent to an event when triggered. The captured data contained in the `FaultReport.txt` file includes:

- Fault report number
- Name of the relay, programmed by the user
- Firmware revision of the relay
- Date and time of trigger
- Name of trigger (specific operand)
- Line/feeder ID via the name of a configured signal source
- Active setting group at the time of trigger
- Pre-fault current and voltage phasors (two cycles before either a 50DD disturbance associated with fault report source or the trigger operate)
- Fault current and voltage phasors (one cycle after the trigger)
- Elements operated at the time of triggering
- Events: 9 before trigger and 7 after trigger (only available via the relay webpage)
- Fault duration times for each breaker (created by the breaker arcing current feature)

The captured data also includes the fault type and the distance to the fault location, as well as the reclose shot number (when applicable) To include fault duration times in the fault report, the user must enable and configure breaker arcing current feature for each of the breakers. Fault duration is reported on a per-phase basis.

The relay allows locating faults, including ground faults, from delta-connected VTs. In this case, the missing zero-sequence voltage is substituted either by the externally provided neutral voltage (broken delta VT) connected to the auxiliary voltage channel of a VT bank, or by the zero-sequence voltage approximated as a voltage drop developed by the zero-sequence current, and user-provided zero-sequence equivalent impedance of the system behind the relay.

The trigger can be any FlexLogic™ operand, but in most applications it is expected to be the same operand, usually a virtual output, that is used to drive an output relay to trip a breaker. To prevent the overwriting of fault events, the disturbance detector should not be used to trigger a fault report. A FAULT RPT TRIG event is automatically created when the report is triggered.

If a number of protection elements are ORed to create a fault report trigger, the first operation of any element causing the OR gate output to become high triggers a fault report. However, If other elements operate during the fault and the first operated element has not been reset (the OR gate output is still high), the fault report is not triggered again. Considering the reset time of protection elements, there is very little chance that fault report can be triggered twice in this manner. As the fault report must capture a usable amount of pre and post-fault data, it can not be triggered faster than every 20 ms.

Each fault report is stored as a file; the relay capacity is fifteen (15) files. An sixteenth (16th) trigger overwrites the oldest file.

The EnerVista UR Setup software is required to view all captured data. The relay faceplate display can be used to view the date and time of trigger, the fault type, the distance location of the fault, and the reclose shot number.

The **FAULT REPORT 1 SOURCE** setting selects the source for input currents and voltages and disturbance detection. The **FAULT 1 REPORT TRIG** setting assigns the FlexLogic™ operand representing the protection element/elements requiring operational fault location calculations. The distance to fault calculations are initiated by this signal. The **FAULT REPORT 1 Z1 MAG** and **FAULT REPORT 1 Z0 MAG** impedances are entered in secondary ohms.

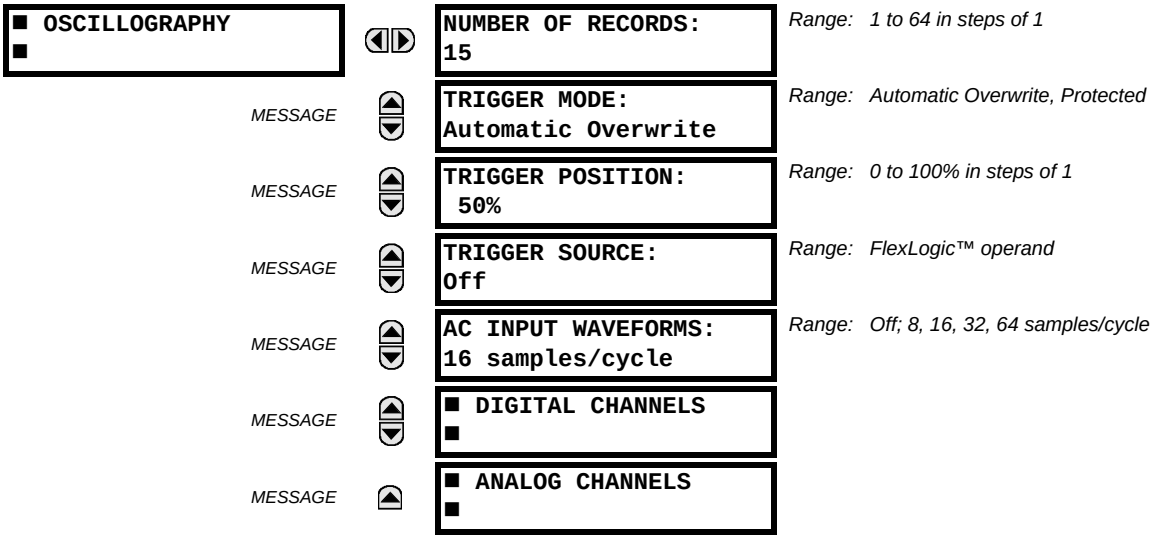
The **FAULT REPORT 1 VT SUBSTITUTION** setting shall be set to “None” if the relay is fed from wye-connected VTs. If delta-connected VTs are used, and the relay is supplied with the neutral (3V0) voltage, this setting shall be set to “V0”. The method is still exact, as the fault locator would combine the line-to-line voltage measurements with the neutral voltage measurement to re-create the line-to-ground voltages. See the **ACTUAL VALUES ⇨⇩ RECORDS ⇨ FAULT REPORTS** menu for additional details. It required to configure the delta and neutral voltages under the source indicated as input for the fault report. Also, the relay will check if the auxiliary signal configured is marked as “Vn” by the user (under VT setup), and inhibit the fault location if the auxiliary signal is labeled differently.

If the broken-delta neutral voltage is not available to the relay, an approximation is possible by assuming the missing zero-sequence voltage to be an inverted voltage drop produced by the zero-sequence current and the user-specified equivalent zero-sequence system impedance behind the relay: $V0 = –Z0 \times I0$. In order to enable this mode of operation, the **FAULT REPORT 1 VT SUBSTITUTION** setting shall be set to “I0”.

The **FAULT REP 1 SYSTEM Z0 MAG** and **FAULT REP 1 SYSTEM Z0 ANGLE** settings are used only when the **VT SUBSTITUTION** setting value is “I0”. The magnitude is to be entered in secondary ohms. This impedance is an average system equivalent behind the relay. It can be calculated as zero-sequence Thevenin impedance at the local bus with the protected line/feeder disconnected. The method is accurate only if this setting matches perfectly the actual system impedance during the fault. If the system exhibits too much variability, this approach is questionable and the fault location results for single-line-to-ground faults shall be trusted with accordingly. It should be kept in mind that grounding points in vicinity of the installation impact the system zero-sequence impedance (grounded loads, reactors, zig-zag transformers, shunt capacitor banks, etc.).

a) MAIN MENU

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ OSCILLOGRAPHY



5

Oscillography records contain waveforms captured at the sampling rate as well as other relay data at the point of trigger. Oscillography records are triggered by a programmable FlexLogic™ operand. Multiple oscillography records may be captured simultaneously.

The **NUMBER OF RECORDS** is selectable, but the number of cycles captured in a single record varies considerably based on other factors such as sample rate and the number of operational modules. There is a fixed amount of data storage for oscillography; the more data captured, the less the number of cycles captured per record. See the **ACTUAL VALUES ⇨⇩ RECORDS ⇨⇩ OSCILLOGRAPHY** menu to view the number of cycles captured per record. The following table provides sample configurations with corresponding cycles/record.

Table 5–2: OSCILLOGRAPHY CYCLES/RECORD EXAMPLE

# RECORDS	# CT/VTS	SAMPLE RATE	# DIGITALS	# ANALOGS	CYCLES/ RECORD
1	1	8	0	0	1872.0
1	1	16	16	0	1685.0
8	1	16	16	0	276.0
8	1	16	16	4	219.5
8	2	16	16	4	93.5
8	2	16	64	16	93.5
8	2	32	64	16	57.6
8	2	64	64	16	32.3
32	2	64	64	16	9.5

A new record may automatically overwrite an older record if **TRIGGER MODE** is set to “Automatic Overwrite”.

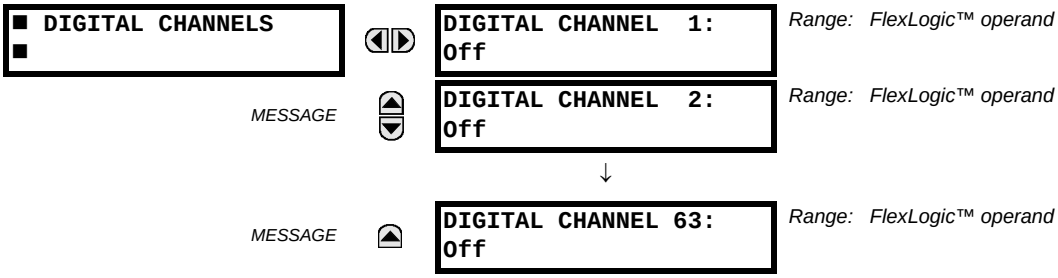
Set the **TRIGGER POSITION** to a percentage of the total buffer size (e.g. 10%, 50%, 75%, etc.). A trigger position of 25% consists of 25% pre- and 75% post-trigger data. The **TRIGGER SOURCE** is always captured in oscillography and may be any FlexLogic™ parameter (element state, contact input, virtual output, etc.). The relay sampling rate is 64 samples per cycle.

The **AC INPUT WAVEFORMS** setting determines the sampling rate at which AC input signals (i.e. current and voltage) are stored. Reducing the sampling rate allows longer records to be stored. This setting has no effect on the internal sampling rate of the relay which is always 64 samples per cycle, i.e. it has no effect on the fundamental calculations of the device.

WARNING **When changes are made to the oscillography settings, all existing oscillography records will be CLEARED.**

b) DIGITAL CHANNELS

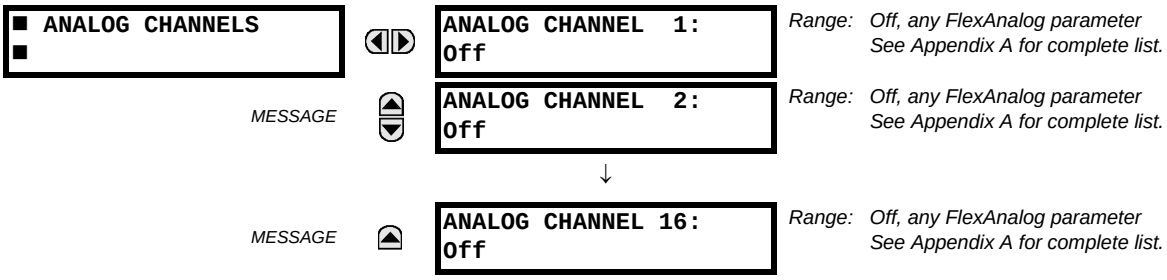
PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ OSCILLOGRAPHY ⇨⇩ DIGITAL CHANNELS



A **DIGITAL 1(63) CHANNEL** setting selects the FlexLogic™ operand state recorded in an oscillography trace. The length of each oscillography trace depends in part on the number of parameters selected here. Parameters set to "Off" are ignored. Upon startup, the relay will automatically prepare the parameter list.

c) ANALOG CHANNELS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ OSCILLOGRAPHY ⇨⇩ ANALOG CHANNELS



An **ANALOG 1(16) CHANNEL** setting selects the metering actual value recorded in an oscillography trace. The length of each oscillography trace depends in part on the number of parameters selected here. Parameters set to "Off" are ignored. The parameters available in a given relay are dependent on: (a) the type of relay, (b) the type and number of CT/VT hardware modules installed, and (c) the type and number of Analog Input hardware modules installed. Upon startup, the relay will automatically prepare the parameter list. A list of all possible analog metering actual value parameters is presented in Appendix A: *FlexAnalog Parameters*. The parameter index number shown in any of the tables is used to expedite the selection of the parameter on the relay display. It can be quite time-consuming to scan through the list of parameters via the relay keypad/display - entering this number via the relay keypad will cause the corresponding parameter to be displayed.

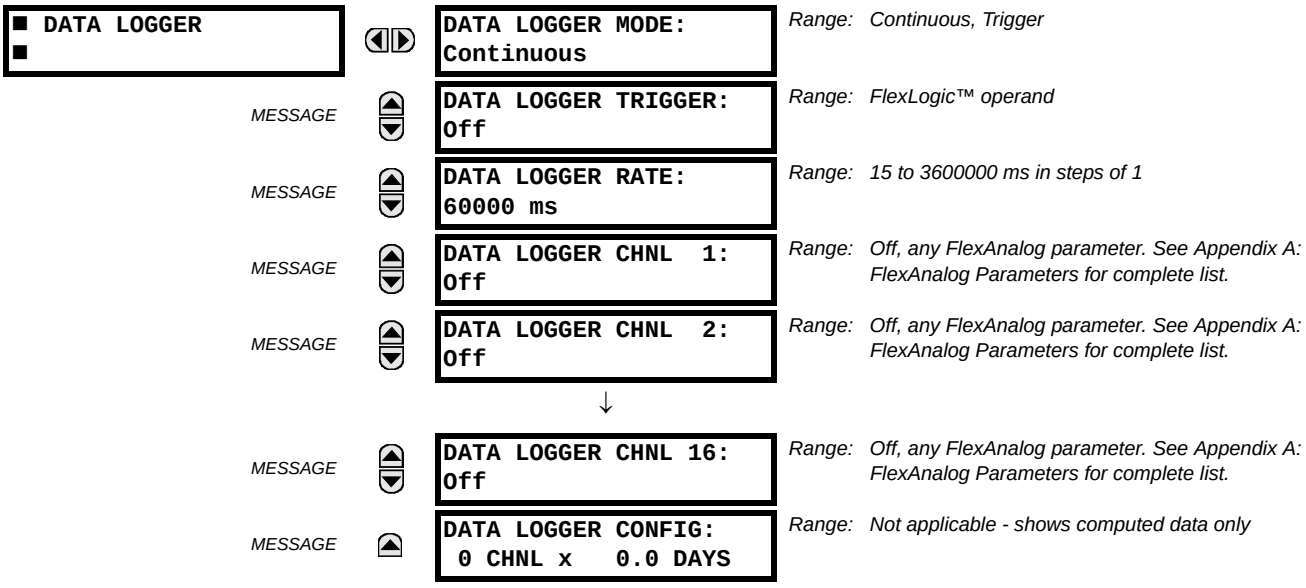
All eight CT/VT module channels are stored in the oscillography file. The CT/VT module channels are named as follows:

<slot_letter><terminal_number>—<I or *V><phase A*, *B*, or *C*, or *4th input>*

The fourth current input in a bank is called IG, and the fourth voltage input in a bank is called VX. For example, F2-IB designates the IB signal on Terminal 2 of the CT/VT module in slot F. If there are no CT/VT modules and analog input modules, no analog traces will appear in the file; only the digital traces will appear.

5.2.9 DATA LOGGER

PATH: SETTINGS ⇨⇩ PRODUCT SETUP ⇨⇩ DATA LOGGER



5

The data logger samples and records up to 16 analog parameters at a user-defined sampling rate. This recorded data may be downloaded to EnerVista UR Setup and displayed with *parameters* on the vertical axis and *time* on the horizontal axis. All data is stored in non-volatile memory, meaning that the information is retained when power to the relay is lost.

For a fixed sampling rate, the data logger can be configured with a few channels over a long period or a larger number of channels for a shorter period. The relay automatically partitions the available memory between the channels in use. Example storage capacities for a system frequency of 60 Hz are shown in the following table.

Table 5–3: DATA LOGGER STORAGE CAPACITY EXAMPLE

SAMPLING RATE	CHANNELS	DAYS	STORAGE CAPACITY
15 ms	1	0.1	954 s
	8	0.1	120 s
	9	0.1	107 s
	16	0.1	60 s
1000 ms	1	0.7	65457 s
	8	0.1	8182 s
	9	0.1	7273 s
	16	0.1	4091 s
60000 ms	1	45.4	3927420 s
	8	5.6	490920 s
	9	5	436380 s
	16	2.8	254460 s
3600000 ms	1	2727.5	235645200 s
	8	340.9	29455200 s
	9	303	26182800 s

NOTE

Changing any setting affecting data logger operation will clear any data that is currently in the log.

- **DATA LOGGER MODE**: This setting configures the mode in which the data logger will operate. When set to “Continuous”, the data logger will actively record any configured channels at the rate as defined by the **DATA LOGGER RATE**. The

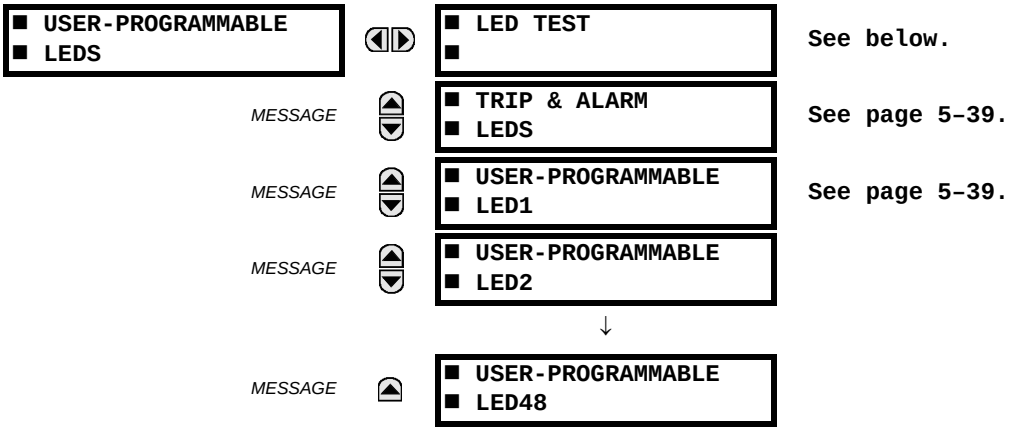
data logger will be idle in this mode if no channels are configured. When set to "Trigger", the data logger will begin to record any configured channels at the instance of the rising edge of the **DATA LOGGER TRIGGER** source FlexLogic™ operand. The **Data Logger will ignore** all subsequent triggers and will continue to record data until the active record is full. Once the data logger is full a **CLEAR DATA LOGGER** command is required to clear the data logger record before a new record can be started. Performing the **CLEAR DATA LOGGER** command will also stop the current record and reset the data logger to be ready for the next trigger.

- **DATA LOGGER TRIGGER**: This setting selects the signal used to trigger the start of a new data logger record. Any FlexLogic™ operand can be used as the trigger source. The **DATA LOGGER TRIGGER** setting only applies when the mode is set to "Trigger".
- **DATA LOGGER RATE:** This setting selects the time interval at which the actual value data will be recorded.
- **DATA LOGGER CHNL 1(16):** This setting selects the metering actual value that is to be recorded in Channel 1(16) of the data log. The parameters available in a given relay are dependent on: the type of relay, the type and number of CT/VT hardware modules installed, and the type and number of Analog Input hardware modules installed. Upon startup, the relay will automatically prepare the parameter list. A list of all possible analog metering actual value parameters is shown in Appendix A: *FlexAnalog Parameters*. The parameter index number shown in any of the tables is used to expedite the selection of the parameter on the relay display. It can be quite time-consuming to scan through the list of parameters via the relay keypad/display – entering this number via the relay keypad will cause the corresponding parameter to be displayed.
- **DATA LOGGER CONFIG:** This display presents the total amount of time the Data Logger can record the channels not selected to "Off" without over-writing old data.

5.2.10 USER-PROGRAMMABLE LEDS

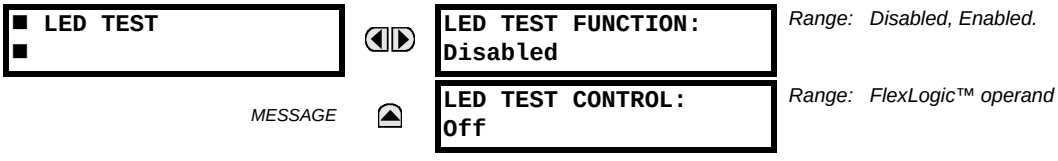
a) MAIN MENU

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE LEDS



b) LED TEST

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE LEDS ⇨ LED TEST



When enabled, the LED Test can be initiated from any digital input or user-programmable condition such as user-programmable pushbutton. The control operand is configured under the **LED TEST CONTROL** setting. The test covers all LEDs, including the LEDs of the optional user-programmable pushbuttons.

The test consists of three stages.

Stage 1: All 62 LEDs on the relay are illuminated. This is a quick test to verify if any of the LEDs is "burned". This stage lasts as long as the control input is on, up to a maximum of 1 minute. After 1 minute, the test will end.

Stage 2: All the LEDs are turned off, and then one LED at a time turns on for 1 second, then back off. The test routine starts at the top left panel, moving from the top to bottom of each LED column. This test checks for hardware failures that lead to more than one LED being turned on from a single logic point. This stage can be interrupted at any time.

Stage 3: All the LEDs are turned on. One LED at a time turns off for 1 second, then back on. The test routine starts at the top left panel moving from top to bottom of each column of the LEDs. This test checks for hardware failures that lead to more than one LED being turned off from a single logic point. This stage can be interrupted at any time.

When testing is in progress, the LEDs are controlled by the test sequence, rather than the protection, control, and monitoring features. However, the LED control mechanism accepts all the changes to LED states generated by the relay and stores the actual LED states (On or Off) in memory. When the test completes, the LEDs reflect the actual state resulting from relay response during testing. The Reset pushbutton will not clear any targets when the LED Test is in progress.

A dedicated FlexLogic™ operand, LED TEST IN PROGRESS, is set for the duration of the test. When the test sequence is initiated, the LED Test Initiated event is stored in the Event Recorder.

The entire test procedure is user-controlled. In particular, Stage 1 can last as long as necessary, and Stages 2 and 3 can be interrupted. The test responds to the position and rising edges of the control input defined by the **LED TEST CONTROL** setting. The control pulses must last at least 250 ms to take effect. The following diagram explains how the test is executed.

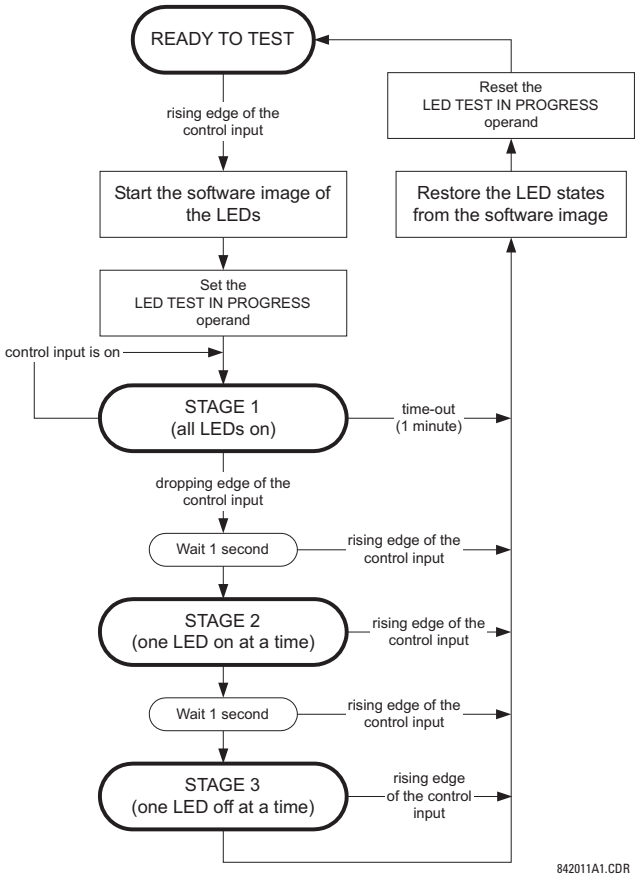


Figure 5–2: LED TEST SEQUENCE

APPLICATION EXAMPLE 1:

Assume one needs to check if any of the LEDs is “burned” through User-Programmable Pushbutton 1. The following settings should be applied. Configure User-Programmable Pushbutton 1 by making the following entries in the **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE PUSHBUTTONS ⇨ USER PUSHBUTTON 1** menu:

PUSHBUTTON 1 FUNCTION: “Self-reset”
PUSHBTN 1 DROP-OUT TIME: “0.10 s”

Configure the LED test to recognize User-Programmable Pushbutton 1 by making the following entries in the SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE LEDS ⇨ LED TEST menu:

LED TEST FUNCTION: "Enabled"
LED TEST CONTROL: "PUSHBUTTON 1 ON"

The test will be initiated when the User-Programmable Pushbutton 1 is pressed. The pushbutton should remain pressed for as long as the LEDs are being visually inspected. When finished, the pushbutton should be released. The relay will then automatically start Stage 2. At this point forward, test may be aborted by pressing the pushbutton.

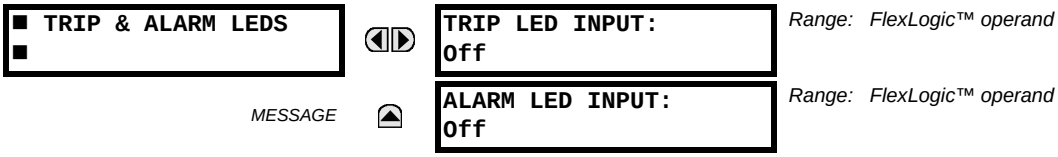
APPLICATION EXAMPLE 2:

Assume one needs to check if any LEDs are "burned" as well as exercise one LED at a time to check for other failures. This is to be performed via User-Programmable Pushbutton 1.

After applying the settings in Application Example 1, hold down the pushbutton as long as necessary to test all LEDs. Next, release the pushbutton to automatically start Stage 2. Once Stage 2 has started, the pushbutton can be released. When Stage 2 is completed, Stage 3 will automatically start. The test may be aborted at any time by pressing the pushbutton.

c) TRIP AND ALARM LEDS

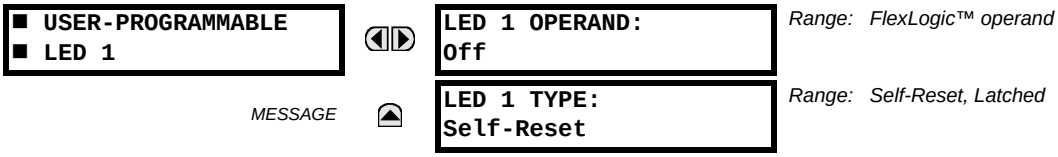
PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE LEDS ⇨⇩ TRIP & ALARM LEDS



The Trip and Alarm LEDs are in the first LED column (enhanced faceplate) and on LED panel 1 (standard faceplate). Each indicator can be programmed to become illuminated when the selected FlexLogic™ operand is in the logic 1 state.

d) USER-PROGRAMMABLE LED 1(48)

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE LEDS ⇨⇩ USER-PROGRAMMABLE LED 1(48)



There are 48 amber LEDs across the relay faceplate LED panels. Each of these indicators can be programmed to illuminate when the selected FlexLogic™ operand is in the logic 1 state.

For the standard faceplate, the LEDs are located as follows.

- LED Panel 2: user-programmable LEDs 1 through 24
- LED Panel 3: user programmable LEDs 25 through 48

For the standard faceplate, the LEDs are located as follows.

- LED column 2: user-programmable LEDs 1 through 12
- LED column 3: user-programmable LEDs 13 through 24
- LED column 4: user-programmable LEDs 25 through 36
- LED column 5: user-programmable LEDs 37 through 48

Refer to the *LED indicators* section in chapter 4 for additional information on the location of these indexed LEDs.

The user-programmable LED settings select the FlexLogic™ operands that control the LEDs. If the **LED 1 TYPE** setting is "Self-Reset" (the default setting), the LED illumination will track the state of the selected LED operand. If the **LED 1 TYPE** setting is "Latched", the LED, once lit, remains so until reset by the faceplate RESET button, from a remote device via a communications channel, or from any programmed operand, even if the LED operand state de-asserts.

Table 5–4: RECOMMENDED SETTINGS FOR USER-PROGRAMMABLE LEDS

SETTING	PARAMETER
LED 1 Operand	SETTING GROUP ACT 1
LED 2 Operand	SETTING GROUP ACT 2
LED 3 Operand	SETTING GROUP ACT 3
LED 4 Operand	SETTING GROUP ACT 4
LED 5 Operand	SETTING GROUP ACT 5
LED 6 Operand	SETTING GROUP ACT 6
LED 7 Operand	Off
LED 8 Operand	Off
LED 9 Operand	BREAKER 1 OPEN
LED 10 Operand	BREAKER 1 CLOSED
LED 11 Operand	BREAKER 1 TROUBLE
LED 12 Operand	Off

SETTING	PARAMETER
LED 13 Operand	Off
LED 14 Operand	BREAKER 2 OPEN
LED 15 Operand	BREAKER 2 CLOSED
LED 16 Operand	BREAKER 2 TROUBLE
LED 17 Operand	SYNC 1 SYNC OP
LED 18 Operand	SYNC 2 SYNC OP
LED 19 Operand	Off
LED 20 Operand	Off
LED 21 Operand	AR ENABLED
LED 22 Operand	AR DISABLED
LED 23 Operand	AR RIP
LED 24 Operand	AR LO

Refer to the *Control of setting groups* example in the *Control elements* section of this chapter for group activation.

5.2.11 USER-PROGRAMMABLE SELF TESTS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE SELF TESTS

5

USER-PROGRAMMABLE SELF TESTS

	DIRECT RING BREAK FUNCTION: Enabled	*Range: Disabled, Enabled. Valid for units equipped with Direct Input/Output module.*
MESSAGE	**DIRECT DEVICE OFF FUNCTION: Enabled**	*Range: Disabled, Enabled. Valid for units equipped with Direct Input/Output module.*
MESSAGE	**REMOTE DEVICE OFF FUNCTION: Enabled**	*Range: Disabled, Enabled. Valid for units that contain a CPU with Ethernet capability.*
MESSAGE	**PRI. ETHERNET FAIL FUNCTION: Disabled**	*Range: Disabled, Enabled. Valid for units that contain a CPU with a primary fiber port.*
MESSAGE	**SEC. ETHERNET FAIL FUNCTION: Disabled**	*Range: Disabled, Enabled. Valid for units that contain a CPU with a redundant fiber port.*
MESSAGE	**BATTERY FAIL FUNCTION: Enabled**	*Range: Disabled, Enabled.*
MESSAGE	**SNTP FAIL FUNCTION: Enabled**	*Range: Disabled, Enabled. Valid for units that contain a CPU with Ethernet capability.*
MESSAGE	**IRIG-B FAIL FUNCTION: Enabled**	*Range: Disabled, Enabled.*
MESSAGE	**ETHERNET SWITCH FAIL FUNCTION: Enabled**	*Range: Disabled, Enabled.*

All major self-test alarms are reported automatically with their corresponding FlexLogic™ operands, events, and targets. Most of the Minor Alarms can be disabled if desired.

When in the “Disabled” mode, minor alarms will not assert a FlexLogic™ operand, write to the event recorder, or display target messages. Moreover, they will not trigger the **ANY MINOR ALARM** or **ANY SELF-TEST** messages. When in the “Enabled” mode, minor alarms continue to function along with other major and minor alarms. Refer to the *Relay Self-Tests* section in Chapter 7 for additional information on major and minor self-test alarms.

5.2.12 CONTROL PUSHBUTTONS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ CONTROL PUSHBUTTONS ⇨ CONTROL PUSHBUTTON 1(7)

```
■ CONTROL
■ PUSHBUTTON 1
```

```
CONTROL PUSHBUTTON 1
FUNCTION: Disabled
```

Range: Disabled, Enabled

MESSAGE

```
CONTROL PUSHBUTTON 1
EVENTS: Disabled
```

Range: Disabled, Enabled

There are three standard control pushbuttons, labeled USER 1, USER 2, and USER 3, on the standard and enhanced front panels. These are user-programmable and can be used for various applications such as performing an LED test, switching setting groups, and invoking and scrolling though user-programmable displays, etc.

Firmware revisions 3.2x and older use these three pushbuttons for manual breaker control. This functionality has been retained – if the breaker control feature is configured to use the three pushbuttons, they cannot be used as user-programmable control pushbuttons.The location of the control pushbuttons are shown in the following figures.

Figure 5–3: CONTROL PUSHBUTTONS (ENHANCED FACEPLATE)

An additional four control pushbuttons are included on the standard faceplate when the L60 is ordered with the twelve user-programmable pushbutton option.

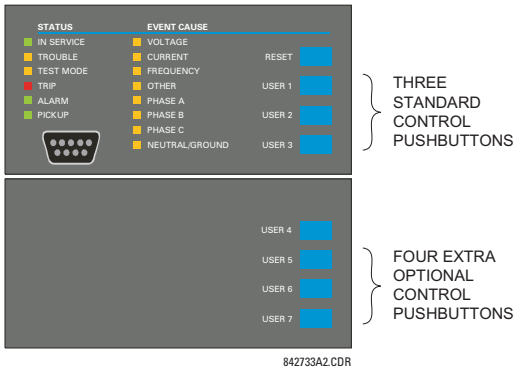


Figure 5–4: CONTROL PUSHBUTTONS (STANDARD FACEPLATE)

Control pushbuttons are not typically used for critical operations and are not protected by the control password. However, by supervising their output operands, the user can dynamically enable or disable control pushbuttons for security reasons.

Each control pushbutton asserts its own FlexLogic™ operand. These operands should be configured appropriately to perform the desired function. The operand remains asserted as long as the pushbutton is pressed and resets when the pushbutton is released. A dropout delay of 100 ms is incorporated to ensure fast pushbutton manipulation will be recognized by various features that may use control pushbuttons as inputs.

An event is logged in the event record (as per user setting) when a control pushbutton is pressed. No event is logged when the pushbutton is released. The faceplate keys (including control keys) cannot be operated simultaneously – a given key must be released before the next one can be pressed.

The control pushbuttons become user-programmable only if the breaker control feature is not configured for manual control via the USER 1 through 3 pushbuttons as shown below. If configured for manual control, breaker control typically uses the larger, optional user-programmable pushbuttons, making the control pushbuttons available for other user applications.

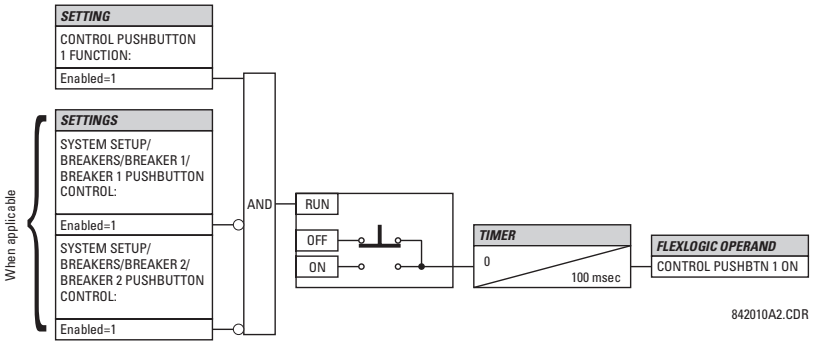


Figure 5–5: CONTROL PUSHBUTTON LOGIC

5.2.13 USER-PROGRAMMABLE PUSHBUTTONS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE PUSHBUTTONS ⇨ USER PUSHBUTTON 1(16)

■ USER PUSHBUTTON 1 ■		PUSHBUTTON 1 FUNCTION: Disabled	*Range: Self-Reset, Latched, Disabled*
	MESSAGE	PUSHBTN 1 ID TEXT:	*Range: Up to 20 alphanumeric characters*
	MESSAGE	PUSHBTN 1 ON TEXT:	*Range: Up to 20 alphanumeric characters*
	MESSAGE	PUSHBTN 1 OFF TEXT:	*Range: Up to 20 alphanumeric characters*
	MESSAGE	PUSHBTN 1 SET: Off	*Range: FlexLogic™ operand*
	MESSAGE	PUSHBTN 1 RESET: Off	*Range: FlexLogic™ operand*
	MESSAGE	PUSHBTN 1 AUTORST: Disabled	*Range: Disabled, Enabled*
	MESSAGE	PUSHBTN 1 AUTORST DELAY: 1.0 s	*Range: 0.2 to 600.0 s in steps of 0.1*
	MESSAGE	PUSHBTN 1 REMOTE: Off	*Range: FlexLogic™ operand*
	MESSAGE	PUSHBTN 1 LOCAL: Off	*Range: FlexLogic™ operand*
	MESSAGE	PUSHBTN 1 DROP-OUT TIME: 0.00 s	*Range: 0 to 60.00 s in steps of 0.05*
	MESSAGE	PUSHBTN 1 LED CTL: Off	*Range: FlexLogic™ operand*
	MESSAGE	PUSHBTN 1 MESSAGE: Disabled	*Range: Disabled, Normal, High Priority*
	MESSAGE	PUSHBUTTON 1 EVENTS: Disabled	*Range: Disabled, Enabled*

The optional user-programmable pushbuttons (specified in the order code) provide an easy and error-free method of entering digital state (on, off) information. The number of available pushbuttons is dependent on the faceplate module ordered with the relay.

- Type P faceplate: standard horizontal faceplate with 12 user-programmable pushbuttons.
- Type Q faceplate: enhanced horizontal faceplate with 16 user-programmable pushbuttons.

The digital state can be entered locally (by directly pressing the front panel pushbutton) or remotely (via FlexLogic™ operands) into FlexLogic™ equations, protection elements, and control elements. Typical applications include breaker control, autorecloser blocking, and setting groups changes. The user-programmable pushbuttons are under the “Control” level of password protection.

The user-configurable pushbuttons for the enhanced faceplate are shown below.

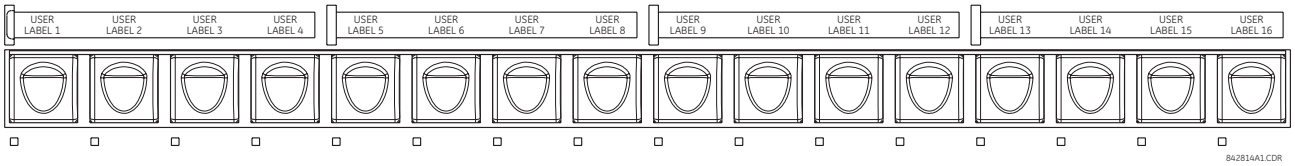


Figure 5–6: USER-PROGRAMMABLE PUSHBUTTONS (ENHANCED FACEPLATE)

The user-configurable pushbuttons for the standard faceplate are shown below.

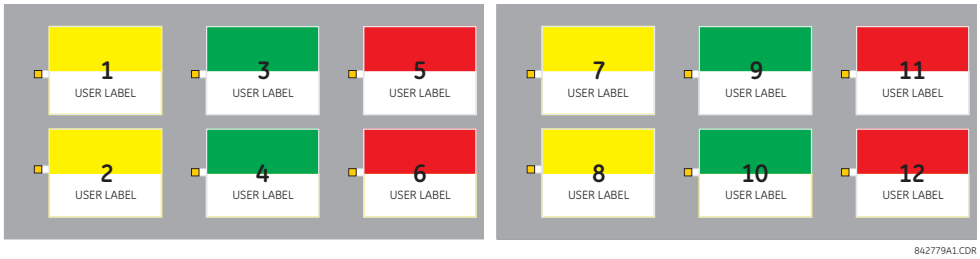


Figure 5–7: USER-PROGRAMMABLE PUSHBUTTONS (STANDARD FACEPLATE)

Both the standard and enhanced faceplate pushbuttons can be custom labeled with a factory-provided template, available online at http://www.GEmultilin.com. The EnerVista UR Setup software can also be used to create labels for the enhanced faceplate.

Each pushbutton asserts its own “On” and “Off” FlexLogic™ operands: PUSHBUTTON 1 ON and PUSHBUTTON 1 OFF. These operands are available for each pushbutton and are used to program specific actions. If any pushbutton is active, the ANY PB ON operand will be asserted.

Each pushbutton has an associated LED indicator. By default, this indicator displays the present status of the corresponding pushbutton (on or off). However, each LED indicator can be assigned to any FlexLogic™ operand through the **PUSHBTN 1 LED CTL** setting.

The pushbuttons can be automatically controlled by activating the operands assigned to the **PUSHBTN 1 SET** (for latched and self-reset mode) and **PUSHBTN 1 RESET** (for latched mode only) settings. The pushbutton reset status is declared when the PUSHBUTTON 1 OFF operand is asserted. The activation and deactivation of user-programmable pushbuttons is dependent on whether latched or self-reset mode is programmed.

- *Latched mode*: In latched mode, a pushbutton can be set (activated) by asserting the operand assigned to the **PUSHBTN 1 SET** setting or by directly pressing the associated front panel pushbutton. The pushbutton maintains the set state until deactivated by the reset command or after a user-specified time delay. The state of each pushbutton is stored in non-volatile memory and maintained through a loss of control power.

  The pushbutton is reset (deactivated) in latched mode by asserting the operand assigned to the **PUSHBTN 1 RESET** setting or by directly pressing the associated active front panel pushbutton.

  It can also be programmed to reset automatically through the **PUSHBTN 1 AUTORST** and **PUSHBTN 1 AUTORST DELAY** settings. These settings enable the autoreset timer and specify the associated time delay. The autoreset timer can be used in select-before-operate (SBO) breaker control applications, where the command type (close/open) or breaker location (feeder number) must be selected prior to command execution. The selection must reset automatically if control is not executed within a specified time period.

- *Self-reset mode*: In self-reset mode, a pushbutton will remain active for the time it is pressed (the *pulse duration*) plus the dropout time specified in the **PUSHBTN 1 DROP-OUT TIME** setting. If the pushbutton is activated via FlexLogic™, the pulse duration is specified by the **PUSHBTN 1 DROP-OUT TIME** only. The time the operand remains assigned to the **PUSHBTN 1 SET** setting has no effect on the pulse duration.

  The pushbutton is reset (deactivated) in self-reset mode when the dropout delay specified in the **PUSHBTN 1 DROP-OUT TIME** setting expires.

NOTE

The pulse duration of the remote set, remote reset, or local pushbutton must be at least 50 ms to operate the pushbutton. This allows the user-programmable pushbuttons to properly operate during power cycling events and various system disturbances that may cause transient assertion of the operating signals.

The local and remote operation of each user-programmable pushbutton can be inhibited through the **PUSHBTN 1 LOCAL** and **PUSHBTN 1 REMOTE** settings, respectively. If local locking is applied, the pushbutton will ignore set and reset commands executed through the front panel pushbuttons. If remote locking is applied, the pushbutton will ignore set and reset commands executed through FlexLogic™ operands.

The locking functions are not applied to the autorestart feature. In this case, the inhibit function can be used in SBO control operations to prevent the pushbutton function from being activated and ensuring “one-at-a-time” select operation.

The locking functions can also be used to prevent the accidental pressing of the front panel pushbuttons. The separate inhibit of the local and remote operation simplifies the implementation of local/remote control supervision.

Pushbutton states can be logged by the event recorder and displayed as target messages. In latched mode, user-defined messages can also be associated with each pushbutton and displayed when the pushbutton is on or changing to off.

- **PUSHBUTTON 1 FUNCTION**: This setting selects the characteristic of the pushbutton. If set to “Disabled”, the pushbutton is not active and the corresponding FlexLogic™ operands (both “On” and “Off”) are de-asserted. If set to “Self-Reset”, the control logic is activated by the pulse (longer than 100 ms) issued when the pushbutton is being physically pressed or virtually pressed via a FlexLogic™ operand assigned to the **PUSHBTN 1 SET** setting.

  When in “Self-Reset” mode and activated locally, the pushbutton control logic asserts the “On” corresponding FlexLogic™ operand as long as the pushbutton is being physically pressed, and after being released the deactivation of the operand is delayed by the drop out timer. The “Off” operand is asserted when the pushbutton element is deactivated. If the pushbutton is activated remotely, the control logic of the pushbutton asserts the corresponding “On” FlexLogic™ operand only for the time period specified by the **PUSHBTN 1 DROP-OUT TIME** setting.

  If set to “Latched”, the control logic alternates the state of the corresponding FlexLogic™ operand between “On” and “Off” on each button press or by virtually activating the pushbutton (assigning set and reset operands). When in the “Latched” mode, the states of the FlexLogic™ operands are stored in a non-volatile memory. Should the power supply be lost, the correct state of the pushbutton is retained upon subsequent power up of the relay.
- **PUSHBTN 1 ID TEXT:** This setting specifies the top 20-character line of the user-programmable message and is intended to provide ID information of the pushbutton. Refer to the *User-definable displays* section for instructions on how to enter alphanumeric characters from the keypad.
- **PUSHBTN 1 ON TEXT:** This setting specifies the bottom 20-character line of the user-programmable message and is displayed when the pushbutton is in the “on” position. Refer to the *User-definable displays* section for instructions on entering alphanumeric characters from the keypad.
- **PUSHBTN 1 OFF TEXT:** This setting specifies the bottom 20-character line of the user-programmable message and is displayed when the pushbutton is activated from the on to the off position and the **PUSHBUTTON 1 FUNCTION** is “Latched”. This message is not displayed when the **PUSHBUTTON 1 FUNCTION** is “Self-reset” as the pushbutton operand status is implied to be “Off” upon its release. The length of the “Off” message is configured with the **PRODUCT SETUP ⇨⇩ DISPLAY PROPERTIES ⇨ FLASH MESSAGE TIME** setting.
- **PUSHBTN 1 SET**: This setting assigns the FlexLogic™ operand serving to operate the pushbutton element and to assert PUSHBUTTON 1 ON operand. The duration of the incoming set signal must be at least 100 ms.
- **PUSHBTN 1 RESET**: This setting assigns the FlexLogic™ operand serving to reset pushbutton element and to assert PUSHBUTTON 1 OFF operand. This setting is applicable only if pushbutton is in latched mode. The duration of the incoming reset signal must be at least 50 ms.
- **PUSHBTN 1 AUTORST**: This setting enables the user-programmable pushbutton autoreset feature. This setting is applicable only if the pushbutton is in the “Latched” mode.

- **PUSHBTN 1 AUTORST DELAY**: This setting specifies the time delay for automatic reset of the pushbutton when in the latched mode.
- **PUSHBTN 1 REMOTE**: This setting assigns the FlexLogic™ operand serving to inhibit pushbutton operation from the operand assigned to the **PUSHBTN 1 SET** or **PUSHBTN 1 RESET** settings.
- **PUSHBTN 1 LOCAL**: This setting assigns the FlexLogic™ operand serving to inhibit pushbutton operation from the front panel pushbuttons. This locking functionality is not applicable to pushbutton autoreset.
- **PUSHBTN 1 DROP-OUT TIME**: This setting applies only to "Self-Reset" mode and specifies the duration of the pushbutton active status after the pushbutton has been released. This setting is required to set the duration of the pushbutton operating pulse.
- **PUSHBTN 1 LED CTL**: This setting assigns the FlexLogic™ operand serving to drive pushbutton LED. If this setting is "Off", then LED operation is directly linked to PUSHBUTTON 1 ON operand.
- **PUSHBTN 1 MESSAGE**: If pushbutton message is set to "High Priority", the message programmed in the **PUSHBTN 1 ID** and **PUSHBTN 1 ON TEXT** settings will be displayed undisturbed as long as PUSHBUTTON 1 ON operand is asserted. The high priority option is not applicable to the **PUSHBTN 1 OFF TEXT** setting.

  This message can be temporary removed if any front panel keypad button is pressed. However, ten seconds of keypad inactivity will restore the message if the PUSHBUTTON 1 ON operand is still active.

  If the **PUSHBTN 1 MESSAGE** is set to "Normal", the message programmed in the **PUSHBTN 1 ID** and **PUSHBTN 1 ON TEXT** settings will be displayed as long as PUSHBUTTON 1 ON operand is asserted, but not longer than time period specified by **FLASH MESSAGE TIME** setting. After the flash time is expired, the default message or other active target message is displayed. The instantaneous reset of the flash message will be executed if any relay front panel button is pressed or any new target or message becomes active.

  The **PUSHBTN 1 OFF TEXT** setting is linked to PUSHBUTTON 1 OFF operand and will be displayed in conjunction with **PUSHBTN 1 ID** only if pushbutton element is in the "Latched" mode. The **PUSHBTN 1 OFF TEXT** message will be displayed as "Normal" if the **PUSHBTN 1 MESSAGE** setting is "High Priority" or "Normal".
- **PUSHBUTTON 1 EVENTS**: If this setting is enabled, each pushbutton state change will be logged as an event into event recorder.

The user-programmable pushbutton logic is shown below.

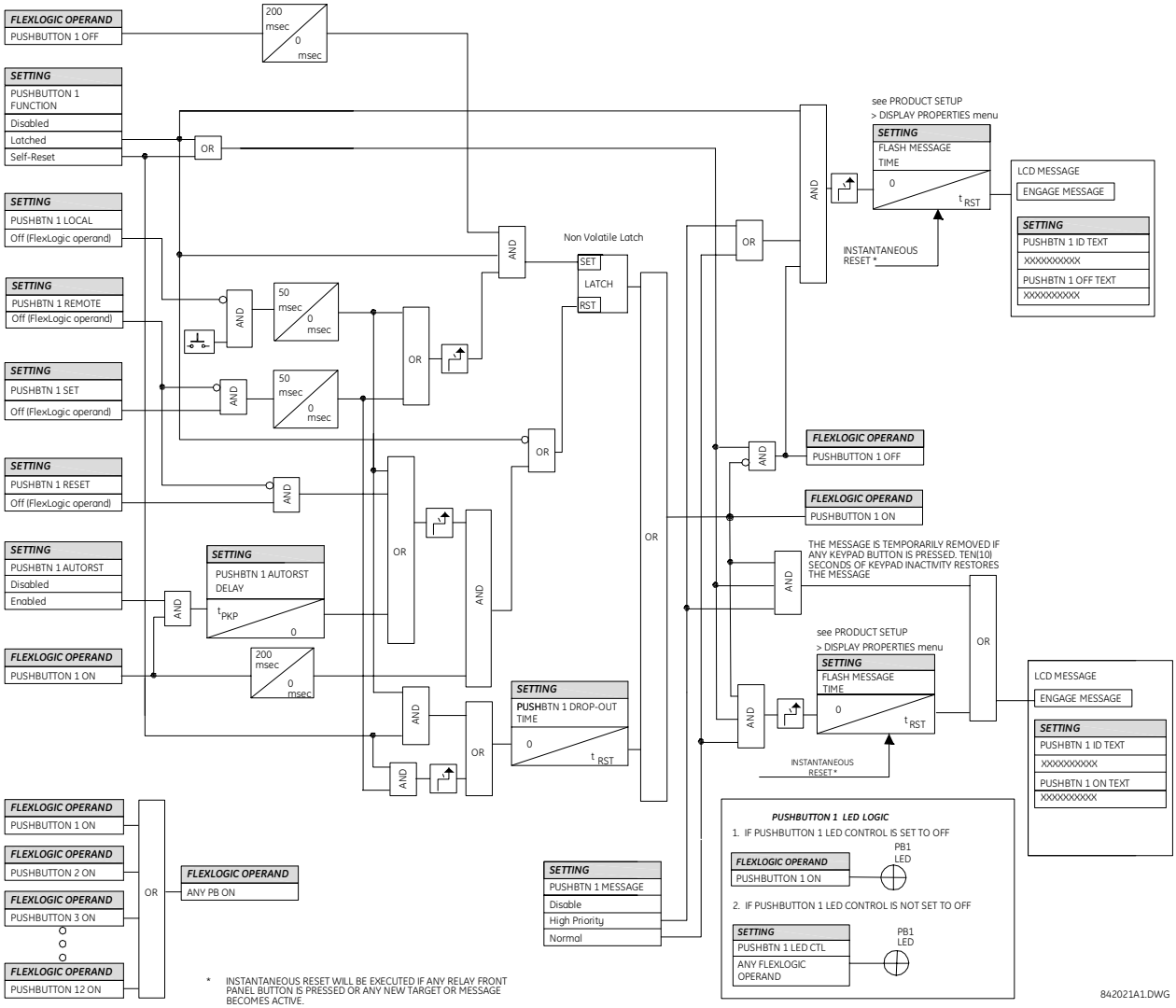


Figure 5–8: USER-PROGRAMMABLE PUSHBUTTON LOGIC

NOTE

User-programmable pushbuttons require a type HP or HQ faceplate. If an HP or HQ type faceplate was ordered separately, the relay order code must be changed to indicate the correct faceplate option. This can be done via EnerVista UR Setup with the **Maintenance > Enable Pushbutton** command.

5.2.14 FLEX STATE PARAMETERS

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ FLEX STATE PARAMETERS

■ FLEX STATE ■ PARAMETERS		PARAMETER 1: Off	*Range: FlexLogic™ operand*
MESSAGE		PARAMETER 2: Off	*Range: FlexLogic™ operand*
	↓		
MESSAGE		PARAMETER 256: Off	*Range: FlexLogic™ operand*

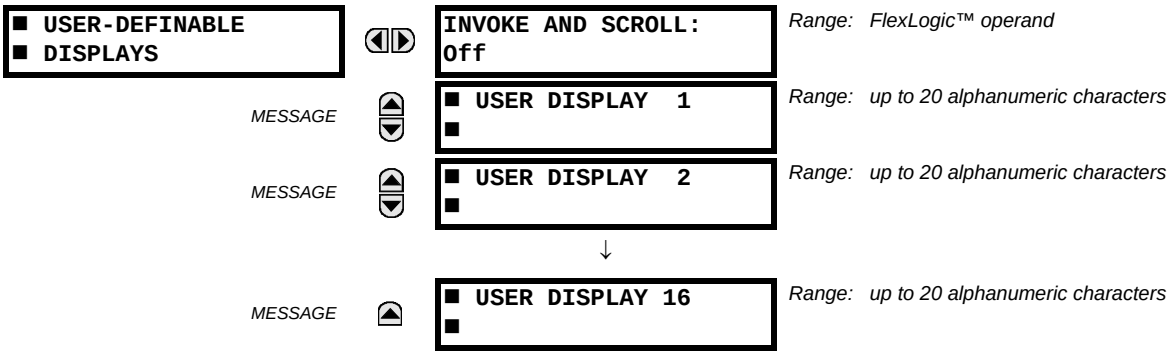
This feature provides a mechanism where any of 256 selected FlexLogic™ operand states can be used for efficient monitoring. The feature allows user-customized access to the FlexLogic™ operand states in the relay. The state bits are packed so that 16 states may be read out in a single Modbus register. The state bits can be configured so that all of the states which are of interest to the user are available in a minimum number of Modbus registers.

The state bits may be read out in the "Flex States" register array beginning at Modbus address 0900h. Sixteen states are packed into each register, with the lowest-numbered state in the lowest-order bit. There are sixteen registers to accommodate the 256 state bits.

5.2.15 USER-DEFINABLE DISPLAYS

a) MAIN MENU

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-DEFINABLE DISPLAYS



This menu provides a mechanism for manually creating up to 16 user-defined information displays in a convenient viewing sequence in the **USER DISPLAYS** menu (between the **TARGETS** and **ACTUAL VALUES** top-level menus). The sub-menus facilitate text entry and Modbus Register data pointer options for defining the User Display content.

Once programmed, the user-definable displays can be viewed in two ways.

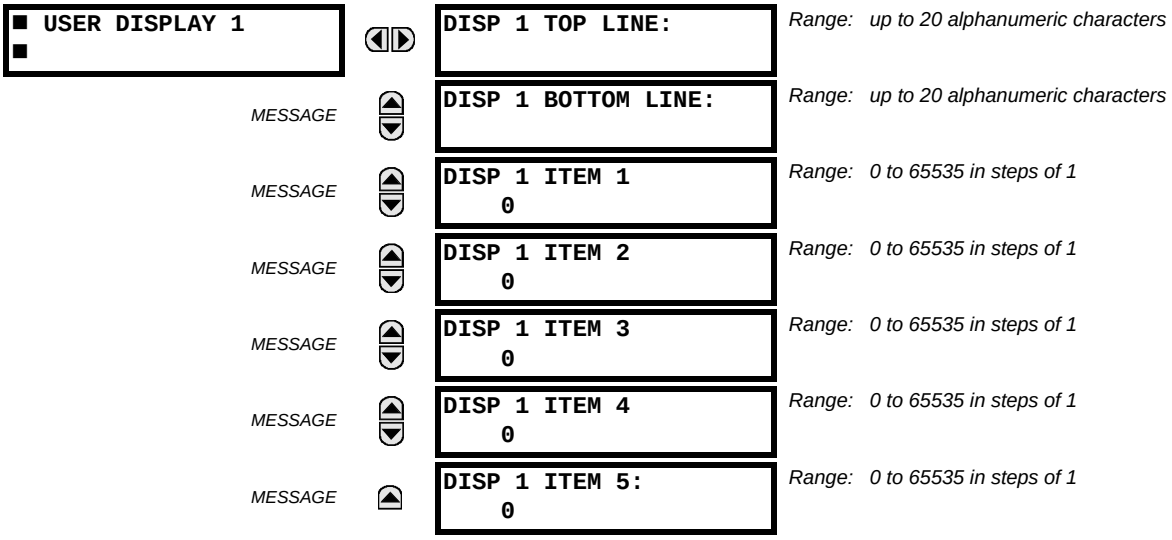
- **KEYPAD**: Use the Menu key to select the **USER DISPLAYS** menu item to access the first user-definable display (note that only the programmed screens are displayed). The screens can be scrolled using the Up and Down keys. The display disappears after the default message time-out period specified by the **PRODUCT SETUP ⇨⇩ DISPLAY PROPERTIES ⇨⇩ DEFAULT MESSAGE TIMEOUT** setting.
- **USER-PROGRAMMABLE CONTROL INPUT**: The user-definable displays also respond to the **INVOKE AND SCROLL** setting. Any FlexLogic™ operand (in particular, the user-programmable pushbutton operands), can be used to navigate the programmed displays.

  On the rising edge of the configured operand (such as when the pushbutton is pressed), the displays are invoked by showing the last user-definable display shown during the previous activity. From this moment onward, the operand acts exactly as the Down key and allows scrolling through the configured displays. The last display wraps up to the first one. The **INVOKE AND SCROLL** input and the Down keypad key operate concurrently.

  When the default timer expires (set by the **DEFAULT MESSAGE TIMEOUT** setting), the relay will start to cycle through the user displays. The next activity of the **INVOKE AND SCROLL** input stops the cycling at the currently displayed user display, not at the first user-defined display. The **INVOKE AND SCROLL** pulses must last for at least 250 ms to take effect.

b) USER DISPLAY 1(16)

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-DEFINABLE DISPLAYS ⇨ USER DISPLAY 1(16)



Any existing system display can be automatically copied into an available user display by selecting the existing display and pressing the ENTER key. The display will then prompt **ADD TO USER DISPLAY LIST?**. After selecting "Yes", a message indicates that the selected display has been added to the user display list. When this type of entry occurs, the sub-menus are automatically configured with the proper content – this content may subsequently be edited.

This menu is used **to enter** user-defined text and/or user-selected Modbus-registered data fields into the particular user display. Each user display consists of two 20-character lines (top and bottom). The tilde (~) character is used to mark the start of a data field - the length of the data field needs to be accounted for. Up to 5 separate data fields (**ITEM 1(5)**) can be entered in a user display - the *n*th tilde (~) refers to the *n*th item.

A User Display may be entered from the faceplate keypad or the EnerVista UR Setup interface (preferred for convenience). The following procedure shows how to enter text characters in the top and bottom lines from the faceplate keypad:

1. Select the line to be edited.
2. Press the decimal key to enter text edit mode.
3. Use either value key to scroll through the characters. A space is selected like a character.
4. Press the decimal key to advance the cursor to the next position.
5. Repeat step 3 and continue entering characters until the desired text is displayed.
6. The HELP key may be pressed at any time for context sensitive help information.
7. Press the ENTER key to store the new settings.

To enter a numerical value for any of the 5 items (the *decimal form* of the selected Modbus address) from the faceplate keypad, use the number keypad. Use the value of '0' for any items not being used. Use the HELP key at any selected system display (setting, actual value, or command) which has a Modbus address, to view the *hexadecimal form* of the Modbus address, then manually convert it to decimal form before entering it (EnerVista UR Setup usage conveniently facilitates this conversion).

Use the MENU key to go to the user displays menu **to view** the user-defined content. The current user displays will show in sequence, changing every 4 seconds. While viewing a user display, press the ENTER key and then select the 'Yes" option **to remove** the display from the user display list. Use the MENU key again **to exit** the user displays menu.

An example User Display setup and result is shown below:

■ USER DISPLAY 1 ■		DISP 1 TOP LINE: Current X ~ A	Shows user-defined text with first Tilde marker.
	MESSAGE	DISP 1 BOTTOM LINE: Current Y ~ A	Shows user-defined text with second Tilde marker.
	MESSAGE	DISP 1 ITEM 1: 6016	Shows decimal form of user-selected Modbus Register Address, corresponding to first Tilde marker.
	MESSAGE	DISP 1 ITEM 2: 6357	Shows decimal form of user-selected Modbus Register Address, corresponding to 2nd Tilde marker.
	MESSAGE	DISP 1 ITEM 3: 0	This item is not being used - there is no corresponding Tilde marker in Top or Bottom lines.
	MESSAGE	DISP 1 ITEM 4: 0	This item is not being used - there is no corresponding Tilde marker in Top or Bottom lines.
	MESSAGE	DISP 1 ITEM 5: 0	This item is not being used - there is no corresponding Tilde marker in Top or Bottom lines.
USER DISPLAYS	→	Current X 0.850 A Current Y 0.327 A	Shows the resultant display content.

5.2.16 DIRECT INPUTS/OUTPUTS

a) MAIN MENU

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ DIRECT I/O

■ DIRECT I/O ■		DIRECT OUTPUT DEVICE ID: 1	*Range: 1 to 16*
	MESSAGE	DIRECT I/O CH1 RING CONFIGURATION: Yes	*Range: Yes, No*
	MESSAGE	DIRECT I/O CH2 RING CONFIGURATION: Yes	*Range: Yes, No*
	MESSAGE	DIRECT I/O DATA RATE: 64 kbps	*Range: 64 kbps, 128 kbps*
	MESSAGE	DIRECT I/O CHANNEL CROSSOVER: Disabled	*Range: Disabled, Enabled*
	MESSAGE	■ CRC ALARM CH1 ■	**See page 5–54.**
	MESSAGE	■ CRC ALARM CH2 ■	**See page 5–54.**
	MESSAGE	■ UNRETURNED ■ MESSAGES ALARM CH1	**See page 5–55.**
	MESSAGE	■ UNRETURNED ■ MESSAGES ALARM CH2	**See page 5–55.**

Direct inputs and outputs are intended for exchange of status information (inputs and outputs) between UR-series relays connected directly via type 7 digital communications cards. The mechanism is very similar to IEC 61850 GSSE, except that communications takes place over a non-switchable isolated network and is optimized for speed. On type 7 cards that support two channels, direct output messages are sent from both channels simultaneously. This effectively sends direct output

messages both ways around a ring configuration. On type 7 cards that support one channel, direct output messages are sent only in one direction. Messages will be resent (forwarded) when it is determined that the message did not originate at the receiver.

Direct output message timing is similar to GSSE message timing. Integrity messages (with no state changes) are sent at least every 1000 ms. Messages with state changes are sent within the main pass scanning the inputs and asserting the outputs unless the communication channel bandwidth has been exceeded. Two self-tests are performed and signaled by the following FlexLogic™ operands:

1. DIRECT RING BREAK (direct input/output ring break). This FlexLogic™ operand indicates that direct output messages sent from a UR-series relay are not being received back by the relay.
2. DIRECT DEVICE 1(16) OFF (direct device offline). This FlexLogic™ operand indicates that direct output messages from at least one direct device are not being received.

Direct input and output settings are similar to remote input and output settings. The equivalent of the remote device name strings for direct inputs and outputs is the **DIRECT OUTPUT DEVICE ID**. The **DIRECT OUTPUT DEVICE ID** identifies the relay in all direct output messages. All UR-series IEDs in a ring should have unique numbers assigned. The IED ID is used to identify the sender of the direct input/output message.

If the direct input/output scheme is configured to operate in a ring (**DIRECT I/O RING CONFIGURATION**: "Yes"), all direct output messages should be received back. If not, the DIRECT INPUT/OUTPUT RING BREAK self-test is triggered. The self-test error is signaled by the DIRECT RING BREAK FlexLogic™ operand.

Select the **DIRECT I/O DATA RATE** to match the data capabilities of the communications channel. All IEDs communicating over direct inputs/outputs must be set to the same data rate. UR-series IEDs equipped with dual-channel communications cards apply the same data rate to both channels. Delivery time for direct input/output messages is approximately 0.2 of a power system cycle at 128 kbps and 0.4 of a power system cycle at 64 kbps, per each 'bridge'.

Table 5–5: DIRECT INPUT AND OUTPUT DATA RATES

MODULE	CHANNEL	SUPPORTED DATA RATES
74	Channel 1	64 kHz
	Channel 2	64 kHz
7L	Channel 1	64 kHz, 128 kHz
	Channel 2	64 kHz, 128 kHz
7M	Channel 1	64 kHz, 128 kHz
	Channel 2	64 kHz, 128 kHz
7P	Channel 1	64 kHz, 128 kHz
	Channel 2	64 kHz, 128 kHz
7T	Channel 1	64 kHz, 128 kHz
7W	Channel 1	64 kHz, 128 kHz
	Channel 2	64 kHz, 128 kHz
7V	Channel 1	64 kHz, 128 kHz
	Channel 2	64 kHz, 128 kHz
2A	Channel 1	64 kHz
2B	Channel 1	64 kHz
	Channel 2	64 kHz
76	Channel 1	64 kHz
77	Channel 1	64 kHz
	Channel 2	64 kHz
75	Channel 1	64 kHz
	Channel 2	64 kHz
7E	Channel 1	64 kHz
	Channel 2	64 kHz
7F	Channel 1	64 kHz
	Channel 2	64 kHz
7G	Channel 1	64 kHz
	Channel 2	64 kHz
7Q	Channel 1	64 kHz
	Channel 2	64 kHz
7R	Channel 1	64 kHz
7S	Channel 1	64 kHz
	Channel 2	64 kHz

NOTE

The G.703 modules are fixed at 64 kbps. The DIRECT I/O DATA RATE setting is not applicable to these modules.

The **DIRECT I/O CHANNEL CROSSOVER** setting applies to L60s with dual-channel communication cards and allows crossing over messages from channel 1 to channel 2. This places all UR-series IEDs into one direct input/output network regardless of the physical media of the two communication channels.

The following application examples illustrate the basic concepts for direct input/output configuration. Please refer to the *Inputs/Outputs* section in this chapter for information on configuring FlexLogic™ operands (flags, bits) to be exchanged.

EXAMPLE 1: EXTENDING THE INPUT/OUTPUT CAPABILITIES OF A UR-SERIES RELAY

Consider an application that requires additional quantities of digital inputs and/or output contacts and/or lines of programmable logic that exceed the capabilities of a single UR-series chassis. The problem is solved by adding an extra UR-series IED, such as the C30, to satisfy the additional input/output and programmable logic requirements. The two IEDs are connected via single-channel digital communication cards as shown in the figure below.

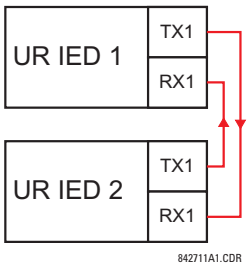


Figure 5–9: INPUT/OUTPUT EXTENSION VIA DIRECT INPUTS/OUTPUTS

In the above application, the following settings should be applied:

UR IED 1: **DIRECT OUTPUT DEVICE ID:** "1"
DIRECT I/O RING CONFIGURATION: "Yes"
DIRECT I/O DATA RATE: "128 kbps"

UR IED 2: **DIRECT OUTPUT DEVICE ID:** "2"
DIRECT I/O RING CONFIGURATION: "Yes"
DIRECT I/O DATA RATE: "128 kbps"

The message delivery time is about 0.2 of power cycle in both ways (at 128 kbps); i.e., from Device 1 to Device 2, and from Device 2 to Device 1. Different communications cards can be selected by the user for this back-to-back connection (fiber, G.703, or RS422).

5

EXAMPLE 2: INTERLOCKING BUSBAR PROTECTION

A simple interlocking busbar protection scheme could be accomplished by sending a blocking signal from downstream devices, say 2, 3, and 4, to the upstream device that monitors a single incomer of the busbar, as shown below.

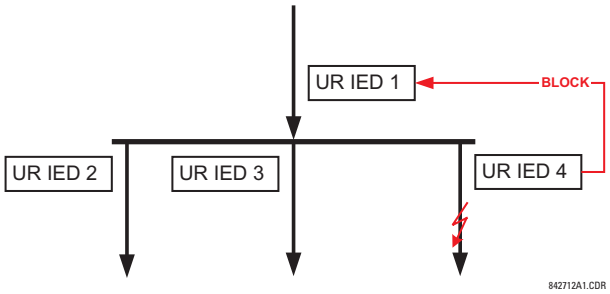


Figure 5–10: SAMPLE INTERLOCKING BUSBAR PROTECTION SCHEME

For increased reliability, a dual-ring configuration (shown below) is recommended for this application.

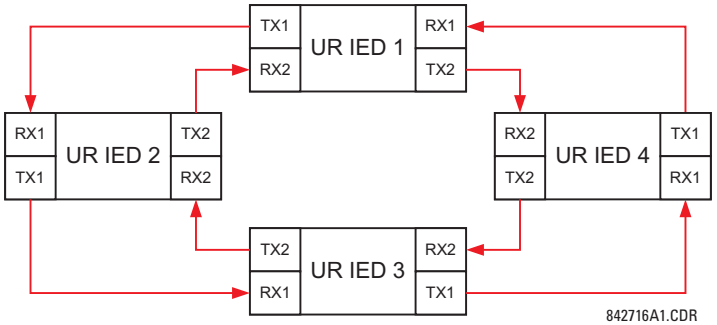


Figure 5–11: INTERLOCKING BUS PROTECTION SCHEME VIA DIRECT INPUTS/OUTPUTS

In the above application, the following settings should be applied:

UR IED 1: **DIRECT OUTPUT DEVICE ID:** "1"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 2: **DIRECT OUTPUT DEVICE ID:** "2"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 3: **DIRECT OUTPUT DEVICE ID:** "3"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 4: **DIRECT OUTPUT DEVICE ID:** "4"
DIRECT I/O RING CONFIGURATION: "Yes"

Message delivery time is approximately 0.2 of power system cycle (at 128 kbps) times number of 'bridges' between the origin and destination. Dual-ring configuration effectively reduces the maximum 'communications distance' by a factor of two.

In this configuration the following delivery times are expected (at 128 kbps) if both rings are healthy:

IED 1 to IED 2: 0.2 of power system cycle; IED 1 to IED 3: 0.4 of power system cycle;
IED 1 to IED 4: 0.2 of power system cycle; IED 2 to IED 3: 0.2 of power system cycle;
IED 2 to IED 4: 0.4 of power system cycle; IED 3 to IED 4: 0.2 of power system cycle

If one ring is broken (say TX2/RX2) the delivery times are as follows:

IED 1 to IED 2: 0.2 of power system cycle; IED 1 to IED 3: 0.4 of power system cycle;
IED 1 to IED 4: 0.6 of power system cycle; IED 2 to IED 3: 0.2 of power system cycle;
IED 2 to IED 4: 0.4 of power system cycle; IED 3 to IED 4: 0.2 of power system cycle

A coordinating timer for this bus protection scheme could be selected to cover the worst case scenario (0.4 of power system cycle). Upon detecting a broken ring, the coordination time should be adaptively increased to 0.6 of power system cycle. The complete application requires addressing a number of issues such as failure of both the communications rings, failure or out-of-service conditions of one of the relays, etc. Self-monitoring flags of the direct inputs/outputs feature would be primarily used to address these concerns.

EXAMPLE 3: PILOT-AIDED SCHEMES

Consider the three-terminal line protection application shown below:

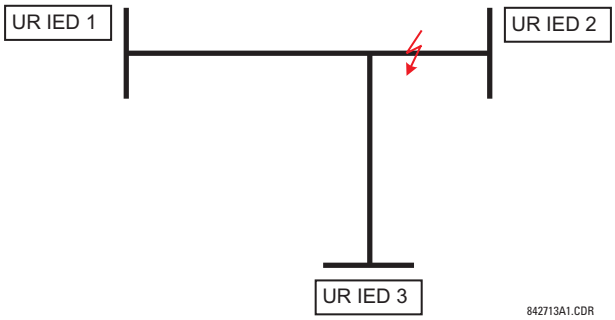


Figure 5–12: THREE-TERMINAL LINE APPLICATION

A permissive pilot-aided scheme could be implemented in a two-ring configuration as shown below (IEDs 1 and 2 constitute a first ring, while IEDs 2 and 3 constitute a second ring):

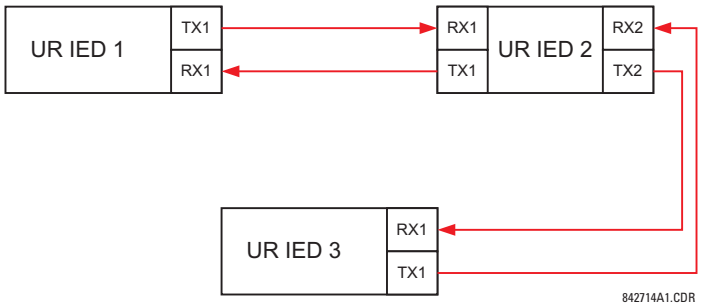


Figure 5–13: SINGLE-CHANNEL OPEN LOOP CONFIGURATION

In the above application, the following settings should be applied:

UR IED 1: **DIRECT OUTPUT DEVICE ID:** "1"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 2: **DIRECT OUTPUT DEVICE ID:** "2"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 3: **DIRECT OUTPUT DEVICE ID:** "3"
DIRECT I/O RING CONFIGURATION: "Yes"

In this configuration the following delivery times are expected (at 128 kbps):

IED 1 to IED 2: 0.2 of power system cycle; IED 1 to IED 3: 0.5 of power system cycle;
IED 2 to IED 3: 0.2 of power system cycle

In the above scheme, IEDs 1 and 3 do not communicate directly. IED 2 must be configured to forward the messages as explained in the *Inputs/Outputs* section. A blocking pilot-aided scheme should be implemented with more security and, ideally, faster message delivery time. This could be accomplished using a dual-ring configuration as shown below.

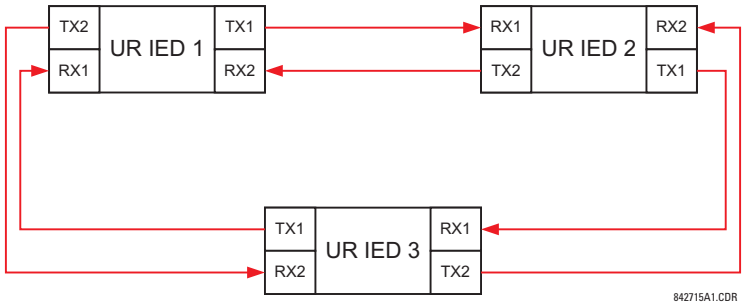


Figure 5–14: DUAL-CHANNEL CLOSED LOOP (DUAL-RING) CONFIGURATION

In the above application, the following settings should be applied:

UR IED 1: **DIRECT OUTPUT DEVICE ID:** "1"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 2: **DIRECT OUTPUT DEVICE ID:** "2"
DIRECT I/O RING CONFIGURATION: "Yes"

UR IED 3: **DIRECT OUTPUT DEVICE ID:** "3"
DIRECT I/O RING CONFIGURATION: "Yes"

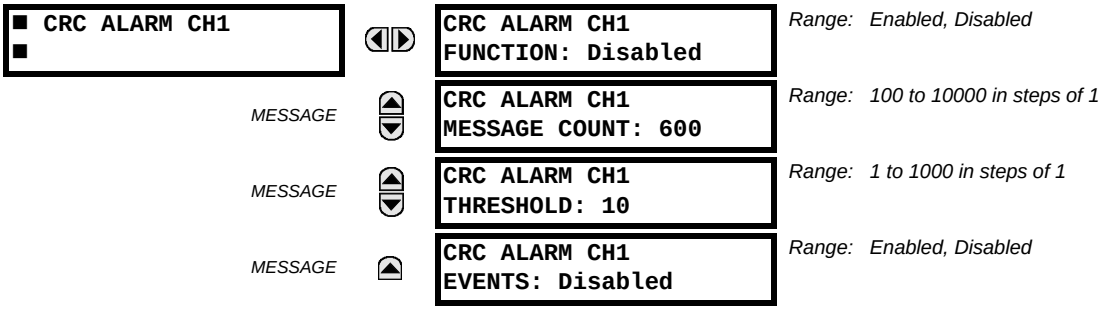
In this configuration the following delivery times are expected (at 128 kbps) if both the rings are healthy:

IED 1 to IED 2: 0.2 of power system cycle; IED 1 to IED 3: 0.2 of power system cycle;
IED 2 to IED 3: 0.2 of power system cycle

The two communications configurations could be applied to both permissive and blocking schemes. Speed, reliability and cost should be taken into account when selecting the required architecture.

b) CRC ALARM CH1(2)

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ DIRECT I/O ⇨⇩ CRC ALARM CH1(2)



The L60 checks integrity of the incoming direct input/output messages using a 32-bit CRC. The CRC Alarm function is available for monitoring the communication medium noise by tracking the rate of messages failing the CRC check. The monitoring function counts all incoming messages, including messages that failed the CRC check. A separate counter adds up messages that failed the CRC check. When the failed CRC counter reaches the user-defined level specified by the **CRC ALARM CH1 THRESHOLD** setting within the user-defined message count **CRC ALARM 1 CH1 COUNT**, the DIR IO CH1 CRC ALARM FlexLogic™ operand is set.

When the total message counter reaches the user-defined maximum specified by the **CRC ALARM CH1 MESSAGE COUNT** setting, both the counters reset and the monitoring process is restarted.

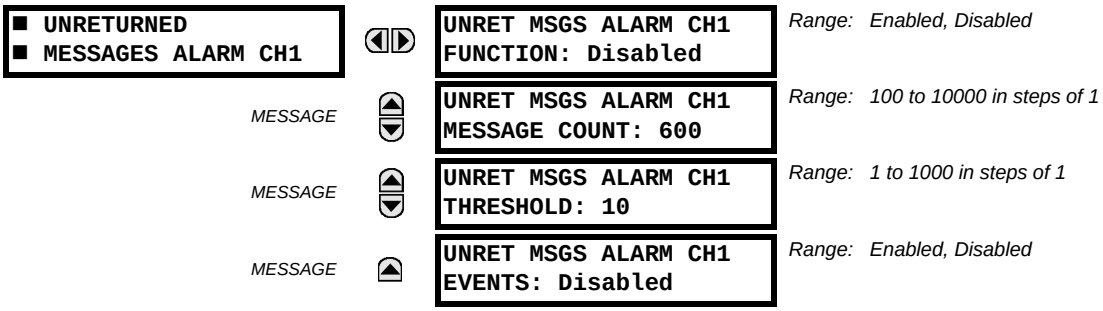
The operand shall be configured to drive an output contact, user-programmable LED, or selected communication-based output. Latching and acknowledging conditions - if required - should be programmed accordingly.

The CRC Alarm function is available on a per-channel basis. The total number of direct input/output messages that failed the CRC check is available as the ACTUAL VALUES ⇨ STATUS ⇨⇩ DIRECT INPUTS ⇨⇩ CRC FAIL COUNT CH1(2) actual value.

- **Message Count and Length of the Monitoring Window:** To monitor communications integrity, the relay sends 1 message per second (at 64 kbps) or 2 messages per second (128 kbps) even if there is no change in the direct outputs. For example, setting the **CRC ALARM CH1 MESSAGE COUNT** to "10000", corresponds a time window of about 160 minutes at 64 kbps and 80 minutes at 128 kbps. If the messages are sent faster as a result of direct outputs activity, the monitoring time interval will shorten. This should be taken into account when determining the **CRC ALARM CH1 MESSAGE COUNT** setting. For example, if the requirement is a maximum monitoring time interval of 10 minutes at 64 kbps, then the **CRC ALARM CH1 MESSAGE COUNT** should be set to $10 \times 60 \times 1 = 600$.
- **Correlation of Failed CRC and Bit Error Rate (BER):** The CRC check may fail if one or more bits in a packet are corrupted. Therefore, an exact correlation between the CRC fail rate and the BER is not possible. Under certain assumptions an approximation can be made as follows. A direct input/output packet containing 20 bytes results in 160 bits of data being sent and therefore, a transmission of 63 packets is equivalent to 10,000 bits. A BER of 10^{-4} implies 1 bit error for every 10,000 bits sent/received. Assuming the best case of only 1 bit error in a failed packet, having 1 failed packet for every 63 received is about equal to a BER of 10^{-4}.

c) UNRETURNED MESSAGES ALARM CH1(2)

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ DIRECT I/O ⇨⇩ UNRETURNED MESSAGES ALARM CH1(2)



The L60 checks integrity of the direct input/output communication ring by counting unreturned messages. In the ring configuration, all messages originating at a given device should return within a pre-defined period of time. The Unreturned Messages Alarm function is available for monitoring the integrity of the communication ring by tracking the rate of unreturned messages. This function counts all the outgoing messages and a separate counter adds the messages have failed to return. When the unreturned messages counter reaches the user-definable level specified by the **UNRET MSGS ALARM CH1 THRESHOLD** setting and within the user-defined message count **UNRET MSGS ALARM CH1 COUNT**, the DIR IO CH1 UNRET ALM FlexLogic™ operand is set.

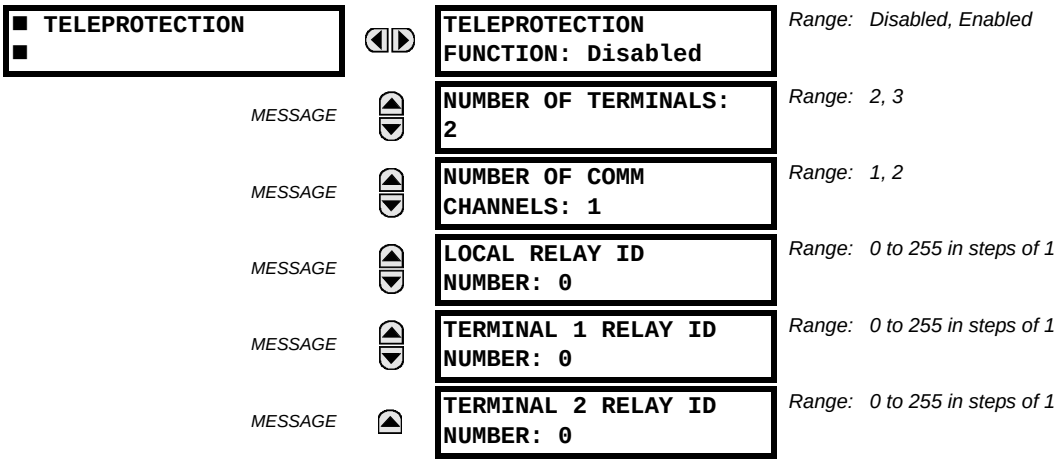
When the total message counter reaches the user-defined maximum specified by the **UNRET MSGS ALARM CH1 MESSAGE COUNT** setting, both the counters reset and the monitoring process is restarted.

The operand shall be configured to drive an output contact, user-programmable LED, or selected communication-based output. Latching and acknowledging conditions, if required, should be programmed accordingly.

The Unreturned Messages Alarm function is available on a per-channel basis and is active only in the ring configuration. The total number of unreturned input/output messages is available as the ACTUAL VALUES ⇨ STATUS ⇨⇩ DIRECT INPUTS ⇨⇩ UNRETURNED MSG COUNT CH1(2) actual value.

5.2.17 TELEPROTECTION

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ TELEPROTECTION



Digital teleprotection functionality is designed to transfer protection commands between 2 or 3 relays in a secure, fast, dependable, and deterministic fashion. Possible applications are permissive or blocking pilot schemes and direct transfer trip (DTT). Teleprotection can be applied over any analog or digital channels and any communications media, such as direct fiber, copper wires, optical networks, or microwave radio links. A mixture of communication media is possible.

Once teleprotection is enabled and the teleprotection input/outputs are configured, data packets are transmitted continuously every 1/4 cycle (3/8 cycle if using C37.94 modules) from peer-to-peer. Security of communication channel data is achieved by using CRC-32 on the data packet.

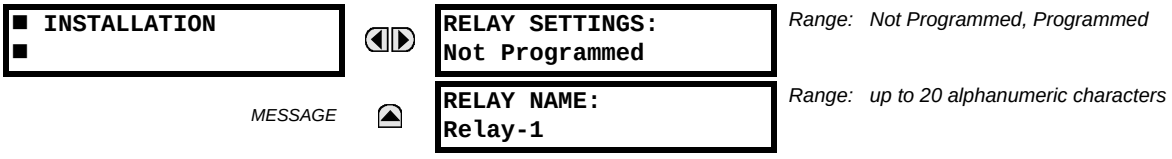
NOTE

Teleprotection inputs/outputs and direct inputs/outputs are mutually exclusive – as such, they cannot be used simulatneously. Once teleprotection inputs/outputs are enabled, direct inputs/outputs are blocked, and *vice versa*.

- **NUMBER OF TERMINALS**: Specifies whether the teleprotection system operates between 2 peers or 3 peers.
- **NUMBER OF CHANNELS**: Specifies how many channels are used. If the **NUMBER OF TERMINALS** is “3” (three-terminal system), set the **NUMBER OF CHANNELS** to “2”. For a two-terminal system, the **NUMBER OF CHANNELS** can set to “1” or “2” (redundant channels).
- **LOCAL RELAY ID NUMBER**, **TERMINAL 1 RELAY ID NUMBER**, and **TERMINAL 2 RELAY ID NUMBER**: In installations that use multiplexers or modems, it is desirable to ensure that the data used by the relays protecting a given line is from the correct relays. The teleprotection function performs this check by reading the message ID sent by transmitting relays and comparing it to the programmed ID in the receiving relay. This check is also used to block inputs if inadvertently set to loopback mode or data is being received from a wrong relay by checking the ID on a received channel. If an incorrect ID is found on a channel during normal operation, the TELEPROT CH1(2) ID FAIL FlexLogic™ operand is set, driving the event with the same name and blocking the teleprotection inputs. For commissioning purposes, the result of channel identification is also shown in the **STATUS ⇨⇩ CHANNEL TESTS ⇨⇩ VALIDITY OF CHANNEL CONFIGURATION** actual value. The default value of “0” for the **LOCAL RELAY ID NUMBER** indicates that relay ID is not to be checked. On two- terminals two-channel systems, the same **LOCAL RELAY ID NUMBER** is transmitted over both channels; as such, only the **TERMINAL 1 ID NUMBER** has to be programmed on the receiving end.

5.2.18 INSTALLATION

PATH: SETTINGS ⇨ PRODUCT SETUP ⇨⇩ INSTALLATION

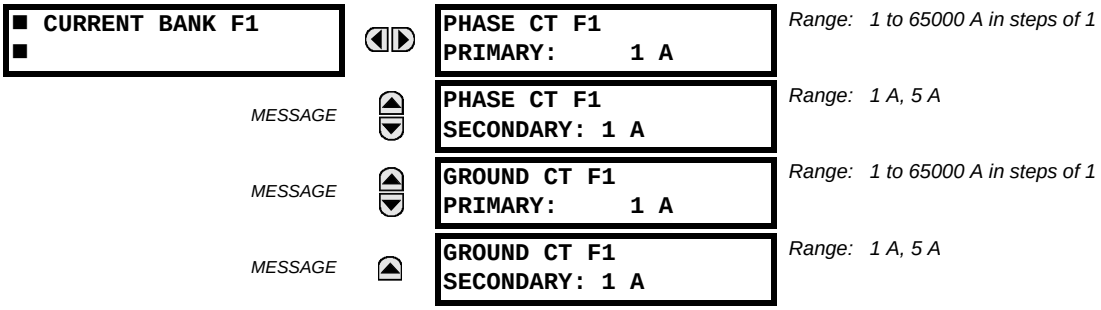


To safeguard against the installation of a relay without any entered settings, the unit will not allow signaling of any output relay until **RELAY SETTINGS** is set to "Programmed". This setting is defaulted to "Not Programmed" when at the factory. The **UNIT NOT PROGRAMMED** self-test error message is displayed until the relay is put into the "Programmed" state.

The **RELAY NAME** setting allows the user to uniquely identify a relay. This name will appear on generated reports. This name is also used to identify specific devices which are engaged in automatically sending/receiving data over the Ethernet communications channel using the IEC 61850 protocol.

a) CURRENT BANKS

PATH: SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨ CURRENT BANK F1(F5)



NOTE

Because energy parameters are accumulated, these values should be recorded and then reset immediately prior to changing CT characteristics.

Two banks of phase/ground CTs can be set, where the current banks are denoted in the following format (*X* represents the module slot position letter):

Xa, where ***X*** = {**F**} and ***a*** = {**1**, **5**}.

See the *Introduction to AC Sources* section at the beginning of this chapter for additional details.

These settings are critical for all features that have settings dependent on current measurements. When the relay is ordered, the CT module must be specified to include a standard or sensitive ground input. As the phase CTs are connected in Wye (star), the calculated phasor sum of the three phase currents (IA + IB + IC = Neutral Current = 3Io) is used as the input for the neutral overcurrent elements. In addition, a zero-sequence (core balance) CT which senses current in all of the circuit primary conductors, or a CT in a neutral grounding conductor may also be used. For this configuration, the ground CT primary rating must be entered. To detect low level ground fault currents, the sensitive ground input may be used. In this case, the sensitive ground CT primary rating must be entered. Refer to *Chapter 3* for more details on CT connections.

Enter the rated CT primary current values. For both 1000:5 and 1000:1 CTs, the entry would be 1000. For correct operation, the CT secondary rating must match the setting (which must also correspond to the specific CT connections used).

The following example illustrates how multiple CT inputs (current banks) are summed as one source current. Given If the following current banks:

F1: CT bank with 500:1 ratio; F5: CT bank with 1000: ratio

The following rule applies:

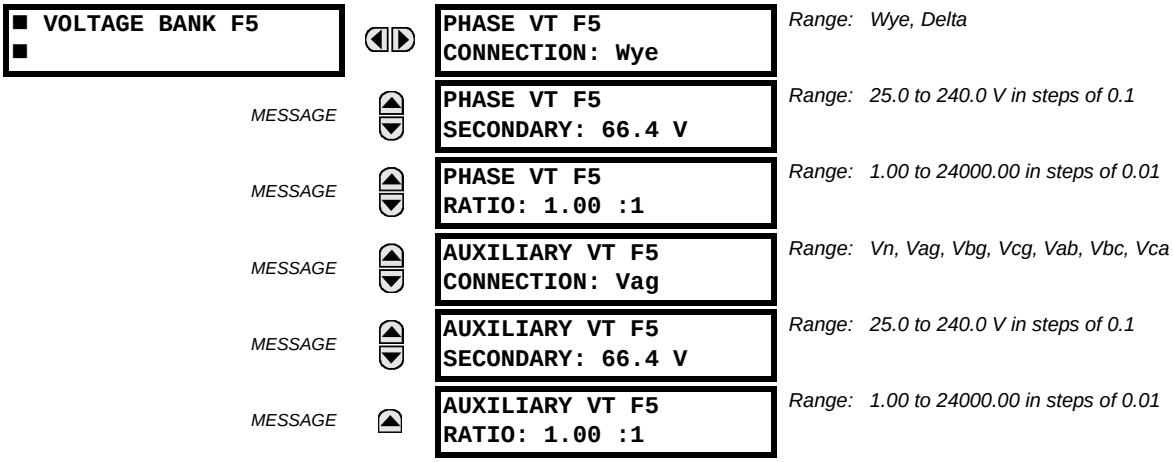
$$\text{SRC 1} = \text{F1} + \text{F5} \qquad \textbf{(EQ 5.6)}$$

1 pu is the highest primary current. In this case, 1000 is entered and the secondary current from the 500:1 and 800:1 ratio CTs will be adjusted to that created by a 1000:1 CT before summation. If a protection element is set up to act on SRC 1 currents, then a pickup level of 1 pu will operate on 1000 A primary.

The same rule applies for current sums from CTs with different secondary taps (5 A and 1 A).

b) VOLTAGE BANKS

PATH: SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨⇩ VOLTAGE BANK F5



One bank of phase/auxiliary VTs can be set, where voltage banks are denoted in the following format (*X* represents the module slot position letter):

Xa, where ***X*** = {**F**} and ***a*** = {**5**}.

See the *Introduction to AC Sources* section at the beginning of this chapter for additional details.

With VTs installed, the relay can perform voltage measurements as well as power calculations. Enter the **PHASE VT F5 CONNECTION** made to the system as "Wye" or "Delta". An open-delta source VT connection would be entered as "Delta".

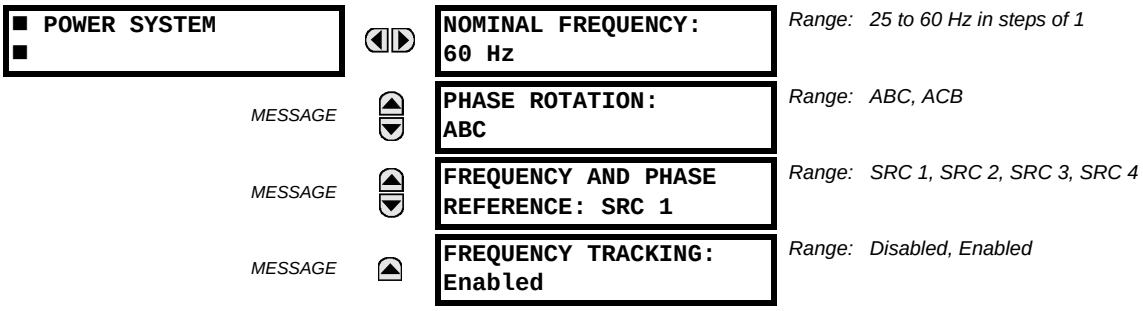
NOTE

The nominal **PHASE VT F5 SECONDARY** voltage setting is the voltage across the relay input terminals when nominal voltage is applied to the VT primary.

For example, on a system with a 13.8 kV nominal primary voltage and with a 14400:120 volt VT in a Delta connection, the secondary voltage would be 115, i.e. (13800 / 14400) × 120. For a Wye connection, the voltage value entered must be the phase to neutral voltage which would be $115 / \sqrt{3} = 66.4$.

On a 14.4 kV system with a Delta connection and a VT primary to secondary turns ratio of 14400:120, the voltage value entered would be 120, i.e. 14400 / 120.

PATH: SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ POWER SYSTEM



The power system **NOMINAL FREQUENCY** value is used as a default to set the digital sampling rate if the system frequency cannot be measured from available signals. This may happen if the signals are not present or are heavily distorted. Before reverting to the nominal frequency, the frequency tracking algorithm holds the last valid frequency measurement for a safe period of time while waiting for the signals to reappear or for the distortions to decay.

The phase sequence of the power system is required to properly calculate sequence components and power parameters. The **PHASE ROTATION** setting matches the power system phase sequence. Note that this setting informs the relay of the actual system phase sequence, either ABC or ACB. CT and VT inputs on the relay, labeled as A, B, and C, must be connected to system phases A, B, and C for correct operation.

The **FREQUENCY AND PHASE REFERENCE** setting determines which signal source is used (and hence which AC signal) for phase angle reference. The AC signal used is prioritized based on the AC inputs that are configured for the signal source: phase voltages takes precedence, followed by auxiliary voltage, then phase currents, and finally ground current.

For three phase selection, phase A is used for angle referencing ($V_{\text{ANGLE REF}} = V_A$), while Clarke transformation of the phase signals is used for frequency metering and tracking ($V_{\text{FREQUENCY}} = (2V_A - V_B - V_C)/3$) for better performance during fault, open pole, and VT and CT fail conditions.

The phase reference and frequency tracking AC signals are selected based upon the Source configuration, regardless of whether or not a particular signal is actually applied to the relay.

Phase angle of the reference signal will always display zero degrees and all other phase angles will be relative to this signal. If the pre-selected reference signal is not measurable at a given time, the phase angles are not referenced.

The phase angle referencing is done via a phase locked loop, which can synchronize independent UR-series relays if they have the same AC signal reference. These results in very precise correlation of time tagging in the event recorder between different UR-series relays provided the relays have an IRIG-B connection.

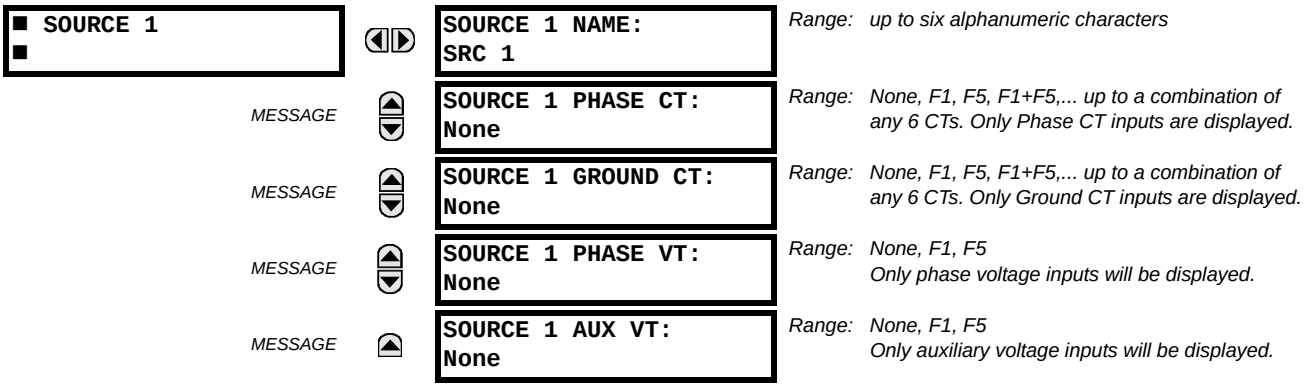
NOTE

FREQUENCY TRACKING should only be set to "Disabled" in very unusual circumstances; consult the factory for special variable-frequency applications.

NOTE

When voltage is supplied to the relay through a VT, it is advisable to assign a source configured with a phase VT voltage (source 3 or 4) to track system frequency from voltage. Source 1 should be assigned to track frequency from current.

PATH: SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES ⇨ SOURCE 1(2)



Two identical source menus are available. The "SRC 1" text can be replaced by with a user-defined name appropriate for the associated source.

“F” represents the module slot position. The number directly following this letter represents either the first bank of four channels (1, 2, 3, 4) called “1” or the second bank of four channels (5, 6, 7, 8) called “5” in a particular CT/VT module. Refer to the *Introduction to AC Sources* section at the beginning of this chapter for additional details on this concept.

It is possible to select the sum of up to six (6) CTs. The first channel displayed is the CT to which all others will be referred. For example, the selection “F1+F5” indicates the sum of each phase from channels “F1” and “F5”, scaled to whichever CT has the higher ratio. Selecting “None” hides the associated actual values.

The approach used to configure the AC sources consists of several steps; first step is to specify the information about each CT and VT input. For CT inputs, this is the nominal primary and secondary current. For VTs, this is the connection type, ratio and nominal secondary voltage. Once the inputs have been specified, the configuration for each source is entered, including specifying which CTs will be summed together.

Table 5–6: SOURCE CONFIGURATION FOR PHASE COMPARISON

FUNCTION	CT/VT MODULE 1 (TYPE 8P)		CT/VT MODULE 2 (TYPE 8F)	
	SRC 1	SRC 2	SRC 3	SRC 4
Phase current	F1 to F3 CT channels (used for 87PC first current and Breaker Failure 1)	Not available	L1 to L3 CT channels (used for 87PC second current and Breaker Failure 2). This source is configurable only if a second CT/VT module is ordered.	Sum of F1:F3 and L1:L3 (used for distance and overcurrent)
Ground current	F1 (Ground overcurrent)	Not available	---	---
Phase voltage	Not available	Not available	---	Three-phase line VT for distance and synchrocheck
Auxiliary voltage	Not available	Not available	Single-phase bus VT for synchrocheck	---

NOTE When two CTs are connected and configured with these settings, it is imperative that the CT rated secondary current is identical for both CTs (that is, both CTs are 1 A rated or both CTs are 5 A rated).

User selection of AC parameters for comparator elements:

CT/VT modules automatically calculate all current and voltage parameters from the available inputs. Users must select the specific input parameters to be measured by every element in the relevant settings menu. The internal design of the element specifies which type of parameter to use and provides a setting for source selection. In elements where the parameter may be either fundamental or RMS magnitude, such as phase time overcurrent, two settings are provided. One setting specifies the source, the second setting selects between fundamental phasor and RMS.

AC input actual values:

The calculated parameters associated with the configured voltage and current inputs are displayed in the current and voltage sections of actual values. Only the phasor quantities associated with the actual AC physical input channels will be displayed here. All parameters contained within a configured source are displayed in the sources section of the actual values.

DISTURBANCE DETECTORS (INTERNAL):

The 50DD element is a sensitive current disturbance detector that detects any disturbance on the protected system. 50DD is intended for use in conjunction with measuring elements, blocking of current based elements (to prevent maloperation as a result of the wrong settings), and starting oscillography data capture. A disturbance detector is provided for each source.

The 50DD function responds to the changes in magnitude of the sequence currents. The disturbance detector scheme logic is as follows:

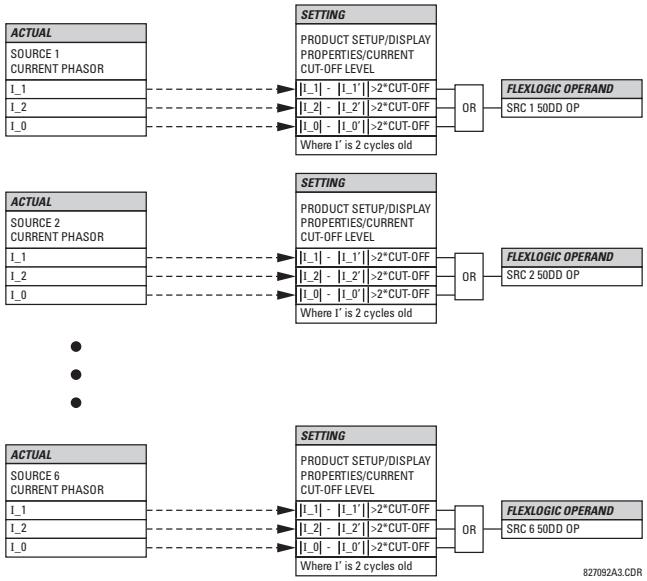
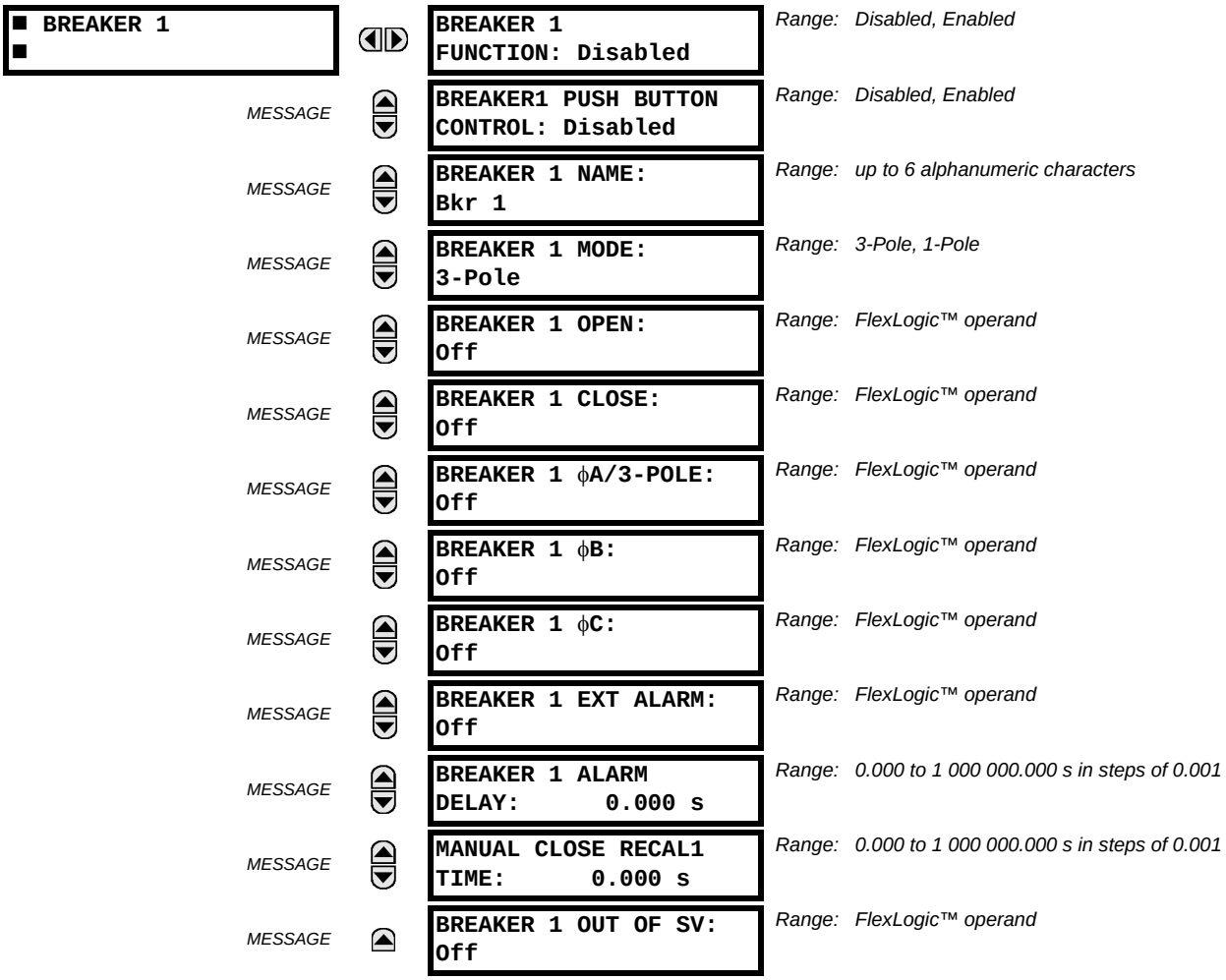


Figure 5–15: DISTURBANCE DETECTOR LOGIC DIAGRAM

The disturbance detector responds to the change in currents of twice the current cut-off level. The default cut-off threshold is 0.02 pu; thus by default the disturbance detector responds to a change of 0.04 pu. The metering sensitivity setting (**PRODUCT SETUP ⇨⇩ DISPLAY PROPERTIES ⇨⇩ CURRENT CUT-OFF LEVEL**) controls the sensitivity of the disturbance detector accordingly.

PATH: SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ BREAKERS ⇨ BREAKER 1(2)



A description of the operation of the breaker control and status monitoring features is provided in chapter 4. Only information concerning programming of the associated settings is covered here. These features are provided for two breakers; a user may use only those portions of the design relevant to a single breaker, which must be breaker 1.

- **BREAKER 1(2) FUNCTION:** Set to "Enable" to allow the operation of any breaker control feature.
- **BREAKER1(2) PUSH BUTTON CONTROL:** Set to "Enable" to allow faceplate push button operations.
- **BREAKER 1(2) NAME:** Assign a user-defined name (up to six characters) to the breaker. This name will be used in flash messages related to breaker 1.
- **BREAKER 1(2) MODE:** Selects "3-pole" mode, where all breaker poles are operated simultaneously, or "1-pole" mode where all breaker poles are operated either independently or simultaneously.
- **BREAKER 1(2) OPEN:** Selects an operand that creates a programmable signal to operate an output relay to open Breaker No. 1.
- **BREAKER 1(2) CLOSE:** Selects an operand that creates a programmable signal to operate an output relay to close Breaker No. 1.
- **BREAKER 1(2) ΦA/3-POLE:** Selects an operand, usually a contact input connected to a breaker auxiliary position tracking mechanism. This input can be either a 52/a or 52/b contact, or a combination the 52/a and 52/b contacts, that must be programmed to create a logic 0 when the breaker is open. If **BREAKER 1 MODE** is selected as "3-Pole", this setting selects a single input as the operand used to track the breaker open or closed position. If the mode is selected as

"1-Pole", the input mentioned above is used to track phase A and settings **BREAKER 1 ΦB** and **BREAKER 1 ΦC** select operands to track phases B and C, respectively.

- **BREAKER 1(2) FB:** If the mode is selected as 3-pole, this setting has no function. If the mode is selected as 1-pole, this input is used to track phase B as above for phase A.
- **BREAKER 1(2) FC:** If the mode is selected as 3-pole, this setting has no function. If the mode is selected as 1-pole, this input is used to track phase C as above for phase A.
- **BREAKER 1(2) EXT ALARM:** Selects an operand, usually an external contact input, connected to a breaker alarm reporting contact.
- **BREAKER 1(2) ALARM DELAY:** Sets the delay interval during which a disagreement of status among the three pole position tracking operands will not declare a pole disagreement, to allow for non-simultaneous operation of the poles.
- **MANUAL CLOSE RECAL1 TIME:** Sets the interval required to maintain setting changes in effect after an operator has initiated a manual close command to operate a circuit breaker.
- **BREAKER 1(2) OUT OF SV:** Selects an operand indicating that breaker 1(2) is out-of-service.

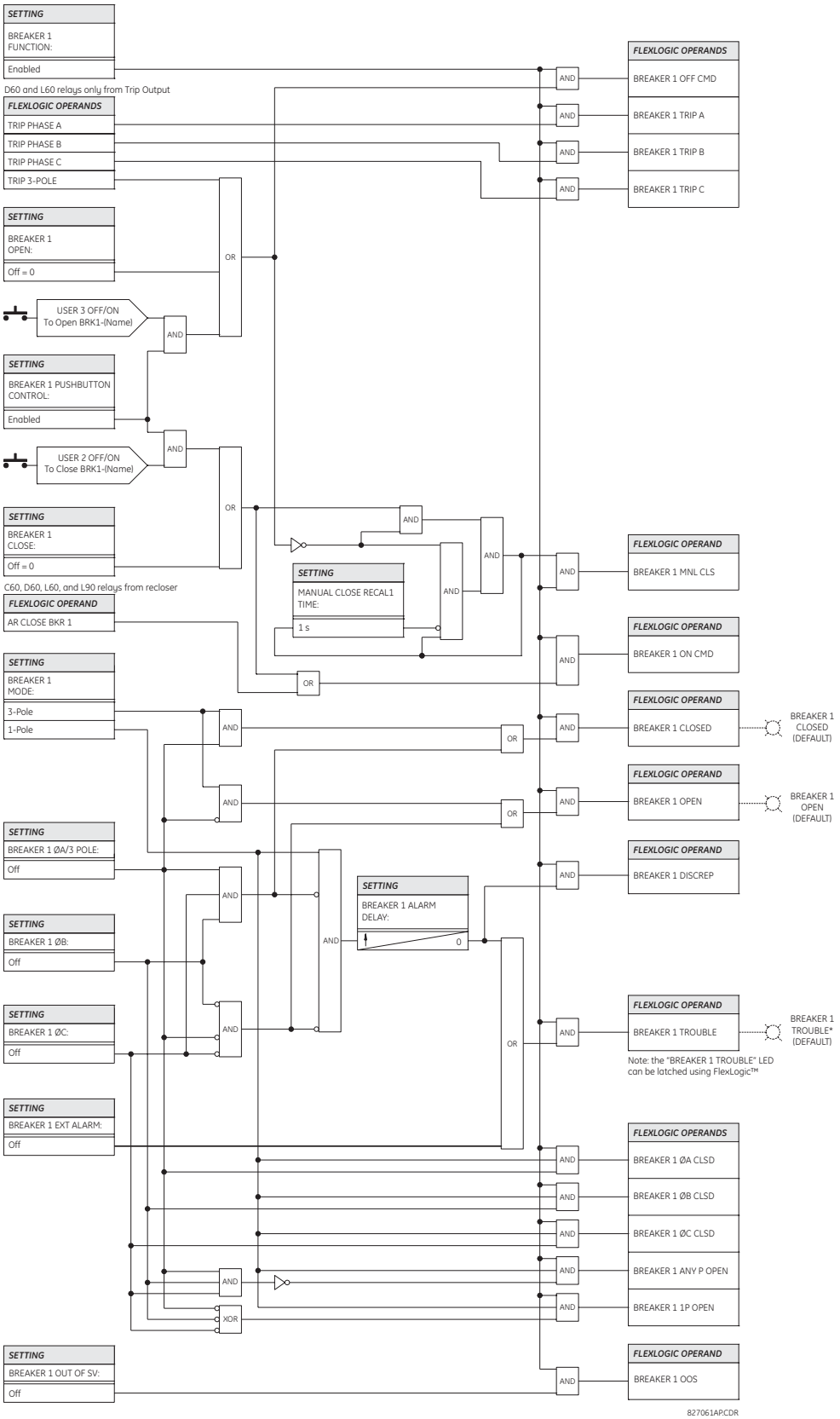


Figure 5–16: DUAL BREAKER CONTROL SCHEME LOGIC

a) SETTINGS

PATH: SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ FLEXCURVES ⇨ FLEXCURVE A(D)

Range: 0 to 65535 ms in steps of 1

FlexCurves™ A through D have settings for entering times to reset/operate at the following pickup levels: 0.00 to 0.98 and 1.03 to 20.00. This data is converted into two continuous curves by linear interpolation between data points. To enter a custom FlexCurve™, enter the reset/operate time (using the VALUE keys) for each selected pickup point (using the MESSAGE UP/DOWN keys) for the desired protection curve (A, B, C, or D).

Table 5–7: FLEXCURVE™ TABLE

RESET	TIME MS	RESET	TIME MS	OPERATE	TIME MS	OPERATE	TIME MS	OPERATE	TIME MS	OPERATE	TIME MS
0.00		0.68		1.03		2.9		4.9		10.5	
0.05		0.70		1.05		3.0		5.0		11.0	
0.10		0.72		1.1		3.1		5.1		11.5	
0.15		0.74		1.2		3.2		5.2		12.0	
0.20		0.76		1.3		3.3		5.3		12.5	
0.25		0.78		1.4		3.4		5.4		13.0	
0.30		0.80		1.5		3.5		5.5		13.5	
0.35		0.82		1.6		3.6		5.6		14.0	
0.40		0.84		1.7		3.7		5.7		14.5	
0.45		0.86		1.8		3.8		5.8		15.0	
0.48		0.88		1.9		3.9		5.9		15.5	
0.50		0.90		2.0		4.0		6.0		16.0	
0.52		0.91		2.1		4.1		6.5		16.5	
0.54		0.92		2.2		4.2		7.0		17.0	
0.56		0.93		2.3		4.3		7.5		17.5	
0.58		0.94		2.4		4.4		8.0		18.0	
0.60		0.95		2.5		4.5		8.5		18.5	
0.62		0.96		2.6		4.6		9.0		19.0	
0.64		0.97		2.7		4.7		9.5		19.5	
0.66		0.98		2.8		4.8		10.0		20.0	

NOTE

The relay using a given FlexCurve™ applies linear approximation for times between the user-entered points. Special care must be applied when setting the two points that are close to the multiple of pickup of 1; that is, 0.98 pu and 1.03 pu. It is recommended to set the two times to a similar value; otherwise, the linear approximation may result in undesired behavior for the operating quantity that is close to 1.00 pu.

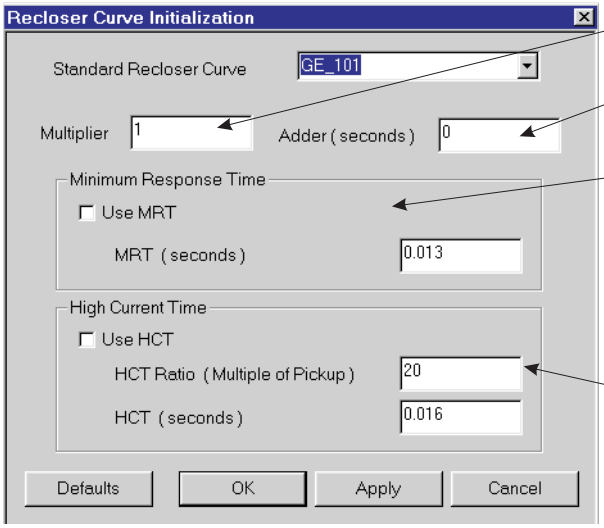
b) FLEXCURVE™ CONFIGURATION WITH ENERVISTA UR SETUP

The EnerVista UR Setup software allows for easy configuration and management of FlexCurves™ and their associated data points. Prospective FlexCurves™ can be configured from a selection of standard curves to provide the best approximate fit, then specific data points can be edited afterwards. Alternately, curve data can be imported from a specified file (.csv format) by selecting the **Import Data From** EnerVista UR Setup setting.

Curves and data can be exported, viewed, and cleared by clicking the appropriate buttons. FlexCurves™ are customized by editing the operating time (ms) values at pre-defined per-unit current multiples. Note that the pickup multiples start at zero (implying the "reset time"), operating time below pickup, and operating time above pickup.

c) RECLOSER CURVE EDITING

Recloser curve selection is special in that recloser curves can be shaped into a composite curve with a minimum response time and a fixed time above a specified pickup multiples. There are 41 recloser curve types supported. These definite operating times are useful to coordinate operating times, typically at higher currents and where upstream and downstream protective devices have different operating characteristics. The recloser curve configuration window shown below appears when the Initialize From EnerVista UR Setup setting is set to “Recloser Curve” and the **Initialize FlexCurve** button is clicked.



Multiplier: Scales (multiplies) the curve operating times

Addr: Adds the time specified in this field (in ms) to each *curve* operating time value.

Minimum Response Time (MRT): If enabled, the MRT setting defines the shortest operating time even if the curve suggests a shorter time at higher current multiples. A composite operating characteristic is effectively defined. For current multiples lower than the intersection point, the curve dictates the operating time; otherwise, the MRT does. An information message appears when attempting to apply an MRT shorter than the minimum curve time.

High Current Time: Allows the user to set a pickup multiple from which point onwards the operating time is fixed. This is normally only required at higher current levels. The **HCT Ratio** defines the high current pickup multiple; the **HCT** defines the operating time.

842721A1.CDR

Figure 5–17: RECLOSER CURVE INITIALIZATION

NOTE

The multiplier and adder settings only affect the curve portion of the characteristic and not the MRT and HCT settings. The HCT settings override the MRT settings for multiples of pickup greater than the HCT ratio.

d) EXAMPLE

A composite curve can be created from the GE_111 standard with MRT = 200 ms and HCT initially disabled and then enabled at eight (8) times pickup with an operating time of 30 ms. At approximately four (4) times pickup, the curve operating time is equal to the MRT and from then onwards the operating time remains at 200 ms (see below).

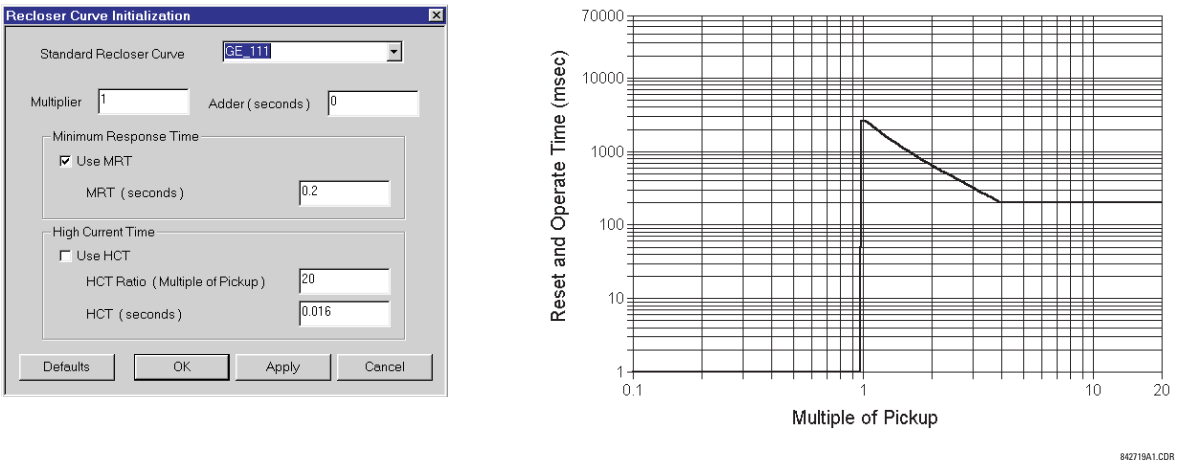


Figure 5–18: COMPOSITE RECLOSER CURVE WITH HCT DISABLED

With the HCT feature enabled, the operating time reduces to 30 ms for pickup multiples exceeding 8 times pickup.

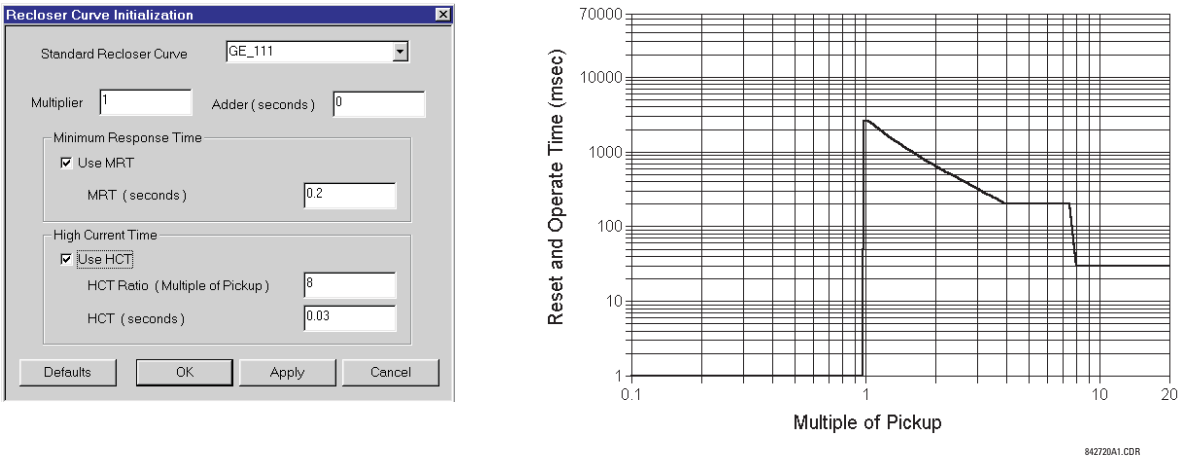


Figure 5–19: COMPOSITE RECLOSER CURVE WITH HCT ENABLED

NOTE

Configuring a composite curve with an increase in operating time at increased pickup multiples is not allowed. If this is attempted, the EnerVista UR Setup software generates an error message and discards the proposed changes.

e) STANDARD RECLOSER CURVES

The standard recloser curves available for the L60 are displayed in the following graphs.

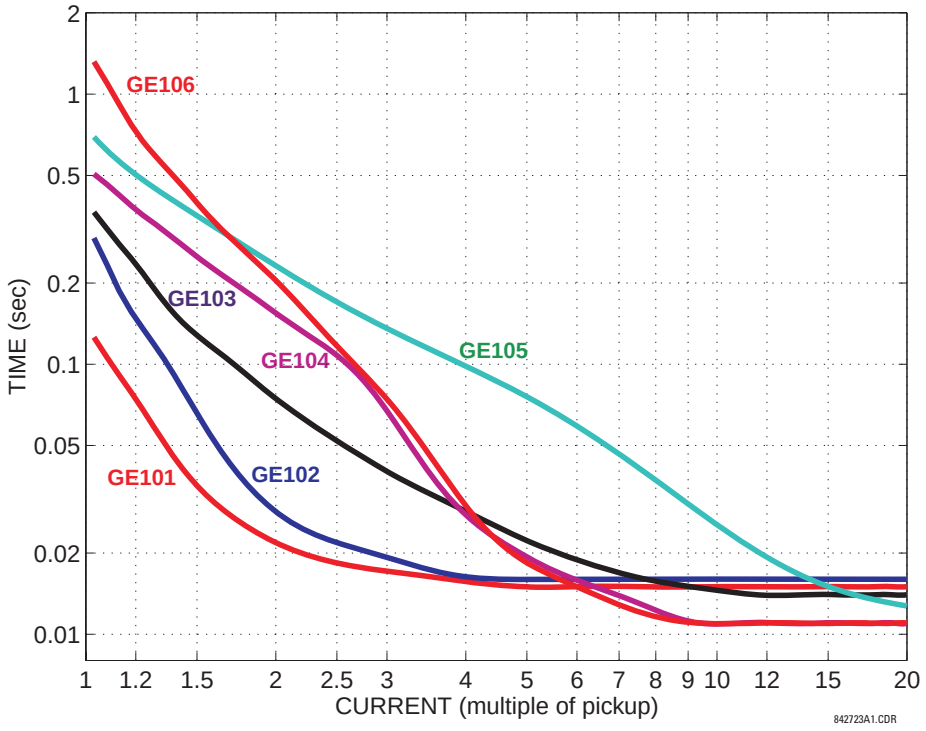


Figure 5–20: RECLOSER CURVES GE101 TO GE106

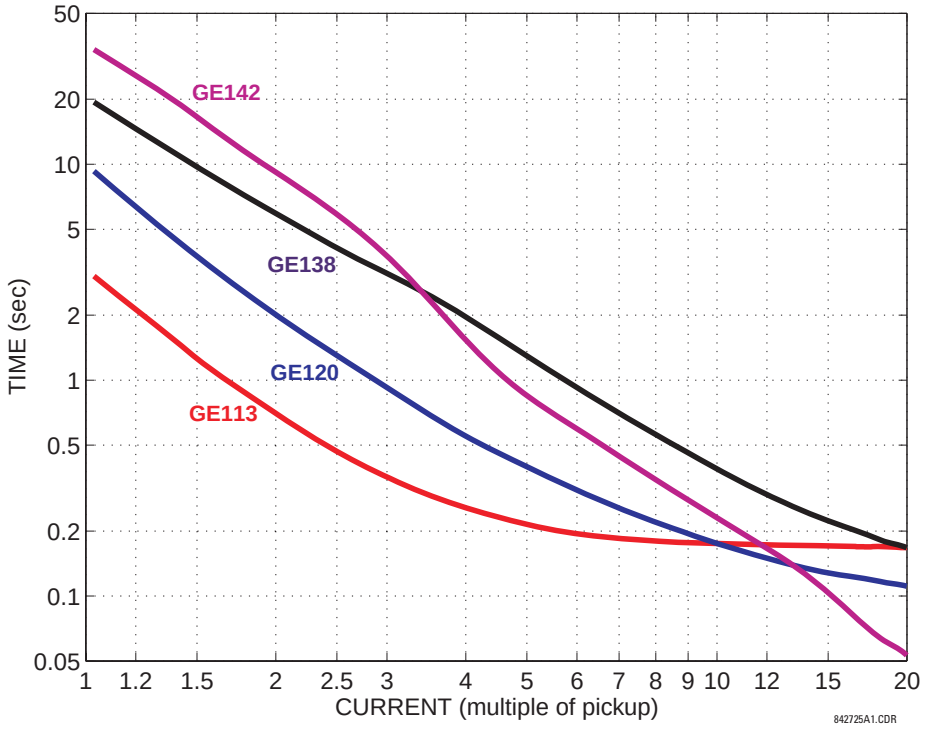


Figure 5–21: RECLOSER CURVES GE113, GE120, GE138 AND GE142

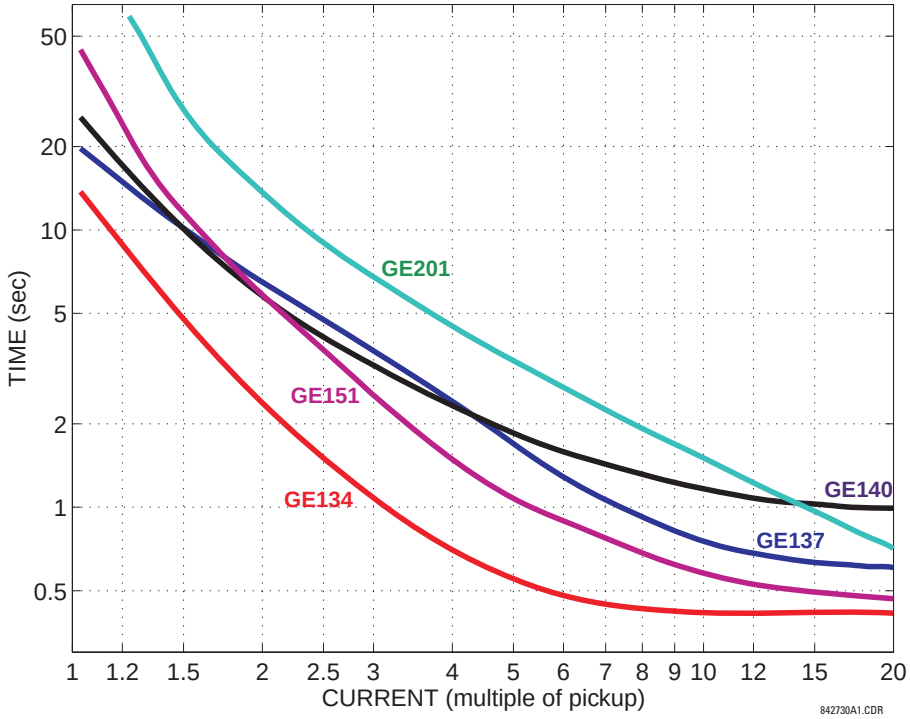


Figure 5–22: RECLOSER CURVES GE134, GE137, GE140, GE151 AND GE201

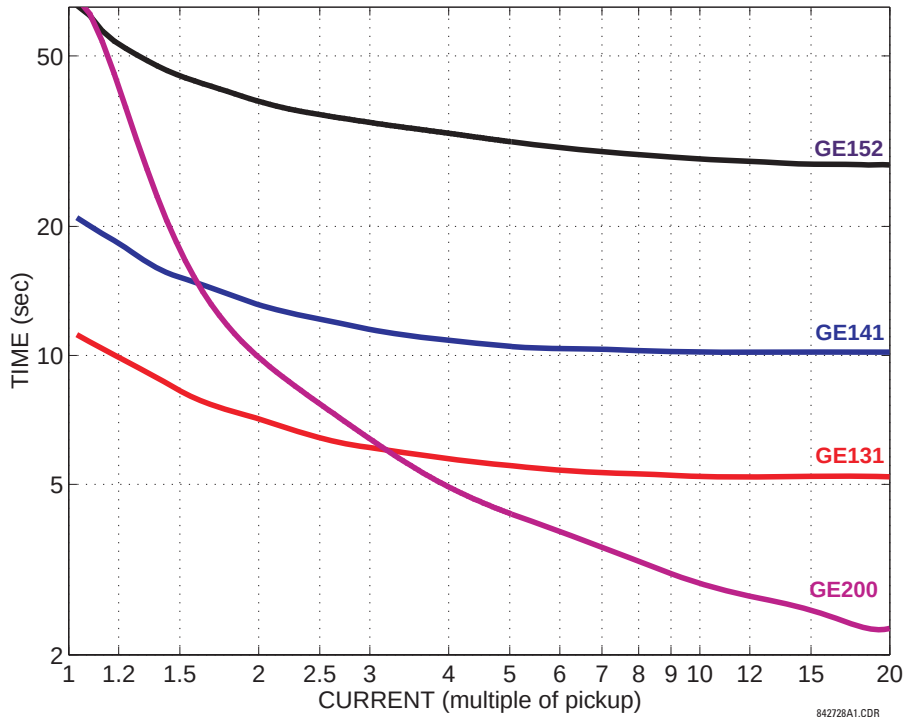


Figure 5–23: RECLOSER CURVES GE131, GE141, GE152, AND GE200

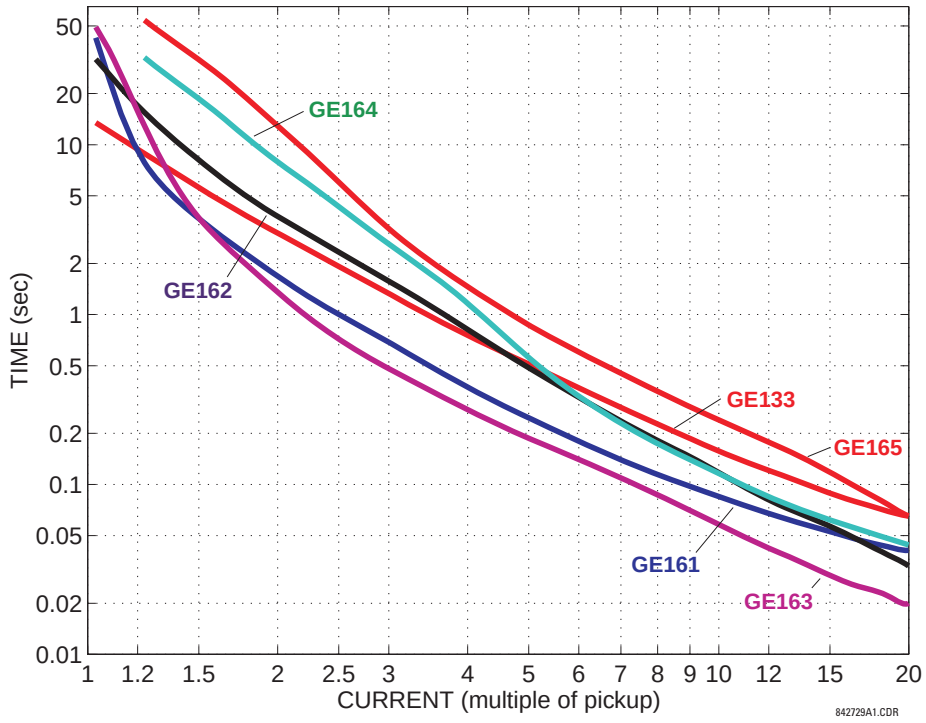


Figure 5–24: RECLOSER CURVES GE133, GE161, GE162, GE163, GE164 AND GE165

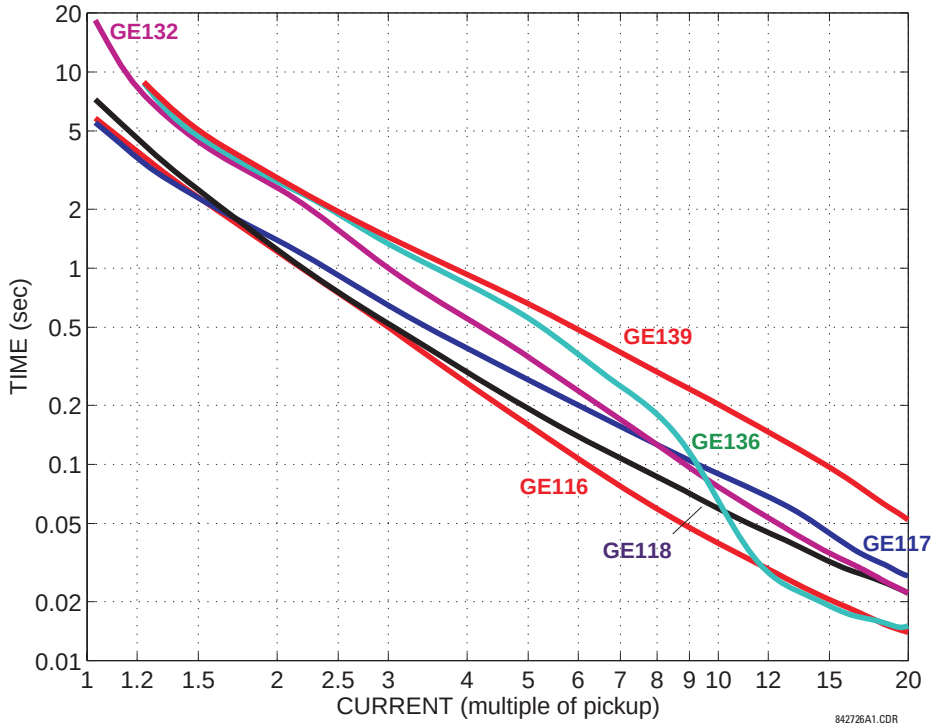


Figure 5–25: RECLOSER CURVES GE116, GE117, GE118, GE132, GE136, AND GE139

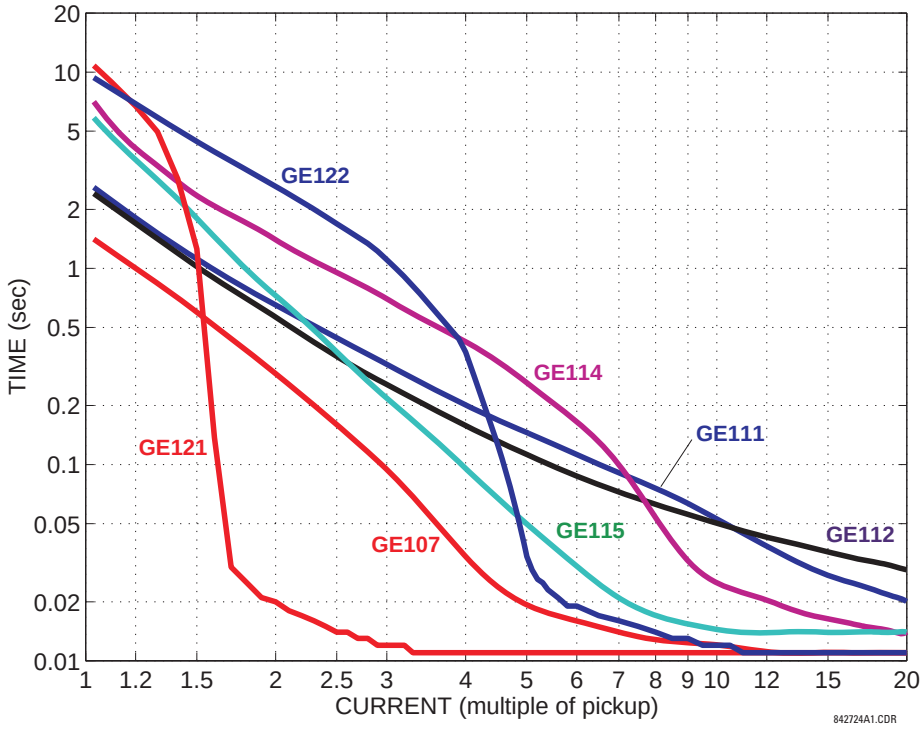


Figure 5–26: RECLOSER CURVES GE107, GE111, GE112, GE114, GE115, GE121, AND GE122

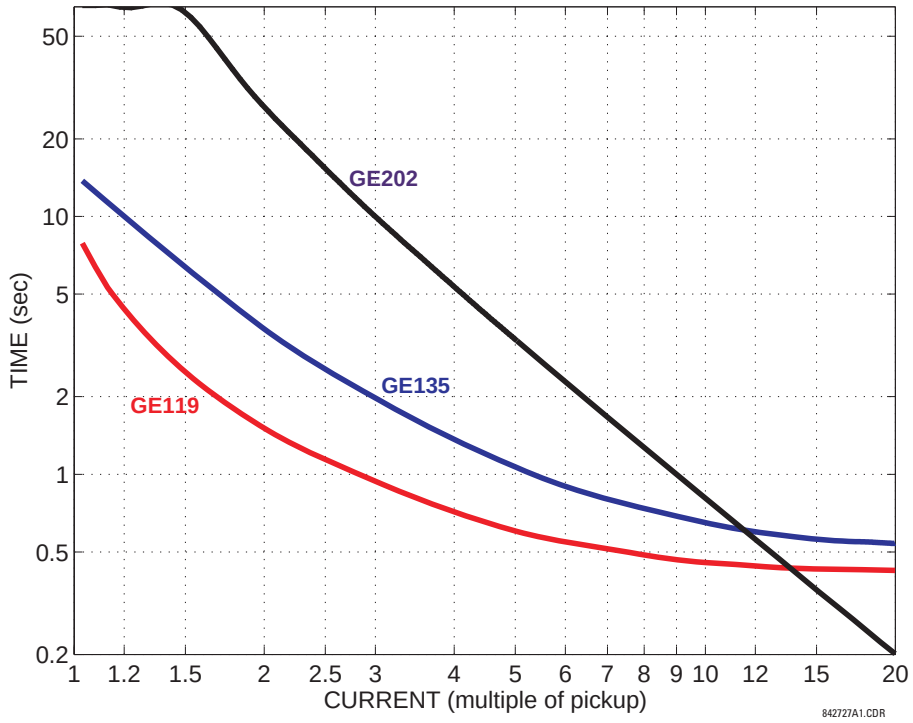


Figure 5–27: RECLOSER CURVES GE119, GE135, AND GE202

To provide maximum flexibility to the user, the arrangement of internal digital logic combines fixed and user-programmed parameters. Logic upon which individual features are designed is fixed, and all other logic, from digital input signals through elements or combinations of elements to digital outputs, is variable. The user has complete control of all variable logic through FlexLogic™. In general, the system receives analog and digital inputs which it uses to produce analog and digital outputs. The major sub-systems of a generic UR-series relay involved in this process are shown below.

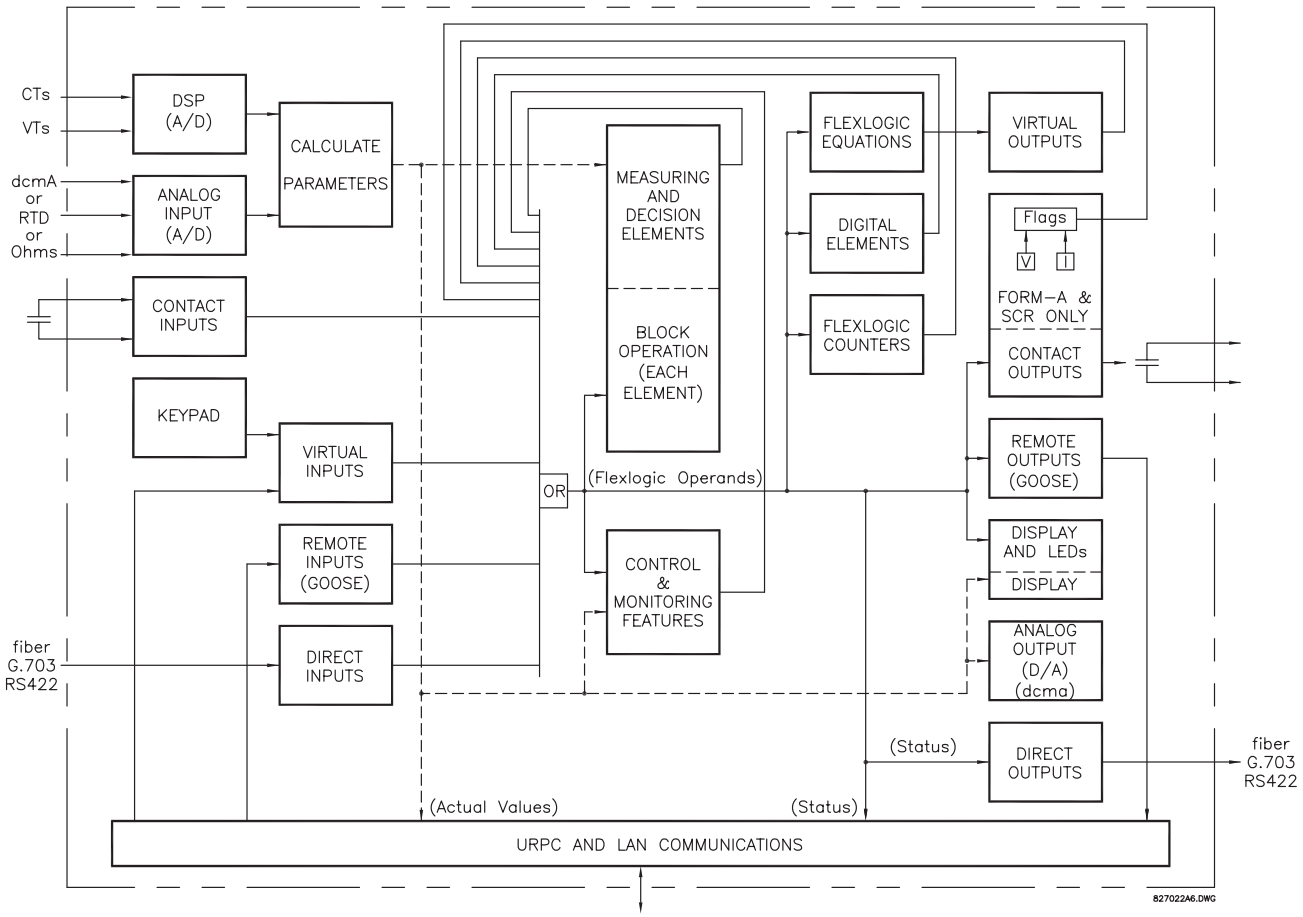


Figure 5–28: UR ARCHITECTURE OVERVIEW

The states of all digital signals used in the L60 are represented by flags (or FlexLogic™ operands, which are described later in this section). A digital “1” is represented by a 'set' flag. Any external contact change-of-state can be used to block an element from operating, as an input to a control feature in a FlexLogic™ equation, or to operate a contact output. The state of the contact input can be displayed locally or viewed remotely via the communications facilities provided. If a simple scheme where a contact input is used to block an element is desired, this selection is made when programming the element. This capability also applies to the other features that set flags: elements, virtual inputs, remote inputs, schemes, and human operators.

If more complex logic than presented above is required, it is implemented via FlexLogic™. For example, if it is desired to have the closed state of contact input H7a and the operated state of the phase undervoltage element block the operation of the phase time overcurrent element, the two control input states are programmed in a FlexLogic™ equation. This equation ANDs the two control inputs to produce a ‘virtual output’ which is then selected when programming the phase time overcurrent to be used as a blocking input. Virtual outputs can only be created by FlexLogic™ equations.

Traditionally, protective relay logic has been relatively limited. Any unusual applications involving interlocks, blocking, or supervisory functions had to be hard-wired using contact inputs and outputs. FlexLogic™ minimizes the requirement for auxiliary components and wiring while making more complex schemes possible.

The logic that determines the interaction of inputs, elements, schemes and outputs is field programmable through the use of logic equations that are sequentially processed. The use of virtual inputs and outputs in addition to hardware is available internally and on the communication ports for other relays to use (distributed FlexLogic™).

FlexLogic™ allows users to customize the relay through a series of equations that consist of operators and operands. The operands are the states of inputs, elements, schemes and outputs. The operators are logic gates, timers and latches (with set and reset inputs). A system of sequential operations allows any combination of specified operands to be assigned as inputs to specified operators to create an output. The final output of an equation is a numbered register called a virtual output. Virtual outputs can be used as an input operand in any equation, including the equation that generates the output, as a seal-in or other type of feedback.

A FlexLogic™ equation consists of parameters that are either operands or operators. Operands have a logic state of 1 or 0. Operators provide a defined function, such as an AND gate or a Timer. Each equation defines the combinations of parameters to be used to set a Virtual Output flag. Evaluation of an equation results in either a 1 (=ON, i.e. flag set) or 0 (=OFF, i.e. flag not set). Each equation is evaluated at least 4 times every power system cycle.

Some types of operands are present in the relay in multiple instances; e.g. contact and remote inputs. These types of operands are grouped together (for presentation purposes only) on the faceplate display. The characteristics of the different types of operands are listed in the table below.

Table 5–8: L60 FLEXLOGIC™ OPERAND TYPES

OPERAND TYPE	STATE	EXAMPLE FORMAT	CHARACTERISTICS [INPUT IS '1' (= ON) IF...]
Contact Input	On	Cont Ip On	Voltage is presently applied to the input (external contact closed).
	Off	Cont Ip Off	Voltage is presently not applied to the input (external contact open).
Contact Output (type Form-A contact only)	Voltage On	Cont Op 1 VOn	Voltage exists across the contact.
	Voltage Off	Cont Op 1 VOff	Voltage does not exists across the contact.
	Current On	Cont Op 1 IOn	Current is flowing through the contact.
	Current Off	Cont Op 1 IOff	Current is not flowing through the contact.
Direct Input	On	DIRECT INPUT 1 On	The direct input is presently in the ON state.
Element (Analog)	Pickup	PHASE TOC1 PKP	The tested parameter is presently above the pickup setting of an element which responds to rising values or below the pickup setting of an element which responds to falling values.
	Dropout	PHASE TOC1 DPO	This operand is the logical inverse of the above PKP operand.
	Operate	PHASE TOC1 OP	The tested parameter has been above/below the pickup setting of the element for the programmed delay time, or has been at logic 1 and is now at logic 0 but the reset timer has not finished timing.
	Block	PHASE TOC1 BLK	The output of the comparator is set to the block function.
Element (Digital)	Pickup	Dig Element 1 PKP	The input operand is at logic 1.
	Dropout	Dig Element 1 DPO	This operand is the logical inverse of the above PKP operand.
	Operate	Dig Element 1 OP	The input operand has been at logic 1 for the programmed pickup delay time, or has been at logic 1 for this period and is now at logic 0 but the reset timer has not finished timing.
Element (Digital Counter)	Higher than	Counter 1 HI	The number of pulses counted is above the set number.
	Equal to	Counter 1 EQL	The number of pulses counted is equal to the set number.
	Lower than	Counter 1 LO	The number of pulses counted is below the set number.
Fixed	On	On	Logic 1
	Off	Off	Logic 0
Remote Input	On	REMOTE INPUT 1 On	The remote input is presently in the ON state.
Virtual Input	On	Virt Ip 1 On	The virtual input is presently in the ON state.
Virtual Output	On	Virt Op 1 On	The virtual output is presently in the set state (i.e. evaluation of the equation which produces this virtual output results in a "1").

The operands available for this relay are listed alphabetically by types in the following table.

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 1 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
CONTROL PUSHBUTTONS	CONTROL PUSHBTN 1 ON	Control pushbutton 1 is being pressed
	CONTROL PUSHBTN 2 ON	Control pushbutton 2 is being pressed
	CONTROL PUSHBTN 3 ON	Control pushbutton 3 is being pressed
	CONTROL PUSHBTN 4 ON	Control pushbutton 4 is being pressed
	CONTROL PUSHBTN 5 ON	Control pushbutton 5 is being pressed
	CONTROL PUSHBTN 6 ON	Control pushbutton 6 is being pressed
	CONTROL PUSHBTN 7 ON	Control pushbutton 7 is being pressed
DIRECT INPUT/ OUTPUT CHANNEL MONITORING	DIR IO CH1 CRC ALARM	The rate of direct input messages received on channel 1 and failing the CRC exceeded the user-specified level.
	DIR IO CH2 CRC ALARM	The rate of direct input messages received on channel 2 and failing the CRC exceeded the user-specified level.
	DIR IO CRC ALARM	The rate of direct input messages failing the CRC exceeded the user-specified level on channel 1 or 2.
	DIR IO CH1 UNRET ALM	The rate of returned direct input/output messages on channel 1 exceeded the user-specified level (ring configurations only).
	DIR IO CH2 UNRET ALM	The rate of returned direct input/output messages on channel 2 exceeded the user-specified level (ring configurations only).
	DIR IO UNRET ALM	The rate of returned direct input/output messages exceeded the user-specified level on channel 1 or 2 (ring configurations only).
ELEMENT: 50DD supervision	50DD SV	Disturbance detector has operated
ELEMENT: 87PC phase comparison	87PC PKP	Phase comparison has picked up
	87PC OP	Phase comparison has operated
	87PC DPO	Phase comparison has dropped out
	87PC TRANS BLOCK OP	Phase comparison transient blocking has operated
	87PC FDL OP	Overcurrent fault detector low has operated
	87PC FDH OP	Overcurrent fault detector high has operated
	87PC BKR ECHO PKP	Open breaker echo of phase comparison has picked up
	87PC V2 FDL OP	Advanced fault detector low, I2*Z - V2 has operated.
	87PC V2 FDH OP	Advanced fault detector high, I2*Z - V2 has operated.
	87PC dI2/dt FDL OP	Advanced fault detector low, rate of change of the negative-sequence current has operated.
	87PC dI2/dt FDH OP	Advanced fault detector high, rate of change of the negative -sequence current has operated.
	87PC dI1/dt FDL OP	Advanced fault detector low, rate of change of the positive-sequence current has operated.
	87PC dI1/dt FDH OP	Advanced fault detector high, rate of change of the positive-sequence current has operated.
ELEMENT: Autoreclose (1P/3P)	AR ENABLED	Autoreclosure is enabled and ready to perform
	AR DISABLED	Autoreclosure is disabled
	AR RIP	Autoreclosure is in “reclose-in-progress” state
	AR 1-P RIP	A single-pole reclosure is in progress
	AR 3-P/1 RIP	A three-pole reclosure is in progress, via dead time 1
	AR 3-P/2 RIP	A three-pole reclosure is in progress, via dead time 2
	AR 3-P/3 RIP	A three-pole reclosure is in progress, via dead time 3
	AR 3-P/4 RIP	A three-pole reclosure is in progress, via dead time 4
	AR LO	Autoreclosure is in lockout state
	AR BKR1 BLK	Reclosure of breaker 1 is blocked
	AR BKR2 BLK	Reclosure of breaker 2 is blocked
	AR CLOSE BKR1	Reclose breaker 1 signal
	AR CLOSE BKR2	Reclose breaker 2 signal
	AR FORCE 3-P TRIP	Force any trip to a three-phase trip
	AR SHOT CNT > 0	The first ‘CLOSE BKR X’ signal has been issued
	AR SHOT CNT = 1	Shot count is equal to 1
	AR SHOT CNT = 2	Shot count is equal to 2
	AR SHOT CNT = 3	Shot count is equal to 3
	AR SHOT CNT = 4	Shot count is equal to 4
	AR ZONE 1 EXTENT	The zone 1 distance function must be set to the extended overreach value
	AR INCOMPLETE SEQ	The incomplete sequence timer timed out
	AR RESET	Autoreclose has been reset either manually or by the reset timer
ELEMENT: Auxiliary overvoltage	AUX OV1 PKP	Auxiliary overvoltage element has picked up
	AUX OV1 DPO	Auxiliary overvoltage element has dropped out
	AUX OV1 OP	Auxiliary overvoltage element has operated
	AUX OV2 to AUX OV3	Same set of operands as shown for AUX OV1
ELEMENT: Auxiliary undervoltage	AUX UV1 PKP	Auxiliary undervoltage element has picked up
	AUX UV1 DPO	Auxiliary undervoltage element has dropped out
	AUX UV1 OP	Auxiliary undervoltage element has operated
	AUX UV2 to AUX UV3	Same set of operands as shown for AUX UV1

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 2 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT: Breaker arcing	BKR ARC 1 OP BKR ARC 2 OP	Breaker arcing current 1 has operated Breaker arcing current 2 has operated
ELEMENT Breaker failure	BKR FAIL 1 RETRIPA BKR FAIL 1 RETRIPB BKR FAIL 1 RETRIPC BKR FAIL 1 RETRIP BKR FAIL 1 T1 OP BKR FAIL 1 T2 OP BKR FAIL 1 T3 OP BKR FAIL 1 TRIP OP	Breaker failure 1 re-trip phase A (only for 1-pole schemes) Breaker failure 1 re-trip phase B (only for 1-pole schemes) Breaker failure 1 re-trip phase C (only for 1-pole schemes) Breaker failure 1 re-trip 3-phase Breaker failure 1 timer 1 is operated Breaker failure 1 timer 2 is operated Breaker failure 1 timer 3 is operated Breaker failure 1 trip is operated
	BKR FAIL 2	Same set of operands as shown for BKR FAIL 1
ELEMENT Breaker flashover	BKR 1 FLSHOVR PKP A BKR 1 FLSHOVR PKP B BKR 1 FLSHOVR PKP C BKR 1 FLSHOVR PKP BKR 1 FLSHOVR OP A BKR 1 FLSHOVR OP B BKR 1 FLSHOVR OP C BKR 1 FLSHOVR OP BKR 1 FLSHOVR DPO A BKR 1 FLSHOVR DPO B BKR 1 FLSHOVR DPO C BKR 1 FLSHOVR DPO	Breaker 1 flashover element phase A has picked up Breaker 1 flashover element phase B has picked up Breaker 1 flashover element phase C has picked up Breaker 1 flashover element has picked up Breaker 1 flashover element phase A has operated Breaker 1 flashover element phase B has operated Breaker 1 flashover element phase C has operated Breaker 1 flashover element has operated Breaker 1 flashover element phase A has dropped out Breaker 1 flashover element phase B has dropped out Breaker 1 flashover element phase C has dropped out Breaker 1 flashover element has dropped out
	BKR 2 FLSHOVR...	Same set of operands as shown for BKR 1 FLSHOVR
ELEMENT: Breaker control	BREAKER 1 OFF CMD BREAKER 1 ON CMD BREAKER 1 ϕA CLSD BREAKER 1 ϕB CLSD BREAKER 1 ϕC CLSD BREAKER 1 CLOSED BREAKER 1 OPEN BREAKER 1 DISCREP BREAKER 1 TROUBLE BREAKER 1 MNL CLS BREAKER 1 TRIP A BREAKER 1 TRIP B BREAKER 1 TRIP C BREAKER 1 ANY P OPEN BREAKER 1 ONE P OPEN BREAKER 1 OOS	Breaker 1 OFF command Breaker 1 ON command Breaker 1 phase A is closed Breaker 1 phase B is closed Breaker 1 phase C is closed Breaker 1 is closed Breaker 1 is open Breaker 1 has discrepancy Breaker 1 trouble alarm Breaker 1 manual close Breaker 1 trip phase A command Breaker 1 trip phase B command Breaker 1 trip phase C command At least one pole of breaker 1 is open Only one pole of breaker 1 is open Breaker 1 is out of service
	BREAKER 2	Same set of operands as shown for BREAKER 1
ELEMENT: CT fail	CT FAIL PKP CT FAIL OP	CT fail has picked up CT fail has dropped out
ELEMENT: Digital counters	Counter 1 HI Counter 1 EQL Counter 1 LO	Digital counter 1 output is ‘more than’ comparison value Digital counter 1 output is ‘equal to’ comparison value Digital counter 1 output is ‘less than’ comparison value
	Counter 2 to Counter 8	Same set of operands as shown for Counter 1
ELEMENT: Digital elements	Dig Element 1 PKP Dig Element 1 OP Dig Element 1 DPO	Digital Element 1 is picked up Digital Element 1 is operated Digital Element 1 is dropped out
	Dig Element 2 to Dig Element 48	Same set of operands as shown for Dig Element 1
ELEMENT: FlexElements™	FxE 1 PKP FxE 1 OP FxE 1 DPO	FlexElement™ 1 has picked up FlexElement™ 1 has operated FlexElement™ 1 has dropped out
	FxE 2 to FxE 8	Same set of operands as shown for FxE 1

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 3 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT: Ground distance	GND DIST Z1 PKP	Ground distance zone 1 has picked up
	GND DIST Z1 OP	Ground distance zone 1 has operated
	GND DIST Z1 OP A	Ground distance zone 1 phase A has operated
	GND DIST Z1 OP B	Ground distance zone 1 phase B has operated
	GND DIST Z1 OP C	Ground distance zone 1 phase C has operated
	GND DIST Z1 PKP A	Ground distance zone 1 phase A has picked up
	GND DIST Z1 PKP B	Ground distance zone 1 phase B has picked up
	GND DIST Z1 PKP C	Ground distance zone 1 phase C has picked up
	GND DIST Z1 SUPN IN	Ground distance zone 1 neutral is supervising
	GND DIST Z1 DPO A	Ground distance zone 1 phase A has dropped out
	GND DIST Z1 DPO B	Ground distance zone 1 phase B has dropped out
	GND DIST Z1 DPO C	Ground distance zone 1 phase C has dropped out
	GND DIST Z2 DIR SUPN	Ground distance zone 2 directional is supervising
	GND DIST Z2 to Z3	Same set of operands as shown for GND DIST Z1
ELEMENT: Ground instantaneous overcurrent	GROUND IOC1 PKP	Ground instantaneous overcurrent 1 has picked up
	GROUND IOC1 OP	Ground instantaneous overcurrent 1 has operated
	GROUND IOC1 DPO	Ground instantaneous overcurrent 1 has dropped out
	GROUND IOC2	Same set of operands as shown for GROUND IOC 1
ELEMENT: Ground time overcurrent	GROUND TOC1 PKP	Ground time overcurrent 1 has picked up
	GROUND TOC1 OP	Ground time overcurrent 1 has operated
	GROUND TOC1 DPO	Ground time overcurrent 1 has dropped out
	GROUND TOC2	Same set of operands as shown for GROUND TOC1
ELEMENT Non-volatile latches	LATCH 1 ON	Non-volatile latch 1 is ON (Logic = 1)
	LATCH 1 OFF	Non-voltage latch 1 is OFF (Logic = 0)
	LATCH 2 to LATCH 16	Same set of operands as shown for LATCH 1
ELEMENT: Line pickup	LINE PICKUP OP	Line pickup has operated
	LINE PICKUP PKP	Line pickup has picked up
	LINE PICKUP DPO	Line pickup has dropped out
	LINE PICKUP I<A	Line pickup detected phase A current below 5% of nominal
	LINE PICKUP I<B	Line pickup detected phase B current below 5% of nominal
	LINE PICKUP I<C	Line pickup detected phase C current below 5% of nominal
	LINE PICKUP UV PKP	Line pickup undervoltage has picked up
	LINE PICKUP LEO PKP	Line pickup line end open has picked up
	LINE PICKUP RCL TRIP	Line pickup operated from overreaching zone 2 when reclosing the line (zone 1 extension functionality)
ELEMENT: Load encroachment	LOAD ENCHR PKP	Load encroachment has picked up
	LOAD ENCHR OP	Load encroachment has operated
	LOAD ENCHR DPO	Load encroachment has dropped out
ELEMENT: Negative-sequence directional overcurrent	NEG SEQ DIR OC1 FWD	Negative-sequence directional overcurrent 1 forward has operated
	NEG SEQ DIR OC1 REV	Negative-sequence directional overcurrent 1 reverse has operated
	NEG SEQ DIR OC2 FWD	Negative-sequence directional overcurrent 1 forward has operated
	NEG SEQ DIR OC2 REV	Negative-sequence directional overcurrent 1 reverse has operated
ELEMENT: Negative-sequence instantaneous overcurrent	NEG SEQ IOC1 PKP	Negative-sequence instantaneous overcurrent 1 has picked up
	NEG SEQ IOC1 OP	Negative-sequence instantaneous overcurrent 1 has operated
	NEG SEQ IOC1 DPO	Negative-sequence instantaneous overcurrent 1 has dropped out
	NEG SEQ IOC2	Same set of operands as shown for NEG SEQ IOC1
ELEMENT: Negative-sequence overvoltage	NEG SEQ OV1 PKP	Negative-sequence overvoltage element has picked up
	NEG SEQ OV1 DPO	Negative-sequence overvoltage element has dropped out
	NEG SEQ OV1 OP	Negative-sequence overvoltage element has operated
	NEG SEQ OV2...	Same set of operands as shown for NEG SEQ OV1
ELEMENT: Negative-sequence time overcurrent	NEG SEQ TOC1 PKP	Negative-sequence time overcurrent 1 has picked up
	NEG SEQ TOC1 OP	Negative-sequence time overcurrent 1 has operated
	NEG SEQ TOC1 DPO	Negative-sequence time overcurrent 1 has dropped out
	NEG SEQ TOC2	Same set of operands as shown for NEG SEQ TOC1
ELEMENT: Neutral instantaneous overcurrent	NEUTRAL IOC1 PKP	Neutral instantaneous overcurrent 1 has picked up
	NEUTRAL IOC1 OP	Neutral instantaneous overcurrent 1 has operated
	NEUTRAL IOC1 DPO	Neutral instantaneous overcurrent 1 has dropped out
	NEUTRAL IOC2	Same set of operands as shown for NEUTRAL IOC1
ELEMENT: Neutral overvoltage	NEUTRAL OV1 PKP	Neutral overvoltage element 1 has picked up
	NEUTRAL OV1 DPO	Neutral overvoltage element 1 has dropped out
	NEUTRAL OV1 OP	Neutral overvoltage element 1 has operated

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 4 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT: Neutral time overcurrent	NEUTRAL TOC1 PKP	Neutral time overcurrent 1 has picked up
	NEUTRAL TOC1 OP	Neutral time overcurrent 1 has operated
	NEUTRAL TOC1 DPO	Neutral time overcurrent 1 has dropped out
	NEUTRAL TOC2	Same set of operands as shown for NEUTRAL TOC1
ELEMENT: Neutral directional overcurrent	NTRL DIR OC1 FWD	Neutral directional overcurrent 1 forward has operated
	NTRL DIR OC1 REV	Neutral directional overcurrent 1 reverse has operated
ELEMENT: Open pole detector	OPEN POLE OP ΦA	Open pole condition is detected in phase A
	OPEN POLE OP ΦB	Open pole condition is detected in phase B
	OPEN POLE OP ΦC	Open pole condition is detected in phase C
	OPEN POLE BKR ΦA OP	Based on the breaker(s) auxiliary contacts, an open pole condition is detected on phase A
	OPEN POLE BKR ΦB OP	Based on the breaker(s) auxiliary contacts, an open pole condition is detected on phase B
	OPEN POLE BKR ΦC OP	Based on the breaker(s) auxiliary contacts, an open pole condition is detected on phase C
	OPEN POLE BLK N	Blocking signal for neutral, ground, and negative-sequence overcurrent element is established
	OPEN POLE BLK AB	Blocking signal for the AB phase distance elements is established
	OPEN POLE BLK BC	Blocking signal for the BC phase distance elements is established
	OPEN POLE BLK CA	Blocking signal for the CA phase distance elements is established
	OPEN POLE REM OP ΦA	Remote open pole condition detected in phase A
	OPEN POLE REM OP ΦB	Remote open pole condition detected in phase B
	OPEN POLE REM OP ΦC	Remote open pole condition detected in phase C
	OPEN POLE OP	Open pole detector is operated
ELEMENT: Phase directional overcurrent	PH DIR1 BLK A	Phase A directional 1 block
	PH DIR1 BLK B	Phase B directional 1 block
	PH DIR1 BLK C	Phase C directional 1 block
	PH DIR1 BLK	Phase directional 1 block
	PH DIR2	Same set of operands as shown for PH DIR1
ELEMENT: Phase distance	PH DIST Z1 PKP	Phase distance zone 1 has picked up
	PH DIST Z1 OP	Phase distance zone 1 has operated
	PH DIST Z1 OP AB	Phase distance zone 1 phase AB has operated
	PH DIST Z1 OP BC	Phase distance zone 1 phase BC has operated
	PH DIST Z1 OP CA	Phase distance zone 1 phase CA has operated
	PH DIST Z1 PKP AB	Phase distance zone 1 phase AB has picked up
	PH DIST Z1 PKP BC	Phase distance zone 1 phase BC has picked up
	PH DIST Z1 PKP CA	Phase distance zone 1 phase CA has picked up
	PH DIST Z1 SUPN IAB	Phase distance zone 1 phase AB IOC is supervising
	PH DIST Z1 SUPN IBC	Phase distance zone 1 phase BC IOC is supervising
	PH DIST Z1 SUPN ICA	Phase distance zone 1 phase CA IOC is supervising
	PH DIST Z1 DPO AB	Phase distance zone 1 phase AB has dropped out
	PH DIST Z1 DPO BC	Phase distance zone 1 phase BC has dropped out
	PH DIST Z1 DPO CA	Phase distance zone 1 phase CA has dropped out
	PH DIST Z2 to Z3	Same set of operands as shown for PH DIST Z1
ELEMENT: Phase instantaneous overcurrent	PHASE IOC1 PKP	At least one phase of phase instantaneous overcurrent 1 has picked up
	PHASE IOC1 OP	At least one phase of phase instantaneous overcurrent 1 has operated
	PHASE IOC1 DPO	At least one phase of phase instantaneous overcurrent 1 has dropped out
	PHASE IOC1 PKP A	Phase A of phase instantaneous overcurrent 1 has picked up
	PHASE IOC1 PKP B	Phase B of phase instantaneous overcurrent 1 has picked up
	PHASE IOC1 PKP C	Phase C of phase instantaneous overcurrent 1 has picked up
	PHASE IOC1 OP A	Phase A of phase instantaneous overcurrent 1 has operated
	PHASE IOC1 OP B	Phase B of phase instantaneous overcurrent 1 has operated
	PHASE IOC1 OP C	Phase C of phase instantaneous overcurrent 1 has operated
	PHASE IOC1 DPO A	Phase A of phase instantaneous overcurrent 1 has dropped out
	PHASE IOC1 DPO B	Phase B of phase instantaneous overcurrent 1 has dropped out
	PHASE IOC1 DPO C	Phase C of phase instantaneous overcurrent 1 has dropped out
	PHASE IOC2	Same set of operands as shown for PHASE IOC1
ELEMENT: Phase overvoltage	PHASE OV1 PKP	At least one phase of overvoltage 1 has picked up
	PHASE OV1 OP	At least one phase of overvoltage 1 has operated
	PHASE OV1 DPO	At least one phase of overvoltage 1 has dropped out
	PHASE OV1 PKP A	Phase A of overvoltage 1 has picked up
	PHASE OV1 PKP B	Phase B of overvoltage 1 has picked up
	PHASE OV1 PKP C	Phase C of overvoltage 1 has picked up
	PHASE OV1 OP A	Phase A of overvoltage 1 has operated
	PHASE OV1 OP B	Phase B of overvoltage 1 has operated
	PHASE OV1 OP C	Phase C of overvoltage 1 has operated
	PHASE OV1 DPO A	Phase A of overvoltage 1 has dropped out
	PHASE OV1 DPO B	Phase B of overvoltage 1 has dropped out
	PHASE OV1 DPO C	Phase C of overvoltage 1 has dropped out

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 5 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT Phase select	PHASE SELECT AG PHASE SELECT BG PHASE SELECT CG PHASE SELECT SLG PHASE SELECT AB PHASE SELECT BC PHASE SELECT CA PHASE SELECT ABG PHASE SELECT BCG PHASE SELECT CAG PHASE SELECT 3P PHASE SELECT MULTI-P PHASE SELECT VOID	Phase A to ground fault is detected. Phase B to ground fault is detected. Phase C to ground fault is detected. Single line to ground fault is detected. Phase A to B fault is detected. Phase B to C fault is detected. Phase C to A fault is detected. Phase A to B to ground fault is detected. Phase B to C to ground fault is detected. Phase C to A to ground fault is detected. Three-phase symmetrical fault is detected. Multi-phase fault is detected Fault type cannot be detected
ELEMENT: Phase time overcurrent	PHASE TOC1 PKP PHASE TOC1 OP PHASE TOC1 DPO PHASE TOC1 PKP A PHASE TOC1 PKP B PHASE TOC1 PKP C PHASE TOC1 OP A PHASE TOC1 OP B PHASE TOC1 OP C PHASE TOC1 DPO A PHASE TOC1 DPO B PHASE TOC1 DPO C	At least one phase of phase time overcurrent 1 has picked up At least one phase of phase time overcurrent 1 has operated At least one phase of phase time overcurrent 1 has dropped out Phase A of phase time overcurrent 1 has picked up Phase B of phase time overcurrent 1 has picked up Phase C of phase time overcurrent 1 has picked up Phase A of phase time overcurrent 1 has operated Phase B of phase time overcurrent 1 has operated Phase C of phase time overcurrent 1 has operated Phase A of phase time overcurrent 1 has dropped out Phase B of phase time overcurrent 1 has dropped out Phase C of phase time overcurrent 1 has dropped out
	PHASE TOC2	Same set of operands as shown for PHASE TOC1
ELEMENT: Phase undervoltage	PHASE UV1 PKP PHASE UV1 OP PHASE UV1 DPO PHASE UV1 PKP A PHASE UV1 PKP B PHASE UV1 PKP C PHASE UV1 OP A PHASE UV1 OP B PHASE UV1 OP C PHASE UV1 DPO A PHASE UV1 DPO B PHASE UV1 DPO C	At least one phase of phase undervoltage 1 has picked up At least one phase of phase undervoltage 1 has operated At least one phase of phase undervoltage 1 has dropped out Phase A of phase undervoltage 1 has picked up Phase B of phase undervoltage 1 has picked up Phase C of phase undervoltage 1 has picked up Phase A of phase undervoltage 1 has operated Phase B of phase undervoltage 1 has operated Phase C of phase undervoltage 1 has operated Phase A of phase undervoltage 1 has dropped out Phase B of phase undervoltage 1 has dropped out Phase C of phase undervoltage 1 has dropped out
	PHASE UV2	Same set of operands as shown for PHASE UV1
ELEMENT: POTT (Permissive overreach transfer trip)	POTT OP POTT TX	Permissive over-reaching transfer trip has operated Permissive signal sent
ELEMENT: Power swing detect	POWER SWING OUTER POWER SWING MIDDLE POWER SWING INNER POWER SWING BLOCK POWER SWING TMR1 PKP POWER SWING TMR2 PKP POWER SWING TMR3 PKP POWER SWING TMR4 PKP POWER SWING TRIP POWER SWING 50DD POWER SWING INCOMING POWER SWING OUTGOING POWER SWING UN/BLOCK	Positive-sequence impedance in outer characteristic Positive-sequence impedance in middle characteristic Positive-sequence impedance in inner characteristic Power swing blocking element operated Power swing timer 1 picked up Power swing timer 2 picked up Power swing timer 3 picked up Power swing timer 4 picked up Out-of-step tripping operated The power swing element detected a disturbance other than power swing An unstable power swing has been detected (incoming locus) An unstable power swing has been detected (outgoing locus) Asserted when a fault occurs after the power swing blocking condition has been established
ELEMENT: Selector switch	SELECTOR 1 POS Y SELECTOR 1 BIT 0 SELECTOR 1 BIT 1 SELECTOR 1 BIT 2 SELECTOR 1 STP ALARM SELECTOR 1 BIT ALARM SELECTOR 1 ALARM SELECTOR 1 PWR ALARM	Selector switch 1 is in Position Y (mutually exclusive operands) First bit of the 3-bit word encoding position of selector 1 Second bit of the 3-bit word encoding position of selector 1 Third bit of the 3-bit word encoding position of selector 1 Position of selector 1 has been pre-selected with the stepping up control input but not acknowledged Position of selector 1 has been pre-selected with the 3-bit control input but not acknowledged Position of selector 1 has been pre-selected but not acknowledged Position of selector switch 1 is undetermined or restored from memory when the relay powers up and synchronizes to the three-bit input
	SELECTOR 2	Same set of operands as shown above for SELECTOR 1

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 6 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT: Setting group	SETTING GROUP ACT 1 SETTING GROUP ACT 2 SETTING GROUP ACT 3 SETTING GROUP ACT 4 SETTING GROUP ACT 5 SETTING GROUP ACT 6	Setting group 1 is active Setting group 2 is active Setting group 3 is active Setting group 4 is active Setting group 5 is active Setting group 6 is active
ELEMENT: Disturbance detector	SRC1 50DD OP SRC2 50DD OP	Source 1 disturbance detector has operated Source 2 disturbance detector has operated
ELEMENT: VTFF (Voltage transformer fuse failure)	SRC1 VT FUSE FAIL OP SRC1 VT FUSE FAIL DPO SRC1 VT FUSE FAIL VOL LOSS	Source 1 VT fuse failure detector has operated Source 1 VT fuse failure detector has dropped out Source 1 has lost voltage signals (V2 below 15% AND V1 below 5% of nominal)
	SRC2 VT FUSE FAIL to SRC VT FUSE FAIL	Same set of operands as shown for SRC1 VT FUSE FAIL
ELEMENT: Synchrocheck	SYNC 1 DEAD S OP SYNC 1 DEAD S DPO SYNC 1 SYNC OP SYNC 1 SYNC DPO SYNC 1 CLS OP SYNC 1 CLS DPO SYNC 1 V1 ABOVE MIN SYNC 1 V1 BELOW MAX SYNC 1 V2 ABOVE MIN SYNC 1 V2 BELOW MAX	Synchrocheck 1 dead source has operated Synchrocheck 1 dead source has dropped out Synchrocheck 1 in synchronization has operated Synchrocheck 1 in synchronization has dropped out Synchrocheck 1 close has operated Synchrocheck 1 close has dropped out Synchrocheck 1 V1 is above the minimum live voltage Synchrocheck 1 V1 is below the maximum dead voltage Synchrocheck 1 V2 is above the minimum live voltage Synchrocheck 1 V2 is below the maximum dead voltage
	SYNC 2	Same set of operands as shown for SYNC 1
ELEMENT: Teleprotection channel tests	TELEPRO CH1 FAIL TELEPRO CH2 FAIL TELEPRO CH1 ID FAIL TELEPRO CH2 ID FAIL TELEPRO CH1 CRC FAIL TELEPRO CH2 CRC FAIL TELEPRO CH1 PKT LOST TELEPRO CH2 PKT LOST	Channel 1 failed Channel 2 failed The ID check for a peer relay on channel 1 has failed The ID check for a peer relay on channel 2 has failed CRC detected packet corruption on channel 1 CRC detected packet corruption on channel 2 CRC detected lost packet on channel 1 CRC detected lost packet on channel 2
ELEMENT: Teleprotection inputs/outputs	TELEPRO INPUT 1-1 On ↓ TELEPRO INPUT 1-16 On TELEPRO INPUT 2-1 On ↓ TELEPRO INPUT 2-16 On	Flag is set, Logic =1 ↓ Flag is set, Logic =1 Flag is set, Logic =1 ↓ Flag is set, Logic =1
ELEMENT Trip output	TRIP 3-POLE TRIP 1-POLE TRIP PHASE A TRIP PHASE B TRIP PHASE C TRIP AR INIT 3-POLE TRIP FORCE 3-POLE	Trip all three breaker poles A single-pole trip-and-reclose operation is initiated Trip breaker pole A, initiate phase A breaker fail and reclose Trip breaker pole B, initiate phase B breaker fail and reclose Trip breaker pole C, initiate phase C breaker fail and reclose Initiate a three-pole reclose Three-pole trip must be initiated
ELEMENT Trip bus	TRIP BUS 1 PKP TRIP BUS 1 OP	Asserted when the trip bus 1 element picks up. Asserted when the trip bus 1 element operates.
	TRIP BUS 2 ...	Same set of operands as shown for TRIP BUS 1
ELEMENT: Wattmetric zero-sequence directional	WATTMETRIC 1 PKP WATTMETRIC 1 OP	Wattmetric directional element 1 has picked up Wattmetric directional element 1 has operated
	WATTMETRIC 2...	Same set of operands as per WATTMETRIC 1 above
FIXED OPERANDS	Off	Logic = 0. Does nothing and may be used as a delimiter in an equation list; used as 'Disable' by other features.
	On	Logic = 1. Can be used as a test setting.
INPUTS/OUTPUTS: Contact inputs	Cont Ip 1 On Cont Ip 2 On ↓ Cont Ip 1 Off Cont Ip 2 Off ↓	(will not appear unless ordered) (will not appear unless ordered) ↓ (will not appear unless ordered) (will not appear unless ordered) ↓

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 7 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
INPUTS/OUTPUTS: Contact outputs, current (from detector on form-A output only)	Cont Op 1 IOn Cont Op 2 IOn ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
	Cont Op 1 IOff Cont Op 2 IOff ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
INPUTS/OUTPUTS: Contact outputs, voltage (from detector on form-A output only)	Cont Op 1 VOn Cont Op 2 VOn ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
	Cont Op 1 VOff Cont Op 2 VOff ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
INPUTS/OUTPUTS Direct inputs	DIRECT INPUT 1 On ↓ DIRECT INPUT On	Flag is set, logic=1 ↓ Flag is set, logic=1
INPUTS/OUTPUTS: Remote inputs	REMOTE INPUT 1 On ↓ REMOTE INPUT 32 On	Flag is set, logic=1 ↓ Flag is set, logic=1
INPUTS/OUTPUTS: Virtual inputs	Virt Ip 1 On ↓ Virt Ip 64 On	Flag is set, logic=1 ↓ Flag is set, logic=1
INPUTS/OUTPUTS: Virtual outputs	Virt Op 1 On ↓ Virt Op 96 On	Flag is set, logic=1 ↓ Flag is set, logic=1
LED INDICATORS: Fixed front panel LEDs	LED IN SERVICE LED TROUBLE LED TEST MODE LED TRIP LED ALARM LED PICKUP LED VOLTAGE LED CURRENT LED FREQUENCY LED OTHER LED PHASE A LED PHASE B LED PHASE C LED NEUTRAL/GROUND	Asserted when the front panel IN SERVICE LED is on. Asserted when the front panel TROUBLE LED is on. Asserted when the front panel TEST MODE LED is on. Asserted when the front panel TRIP LED is on. Asserted when the front panel ALARM LED is on. Asserted when the front panel PICKUP LED is on. Asserted when the front panel VOLTAGE LED is on. Asserted when the front panel CURRENT LED is on. Asserted when the front panel FREQUENCY LED is on. Asserted when the front panel OTHER LED is on. Asserted when the front panel PHASE A LED is on. Asserted when the front panel PHASE B LED is on. Asserted when the front panel PHASE C LED is on. Asserted when the front panel NEUTRAL/GROUND LED is on.
LED INDICATORS: LED test	LED TEST IN PROGRESS	An LED test has been initiated and has not finished.
LED INDICATORS: User-programmable LEDs	LED USER 1	Asserted when user-programmable LED 1 is on.
	LED USER 2 to 48	The operand above is available for user-programmable LEDs 2 through 48.
REMOTE DEVICES	REMOTE DEVICE 1 On ↓ REMOTE DEVICE 16 On	Flag is set, logic=1 ↓ Flag is set, logic=1
	REMOTE DEVICE 1 Off ↓ REMOTE DEVICE 16 Off	Flag is set, logic=1 ↓ Flag is set, logic=1
RESETTING	RESET OP RESET OP (COMMS) RESET OP (OPERAND) RESET OP (PUSHBUTTON)	Reset command is operated (set by all 3 operands below) Communications source of the reset command Operand (assigned in the **INPUTS/OUTPUTS ⇨⇩ RESETTING** menu) source of the reset command Reset key (pushbutton) source of the reset command

Table 5–9: L60 FLEXLOGIC™ OPERANDS (Sheet 8 of 8)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
SELF-DIAGNOSTICS	ANY MAJOR ERROR	Any of the major self-test errors generated (major error)
	ANY MINOR ERROR	Any of the minor self-test errors generated (minor error)
	ANY SELF-TEST	Any self-test errors generated (generic, any error)
	BATTERY FAIL	See description in *Chapter 7: Commands and Targets*
	DIRECT DEVICE OFF	See description in *Chapter 7: Commands and Targets*
	DIRECT RING BREAK	See description in *Chapter 7: Commands and Targets*
	DSP ERROR	See description in *Chapter 7: Commands and Targets*
	EEPROM DATA ERROR	See description in *Chapter 7: Commands and Targets*
	EQUIPMENT MISMATCH	See description in *Chapter 7: Commands and Targets*
	FLEXLOGIC ERR TOKEN	See description in *Chapter 7: Commands and Targets*
	IRIG-B FAILURE	See description in *Chapter 7: Commands and Targets*
	LATCHING OUT ERROR	See description in *Chapter 7: Commands and Targets*
	LOW ON MEMORY	See description in *Chapter 7: Commands and Targets*
	NO DSP INTERRUPTS	See description in *Chapter 7: Commands and Targets*
	PRI ETHERNET FAIL	See description in *Chapter 7: Commands and Targets*
	PROGRAM MEMORY	See description in *Chapter 7: Commands and Targets*
	PROTOTYPE FIRMWARE	See description in *Chapter 7: Commands and Targets*
	REMOTE DEVICE OFF	See description in *Chapter 7: Commands and Targets*
	SEC ETHERNET FAIL	See description in *Chapter 7: Commands and Targets*
	SNTP FAILURE	See description in *Chapter 7: Commands and Targets*
	SYSTEM EXCEPTION	See description in *Chapter 7: Commands and Targets*
	UNIT NOT CALIBRATED	See description in *Chapter 7: Commands and Targets*
	UNIT NOT PROGRAMMED	See description in *Chapter 7: Commands and Targets*
	WATCHDOG ERROR	See description in *Chapter 7: Commands and Targets*
UNAUTHORIZED ACCESS ALARM	UNAUTHORIZED ACCESS	Asserted when a password entry fails while accessing a password-protected level of the relay.
USER-PROGRAMMABLE PUSHBUTTONS	PUSHBUTTON 1 ON	Pushbutton number 1 is in the “On” position
	PUSHBUTTON 1 OFF	Pushbutton number 1 is in the “Off” position
	ANY PB ON	Any of twelve pushbuttons is in the “On” position
	PUSHBUTTON 2 to 12	Same set of operands as PUSHBUTTON 1

Some operands can be re-named by the user. These are the names of the breakers in the breaker control feature, the ID (identification) of contact inputs, the ID of virtual inputs, and the ID of virtual outputs. If the user changes the default name/ID of any of these operands, the assigned name will appear in the relay list of operands. The default names are shown in the FlexLogic™ operands table above.

The characteristics of the logic gates are tabulated below, and the operators available in FlexLogic™ are listed in the FlexLogic™ operators table.

Table 5–10: FLEXLOGIC™ GATE CHARACTERISTICS

GATES	NUMBER OF INPUTS	OUTPUT IS ‘1’ (= ON) IF...
NOT	1	input is ‘0’
OR	2 to 16	any input is ‘1’
AND	2 to 16	all inputs are ‘1’
NOR	2 to 16	all inputs are ‘0’
NAND	2 to 16	any input is ‘0’
XOR	2	only one input is ‘1’

Table 5–11: FLEXLOGIC™ OPERATORS

TYPE	SYNTAX	DESCRIPTION	NOTES
Editor	INSERT	Insert a parameter in an equation list.	
	DELETE	Delete a parameter from an equation list.	
End	END	The first END encountered signifies the last entry in the list of processed FlexLogic™ parameters.	
One-shot	POSITIVE ONE SHOT	One shot that responds to a positive going edge.	A 'one shot' refers to a single input gate that generates a pulse in response to an edge on the input. The output from a 'one shot' is True (positive) for only one pass through the FlexLogic™ equation. There is a maximum of 64 'one shots'.
	NEGATIVE ONE SHOT	One shot that responds to a negative going edge.	
	DUAL ONE SHOT	One shot that responds to both the positive and negative going edges.	
Logic gate	NOT	Logical NOT	Operates on the previous parameter.
	OR(2) ↓ OR(16)	2 input OR gate ↓ 16 input OR gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	AND(2) ↓ AND(16)	2 input AND gate ↓ 16 input AND gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	NOR(2) ↓ NOR(16)	2 input NOR gate ↓ 16 input NOR gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	NAND(2) ↓ NAND(16)	2 input NAND gate ↓ 16 input NAND gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	XOR(2)	2 input Exclusive OR gate	Operates on the 2 previous parameters.
	LATCH (S,R)	Latch (set, reset): reset-dominant	The parameter preceding LATCH(S,R) is the reset input. The parameter preceding the reset input is the set input.
Timer	TIMER 1 ↓ TIMER 32	Timer set with FlexLogic™ timer 1 settings. ↓ Timer set with FlexLogic™ timer 32 settings.	The timer is started by the preceding parameter. The output of the timer is TIMER #.
Assign virtual output	= Virt Op 1 ↓ = Virt Op 96	Assigns previous FlexLogic™ operand to virtual output 1. ↓ Assigns previous FlexLogic™ operand to virtual output 96.	The virtual output is set by the preceding parameter

5.4.2 FLEXLOGIC™ RULES

When forming a FlexLogic™ equation, the sequence in the linear array of parameters must follow these general rules:

1. Operands must precede the operator which uses the operands as inputs.
2. Operators have only one output. The output of an operator must be used to create a virtual output if it is to be used as an input to two or more operators.
3. Assigning the output of an operator to a virtual output terminates the equation.
4. A timer operator (e.g. "TIMER 1") or virtual output assignment (e.g. " = Virt Op 1") may only be used once. If this rule is broken, a syntax error will be declared.

5.4.3 FLEXLOGIC™ EVALUATION

Each equation is evaluated in the order in which the parameters have been entered.

NOTE

FlexLogic™ provides latches which by definition have a memory action, remaining in the set state after the set input has been asserted. However, they are *volatile*; i.e. they reset on the re-application of control power.

When making changes to settings, all FlexLogic™ equations are re-compiled whenever any new setting value is entered, so all latches are automatically reset. If it is necessary to re-initialize FlexLogic™ during testing, for example, it is suggested to power the unit down and then back up.

5.4.4 FLEXLOGIC™ EXAMPLE

This section provides an example of implementing logic for a typical application. The sequence of the steps is quite important as it should minimize the work necessary to develop the relay settings. Note that the example presented in the figure below is intended to demonstrate the procedure, not to solve a specific application situation.

In the example below, it is assumed that logic has already been programmed to produce virtual outputs 1 and 2, and is only a part of the full set of equations used. When using FlexLogic™, it is important to make a note of each virtual output used – a virtual output designation (1 to 96) can only be properly assigned once.

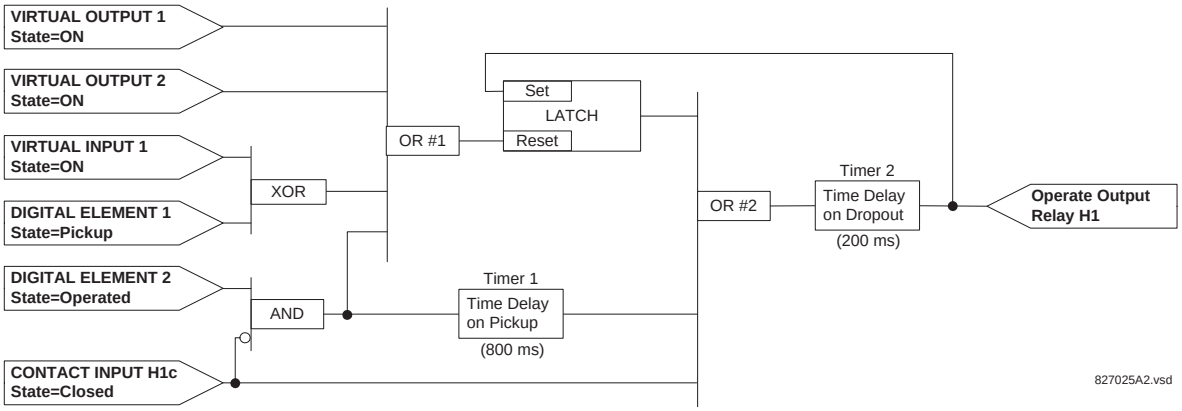


Figure 5–29: EXAMPLE LOGIC SCHEME

1. Inspect the example logic diagram to determine if the required logic can be implemented with the FlexLogic™ operators. If this is not possible, the logic must be altered until this condition is satisfied. Once this is done, count the inputs to each gate to verify that the number of inputs does not exceed the FlexLogic™ limits, which is unlikely but possible. If the number of inputs is too high, subdivide the inputs into multiple gates to produce an equivalent. For example, if 25 inputs to an AND gate are required, connect Inputs 1 through 16 to AND(16), 17 through 25 to AND(9), and the outputs from these two gates to AND(2).

   Inspect each operator between the initial operands and final virtual outputs to determine if the output from the operator is used as an input to more than one following operator. If so, the operator output must be assigned as a virtual output.

For the example shown above, the output of the AND gate is used as an input to both OR#1 and Timer 1, and must therefore be made a virtual output and assigned the next available number (i.e. Virtual Output 3). The final output must also be assigned to a virtual output as virtual output 4, which will be programmed in the contact output section to operate relay H1 (that is, contact output H1).

Therefore, the required logic can be implemented with two FlexLogic™ equations with outputs of virtual output 3 and virtual output 4 as shown below.

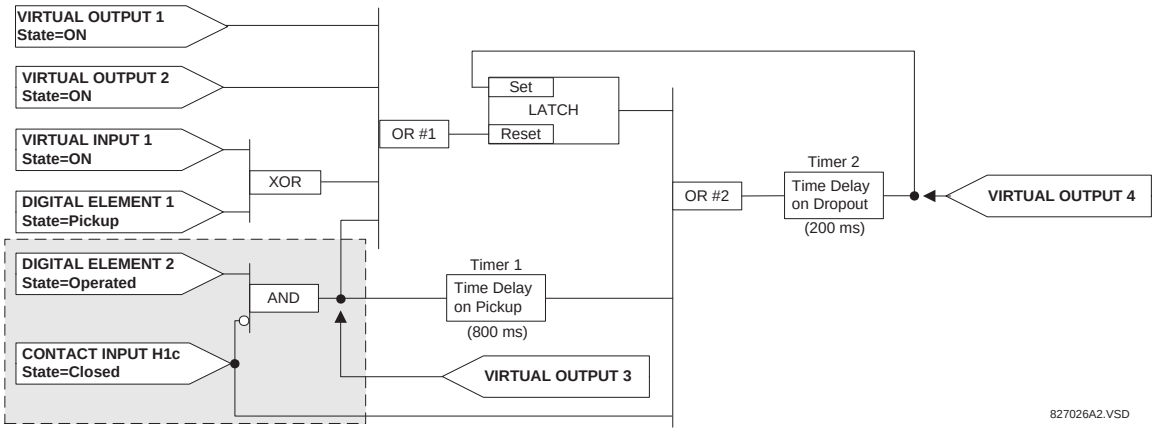


Figure 5–30: LOGIC EXAMPLE WITH VIRTUAL OUTPUTS

2. Prepare a logic diagram for the equation to produce virtual output 3, as this output will be used as an operand in the virtual output 4 equation (create the equation for every output that will be used as an operand first, so that when these operands are required they will already have been evaluated and assigned to a specific virtual output). The logic for virtual output 3 is shown below with the final output assigned.

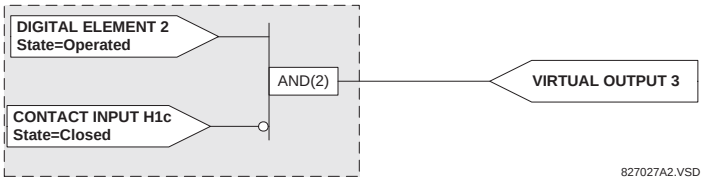


Figure 5–31: LOGIC FOR VIRTUAL OUTPUT 3

3. Prepare a logic diagram for virtual output 4, replacing the logic ahead of virtual output 3 with a symbol identified as virtual output 3, as shown below.

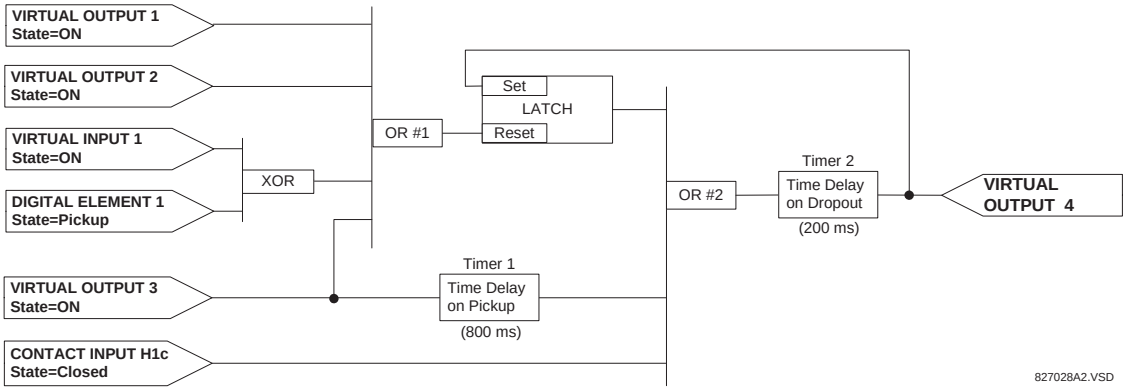


Figure 5–32: LOGIC FOR VIRTUAL OUTPUT 4

4. Program the FlexLogic™ equation for virtual output 3 by translating the logic into available FlexLogic™ parameters. The equation is formed one parameter at a time until the required logic is complete. It is generally easier to start at the output end of the equation and work back towards the input, as shown in the following steps. It is also recommended to list operator inputs from bottom to top. For demonstration, the final output will be arbitrarily identified as parameter 99,

and each preceding parameter decremented by one in turn. Until accustomed to using FlexLogic™, it is suggested that a worksheet with a series of cells marked with the arbitrary parameter numbers be prepared, as shown below.

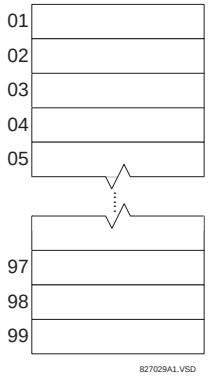


Figure 5–33: FLEXLOGIC™ WORKSHEET

5. Following the procedure outlined, start with parameter 99, as follows:

   99: The final output of the equation is virtual output 3, which is created by the operator "= Virt Op n". This parameter is therefore "= Virt Op 3."

   98: The gate preceding the output is an AND, which in this case requires two inputs. The operator for this gate is a 2-input AND so the parameter is “AND(2)”. Note that FlexLogic™ rules require that the number of inputs to most types of operators must be specified to identify the operands for the gate. As the 2-input AND will operate on the two operands preceding it, these inputs must be specified, starting with the lower.

   97: This lower input to the AND gate must be passed through an inverter (the NOT operator) so the next parameter is “NOT”. The NOT operator acts upon the operand immediately preceding it, so specify the inverter input next.

   96: The input to the NOT gate is to be contact input H1c. The ON state of a contact input can be programmed to be set when the contact is either open or closed. Assume for this example the state is to be ON for a closed contact. The operand is therefore “Cont Ip H1c On”.

   95: The last step in the procedure is to specify the upper input to the AND gate, the operated state of digital element 2. This operand is "DIG ELEM 2 OP".

   Writing the parameters in numerical order can now form the equation for virtual output 3:

```
[95] DIG ELEM 2 OP
[96] Cont Ip H1c On
[97] NOT
[98] AND(2)
[99] = Virt Op 3
```

It is now possible to check that this selection of parameters will produce the required logic by converting the set of parameters into a logic diagram. The result of this process is shown below, which is compared to the logic for virtual output 3 diagram as a check.

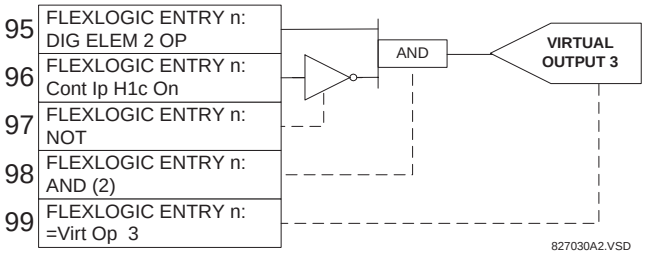


Figure 5–34: FLEXLOGIC™ EQUATION FOR VIRTUAL OUTPUT 3

6. Repeating the process described for virtual output 3, select the FlexLogic™ parameters for Virtual Output 4.

99: The final output of the equation is virtual output 4 which is parameter “= Virt Op 4".

98: The operator preceding the output is timer 2, which is operand “TIMER 2". Note that the settings required for the timer are established in the timer programming section.

97: The operator preceding timer 2 is OR #2, a 3-input OR, which is parameter “OR(3)”.

96: The lowest input to OR #2 is operand “Cont Ip H1c On”.

95: The center input to OR #2 is operand “TIMER 1".

94: The input to timer 1 is operand “Virt Op 3 On".

93: The upper input to OR #2 is operand “LATCH (S,R)”.

92: There are two inputs to a latch, and the input immediately preceding the latch reset is OR #1, a 4-input OR, which is parameter “OR(4)”.

91: The lowest input to OR #1 is operand “Virt Op 3 On".

90: The input just above the lowest input to OR #1 is operand “XOR(2)”.

89: The lower input to the XOR is operand “DIG ELEM 1 PKP”.

88: The upper input to the XOR is operand “Virt Ip 1 On".

87: The input just below the upper input to OR #1 is operand “Virt Op 2 On".

86: The upper input to OR #1 is operand “Virt Op 1 On".

85: The last parameter is used to set the latch, and is operand “Virt Op 4 On".

The equation for virtual output 4 is:

```
[85] Virt Op 4 On
[86] Virt Op 1 On
[87] Virt Op 2 On
[88] Virt Ip 1 On
[89] DIG ELEM 1 PKP
[90] XOR(2)
[91] Virt Op 3 On
[92] OR(4)
[93] LATCH (S,R)
[94] Virt Op 3 On
[95] TIMER 1
[96] Cont Ip H1c On
[97] OR(3)
[98] TIMER 2
[99] = Virt Op 4
```

It is now possible to check that the selection of parameters will produce the required logic by converting the set of parameters into a logic diagram. The result of this process is shown below, which is compared to the logic for virtual output 4 diagram as a check.

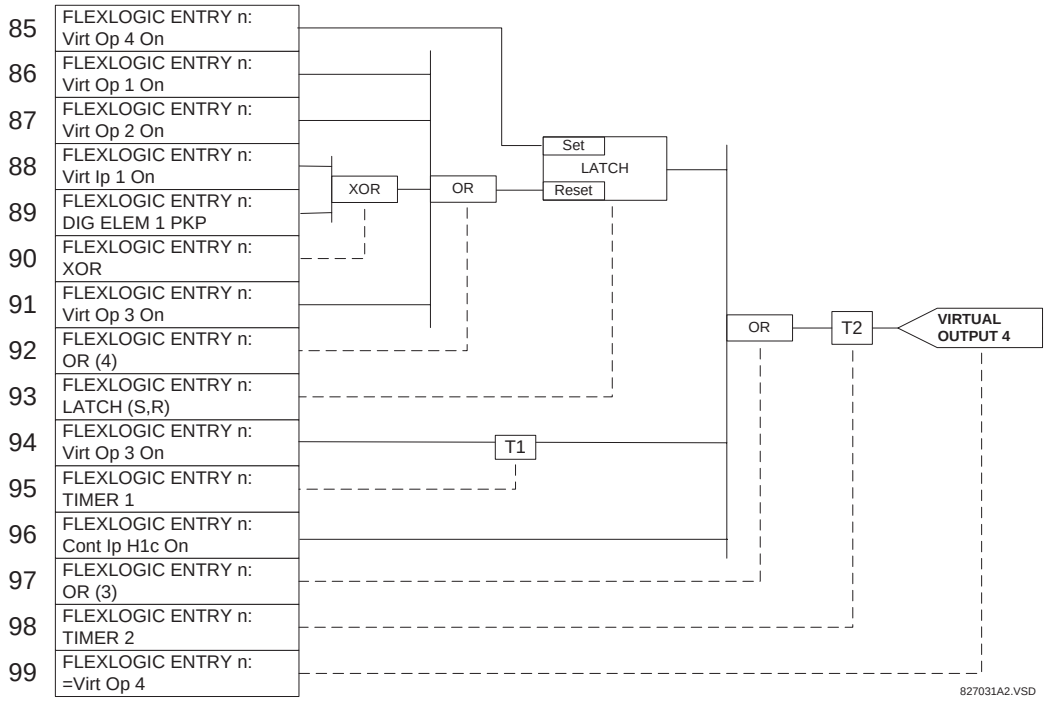


Figure 5–35: FLEXLOGIC™ EQUATION FOR VIRTUAL OUTPUT 4

7. Now write the complete FlexLogic™ expression required to implement the logic, making an effort to assemble the equation in an order where Virtual Outputs that will be used as inputs to operators are created before needed. In cases where a lot of processing is required to perform logic, this may be difficult to achieve, but in most cases will not cause problems as all logic is calculated at least four times per power frequency cycle. The possibility of a problem caused by sequential processing emphasizes the necessity to test the performance of FlexLogic™ before it is placed in service.

   In the following equation, virtual output 3 is used as an input to both latch 1 and timer 1 as arranged in the order shown below:

```
DIG ELEM 2 OP
Cont Ip H1c On
NOT
AND(2)
= Virt Op 3
Virt Op 4 On
Virt Op 1 On
Virt Op 2 On
Virt Ip 1 On
DIG ELEM 1 PKP
XOR(2)
Virt Op 3 On
OR(4)
LATCH (S,R)
Virt Op 3 On
TIMER 1
Cont Ip H1c On
OR(3)
TIMER 2
= Virt Op 4
END
```

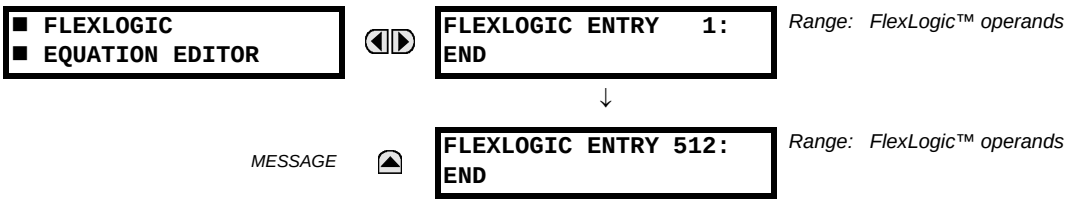
   In the expression above, the virtual output 4 input to the four-input OR is listed before it is created. This is typical of a form of feedback, in this case, used to create a seal-in effect with the latch, and is correct.

8. The logic should always be tested after it is loaded into the relay, in the same fashion as has been used in the past. Testing can be simplified by placing an "END" operator within the overall set of FlexLogic™ equations. The equations will then only be evaluated up to the first "END" operator.

   The "On" and "Off" operands can be placed in an equation to establish a known set of conditions for test purposes, and the "INSERT" and "DELETE" commands can be used to modify equations.

5.4.5 FLEXLOGIC™ EQUATION EDITOR

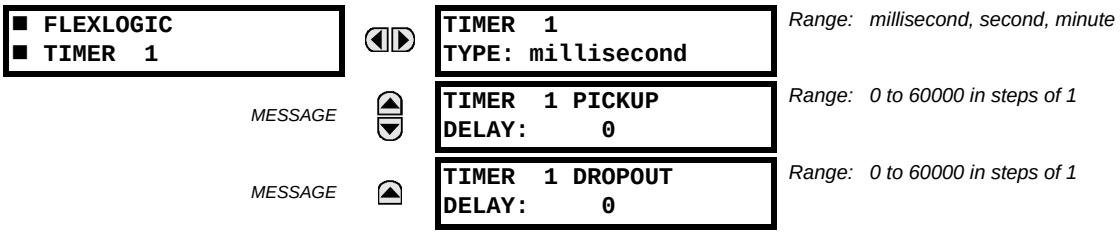
PATH: SETTINGS ⇨⇩ FLEXLOGIC ⇨ FLEXLOGIC EQUATION EDITOR



There are 512 FlexLogic™ entries available, numbered from 1 to 512, with default END entry settings. If a "Disabled" Element is selected as a FlexLogic™ entry, the associated state flag will never be set to '1'. The '+/–' key may be used when editing FlexLogic™ equations from the keypad to quickly scan through the major parameter types.

5.4.6 FLEXLOGIC™ TIMERS

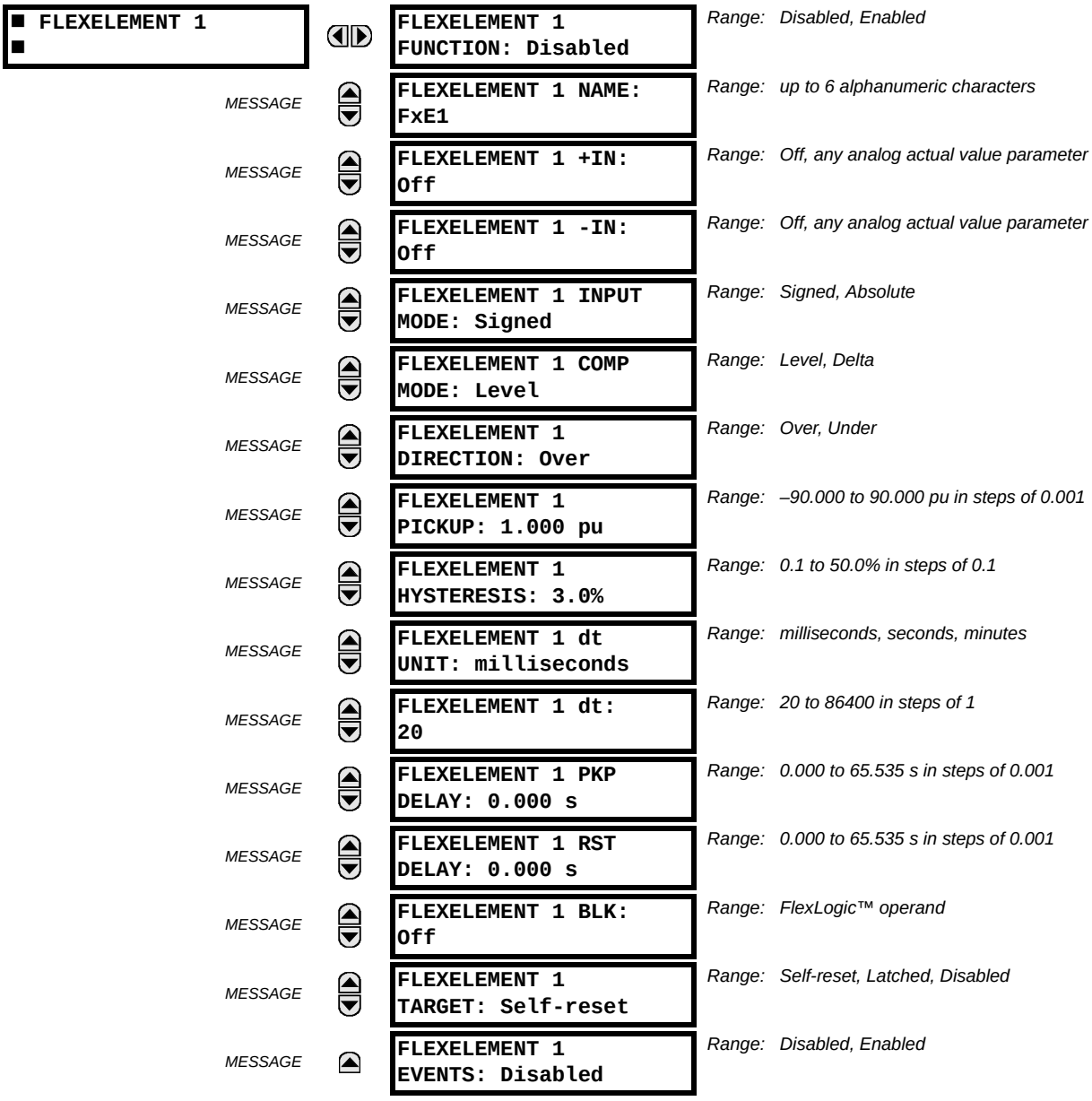
PATH: SETTINGS ⇨⇩ FLEXLOGIC ⇨⇩ FLEXLOGIC TIMERS ⇨ FLEXLOGIC TIMER 1(32)



There are 32 identical FlexLogic™ timers available. These timers can be used as operators for FlexLogic™ equations.

- **TIMER 1 TYPE:** This setting is used to select the time measuring unit.
- **TIMER 1 PICKUP DELAY:** Sets the time delay to pickup. If a pickup delay is not required, set this function to "0".
- **TIMER 1 DROPOUT DELAY:** Sets the time delay to dropout. If a dropout delay is not required, set this function to "0".

PATH: SETTING ⇨⇩ FLEXLOGIC ⇨⇩ FLEXELEMENTS ⇨ FLEXELEMENT 1(8)



A FlexElement™ is a universal comparator that can be used to monitor any analog actual value calculated by the relay or a net difference of any two analog actual values of the same type. The effective operating signal could be treated as a signed number or its absolute value could be used as per user's choice.

The element can be programmed to respond either to a signal level or to a rate-of-change (delta) over a pre-defined period of time. The output operand is asserted when the operating signal is higher than a threshold or lower than a threshold as per user's choice.

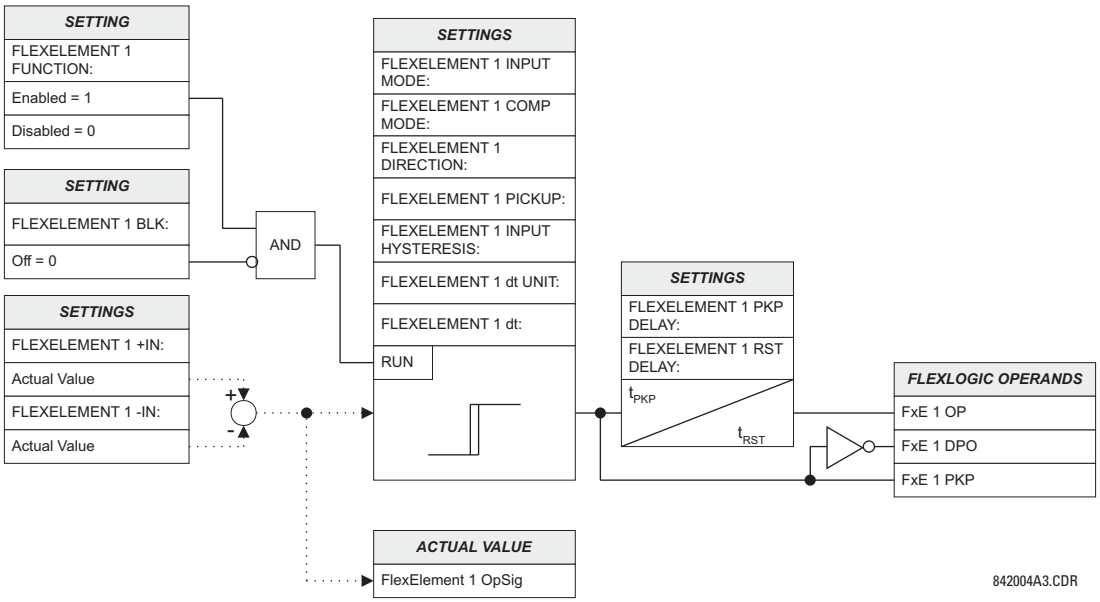


Figure 5–36: FLEXELEMENT™ SCHEME LOGIC

The **FLEXELEMENT 1 +IN** setting specifies the first (non-inverted) input to the FlexElement™. Zero is assumed as the input if this setting is set to "Off". For proper operation of the element at least one input must be selected. Otherwise, the element will not assert its output operands.

This **FLEXELEMENT 1 –IN** setting specifies the second (inverted) input to the FlexElement™. Zero is assumed as the input if this setting is set to "Off". For proper operation of the element at least one input must be selected. Otherwise, the element will not assert its output operands. This input should be used to invert the signal if needed for convenience, or to make the element respond to a differential signal such as for a top-bottom oil temperature differential alarm. The element will not operate if the two input signals are of different types, for example if one tries to use active power and phase angle to build the effective operating signal.

The element responds directly to the differential signal if the **FLEXELEMENT 1 INPUT MODE** setting is set to "Signed". The element responds to the absolute value of the differential signal if this setting is set to "Absolute". Sample applications for the "Absolute" setting include monitoring the angular difference between two phasors with a symmetrical limit angle in both directions; monitoring power regardless of its direction, or monitoring a trend regardless of whether the signal increases of decreases.

The element responds directly to its operating signal – as defined by the **FLEXELEMENT 1 +IN**, **FLEXELEMENT 1 –IN** and **FLEXELEMENT 1 INPUT MODE** settings – if the **FLEXELEMENT 1 COMP MODE** setting is set to "Level". The element responds to the rate of change of its operating signal if the **FLEXELEMENT 1 COMP MODE** setting is set to "Delta". In this case the **FLEXELEMENT 1 dt UNIT** and **FLEXELEMENT 1 dt** settings specify how the rate of change is derived.

The **FLEXELEMENT 1 DIRECTION** setting enables the relay to respond to either high or low values of the operating signal. The following figure explains the application of the **FLEXELEMENT 1 DIRECTION**, **FLEXELEMENT 1 PICKUP** and **FLEXELEMENT 1 HYSTERESIS** settings.

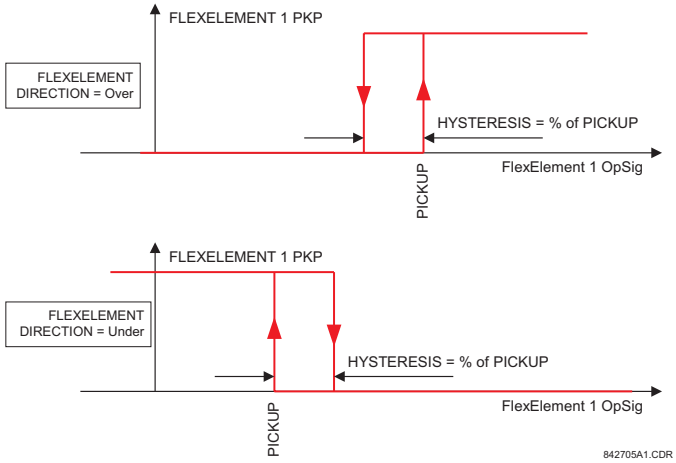


Figure 5–37: FLEXELEMENT™ DIRECTION, PICKUP, AND HYSTERESIS

In conjunction with the **FLEXELEMENT 1 INPUT MODE** setting the element could be programmed to provide two extra characteristics as shown in the figure below.

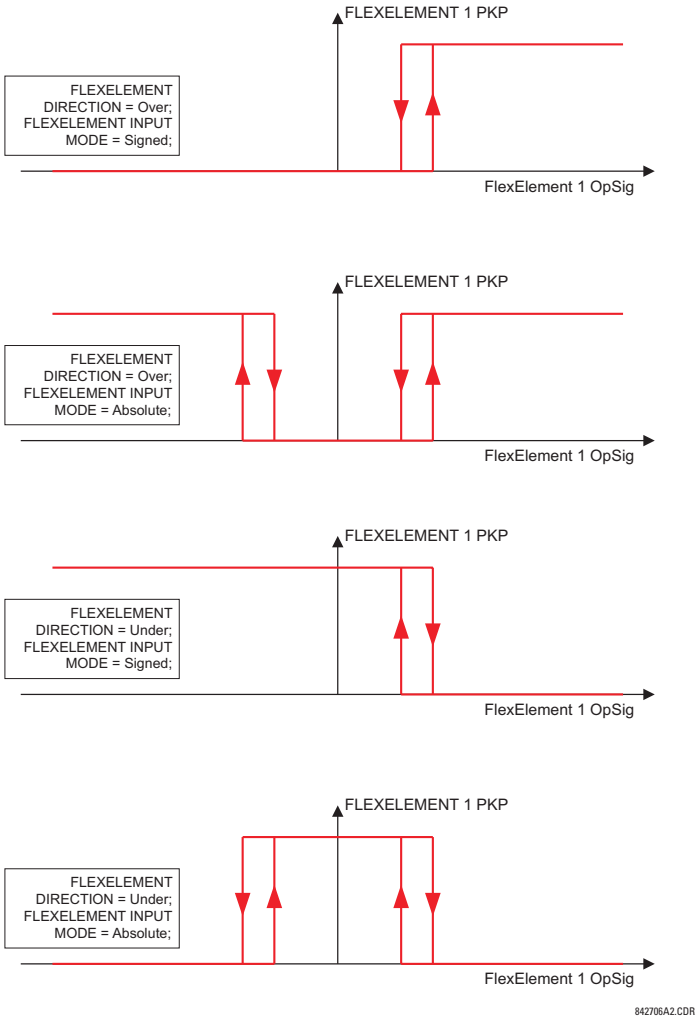


Figure 5–38: FLEXELEMENT™ INPUT MODE SETTING

The **FLEXELEMENT 1 PICKUP** setting specifies the operating threshold for the effective operating signal of the element. If set to "Over", the element picks up when the operating signal exceeds the **FLEXELEMENT 1 PICKUP** value. If set to "Under", the element picks up when the operating signal falls below the **FLEXELEMENT 1 PICKUP** value.

The **FLEXELEMENT 1 HYSTERESIS** setting controls the element dropout. It should be noticed that both the operating signal and the pickup threshold can be negative facilitating applications such as reverse power alarm protection. The FlexElement™ can be programmed to work with all analog actual values measured by the relay. The **FLEXELEMENT 1 PICKUP** setting is entered in per-unit values using the following definitions of the base units:

Table 5–12: FLEXELEMENT™ BASE UNITS

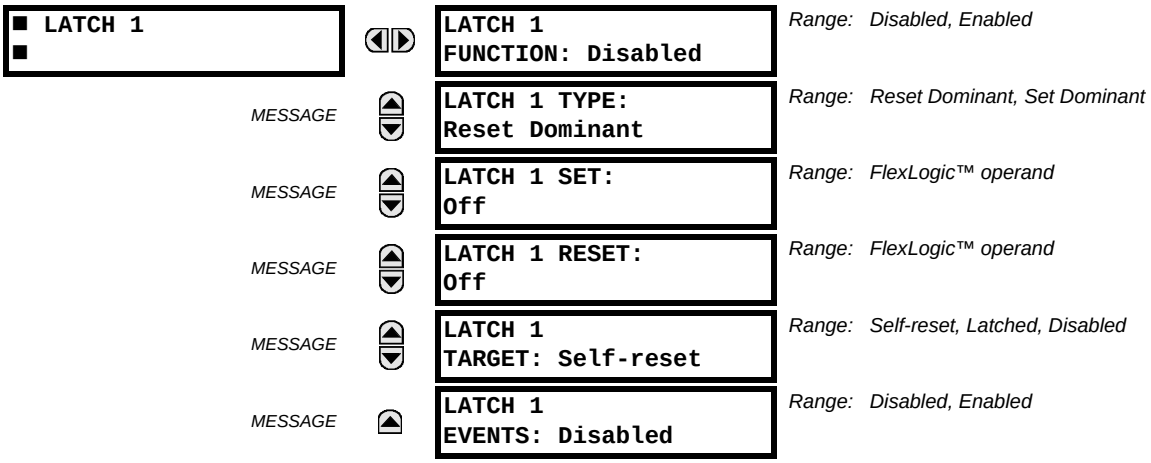
BREAKER ARCING AMPS (Brk X Arc Amp A, B, and C)	BASE = 2000 $kA^2 \times$ cycle
dcmA	BASE = maximum value of the **DCMA INPUT MAX** setting for the two transducers configured under the +IN and –IN inputs.
FREQUENCY	f_{BASE} = 1 Hz
PHASE ANGLE	φ_{BASE} = 360 degrees (see the UR angle referencing convention)
POWER FACTOR	PF_{BASE} = 1.00
RTDs	BASE = 100°C
SOURCE CURRENT	I_{BASE} = maximum nominal primary RMS value of the +IN and –IN inputs
SOURCE POWER	P_{BASE} = maximum value of $V_{BASE} \times I_{BASE}$ for the +IN and –IN inputs
SOURCE VOLTAGE	V_{BASE} = maximum nominal primary RMS value of the +IN and –IN inputs
SYNCHROCHECK (Max Delta Volts)	V_{BASE} = maximum primary RMS value of all the sources related to the +IN and –IN inputs

The **FLEXELEMENT 1 HYSTERESIS** setting defines the pickup–dropout relation of the element by specifying the width of the hysteresis loop as a percentage of the pickup value as shown in the FlexElement™ Direction, Pickup, and Hysteresis diagram.

The **FLEXELEMENT 1 DT UNIT** setting specifies the time unit for the setting **FLEXELEMENT 1 dt**. This setting is applicable only if **FLEXELEMENT 1 COMP MODE** is set to "Delta". The **FLEXELEMENT 1 DT** setting specifies duration of the time interval for the rate of change mode of operation. This setting is applicable only if **FLEXELEMENT 1 COMP MODE** is set to "Delta".

This **FLEXELEMENT 1 PKP DELAY** setting specifies the pickup delay of the element. The **FLEXELEMENT 1 RST DELAY** setting specifies the reset delay of the element.

PATH: SETTINGS ⇨⇩ FLEXLOGIC ⇨⇩ NON-VOLATILE LATCHES ⇨ LATCH 1(16)



The non-volatile latches provide a permanent logical flag that is stored safely and will not reset upon reboot after the relay is powered down. Typical applications include sustaining operator commands or permanently block relay functions, such as Autorecloser, until a deliberate interface action resets the latch. The settings element operation is described below:

- **LATCH 1 TYPE**: This setting characterizes Latch 1 to be Set- or Reset-dominant.
- **LATCH 1 SET**: If asserted, the specified FlexLogic™ operands 'sets' Latch 1.
- **LATCH 1 RESET**: If asserted, the specified FlexLogic™ operand 'resets' Latch 1.

LATCH N TYPE	LATCH N SET	LATCH N RESET	LATCH N ON	LATCH N OFF
Reset Dominant	ON	OFF	ON	OFF
	OFF	OFF	Previous State	Previous State
	ON	ON	OFF	ON
	OFF	ON	OFF	ON
Set Dominant	ON	OFF	ON	OFF
	ON	ON	ON	OFF
	OFF	OFF	Previous State	Previous State
	OFF	ON	OFF	ON

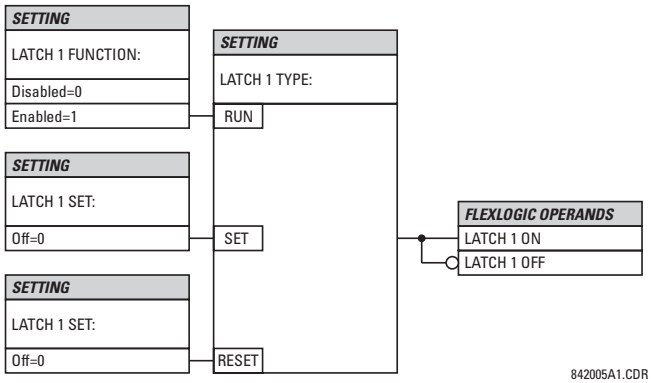


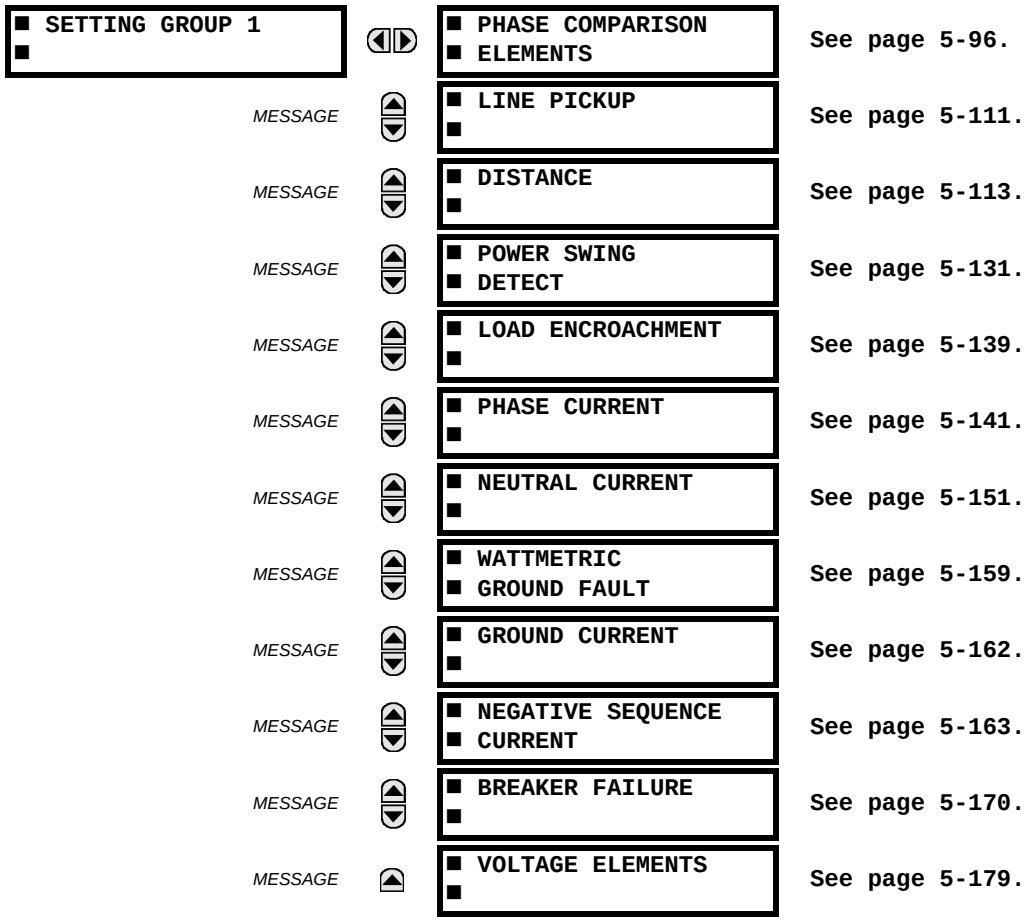
Figure 5–39: NON-VOLATILE LATCH OPERATION TABLE (N = 1 to 16) AND LOGIC

5.5.1 OVERVIEW

Each protection element can be assigned up to six different sets of settings according to Setting Group designations 1 to 6. The performance of these elements is defined by the active Setting Group at a given time. Multiple setting groups allow the user to conveniently change protection settings for different operating situations (e.g. altered power system configuration, season of the year). The active setting group can be preset or selected via the **SETTING GROUPS** menu (see the *Control Elements* section later in this chapter). See also the *Introduction to Elements* section at the beginning of this chapter.

5.5.2 SETTING GROUP

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6)



Each of the six setting group menus is identical. **SETTING GROUP 1** (the default active group) automatically becomes active if no other group is active (see the *Control Elements* section for additional details).

5.5.3 PHASE COMPARISON ELEMENTS

a) MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ PHASE COMPARISON ELEMENTS

■ PHASE COMPARISON ■ ELEMENTS		■ 87PC SCHEME ■	See page 5–96.
	MESSAGE	■ ADVANCED ■ FAULT DETECTORS	See page 5–102.
	MESSAGE	■ CHARGE CURRENT ■ COMPENSATION	See page 5–106.
	MESSAGE	■ OPEN BREAKER ■ ECHO	See page 5–108.

b) 87PC SCHEME

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ PHASE COMPARISON ELEMENTS ⇨ 87PC SCHEME

■ 87PC SCHEME ■		87PC FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	87PC SCHEME SELECT: 2TL-TR-SPC-2FC	*Range: 2TL-TR-SPC-2FC, 2TL-BL-SPC-2FC, 2TL-TR-DPC-3FC, etc.*
	MESSAGE	87PC BLOCK: Off	*Range: FlexLogic™ operand*
	MESSAGE	87PC SIGNAL SOURCE: One Source Current	*Range: One Source Current, Two Sources Current*
	MESSAGE	87PC SIGNAL: Mixed I_2-K*I_1	*Range: Mixed I_2–K*I_1, 3I_0*
	MESSAGE	87PC MIXED SIGNAL K: 0.20	*Range: 0.00 to 0.25 in steps of 0.01*
	MESSAGE	87PC MIXED SIGNAL REF ANGLE: 0°	*Range: 0 to 359° in steps of 1*
	MESSAGE	87PC FDL PICKUP: 0.50 pu	*Range: 0.02 to 15.00 pu in steps of 0.01*
	MESSAGE	87PC FDL AUX: Off	*Range: FlexLogic™ operand*
	MESSAGE	87PC FDH PICKUP: 0.75 pu	*Range: 0.05 to 15.00 pu in steps of 0.01*
	MESSAGE	87PC FDH AUX: Off	*Range: FlexLogic™ operand*
	MESSAGE	87PC CH1 ASYMMETRY: 0.0 ms	*Range: –5.0 to 5.0 ms in steps of 0.1*
	MESSAGE	87PC CH2 ASYMMETRY: 0.0 ms	*Range: –5.0 to 5.0 ms in steps of 0.1*
	MESSAGE	87PC CH1 DELAY: 0.0 ms	*Range: 0.0 to 30.0 ms in steps of 0.1*
	MESSAGE	87PC CH2 DELAY: 0.0 ms	*Range: 0.0 to 30.0 ms in steps of 0.1*

MESSAGE
87PC CH1 RX VOLT:
12.0 V
Range: 0.0 to 125.0 V in steps of 0.1

MESSAGE
87PC CH2 RX VOLT:
12.0 V
Range: 0.0 to 125.0 V in steps of 0.1

MESSAGE
87PC TRIP SECURITY:
First Coincidence
Range: First Coincidence, Enhanced

MESSAGE
87PC SECOND COINCID
TIMER: 40 ms
Range: 10 to 200 ms in steps of 1

MESSAGE
87PC STABILITY
ANGLE: 75°
Range: 40 to 140° in steps of 5

MESSAGE
87PC ENHANCED STAB
ANGLE: 110°
Range: 40 to 180° in steps of 5

MESSAGE
87PC RESET DELAY:
30 ms
Range: 0 to 200 ms in steps of 1

MESSAGE
87PC TRANS BLOCK
PICKUP: 0.030 s
Range: 0 to 65.535 s in steps of 0.001

MESSAGE
87PC TRANS BLOCK
RESET: 0.030 s
Range: 0 to 65.535 s in steps of 0.001

MESSAGE
87PC CHNL LOSS TRIP
WINDOW: 0 msec
Range: 0 to 500 ms in steps of 1

MESSAGE
87PC HIGH-SPEED TRIP
CONTACT 1: Off
Range: Off, available contact outputs

MESSAGE
87PC HIGH-SPEED TRIP
CONTACT 2: Off
Range: Off, available contact outputs

MESSAGE
87PC TARGET:
Self-Reset
Range: Self-Reset, Latched, Disabled

MESSAGE
87PC EVENTS:
Disabled
Range: Disabled, Enabled

The phase comparison tripping scheme menu provides the main setup for the phase comparison relay.

- **87PC SCHEME SELECT:** Selects the phase comparison element scheme logic as follows:

  2TL-TR-SPC-2FC: two-terminal line, permissive tripping, single phase comparison, two frequency channel.
  2TL-BL-SPC-2FC: two-terminal line, blocking scheme, single phase comparison, two frequency channel.
  2TL-UB-DPC-2FC: two-terminal line, unblocking, dual phase comparison, two frequency channel (FSK PLC only); scheme cannot be used for breaker-and-a-half applications.
  2TL-TR-DPC-3FC: two-terminal line, permissive tripping, dual phase comparison, three frequency channel.
  2TL-BL-DPC-3FC: three-terminal line, blocking scheme, dual phase comparison, three frequency channel.
  3TL-TR-SPC-2FC: three-terminal line, permissive tripping scheme, single phase comparison, two frequency channel carrier to two other terminals.
  3TL-BL-SPC-2FC: three-terminal line, blocking scheme, single phase comparison, two frequency channel carrier to two other terminals.
  3TL-TR-DPC-3FC: three-terminal line, permissive tripping scheme, dual phase comparison, three frequency channel carrier to two other terminals.
  3TL-BL-SPC-3FC: three-terminal line, blocking scheme, dual phase comparison, three frequency channel carrier to two other terminals.

NOTE

1. A two-frequency channel (2FC) can be either amplitude modulated (AM) on-off carrier or a high-low frequency shift keying (FSK) system.
2. Additional information about phase comparison schemes can be found in the *Theory of Operation* chapter.

3. In blocking schemes, the open breaker echo element must be disabled.

- **87PC BLOCK:** Selects a Flexlogic™ operand that blocks operation of the phase comparison scheme (for example, an operand that indicates operation of a communications channel failure detector).
- **87PC SIGNAL SOURCE**: Selects whether current is supplied from one current source (either single-breaker CT application or dual-breakers with CTs summed externally) or from two separate sources (breaker-and-a-half or ring configurations), where currents from both CTs are fed into the L60 individually.
- **87PC SIGNAL:** A mixed I_2 – K × I_1 signal or a single 3I_0 signal can be chosen as the operating signal for the FDH and FDL detectors and squaring amplifier. The constant K in the mixed excitation signal is adjustable.
- **87PC MIXED SIGNAL K:** Selects the K factor used in the mixed excitation operating signal I_2 – K × I_1.
- **87PC MIXED SIGNAL REF ANGLE**: This setting applies exclusively to the negative-sequence mixed mode operating current ("Mixed I_2-K*I_1") and specifies a leading angular shift for the originally developed operating signal. The operating signal is always developed taking phase A as reference for calculating symmetrical components. This setting can be used to control the angular position of the operating current with respect to the voltage of any phase that might be used by the line carrier in a particular application. This allows minimizing the impact of positive corona on dependability of single-comparison blocking schemes. Effectively this setting shifts the transmitted pulses in time with the intent to minimize – for majority of faults – the overlap between the space periods and positive peaks of the voltage in the phase used by the carrier. Normally, this angle shall be adjusted to follow the conductor used by the carrier plus the extra line characteristic angle (approximately 90°).

  The following setting rule applies particularly for blocking schemes:

REF ANGLE SETTING	PHASE ROTATION, ABC	PHASE ROTATION, ACB
Carrier in phase A	90°	90°
Carrier in phase B	240° + 90° = 330°	120° + 90° = 110°
Carrier in phase C	120° + 90° = 110°	240° + 90° = 330°

  Some applications are not concerned with the corona effect, such as when the applied carrier uses narrow-band filtering, or similar techniques improving security and dependability of transmission.

  Shifting the angle reference is considered an advanced principle and does not have to be used in all applications. If used in situations that are not concerned with the corona effect, this setting will not alter operation of the relay: neither improves it, nor impairs it. The only effect would be in possibly different operating times for different fault types, with the average times unchanged.

  NOTE This setting must be set identically at all line terminals or the scheme will be dramatically impacted to the extent of entirely diminishing security and/or dependability. The same caution applies to the scheme type, operating current, and *K* settings.

- **87PC FDL PICKUP:** This setting is used to select the FDL pickup value. FDL is used as a start-keying element.
- **87PC FDL AUX**: This setting assigns an auxiliary element (an impedance element, for example) in parallel with FDL to start channel keying. This is beneficial for power system conditions when FDL cannot pick up.
- **87PC FDH PICKUP:** This setting is used to select FDH pickup value. FDH is used as a trip-arming element.
- **87PC FDH AUX**: This setting assigns an auxiliary element (an impedance element, for example) in parallel with FDH to permit tripping. This is beneficial for power system conditions where FDH cannot pick up.
- **87PC CH1(2) ASYMMETRY:** These settings set the symmetry adjustment to make "positive" and "negative" halves of the power cycle of the received signal from the remote terminal via communication channel noise symmetrical. Refer to the test procedures for more detailed information.
- **87PC CH1(2) DELAY:** These settings delay the local signal until the remote signal is received. Refer to the test procedures for more detailed information.
- **87PC CH1(2) RX VOLT**: These settings select a threshold for the signal received from the carrier(s). They are dependent on the carrier nominal output voltage. A value of 10 to 20% of carrier nominal output voltage is recommended.
- **87PC TRIP SECURITY**: This setting controls security of the response of the 87PC function on the first and following coincidence periods. When set to "First Coincidence" the function uses the primary **87PC STABILITY ANGLE** setting and operates when the integrated value exceeds the setting. Each coincidence period is treated independently. When set to "Enhanced", the function applies the value for the first coincidence period specified by **87PC ENHANCED STAB ANGLE**

setting. If the integrated value is less than this more stringent stability angle setting, the function does not trip. If the integrated value is greater than the regular stability angle setting, but less than the enhanced trip level, the function arms itself toward tripping on the next coincidence. The regular stability angle value specified by the **87PC STABILITY ANGLE** setting controls tripping on the next coincidence.

- **87PC SECOND COINCID TIMER**: This setting applies only if the **87PC TRIP SECURITY** mode is set to "Enhanced". The specified time opens a window for tripping on the second coincidence if the first coincidence does not satisfy the more stringent stability angle setting. This value is typically set to 1.25 cycles in dual comparison applications and 2 cycles in single comparison applications.
- **87PC STABILITY ANGLE:** This setting is used to select the stability angle for trip security.
- **87PC ENHANCED STAB ANGLE**: This setting specifies the more stringent stability angle allowing the scheme to trip safely on the first coincidence. This setting applies only if the **87PC TRIP SECURITY** mode is set to "Enhanced". This setting is typically 30° to 40° higher than the regular stability angle specified by the **87PC STABILITY ANGLE** setting.

  The enhanced trip security is illustrated below. In part a) of the figure, tripping occurs at the first coincidence if the integrator exceeds the enhanced stability angle setting. In part b) of the figure, tripping occurs at the second coincidence if at the first coincidence integrator exceeded the stability angle setting but did not reach the enhanced stability angle setting.

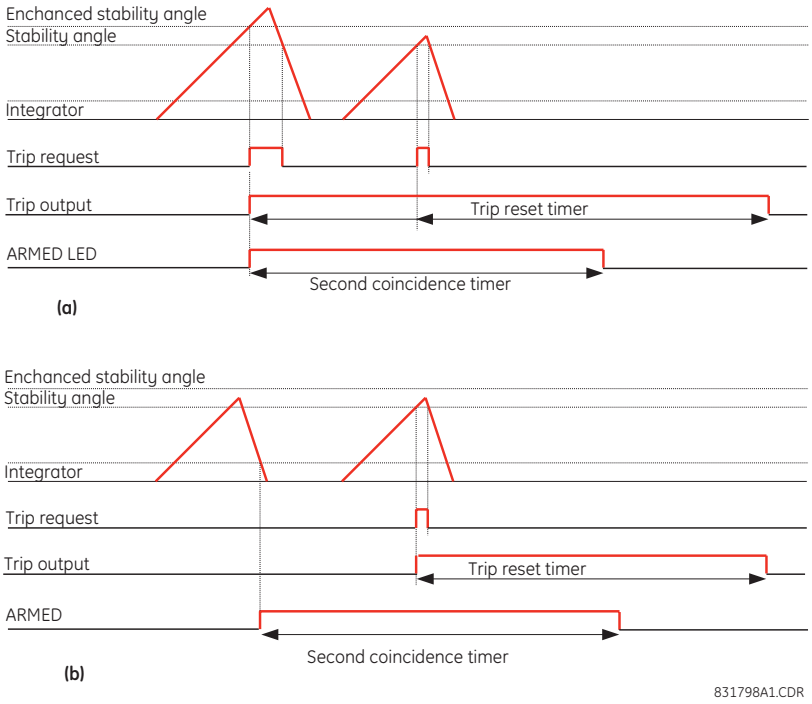


Figure 5–40: ENHANCED TRIP SECURITY

- **87PC RESET DELAY**: This setting is used to seal-in the output phase comparison element after operating by the time defined by this setting. A value of 30 ms or higher is recommended. A value of 0 ms operates the element during integrated coincidence only, meaning that the 87PC OP output operand is set and reset on every cycle.
- **87PC TRANS BLOCK PICKUP:** This setting increases sensitivity during and after the clearing of an external fault and prevents false tripping during transient current intervals.
- **87PC TRANS BLOCK RESET:** Resets transient blocking and allows tripping.
- **87PC CHNL LOSS TRIP WINDOW:** This setting is applicable to the 2TL-UB-DPC-2FC scheme only. If a loss of carrier is detected in the course of the fault, a trip is allowed for the time defined by this setting (default value is 0). The trip is blocked after the expiration of this time window.
- **87PC HIGH-SPEED CONTACT 1(2)**: These settings allow decreasing of the tripping time by up to ¼ of the power cycle by bypassing FlexLogic™ execution and sending trip command directly from the 87PC function to the contact output. These setting are used for breaker 1 and 2 (if used) trip coil connections.

Phase comparison signals are important for the analysis of 87PC operation. As such, they are recorded in oscillography. A list of the 87PC channels recorded in oscillography is shown below.

Table 5–13: 87PC OSCILLOGRAPHY CHANNELS

CFG FILE LABEL	DESCRIPTION
X1: IA	Phase A of the F module CT bank
X2: IB	Phase B of the F module CT bank
X3: IC	Phase C of the F module CT bank
X#: IA	Phase A of the X module CT bank
X#: IB	Phase B of the X module CT bank
X#: IC	Phase C of the X module CT bank
87PC BKR1 Current	Effective mixed operating signal of BKR1
87PC BKR1 POS	Positive current pulse for the first breaker
87PC BKR1 NEG	Negative current pulse for the first breaker
87PC BKR1 Mag	Magnitude of the effective operating signal of BKR1
87PC BKR1 FDL	Low-set fault detection for the first breaker
87PC BKR1 FDH	High-set fault detection for the first breaker
87PC BKR2 Current	Effective mixed operating signal of BKK2
87PC BKR2 POS	Positive current pulse for the second breaker
87PC BKR2 NEG	Negative current pulse for the second breaker
87PC BKR2 Mag	Magnitude of the effective operating signal of BKR2
87PC BKR2 FDL	Low-set fault detection for the second breaker
87PC BKR2 FDH	High-set fault detection for the second breaker
87PC POS	Positive current local pulse for both breakers
87PC NEG	Negative current local pulse for both breakers
87PC FDL	Low-set fault detection for both breakers
87PC FDH	High-set fault detection for both breakers
87PC Rx1P Voltage	Received pulse (voltage) on channel 1P
87PC Rx1P	Received pulse on channel 1P
87PC Rx1N Voltage	Received (voltage) on channel 1N
87PC Rx1N	Received pulse on channel 1N
87PC Rx2P Voltage	Received pulse (voltage) on channel 2P
87PC Rx2P	Received pulse on channel 2P
87PC Rx2N Voltage	Received pulse (voltage) on channel 2N
87PC Rx2N	Received pulse on channel 2N
87PC POS Aligned	Aligned (delayed) local positive pulse
87PC NEG Aligned	Aligned (delayed) local negative pulse
87PC Rx1P Aligned	Received and conditioned pulse on channel 1P
87PC Rx1N Aligned	Received and conditioned pulse on channel 1N
87PC Rx2P Aligned	Received and conditioned pulse on channel 2P
87PC Rx2N Aligned	Received and conditioned pulse on channel 2N
87PC POS Int Input	Input of the positive integrator
87PC NEG Int Input	Input of the negative integrator
87PC POS Integrator	Positive integrator in (degrees)
87PC NEG Integrator	Negative integrator in (degrees)

Refer to Chapter 9: *Application of Settings* for the calculation examples for the 87PC element.

In single phase comparison schemes, coincidence of the local and remote squares is detected during half the power cycle only, positive or negative. As a result, some delay in operation can be expected under “unfavorable” fault inception. This weakness of the single phase comparison schemes is eliminated in dual phase comparison schemes but cost of the communication link is higher.

Some advantages of dual phase comparison and two frequency FSK PLC are incorporated in the unblocking scheme. Since there is no third or guard frequency available, the PLC low frequency signal serves as the guard frequency for some logic implemented in this scheme. Tripping is permitted if the FDL relay sees the change in received signal form low to high (indicated that communication link is healthy and remote relay detected the fault) within 20 ms after fault is detected. If the PLC low frequency has not being received prior the fault detection, the trip output is blocked as well. Another enhancement of this scheme is the trip window defined by the **87PC CHNL LOSS TRIP WINDOW** setting. This logic allows the relay to make a trip decision within this time if the PLC signal was lost in the course of the fault.

The phase comparison function can be used for three-terminal line protection and breaker-and-a-half configuration. The feature combines the advantages of the modern digital relay with the traditional “analog principle” approach. Pulses received from a PLC are digitally sampled at 64 samples per cycle, providing excellent resolution. This also eliminates carrier building-up and tailing-off problems, since the voltage threshold for received pulses is user-programmable. If a pulse received from PLC is consciously distorted and is not equal to half of the sinewave, it can be adjusted with the **87PC CH1(2) ASYMMETRY** settings. All phase comparison signals are captured and available in oscillography for commissioning, troubleshooting, and analysis purposes. The L60 features excellent stability during channel noise due to the high sampling rate of the received signal, and the unique integrator makes the digital phase-comparison relay fully equivalent to analogue phase-comparison relays.

The following figure illustrates the phase comparison logic. The choice of the scheme must made by protection and control engineer according to the communication equipment employed, requirements of trip speed, and reliability. These schemes are considered in Chapter 8: *Theory of Operation*.

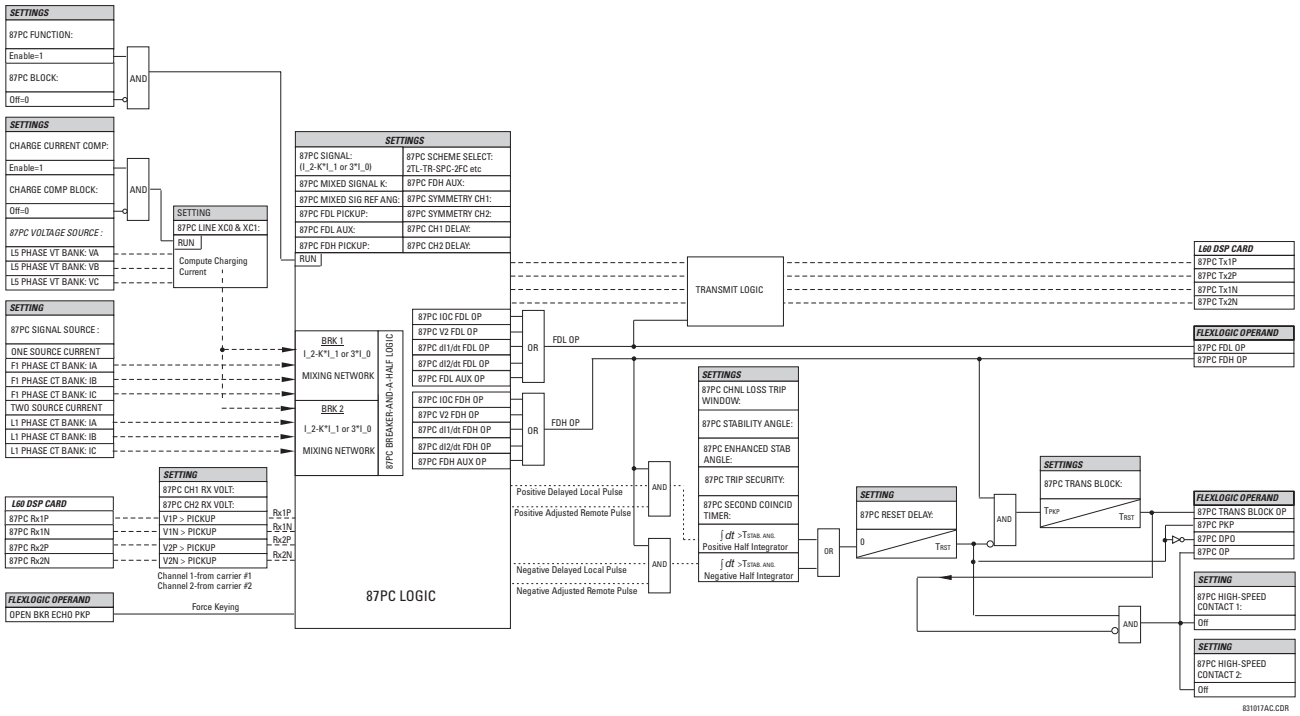
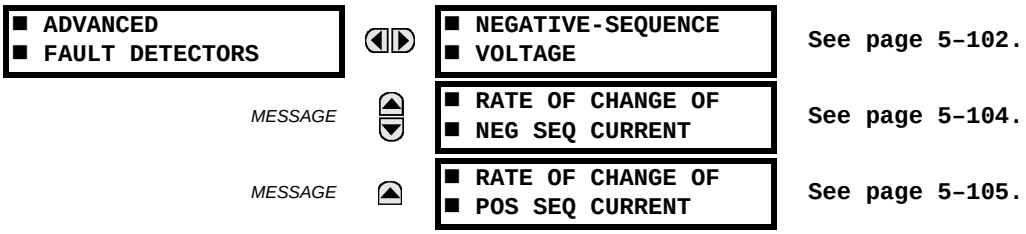


Figure 5–41: OVERALL PHASE COMPARISON LOGIC

c) ADVANCED FAULT DETECTORS MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ PHASE COMPARISON ELEMENTS ⇨⇩ ADVANCED FAULT DETECTORS



Three advanced fault detectors are provided.

The negative-sequence voltage element responds to the $I \times Z - V$ term for negative-sequence voltage and current and is meant to detect faults under weak system conditions.

The negative-sequence current rate of change element responds to the increment in the magnitude of the negative-sequence current over a half-a-cycle moving data window, and is meant to detect faults under load unbalance such as on untransposed high voltage transmission lines or in a vicinity of electrical traction systems causing significant negative-sequence current unbalance.

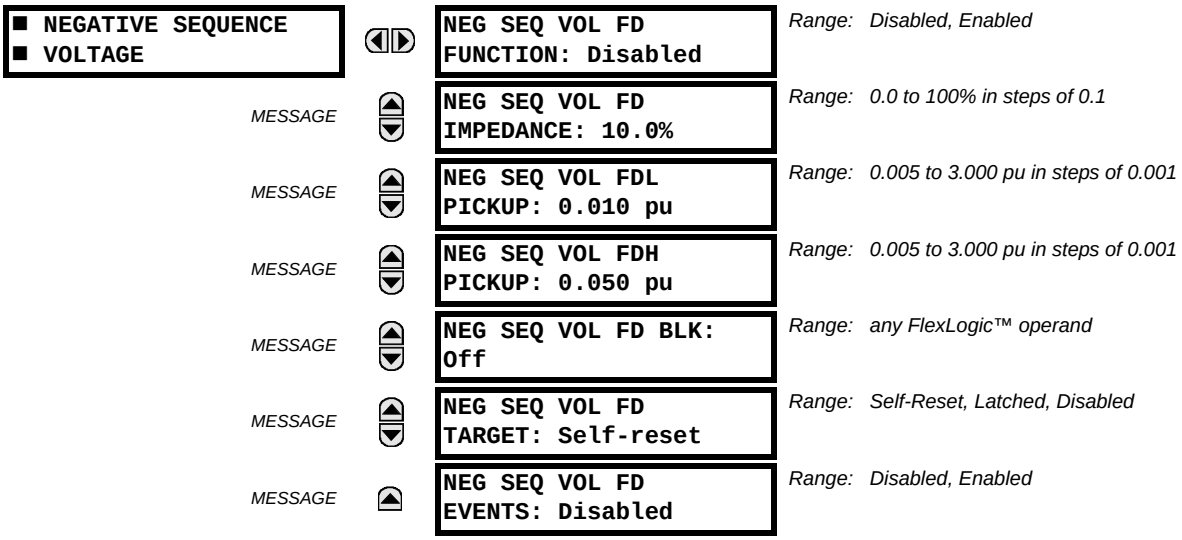
The positive-sequence current rate of change element responds to the increment in the magnitude of the positive-sequence current over a half-a-cycle moving data window, and is meant to detect three-phase balance faults under high load conditions.

All three detectors operate independently from each other, and independently from the instantaneous overcurrent FDL and FDH comparators embedded in the 87PC function. Each detector supports the low and high setting levels to facilitate starting and supervise tripping. When enabled, a given detector is automatically used to control the 87PC function. Effectively all detectors are ORed before they are routed to the 87PC element.

The overcurrent fault detectors respond to the effective operating current of the 87PC function. The advanced fault detectors respond to their operating signals irrespective of the 87PC current configured.

d) NEGATIVE-SEQUENCE VOLTAGE FAULT DETECTION

PATH: SETTINGS ⇨⇩ GROUPED... ⇨ PHASE COMPARISON... ⇨⇩ ADVANCED FAULT DETECTORS ⇨ NEGATIVE SEQUENCE VOLTAGE



The element responds to the magnitude of the $I\_2 \times Z - V\_2$ voltage term in the signal source associated with the 87PC function. The impedance factor is controlled by an independent setting. Two voltage thresholds are provided for the low-set and high-set operation controlling keying and tripping, respectively.

- **NEG SEQ VOL FD FUNCTION**: This setting enables or disables the negative-sequence voltage fault detection. Note that all fault detectors operate in parallel toward the 87PC function. If not required, a given fault detector shall be dis-

abled. To effectively disable the overcurrent fault detectors under the main 87PC menu, set their threshold very high. This function requires voltages to operate, and uses the first voltage bank configured in the relay.

- **NEG SEQ VOL FD IMPEDANCE**: This setting defines the relative magnitude of the $I\_2 \times Z$ term augmented to the negative-sequence voltage. The element uses the positive-sequence line impedance – both magnitude and angle – as defined under **SETTINGS ⇨⇩ PRODUCT SETUP ⇨⇩ FAULT REPORTS ⇨ FAULT REPORT**. This setting controls the percentage of the line impedance used in the $I\_2 \times Z - V\_2$ voltage term.
- **NEG SEQ VOL FDL PICKUP**: This setting controls pickup of the low-set stage used to control the key operation. The nominal phase-to-ground voltage of the VT bank of the relay is 1 pu. For example, for a phase VT bank configured in wye and having 63.5 V nominal secondary, or for a phase VT bank configured in delta and having 110 V nominal secondary, 1 pu is equivalent to 63.5 V.
- **NEG SEQ VOL FDH PICKUP**: This setting controls pickup of the high-set stage used to control the trip operation. The nominal phase-to-ground voltage of the VT bank of the relay is 1 pu.
- **NEG SEQ VOL FD BLK**: The fault detector is hard-wired to the 87PC scheme. It can be disabled permanently using the function setting or blocked temporarily using this block setting. Indicate a FlexLogic™ operand to block the negative-sequence voltage fault detector upon assertion.
- **NEG SEQ VOL FD TARGET**: This setting controls the targets of the function. These targets operate independently from the 87PC targets.
- **NEG SEQ VOL FD EVENTS**: This setting controls event recording of the function. These events are logged independently from the 87PC events.

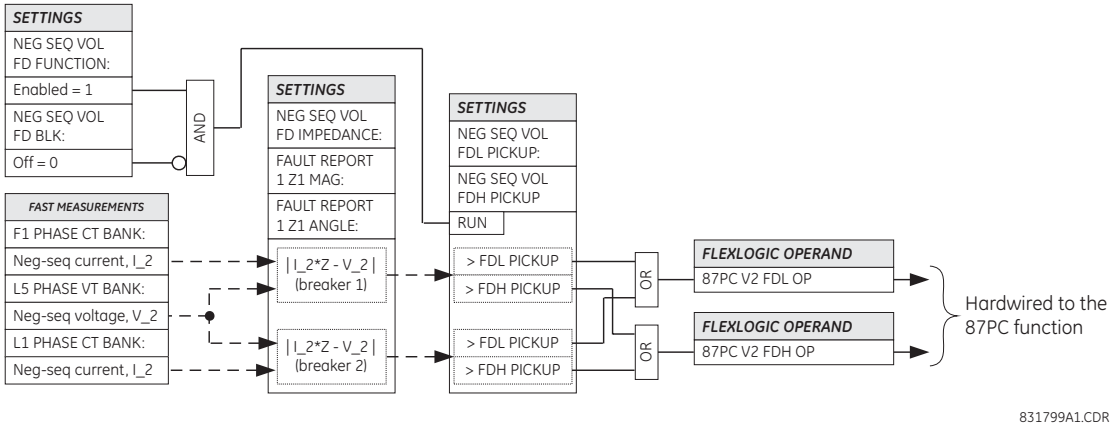
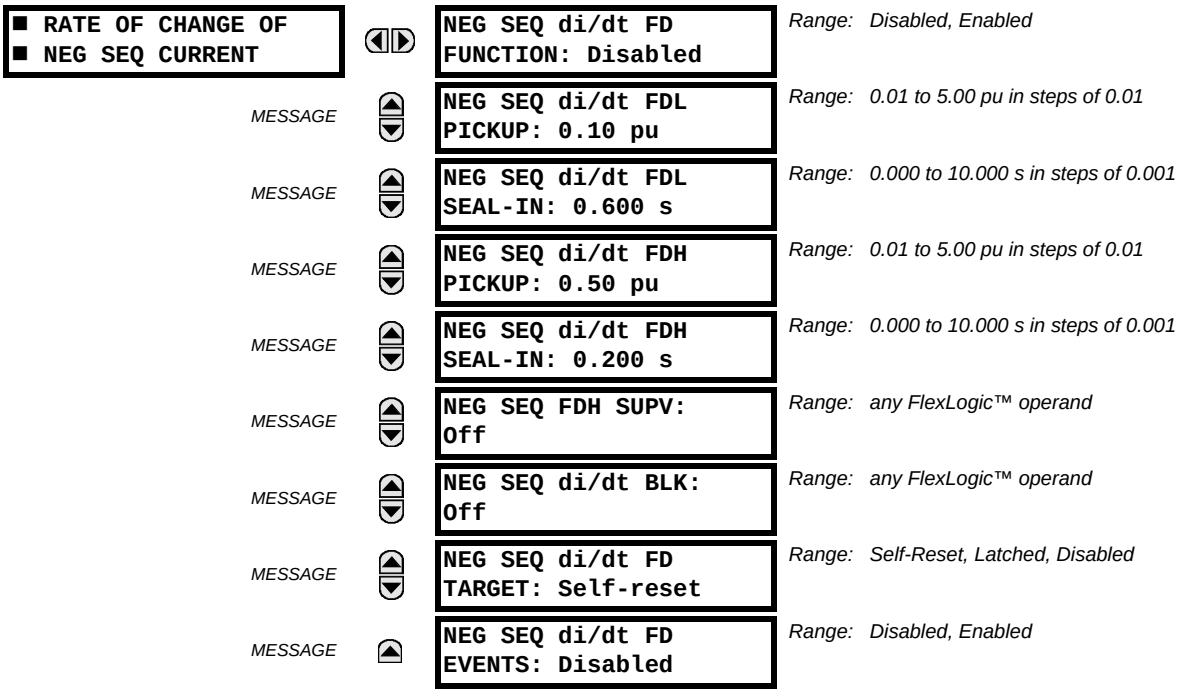


Figure 5–42: NEGATIVE-SEQUENCE VOLTAGE FAULT DETECTOR LOGIC

e) RATE OF CHANGE OF NEGATIVE-SEQUENCE CURRENT FAULT DETECTION

PATH: SETTINGS ⇨⇩ GROUPED... ⇨ PHASE COMPARISON... ⇨⇩ ADVANCED FAULT... ⇨⇩ RATE OF CHANGE OF NEG SEQ CURRENT



The element responds to the change in magnitude of the negative-sequence current over a sliding window of half a power system cycle. Two voltage thresholds are provided for the low-set and high-set operation controlling keying and tripping. The raw *di* / *dt* condition of the element detects the change and resets when reaching a steady state fault condition. As such, a seal-in timer is provided to maintain the detected fault condition for a user specified period of time.

- **NEG SEQ di/dt FD FUNCTION**: This setting enables or disables the rate of change of negative-sequence current fault detection. Note that all fault detectors operate in parallel toward the 87PC function. If not required, a given fault detector shall be disabled. To effectively disable the overcurrent fault detectors under the main 87PC menu, set their threshold very high.
- **NEG SEQ di/dt FDL PICKUP**: This setting controls pickup of the low set stage of the element used to control the key operation. The nominal current of the phase CT bank of the relay is 1 pu.
- **NEG SEQ di/dt FDL SEAL-IN**: This setting defines seal-in time of the FDL function. To equalize the response between all terminals of the line, the timer is started at the rising edge of the raw *di* / *dt* condition.
- **NEG SEQ di/dt FDH PICKUP**: This setting controls pickup of the high set stage of the element used to control the trip operation. The nominal current of the phase CT bank of the relay is 1 pu.
- **NEG SEQ di/dt FDH SEAL-IN**: This setting defines seal-in time of the FDH function. To equalize the response between all terminals of the line, the timer is started at the rising edge of the raw *di* / *dt* condition. In this way, the fault detectors reset approximately at the same time at all line terminals, regardless of responses of individual raw conditions potentially different at different line terminals.
- **NEG SEQ FDH SUPV**: This setting provides seal-in control of the FDH function for the symmetrical external three-phase faults starting as non-symmetrical defined by the **NEG SEQ DI/DT FDH SEAL-IN** setting time. The overreaching distance function should typically be assigned with this setting.
- **NEG SEQ di/dt BLK**: Note that the fault detector is hard-wired to the 87PC scheme. It can be disabled permanently using the function setting or blocked temporarily using this block setting. Select a FlexLogic™ operand that, if asserted, should block this fault detector.
- **NEG SEQ di/dt FD TARGET:** This setting controls targets of the function. These targets operate independently from the 87PC targets.

- **NEG SEQ di/dt FD EVENTS**: This setting controls event recording of the function. These events are logged independently from the 87PC events.

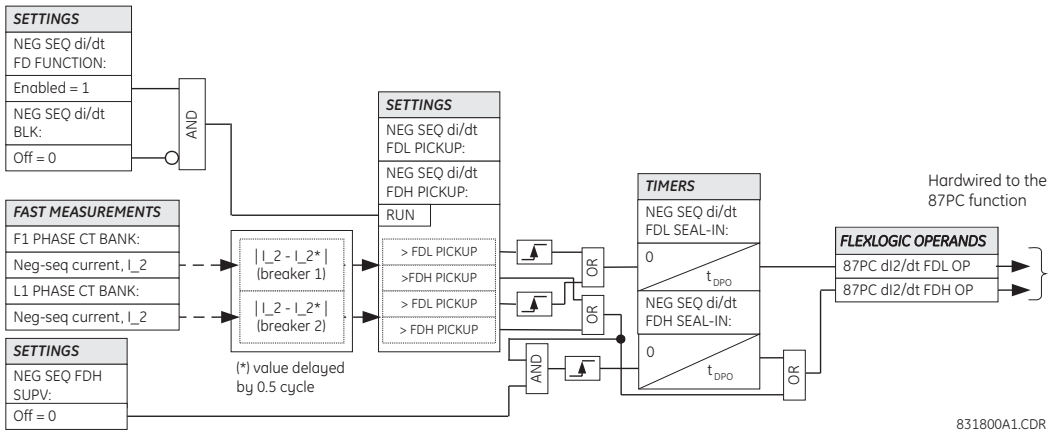


Figure 5–43: NEGATIVE-SEQUENCE CURRENT RATE OF CHANGE FAULT DETECTOR LOGIC

f) RATE OF CHANGE OF POSITIVE-SEQUENCE CURRENT FAULT DETECTION

PATH: SETTINGS ⇨⇩ GROUPED... ⇨ PHASE COMPARISON... ⇨⇩ ADVANCED FAULT... ⇨⇩ RATE OF CHANGE OF POS SEQ CURRENT

■ RATE OF CHANGE OF ■ POS SEQ CURRENT	POS SEQ di/dt FD FUNCTION: Disabled	*Range: Disabled, Enabled*
MESSAGE	POS SEQ di/dt FDL PICKUP: 0.10 pu	*Range: 0.01 to 5.00 pu in steps of 0.01*
MESSAGE	POS SEQ di/dt FDL SEAL-IN: 0.600 s	*Range: 0.000 to 10.000 s in steps of 0.001*
MESSAGE	POS SEQ di/dt FDH PICKUP: 0.50 pu	*Range: 0.01 to 5.00 pu in steps of 0.01*
MESSAGE	POS SEQ di/dt FDH SEAL-IN: 0.200 s	*Range: 0.000 to 10.000 s in steps of 0.001*
MESSAGE	POS SEQ FDH SUPV: Off	*Range: any FlexLogic™ operand*
MESSAGE	POS SEQ di/dt BLK: Off	*Range: any FlexLogic™ operand*
MESSAGE	POS SEQ di/dt FD TARGET: Self-reset	*Range: Self-Reset, Latched, Disabled*
MESSAGE	POS SEQ di/dt FD EVENTS: Disabled	*Range: Disabled, Enabled*

The element responds to the change in magnitude of the positive-sequence current over a sliding window of half a power system cycle. Two current thresholds are provided for the low-set and high-set operation controlling keying and tripping. The raw *di* / *dt* condition of the element detects the change and resets when reaching a steady state fault condition. As such, a seal-in timer is provided to maintain the detected fault condition for a user specified period of time.

- **POS SEQ di/dt FD FUNCTION**: This setting enables or disables the rate of change of positive-sequence current fault detection. Note that all fault detectors operate in parallel toward the 87PC function. If not required, a given fault detector shall be disabled. To effectively disable the overcurrent fault detectors under the main 87PC menu, set their threshold very high.

- **POS SEQ di/dt FDL PICKUP**: This setting controls pickup of the low set stage of the element used to control the key operation. Nominal current of the phase CT bank of the relay is 1 pu.
- **POS SEQ di/dt FDL SEAL-IN**: This setting defines seal-in time of the FDL function. To equalize the response between all terminals of the line, the timer is started at the rising edge of the raw *di* / *dt* condition.
- **POS SEQ di/dt FDH PICKUP**: This setting controls pickup of the high set stage of the element used to control the trip operation. Nominal current of the phase CT bank of the relay is 1pu.
- **POS SEQ di/dt FDH SEAL-IN**: This setting defines seal-in time of the function. To equalize the response between all terminals of the line, the timer is started at the rising edge of the raw *di* / *dt* condition. In this way, the fault detectors reset approximately at the same time at all line terminals, regardless of responses of individual raw conditions potentially different at different line terminals.
- **POS SEQ FDH SUPV**: This setting provides seal-in control of the FDH function for the symmetrical external three-phase faults starting as non-symmetrical defined by the **POS SEQ DI/DT FDH SEAL-IN** setting time. The overreaching distance function should typically be assigned with this setting.
- **POS SEQ di/dt BLK**: Note that the fault detector is hard-wired to the 87PC scheme. It can be disabled permanently using the function setting, or blocked temporarily using this block setting. Select a FlexLogic™ operand that, if asserted, should block this fault detector.
- **POS SEQ di/dt FD TARGET**: This setting controls targets of the function. These targets operate independently from the 87PC targets.
- **POS SEQ di/dt FD EVENTS**: This setting controls event recording of the function. These events are logged independently from the 87PC events.

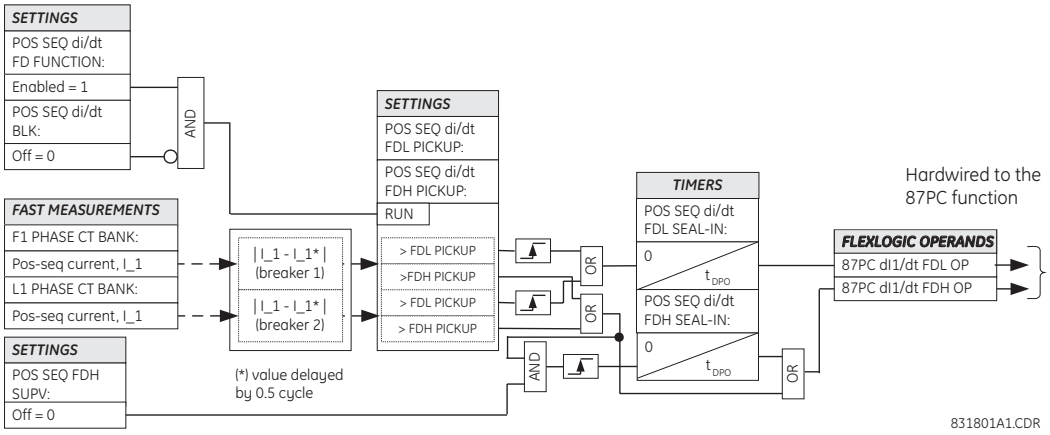


Figure 5–44: POSITIVE-SEQUENCE CURRENT RATE OF CHANGE FAULT DETECTOR LOGIC

g) CHARGE CURRENT COMPENSATION

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ PHASE COMPARISON ELEMENTS ⇨⇩ CHARGE CURRENT COMPENSATION

■ CHARGE CURRENT ■ COMPENSATION	◀▶	CHARGE CURRENT COMPENSATN: Disabled	*Range: Disabled, Enabled*
MESSAGE	▲▼	CHARGE COMPENST BLK: Off	*Range: any FlexLogic™ operand*
MESSAGE	▲▼	POS SEQ CAPACITIVE REACTANCE: 0.100 KΩ	*Range: 0.100 to 65.535 kΩ in steps of 0.001*
MESSAGE	▲	ZERO SEQ CAPACITIVE REACTANCE: 0.100 KΩ	*Range: 0.100 to 65.535 kΩ in steps of 0.001*

- **CHARGING CURRENT COMPENSATN**: This setting enables/disables the charging current calculations and corrections of the mixed current used as an operating quantity for fault detectors and square pulses. The voltage signals used for charging current compensation are taken from source 3 or 4 assigned with the three-phase voltage bank on

the L5 voltage bank. As such, it's critical to ensure that three-phase line voltage is assigned to this source and voltage bank settings are entered correctly. Half (or one-third for the three-terminal line, as defined by the **87PC SCHEME SELECT** setting) of the line charging current is subtracted from the line current. The following diagram shows possible configurations.

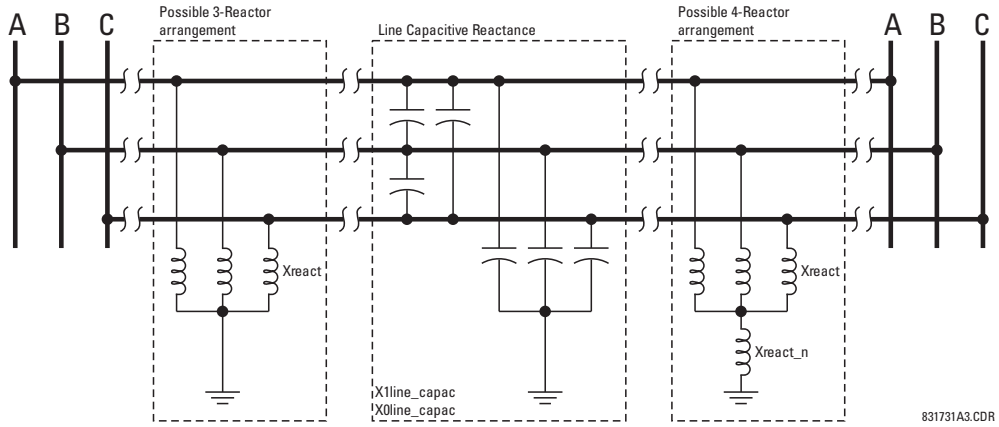


Figure 5–45: CHARGING CURRENT COMPENSATION CONFIGURATIONS

- **CHARGE COMPENST BLOCK**: This setting selects an input to block charging current compensation. This input is typically the VT fuse fail element of the source, where the three-phase VT is configured with this setting to block compensation. Blocking charging current compensation at one end of the line does not block charging current compensation on the other end. However, even with compensation operating at one end ½ (or 1/3) of the charging current is still removed from the net phase comparison current. Alternatively, the customer may choose to switch to another setting group with more conservative phase comparison settings during a VT fuse fail condition.
- **POSITIVE and ZERO SEQUENCE CAPACITIVE REACTANCE:** The values of positive and zero sequence capacitive reactance of the protected line are required for charging current compensation calculations. The line capacitive reactance values should be entered in **primary kilo-ohms** for the total line length. Details of the charging current compensation algorithm can be found in Chapter 8: *Theory of Operation*.

  If shunt reactors are also installed on the line, the resulting value entered in the **POS SEQ CAPACITIVE REACTANCE** and **ZERO SEQ CAPACITIVE REACTANCE** settings should be calculated as follows:

  1. No shunt reactors on the line or reactor current is subtracted from the line current, forcing the L60 to measure the uncompensated by shunt reactors load/fault current plus the full charging current.

$$X_{C1} = X_{1\text{line\_capac}} \quad , X_{C0} = X_{0\text{line\_capac}} \qquad \textbf{(EQ 5.7)}$$

  2. **Three-reactor arrangement:** three identical line reactors (X_{react}) solidly connected phase to ground.

$$X_{C1} = \frac{X_{1\text{line\_capac}} \cdot X_{react}}{X_{react} - X_{1\text{line\_capac}}} \quad , X_{C0} = \frac{X_{0\text{line\_capac}} \cdot X_{react}}{X_{react} - X_{0\text{line\_capac}}} \qquad \textbf{(EQ 5.8)}$$

  3. **Four-reactor arrangement:** three identical line reactors (X_{react}) wye-connected with the fourth reactor (X_{react_n}) connected between reactor-bank neutral and the ground.

$$X_{C1} = \frac{X_{1\text{line\_capac}} \cdot X_{react}}{X_{react} - X_{1\text{line\_capac}}} \quad , X_{C0} = \frac{X_{0\text{line\_capac}} \cdot (X_{react} + 3X_{react\_n})}{X_{react} + 3X_{react\_n} - X_{0\text{line\_capac}}} \qquad \textbf{(EQ 5.9)}$$

  $X_{1\text{line\_capac}}$ = the total line positive-sequence capacitive reactance
  $X_{0\text{line\_capac}}$ = the total line zero-sequence capacitive reactance
  X_{react} = the total reactor inductive reactance per phase. If identical reactors are installed at both ends of the line, the inductive reactance is divided by 2 (or 3 for a three-terminal line) before inserting in the above equations. If the reactors installed at both ends of the line are different, the following equations apply:

  1. For a two-terminal line: $X_{react} = 1 \Big/ \left(\frac{1}{X_{react\_terminal1}} + \frac{1}{X_{react\_terminal2}} \right)$

2. **For a three-terminal line:** $X_{react} = 1 \Big/ \left(\frac{1}{X_{react\_terminal1}} + \frac{1}{X_{react\_terminal2}} + \frac{1}{X_{react\_terminal3}} \right)$

X_{react_n} = the total neutral reactor inductive reactance. If identical reactors are installed at both ends of the line, the inductive reactance is divided by 2 (or 3 for a three-terminal line) before inserting in the above equations. If the reactors installed at both ends of the line are different, the following equations apply:

1. **For a two-terminal line:** $X_{react\_n} = 1 \Big/ \left(\frac{1}{X_{react\_n\_terminal1}} + \frac{1}{X_{react\_n\_terminal2}} \right)$
2. **For a three-terminal line:** $X_{react\_n} = 1 \Big/ \left(\frac{1}{X_{react\_n\_terminal1}} + \frac{1}{X_{react\_\_n\_terminal2}} + \frac{1}{X_{react\_n\_terminal3}} \right)$

NOTE

Charging current compensation calculations should be performed for an arrangement where the VTs are connected to the line side of the circuit; otherwise, opening the breaker at one end of the line will cause a calculation error. The calculated charging current per line terminal is recorded in oscillography per each phase.

h) OPEN BREAKER ECHO

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ PHASE COMPARISON ELEMENTS ⇨⇩ OPEN BREAKER ECHO

■ OPEN BREAKER ■ ECHO		OPEN BREAKER KEYING: Disabled	*Range: Disabled, Enabled*
	MESSAGE	BRK 1 AUX CONTACT: Off	*Range: FlexLogic™ operand*
	MESSAGE	BRK 1 CONT SUPV: Off	*Range: FlexLogic™ operand*
	MESSAGE	BRK 2 AUX CONTACT: Off	*Range: FlexLogic™ operand*
	MESSAGE	BRK 2 CONT SUPV: Off	*Range: FlexLogic™ operand*
	MESSAGE	OPEN BREAKER KEYING PKP DELAY: 0.000 s	*Range: 0.000 to 50.000 s in steps of 0.001*
	MESSAGE	OPEN BREAKER KEYING RST DELAY: 0.000 s	*Range: 0.000 to 50.000 s in steps of 0.001*
	MESSAGE	WEAK-INFEED KEYING: Off	*Range: FlexLogic™ operand*
	MESSAGE	WEAK-INFEED SUPV: Off	*Range: FlexLogic™ operand*
	MESSAGE	WEAK-INFEED PICKUP DELAY: 0.000 s	*Range: 0.000 to 50.000 s in steps of 0.001*
	MESSAGE	WEAK-INFEED RESET DELAY: 0.035 s	*Range: 0.000 to 50.000 s in steps of 0.001*

As operation of the permissive tripping mode of phase comparison protection and tripping of the line is fundamentally dependent on transmitting the signal to the remote end of the line, some cases of system operating conditions require attention:

1. If a line is open at one end, the phase comparison element is unable to detect an internal fault and give trip permission to the remote terminal relay.
2. A weak-infeed or no fault infeed at one end of the faulted line may prevent phase comparison element trip. Consequently, instant conversion from weak-infeed logic with sending permissive continuous signal to fault logic with sending square waves is required in case of the external fault at the adjacent or internal fault for proper operation of phase comparison relay at the remote line's terminal.

The open breaker echo element should be applied to any particular application according to local system conditions. The element settings are described below:

- **OPEN BREAKER KEYING**: Disables/enables the open breaker keying feature.
- **BRK 1 AUX CONTACT**: Assigns a FlexLogic™ operand to control open/close state of breaker 1 with either 52a or 52b type contact to create logic "1" when the breaker is open.
- **BRK 1 CONT SUPV**: Selects a supervising element such as a test/normal switch usually used in breaker 1 control schemes or any other elements. If no element is required, the default value "Off" should be used.
- **BRK 2 AUX CONTACT**: If supervision of two breakers is required, this setting is used to assign a FlexLogic™ operand to control open/close state of the Breaker #2 with either 52a or 52b type contact to create logic "1" when the breaker is open.
- **BRK 2 CONT SUPV**: Selects a supervising element such as a test/normal switch usually used in breaker 2 control schemes or any other elements. If no element is required, the default value "Off" should be used.
- **OPEN BREAKER KEYING PKP DELAY**: Delays the operation of open breaker keying to override disagreement between main and auxiliary contacts of the breaker or any other operating conditions.
- **OPEN BREAKER KEYING RST DELAY**: Delays the reset of open breaker keying to override disagreement between main and auxiliary contacts of the breaker or any other operating conditions.
- **WEAK-INFEED KEYING**: This setting assigns a sensitive phase-current element for weak-infeed keying control. It should be normally picked up with a minimum line load current. An instantaneous overcurrent element or a group of overcurrent elements are suitable for this purpose.
- **WEAK-INFEED SUPV**: This setting selects a weak-infeed supervising element from FlexLogic™ operands. An under-voltage element, auxiliary contacts of breakers indicating close position, or other elements can be useful for no-current supervision.
- **WEAK-INFEED PICKUP DELAY**: This setting delays operation of weak-infeed keying during some transient conditions (such as breaker reclosure, etc.).
- **WEAK-INFEED RESET DELAY**: The weak-infeed keying function incorporates a default 35 ms reset delay to assure reset coordination with the FDH trip-level fault detector at the remote terminal during fault clearing. The default reset time can be changed according to local conditions.

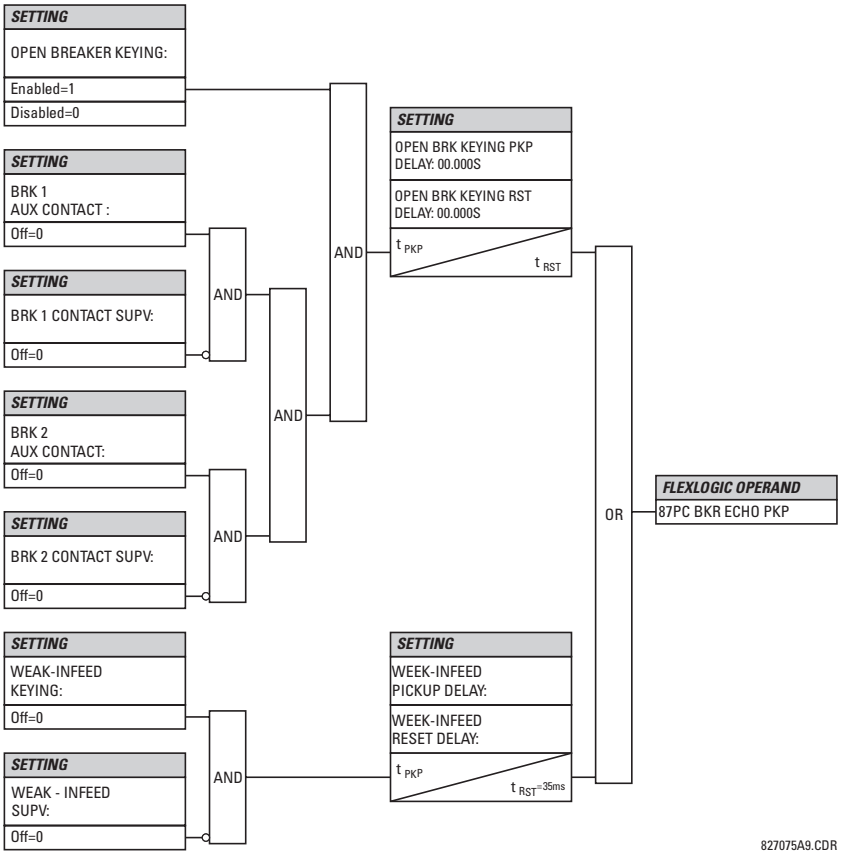
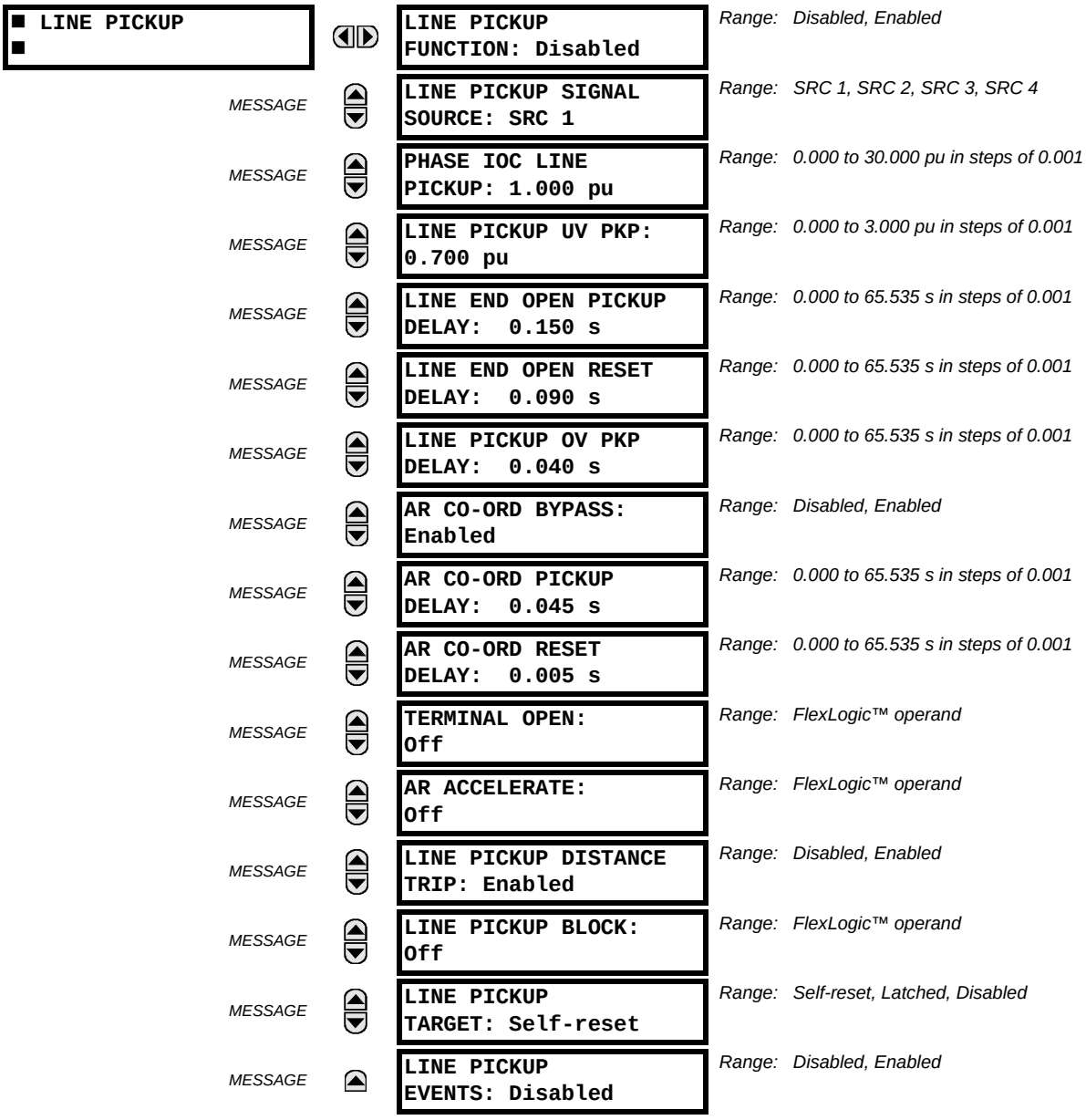


Figure 5–46: OPEN BREAKER ECHO SCHEME LOGIC

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ LINE PICKUP



The line pickup feature uses a combination of undercurrent and undervoltage to identify a line that has been de-energized (line end open). Alternately, the user may assign a FlexLogic™ operand to the **TERMINAL OPEN** setting that specifies the terminal status. Three instantaneous overcurrent elements are used to identify a previously de-energized line that has been closed onto a fault. Faults other than close-in faults can be identified satisfactorily with the distance elements.

Co-ordination features are included to ensure satisfactory operation when high speed 'automatic reclosure (AR)' is employed. The **AR CO-ORD DELAY** setting allows the overcurrent setting to be below the expected load current seen after reclose. Co-ordination is achieved by all of the **LINE PICKP UV** elements resetting and blocking the trip path before the **AR CO-ORD DELAY** times out. The **AR CO-ORD BYPASS** setting is normally enabled. It is disabled if high speed autoreclosure is implemented.

The line pickup protection incorporates zone 1 extension capability. When the line is being re-energized from the local terminal, pickup of an overreaching zone 2 or excessive phase current within eight power cycles after the autorecloser issues a close command results in the LINE PICKUP RCL TRIP FlexLogic™ operand. For security, the overcurrent trip is supervised

by an undervoltage condition, which in turn is controlled by the VT FUSE FAIL OP operand with a 10 ms coordination timer. If a trip from distance in not required, then it can be disabled with the **LINE PICKUP DISTANCE TRIP** setting. Configure the LINE PICKUP RCL TRIP operand to perform a trip action if the intent is apply zone 1 extension.

The zone 1 extension philosophy used here normally operates from an under-reaching zone, and uses an overreaching distance zone when reclosing the line with the other line end open. The **AR ACCELERATE** setting is provided to achieve zone 1 extension functionality if external autoreclosure is employed. Another zone 1 extension approach is to permanently apply an overreaching zone, and reduce the reach when reclosing. This philosophy can be programmed via the autoreclose scheme.

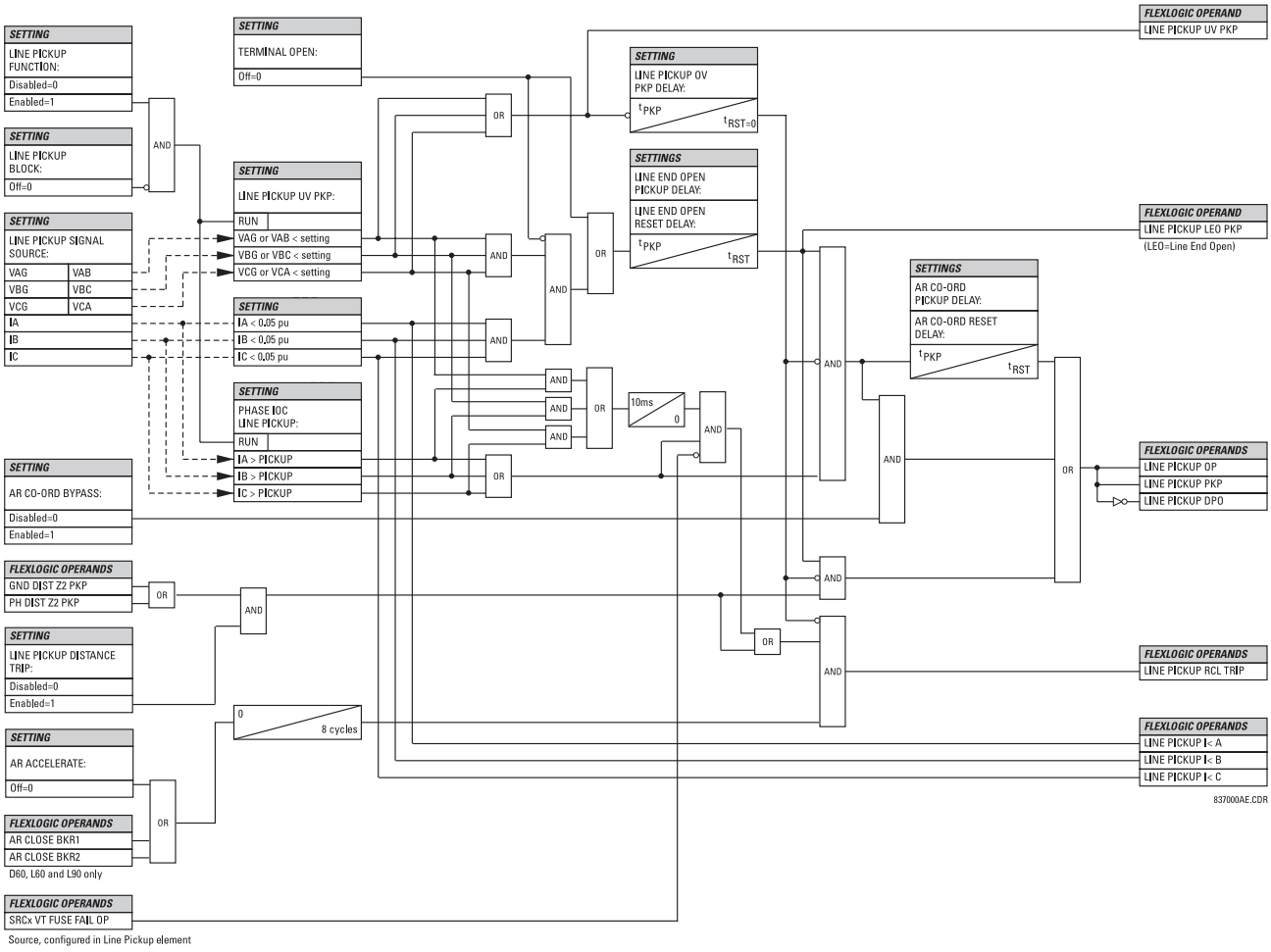
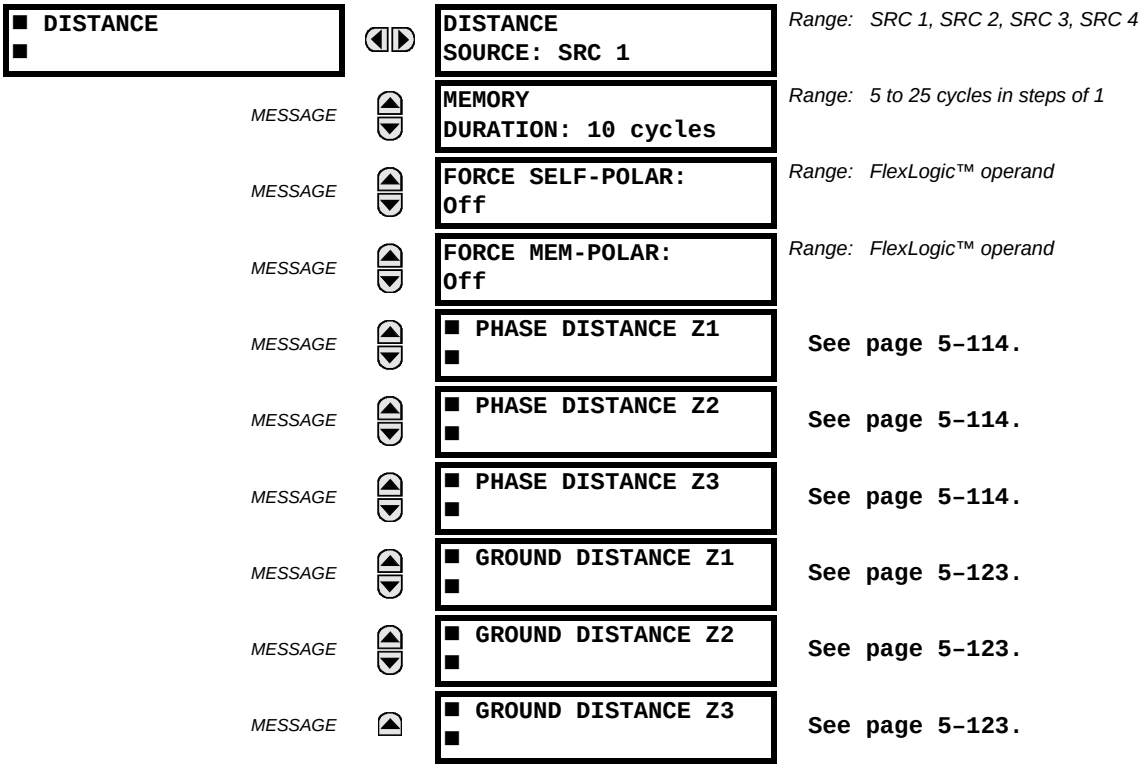


Figure 5–47: LINE PICKUP SCHEME LOGIC

a) MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE



Four common settings are available for distance protection. The **DISTANCE SOURCE** identifies the signal source for all distance functions. The mho distance functions use a dynamic characteristic: the positive-sequence voltage – either memorized or actual – is used as a polarizing signal. The memory voltage is also used by the built-in directional supervising functions applied for both the mho and quad characteristics.

The **MEMORY DURATION** setting specifies the length of time a memorized positive-sequence voltage should be used in the distance calculations. After this interval expires, the relay checks the magnitude of the actual positive-sequence voltage. If it is higher than 10% of the nominal, the actual voltage is used, if lower – the memory voltage continues to be used.

The memory is established when the positive-sequence voltage stays above 80% of its nominal value for five power system cycles. For this reason it is important to ensure that the nominal secondary voltage of the VT is entered correctly under the SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨⇩ VOLTAGE BANK menu.

Set **MEMORY DURATION** long enough to ensure stability on close-in reverse three-phase faults. For this purpose, the maximum fault clearing time (breaker fail time) in the substation should be considered. On the other hand, the **MEMORY DURATION** cannot be too long as the power system may experience power swing conditions rotating the voltage and current phasors slowly while the memory voltage is static, as frozen at the beginning of the fault. Keeping the memory in effect for too long may eventually lead to incorrect operation of the distance functions.

The distance zones can be forced to become self-polarized through the **FORCE SELF-POLAR** setting. Any user-selected condition (FlexLogic™ operand) can be configured to force self-polarization. When the selected operand is asserted (logic 1), the distance functions become self-polarized regardless of other memory voltage logic conditions. When the selected operand is de-asserted (logic 0), the distance functions follow other conditions of the memory voltage logic as shown below.

The distance zones can be forced to become memory-polarized through the **FORCE MEM-POLAR** setting. Any user-selected condition (any FlexLogic™ operand) can be configured to force memory polarization. When the selected operand is asserted (logic 1), the distance functions become memory-polarized regardless of the positive-sequence voltage magnitude at this time. When the selected operand is de-asserted (logic 0), the distance functions follow other conditions of the memory voltage logic.

The **FORCE SELF-POLAR** and **FORCE MEM-POLAR** settings should never be asserted simultaneously. If this happens, the logic will give higher priority to forcing self-polarization as indicated in the logic below. This is consistent with the overall philosophy of distance memory polarization.

NOTE

The memory polarization cannot be applied permanently but for a limited time only; the self-polarization may be applied permanently and therefore should take higher priority.

NOTE

The distance zones of the L60 are identical to that of the UR-series D60 Line Distance Relay. For additional information on the L60 distance functions, please refer to Chapter 8 of the D60 manual, available on the GE EnerVista CD or free of charge on the GE Multilin web page.

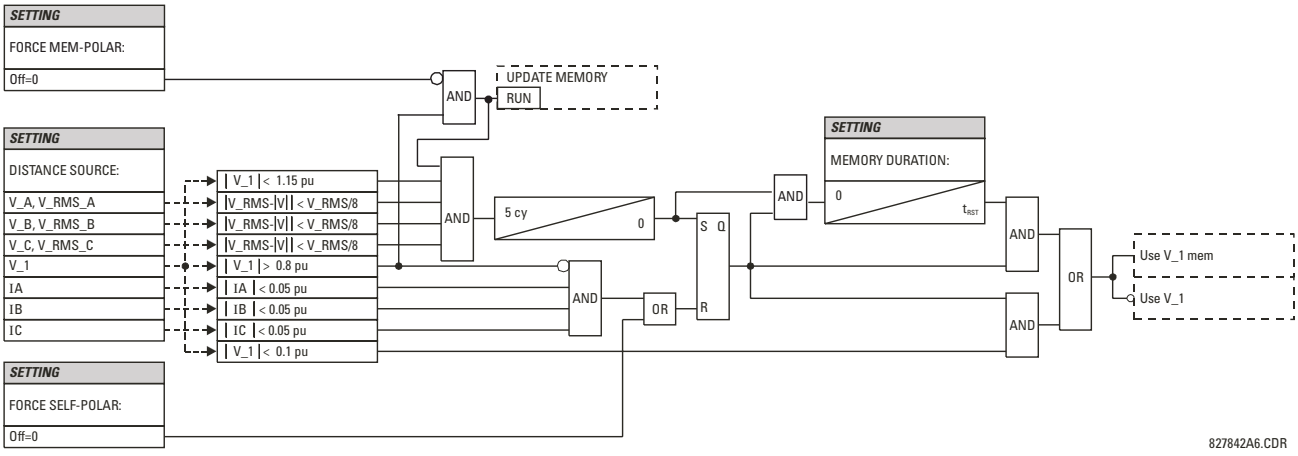
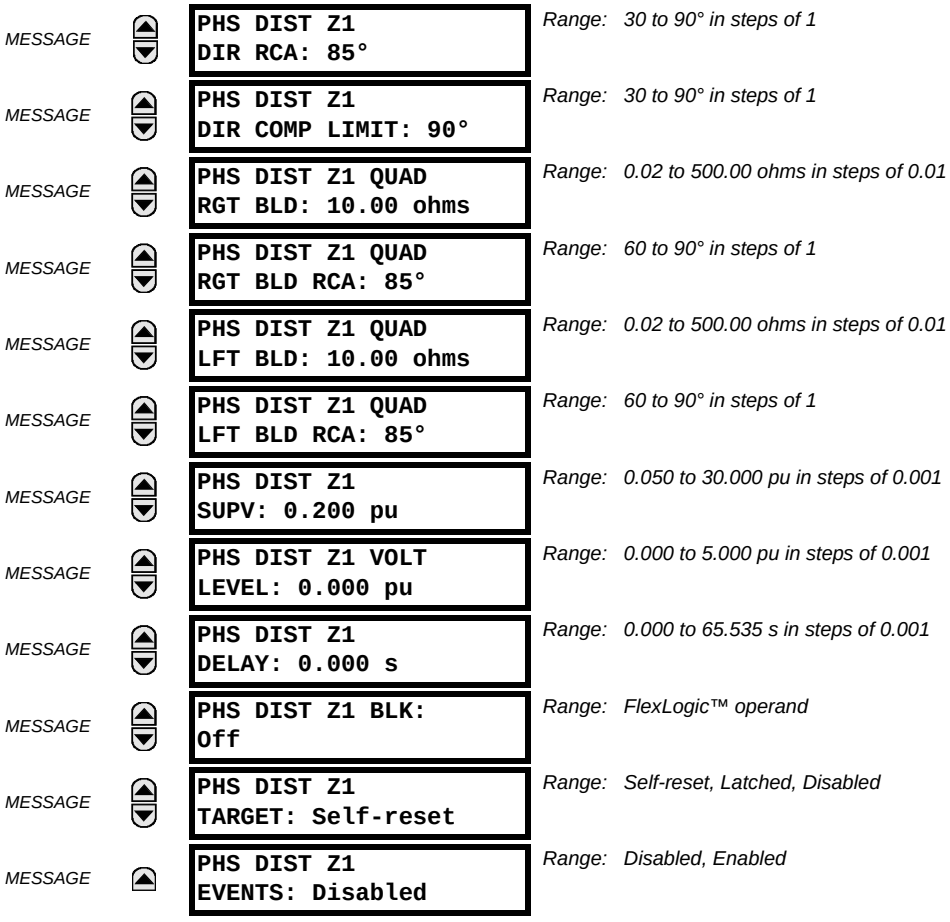


Figure 5–48: MEMORY VOLTAGE LOGIC

b) PHASE DISTANCE

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE ⇨⇩ PHASE DISTANCE Z1(Z3)

■ PHASE DISTANCE Z1 ■		PHS DIST Z1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	PHS DIST Z1 DIR: Forward	*Range: Forward, Reverse, Non-directional*
	MESSAGE	PHS DIST Z1 SHAPE: Mho	*Range: Mho, Quad*
	MESSAGE	PHS DIST Z1 XFMR VOL CONNECTION: None	*Range: None, Dy1, Dy3, Dy5, Dy7, Dy9, Dy11, Yd1, Yd3, Yd5, Yd7, Yd9, Yd11*
	MESSAGE	PHS DIST Z1 XFMR CUR CONNECTION: None	*Range: None, Dy1, Dy3, Dy5, Dy7, Dy9, Dy11, Yd1, Yd3, Yd5, Yd7, Yd9, Yd11*
	MESSAGE	PHS DIST Z1 REACH: 2.00 ohms	*Range: 0.02 to 500.00 ohms in steps of 0.01*
	MESSAGE	PHS DIST Z1 RCA: 85°	*Range: 30 to 90° in steps of 1*
	MESSAGE	PHS DIST Z1 REV REACH: 2.00 ohms	*Range: 0.02 to 500.00 ohms in steps of 0.01*
	MESSAGE	PHS DIST Z1 REV REACH RCA: 85°	*Range: 30 to 90° in steps of 1*
	MESSAGE	PHS DIST Z1 COMP LIMIT: 90°	*Range: 30 to 90° in steps of 1*



The phase mho distance function uses a dynamic 100% memory-polarized mho characteristic with additional reactance, directional, and overcurrent supervising characteristics. When set to “Non-directional”, the mho function becomes an offset mho with the reverse reach controlled independently from the forward reach, and all the directional characteristics removed.

The phase quadrilateral distance function is comprised of a reactance characteristic, right and left blinders, and 100% memory-polarized directional and current supervising characteristics. When set to “Non-directional”, the quadrilateral function applies a reactance line in the reverse direction instead of the directional comparators. Refer to Chapter 8 for additional information.

Each phase distance zone is configured individually through its own setting menu. All of the settings can be independently modified for each of the zones except:

1. The **SIGNAL SOURCE** setting (common for the distance elements of all zones as entered under **SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE**).
2. The **MEMORY DURATION** setting (common for the distance elements of all zones as entered under **SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE**).

The common distance settings described earlier must be properly chosen for correct operation of the phase distance elements. Additional details may be found in Chapter 8: *Theory of Operation*.

Although all zones can be used as either instantaneous elements (pickup [PKP] and dropout [DPO] FlexLogic™ operands) or time-delayed elements (operate [OP] FlexLogic™ operands), only zone 1 is intended for the instantaneous under-reaching tripping mode.

WARNING

Ensure that the PHASE VT SECONDARY VOLTAGE setting (see the SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨⇩ VOLTAGE BANK menu) is set correctly to prevent improper operation of associated memory action.

- **PHS DIST Z1 DIR:** All phase distance zones are reversible. The forward direction is defined by the **PHS DIST Z1 RCA** setting, whereas the reverse direction is shifted 180° from that angle. The non-directional zone spans between the forward reach impedance defined by the **PHS DIST Z1 REACH** and **PHS DIST Z1 RCA** settings, and the reverse reach impedance defined by **PHS DIST Z1 REV REACH** and **PHS DIST Z1 REV REACH RCA** as illustrated below.
- **PHS DIST Z1 SHAPE:** This setting selects the shape of the phase distance function between the mho and quadrilateral characteristics. The selection is available on a per-zone basis. The two characteristics and their possible variations are shown in the following figures.

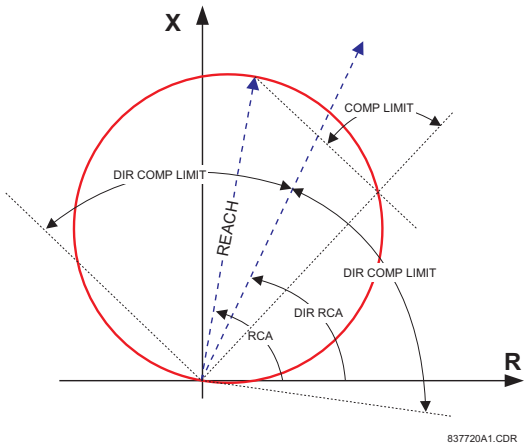


Figure 5–49: DIRECTIONAL MHO DISTANCE CHARACTERISTIC

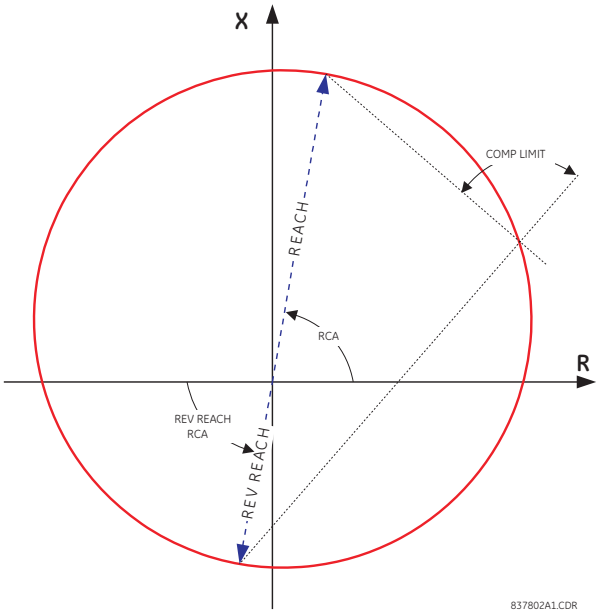


Figure 5–50: NON-DIRECTIONAL MHO DISTANCE CHARACTERISTIC

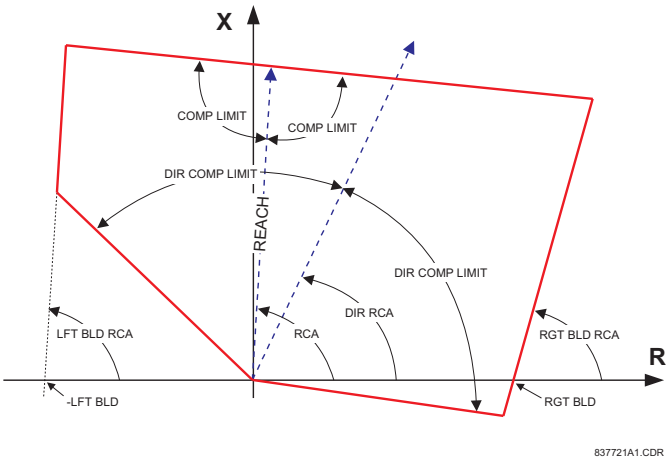


Figure 5–51: DIRECTIONAL QUADRILATERAL PHASE DISTANCE CHARACTERISTIC

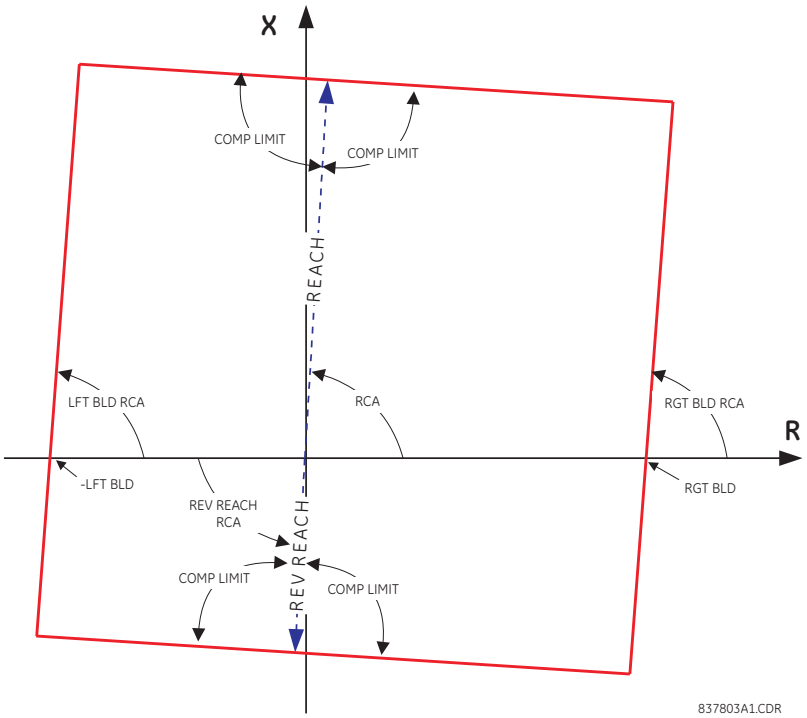


Figure 5–52: NON-DIRECTIONAL QUADRILATERAL PHASE DISTANCE CHARACTERISTIC

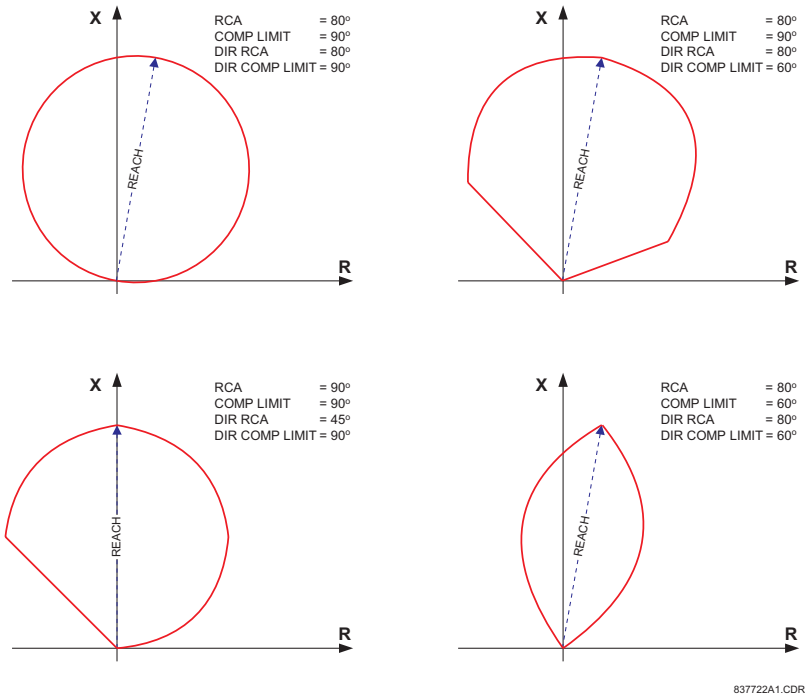


Figure 5–53: MHO DISTANCE CHARACTERISTIC SAMPLE SHAPES

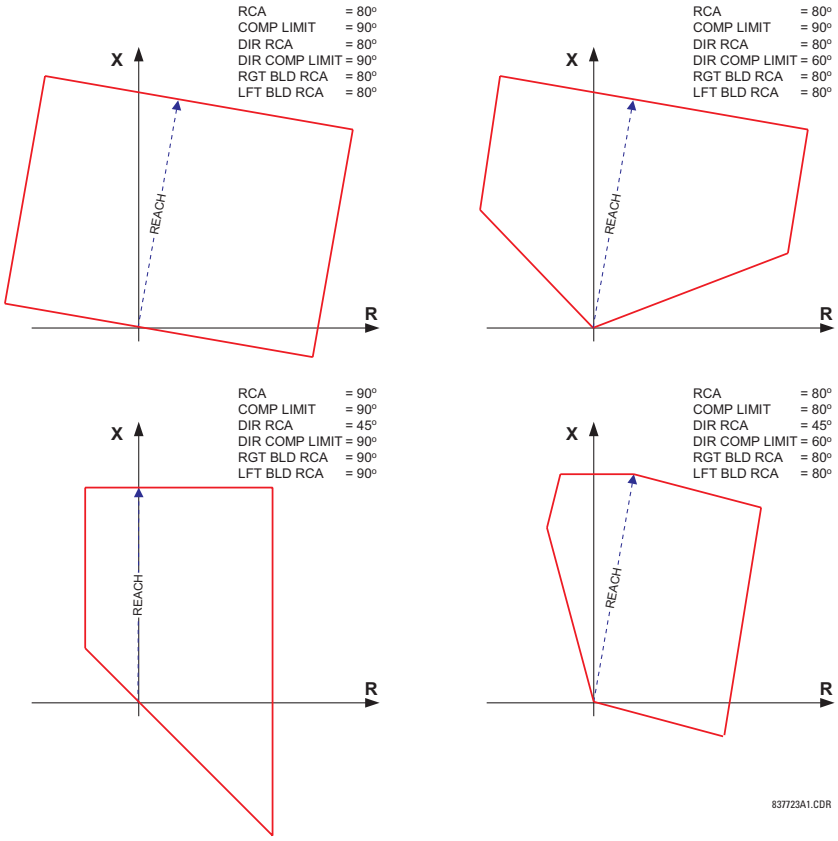


Figure 5–54: QUADRILATERAL DISTANCE CHARACTERISTIC SAMPLE SHAPES

- **PHS DIST Z1 XFMR VOL CONNECTION:** The phase distance elements can be applied to look through a three-phase delta-wye or wye-delta power transformer. In addition, VTs and CTs could be located independently from one another at different windings of the transformer. If the potential source is located at the correct side of the transformer, this setting shall be set to “None”.

  This setting specifies the location of the voltage source with respect to the involved power transformer in the direction of the zone. The following figure illustrates the usage of this setting. In section (a), Zone 1 is looking through a transformer from the delta into the wye winding. Therefore, the Z1 setting shall be set to “Dy11”. In section (b), Zone 3 is looking through a transformer from the wye into the delta winding. Therefore, the Z3 setting shall be set to “Yd1”. The zone is restricted by the potential point (location of the VTs) as illustrated in Figure (e).

- **PHS DIST Z1 XFMR CUR CONNECTION:** This setting specifies the location of the current source with respect to the involved power transformer in the direction of the zone. In section (a) of the following figure, Zone 1 is looking through a transformer from the delta into the wye winding. Therefore, the Z1 setting shall be set to “Dy11”. In section (b), the CTs are located at the same side as the read point. Therefore, the Z3 setting shall be set to “None”.

  See the *Theory of Operation* chapter for more details, and the *Application of Settings* chapter for information on calculating distance reach settings in applications involving power transformers.

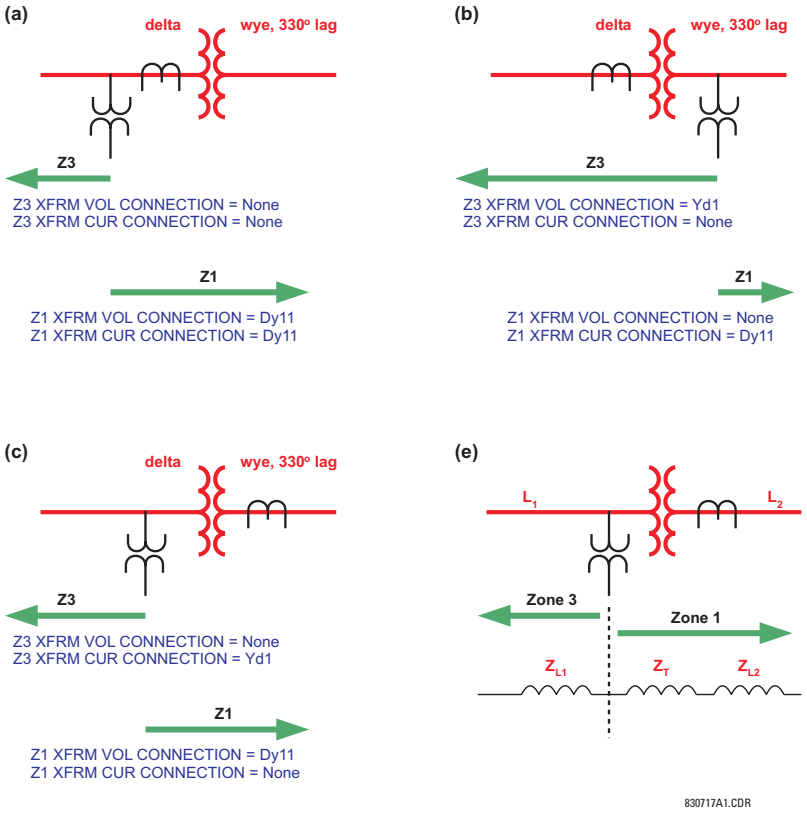


Figure 5–55: APPLICATIONS OF THE PH DIST XFMR VOL/CUR CONNECTION SETTINGS

- **PHS DIST Z1 REACH:** This setting defines the zone reach for the forward and reverse applications. In the non-directional applications, this setting defines the forward reach of the zone. The reverse reach impedance in non-directional applications is set independently. The reach impedance is entered in secondary ohms. The reach impedance angle is entered as the **PHS DIST Z1 RCA** setting.

- **PHS DIST Z1 RCA:** This setting specifies the characteristic angle (similar to the ‘maximum torque angle’ in previous technologies) of the phase distance characteristic for the forward and reverse applications. In the non-directional applications, this setting defines the angle of the forward reach impedance. The reverse reach impedance in the non-directional applications is set independently. The setting is an angle of reach impedance as shown in the distance characteristic figures shown earlier. This setting is independent from **PHS DIST Z1 DIR RCA**, the characteristic angle of an extra directional supervising function.

- **PHS DIST Z1 REV REACH**: This setting defines the reverse reach of the zone set to non-directional (**PHS DIST Z1 DIR** setting). The value must be entered in secondary ohms. This setting does not apply when the zone direction is set to "Forward" or "Reverse".
- **PHS DIST Z1 REV REACH RCA**: This setting defines the angle of the reverse reach impedance if the zone is set to non-directional (**PHS DIST Z1 DIR** setting). This setting does not apply when the zone direction is set to "Forward" or "Reverse".
- **PHS DIST Z1 COMP LIMIT:** This setting shapes the operating characteristic. In particular, it produces the lens-type characteristic of the mho function and a tent-shaped characteristic of the reactance boundary of the quadrilateral function. If the mho shape is selected, the same limit angle applies to both the mho and supervising reactance comparators. In conjunction with the mho shape selection, the setting improves loadability of the protected line. In conjunction with the quadrilateral characteristic, this setting improves security for faults close to the reach point by adjusting the reactance boundary into a tent-shape.
- **PHS DIST Z1 DIR RCA:** This setting selects the characteristic angle (or maximum torque angle) of the directional supervising function. If the mho shape is applied, the directional function is an extra supervising function as the dynamic mho characteristic is itself directional. In conjunction with the quadrilateral shape, this setting defines the only directional function built into the phase distance element. The directional function uses the memory voltage for polarization. This setting typically equals the distance characteristic angle **PHS DIST Z1 RCA**.
- **PHS DIST Z1 DIR COMP LIMIT:** Selects the comparator limit angle for the directional supervising function.
- **PHS DIST Z1 QUAD RGT BLD:** This setting defines the right blinder position of the quadrilateral characteristic along the resistive axis of the impedance plane (see the *Quadrilateral Distance Characteristic* figures). The angular position of the blinder is adjustable with the use of the **PHS DIST Z1 QUAD RGT BLD RCA** setting. This setting applies only to the quadrilateral characteristic and should be set giving consideration to the maximum load current and required resistive coverage.
- **PHS DIST Z1 QUAD RGT BLD RCA:** This setting defines the angular position of the right blinder of the quadrilateral characteristic (see the *Quadrilateral Distance Characteristic* figures).
- **PHS DIST Z1 QUAD LFT BLD:** This setting defines the left blinder position of the quadrilateral characteristic along the resistive axis of the impedance plane (see the Quadrilateral Distance Characteristic figure). The angular position of the blinder is adjustable with the use of the **PHS DIST Z1 QUAD LFT BLD RCA** setting. This setting applies only to the quadrilateral characteristic and should be set with consideration to the maximum load current.
- **PHS DIST Z1 QUAD LFT BLD RCA:** This setting defines the angular position of the left blinder of the quadrilateral characteristic (see the *Quadrilateral Distance Characteristic* figures).
- **PHS DIST Z1 SUPV:** The phase distance elements are supervised by the magnitude of the line-to-line current (fault loop current used for the distance calculations). For convenience, $\sqrt{3}$ is accommodated by the pickup (i.e., before being used, the entered value of the threshold setting is multiplied by $\sqrt{3}$).

  If the minimum fault current level is sufficient, the current supervision pickup should be set above maximum full load current preventing maloperation under VT fuse fail conditions. This requirement may be difficult to meet for remote faults at the end of Zones 2 through 3. If this is the case, the current supervision pickup would be set below the full load current, but this may result in maloperation during fuse fail conditions.
- **PHS DIST Z1 VOLT LEVEL:** This setting is relevant for applications on series-compensated lines, or in general, if series capacitors are located between the relaying point and a point where the zone shall not overreach. For plain (non-compensated) lines, set to zero. Otherwise, the setting is entered in per unit of the phase VT bank configured under the **DISTANCE SOURCE**. Effectively, this setting facilitates dynamic current-based reach reduction. In non-directional applications (**PHS DIST Z1 DIR** set to "Non-directional"), this setting applies only to the forward reach of the non-directional zone. See Chapters 8 and 9 for information on calculating this setting for series compensated lines.
- **PHS DIST Z1 DELAY:** This setting allows the user to delay operation of the distance elements and implement stepped distance protection. The distance element timers for Zones 2 through 3 apply a short dropout delay to cope with faults located close to the zone boundary when small oscillations in the voltages and/or currents could inadvertently reset the timer. Zone 1 does not need any drop out delay since it is sealed-in by the presence of current.
- **PHS DIST Z1 BLK:** This setting enables the user to select a FlexLogic™ operand to block a given distance element. VT fuse fail detection is one of the applications for this setting.

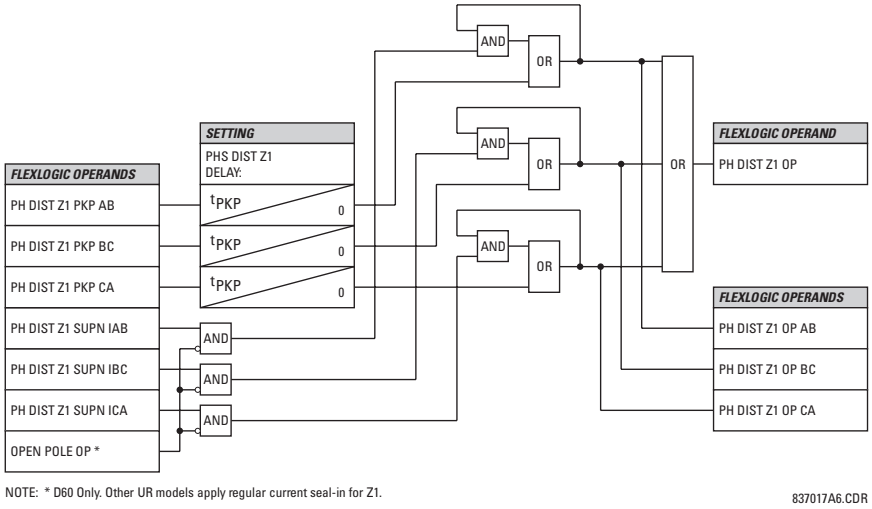


Figure 5–56: PHASE DISTANCE ZONE 1 OP SCHEME

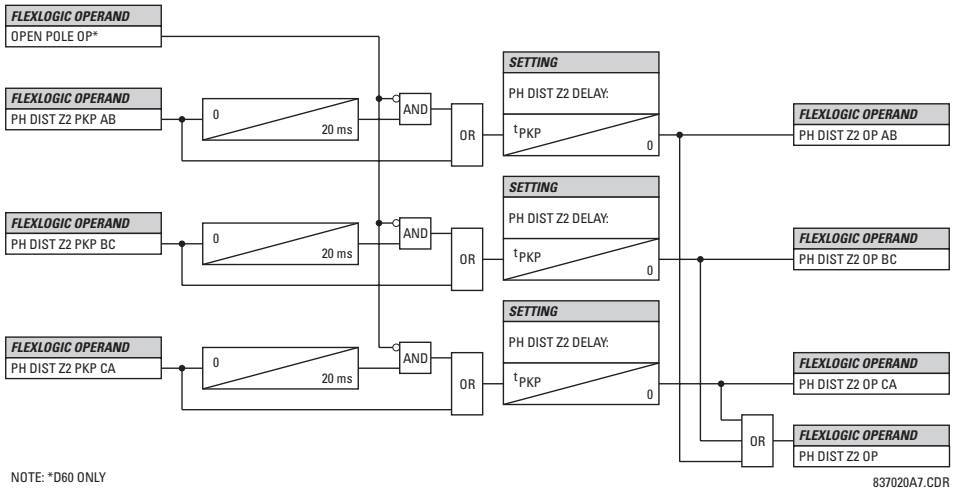


Figure 5–57: PHASE DISTANCE ZONE 2 TO ZONE 3 OP SCHEME

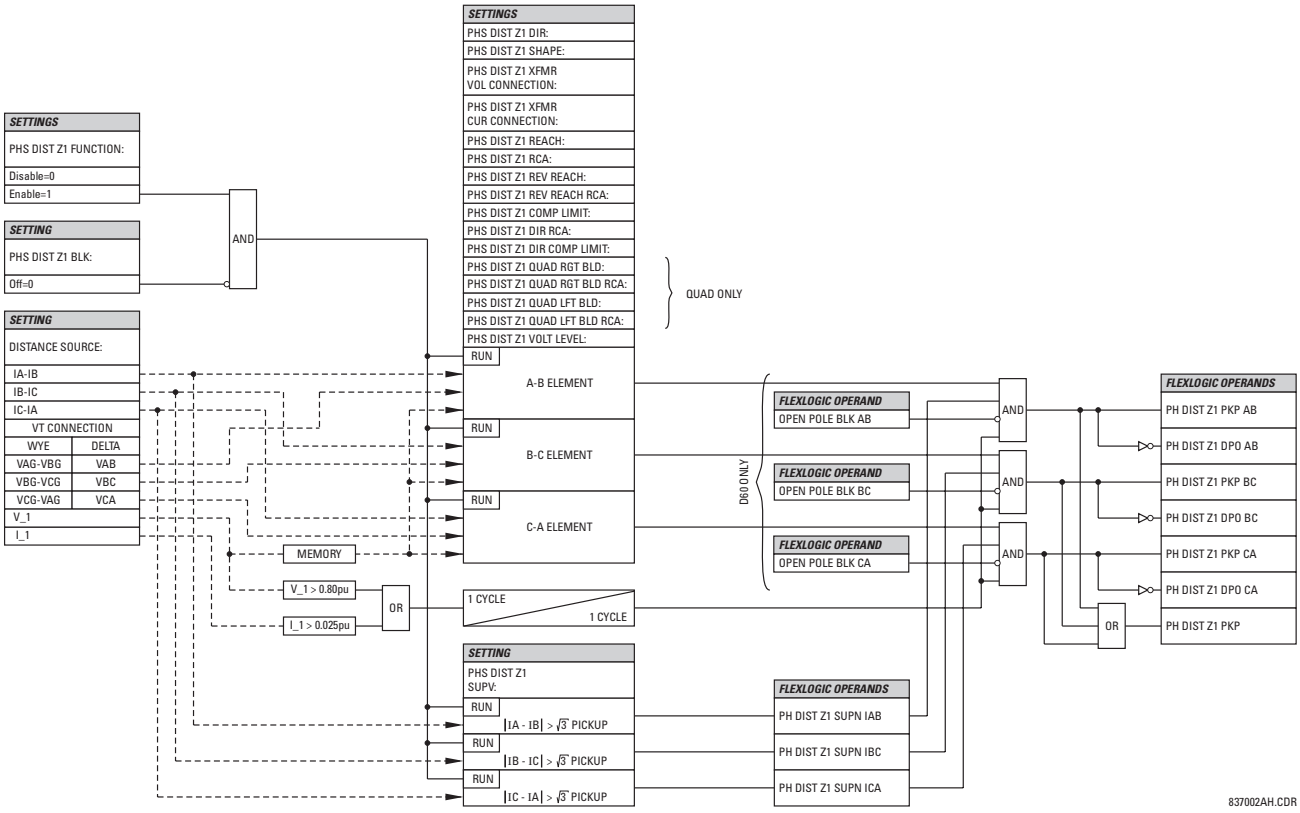
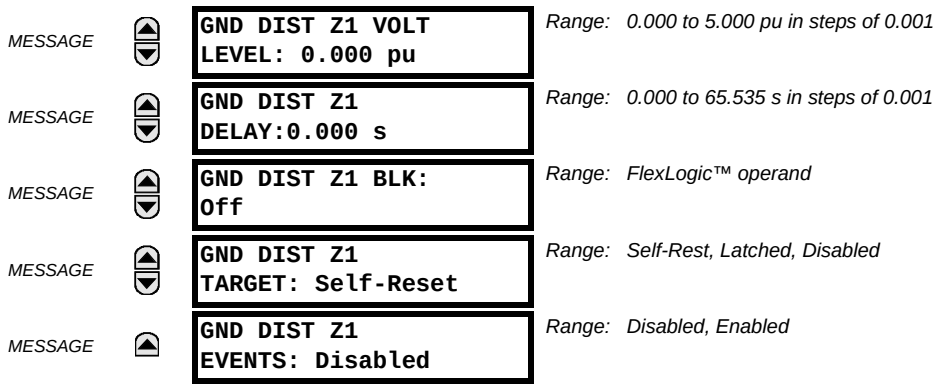


Figure 5–58: PHASE DISTANCE ZONE 1 TO ZONE 3 SCHEME LOGIC

c) GROUND DISTANCE

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE ⇨⇩ GROUND DISTANCE Z1(Z3)

■ GROUND DISTANCE Z1 ■		GND DIST Z1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	GND DIST Z1 DIR: Forward	Range: Forward, Reverse, Non-directional
	MESSAGE	GND DIST Z1 SHAPE: Mho	Range: Mho, Quad
	MESSAGE	GND DIST Z1 Z0/Z1 MAG: 2.70	Range: 0.00 to 10.00 in steps of 0.01
	MESSAGE	GND DIST Z1 Z0/Z1 ANG: 0°	Range: –90 to 90° in steps of 1
	MESSAGE	GND DIST Z1 ZOM/Z1 MAG: 0.00	Range: 0.00 to 7.00 in steps of 0.01
	MESSAGE	GND DIST Z1 ZOM/Z1 ANG: 0°	Range: –90 to 90° in steps of 1
	MESSAGE	GND DIST Z1 REACH: 2.00 Ω	Range: 0.02 to 500.00 Ω in steps of 0.01
	MESSAGE	GND DIST Z1 RCA: 85°	Range: 30 to 90° in steps of 1
	MESSAGE	GND DIST Z1 REV REACH: 2.00 Ω	Range: 0.02 to 500.00 Ω in steps of 0.01
	MESSAGE	GND DIST Z1 REV REACH RCA: 85°	Range: 30 to 90° in steps of 1
	MESSAGE	GND DIST Z1 POL CURRENT: Zero-seq	Range: Zero-seq, Neg-seq
	MESSAGE	GND DIST Z1 NON-HOMOGEN ANG: 0.0°	Range: –40.0 to 40.0° in steps of 0.1
	MESSAGE	GND DIST Z1 COMP LIMIT: 90°	Range: 30 to 90° in steps of 1
	MESSAGE	GND DIST Z1 DIR RCA: 85°	Range: 30 to 90° in steps of 1
	MESSAGE	GND DIST Z1 DIR COMP LIMIT: 90°	Range: 30 to 90° in steps of 1
	MESSAGE	GND DIST Z1 QUAD RGT BLD: 10.00 Ω	Range: 0.02 to 500.00 Ω in steps of 0.01
	MESSAGE	GND DIST Z1 QUAD RGT BLD RCA: 85°	Range: 60 to 90° in steps of 1
	MESSAGE	GND DIST Z1 QUAD LFT BLD: 10.00 Ω	Range: 0.02 to 500.00 Ω in steps of 0.01
	MESSAGE	GND DIST Z1 QUAD LFT BLD RCA: 85°	Range: 60 to 90° in steps of 1
	MESSAGE	GND DIST Z1 SUPV: 0.200 pu	Range: 0.050 to 30.000 pu in steps of 0.001



The ground mho distance function uses a dynamic 100% memory-polarized mho characteristic with additional reactance, directional, current, and phase selection supervising characteristics. The ground quadrilateral distance function is composed of a reactance characteristic, right and left blinders, and 100% memory-polarized directional, overcurrent, and phase selection supervising characteristics.

When set to non-directional, the mho function becomes an offset mho with the reverse reach controlled independently from the forward reach, and all the directional characteristics removed. When set to non-directional, the quadrilateral function applies a reactance line in the reverse direction instead of the directional comparators.

The reactance supervision for the mho function uses the zero-sequence current for polarization. The reactance line of the quadrilateral function uses either zero-sequence or negative-sequence current as a polarizing quantity. The selection is controlled by a user setting and depends on the degree of non-homogeneity of the zero-sequence and negative-sequence equivalent networks.

The directional supervision uses memory voltage as polarizing quantity and both zero- and negative-sequence currents as operating quantities.

The phase selection supervision restrains the ground elements during double-line-to-ground faults as they – by principles of distance relaying – may be inaccurate in such conditions. Ground distance zones 1 through 3 apply additional zero-sequence directional supervision. See Chapter 8 for additional details.

Each ground distance zone is configured individually through its own setting menu. All of the settings can be independently modified for each of the zones except:

1. The **SIGNAL SOURCE** setting (common for both phase and ground elements for all zones as entered under the **SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE** menu).
2. The **MEMORY DURATION** setting (common for both phase and ground elements for all zones as entered under the **SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE** menu).

The common distance settings noted at the start of the Distance section must be properly chosen for correct operation of the ground distance elements.

Although all ground distance zones can be used as either instantaneous elements (pickup [PKP] and dropout [DPO] FlexLogic™ signals) or time-delayed elements (operate [OP] FlexLogic™ signals), only zone 1 is intended for the instantaneous under-reaching tripping mode.

WARNING

Ensure that the PHASE VT SECONDARY VOLTAGE (see the SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨⇩ VOLTAGE BANK menu) is set correctly to prevent improper operation of associated memory action.

- **GND DIST Z1 DIR:** All ground distance zones are reversible. The forward direction is defined by the **GND DIST Z1 RCA** setting and the reverse direction is shifted by 180° from that angle. The non-directional zone spans between the forward reach impedance defined by the **GND DIST Z1 REACH** and **GND DIST Z1 RCA** settings, and the reverse reach impedance defined by the **GND DIST Z1 REV REACH** and **GND DIST Z1 REV REACH RCA** settings.
- **GND DIST Z1 SHAPE:** This setting selects the shape of the ground distance characteristic between the mho and quadrilateral characteristics. The selection is available on a per-zone basis.

  The directional and non-directional quadrilateral ground distance characteristics are shown below. The directional and non-directional mho ground distance characteristics are the same as those shown for the phase distance element in the previous sub-section.

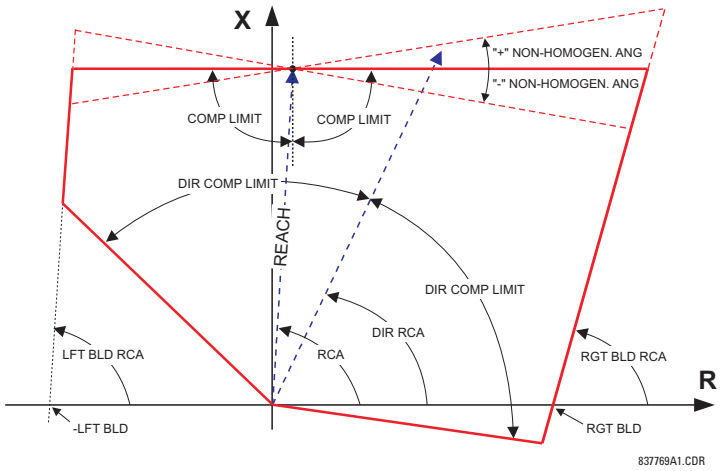


Figure 5–59: DIRECTIONAL QUADRILATERAL GROUND DISTANCE CHARACTERISTIC

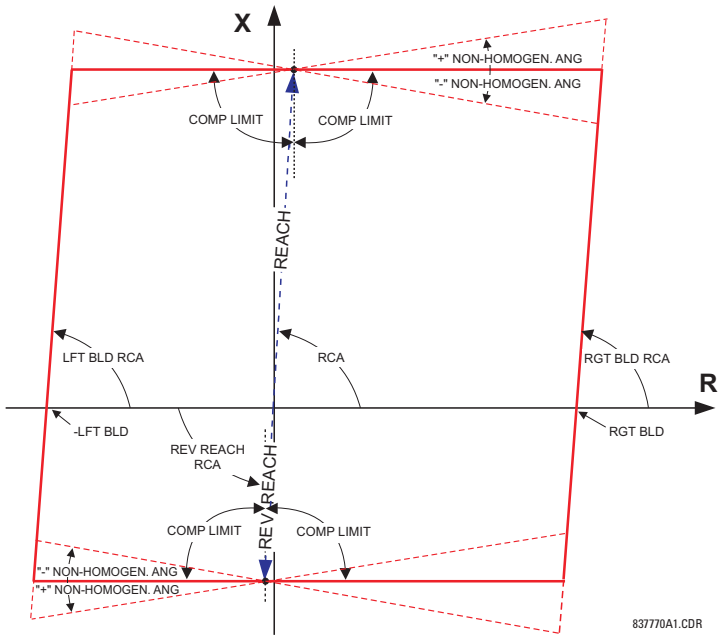


Figure 5–60: NON-DIRECTIONAL QUADRILATERAL GROUND DISTANCE CHARACTERISTIC

- **GND DIST Z1 Z0/Z1 MAG:** This setting specifies the ratio between the zero-sequence and positive-sequence impedance required for zero-sequence compensation of the ground distance elements. This setting is available on a per-zone basis, enabling precise settings for tapped, non-homogeneous, and series compensated lines.
- **GND DIST Z1 Z0/Z1 ANG:** This setting specifies the angle difference between the zero-sequence and positive-sequence impedance required for zero-sequence compensation of the ground distance elements. The entered value is the zero-sequence impedance angle minus the positive-sequence impedance angle. This setting is available on a per-zone basis, enabling precise values for tapped, non-homologous, and series-compensated lines.
- **GND DIST Z1 ZOM/Z1 MAG:** The ground distance elements can be programmed to apply compensation for the zero-sequence mutual coupling between parallel lines. If this compensation is required, the ground current from the parallel line (3I_0) measured in the direction of the zone being compensated must be connected to the ground input CT of the CT bank configured under the **DISTANCE SOURCE**. This setting specifies the ratio between the magnitudes of the mutual zero-sequence impedance between the lines and the positive-sequence impedance of the protected line. It is imperative to set this setting to zero if the compensation is not to be performed.

- **GND DIST Z1 ZOM/Z1 ANG:** This setting specifies the angle difference between the mutual zero-sequence impedance between the lines and the positive-sequence impedance of the protected line.
- **GND DIST Z1 REACH:** This setting defines the reach of the zone for the forward and reverse applications. In non-directional applications, this setting defines the forward reach of the zone. The reverse reach impedance in non-directional applications is set independently. The angle of the reach impedance is entered as the **GND DIST Z1 RCA** setting. The reach impedance is entered in secondary ohms.
- **GND DIST Z1 RCA:** This setting specifies the characteristic angle (similar to the maximum torque angle in previous technologies) of the ground distance characteristic for the forward and reverse applications. In the non-directional applications this setting defines the forward reach of the zone. The reverse reach impedance in the non-directional applications is set independently. This setting is independent from the **GND DIST Z1 DIR RCA** setting (the characteristic angle of an extra directional supervising function).

  NOTE

  The relay internally performs zero-sequence compensation for the protected circuit based on the values entered for **GND DIST Z1 Z0/Z1 MAG** and **GND DIST Z1 Z0/Z1 ANG**, and if configured to do so, zero-sequence compensation for mutual coupling based on the values entered for **GND DIST Z1 Z0M/Z1 MAG** and **GND DIST Z1 Z0M/Z1 ANG**. The **GND DIST Z1 REACH** and **GND DIST Z1 RCA** should, therefore, be entered in terms of positive sequence quantities. Refer to chapters 8 for additional information
- **GND DIST Z1 REV REACH**: This setting defines the reverse reach of the zone set to non-directional (**GND DIST Z1 DIR** setting). The value must be entered in secondary ohms. This setting does not apply when the zone direction is set to "Forward" or "Reverse".
- **GND DIST Z1 REV REACH RCA**: This setting defines the angle of the reverse reach impedance if the zone is set to non-directional (**GND DIST Z1 DIR** setting). This setting does not apply when the zone direction is set to "Forward" or "Reverse".
- **GND DIST Z1 POL CURRENT**: This setting applies only if the **GND DIST Z1 SHAPE** is set to "Quad" and controls the polarizing current used by the reactance comparator of the quadrilateral characteristic. Either the zero-sequence or negative-sequence current could be used. In general, a variety of system conditions must be examined to select an optimum polarizing current. This setting becomes less relevant when the resistive coverage and zone reach are set conservatively. Also, this setting is more relevant in lower voltage applications such as on distribution lines or cables, as compared with high-voltage transmission lines. This setting applies to both the **Z1** and reverse reactance lines if the zone is set to non-directional. Refer to chapters 8 and 9 for additional information.
- **GND DIST Z1 NON-HOMOGEN ANG**: This setting applies only if the **GND DIST Z1 SHAPE** is set to "Quad" and provides a method to correct the angle of the polarizing current of the reactance comparator for non-homogeneity of the zero-sequence or negative-sequence networks. In general, a variety of system conditions must be examined to select this setting. In many applications this angle is used to reduce the reach at high resistances in order to avoid overreaching under far-out reach settings and/or when the sequence networks are greatly non-homogeneous. This setting applies to both the forward and reverse reactance lines if the zone is set to non-directional. Refer to chapters 8 and 9 for additional information.
- **GND DIST Z1 COMP LIMIT:** This setting shapes the operating characteristic. In particular, it enables a lens-shaped characteristic of the mho function and a tent-shaped characteristic of the quadrilateral function reactance boundary. If the mho shape is selected, the same limit angle applies to mho and supervising reactance comparators. In conjunction with the mho shape selection, this setting improves loadability of the protected line. In conjunction with the quadrilateral characteristic, this setting improves security for faults close to the reach point by adjusting the reactance boundary into a tent-shape.
- **GND DIST Z1 DIR RCA:** Selects the characteristic angle (or 'maximum torque angle') of the directional supervising function. If the mho shape is applied, the directional function is an extra supervising function, as the dynamic mho characteristic itself is a directional one. In conjunction with the quadrilateral shape selection, this setting defines the only directional function built into the ground distance element. The directional function uses memory voltage for polarization.
- **GND DIST Z1 DIR COMP LIMIT**: This setting selects the comparator limit angle for the directional supervising function.
- **GND DIST Z1 QUAD RGT BLD**: This setting defines the right blinder position of the quadrilateral characteristic along the resistive axis of the impedance plane (see the *Quadrilateral Distance Characteristic* figure). The angular position of the blinder is adjustable with the use of the **GND DIST Z1 QUAD RGT BLD RCA** setting. This setting applies only to the quadrilateral characteristic and should be set with consideration to the maximum load current and required resistive coverage.

- **GND DIST Z1 QUAD RGT BLD RCA**: This setting defines the angular position of the right blinder of the quadrilateral characteristic (see the *Quadrilateral distance characteristic* figure).
- **GND DIST Z1 QUAD LFT BLD**: This setting defines the left blinder position of the quadrilateral characteristic along the resistive axis of the impedance plane (see the *Quadrilateral distance characteristic* figure). The angular position of the blinder is adjustable with the use of the **GND DIST Z1 QUAD LFT BLD RCA** setting. This setting applies only to the quadrilateral characteristic and should be set with consideration to the maximum load current.
- **GND DIST Z1 QUAD LFT BLD RCA**: This setting defines the angular position of the left blinder of the quadrilateral characteristic (see the *Quadrilateral distance characteristic* figure).
- **GND DIST Z1 SUPV**: The ground distance elements are supervised by the magnitude of the neutral (3I_0) current. The current supervision pickup should be set above the maximum unbalance current under maximum load conditions preventing maloperation due to VT fuse failure.
- **GND DIST Z1 VOLT LEVEL:** This setting is relevant for applications on series-compensated lines, or in general, if series capacitors are located between the relaying point and a point for which the zone shall not overreach. For plain (non-compensated) lines, this setting shall be set to zero. Otherwise, the setting is entered in per unit of the VT bank configured under the **DISTANCE SOURCE**. Effectively, this setting facilitates dynamic current-based reach reduction. In non-directional applications (**GND DIST Z1 DIR** set to "Non-directional"), this setting applies only to the forward reach of the non-directional zone. See Chapter 8 and 9 for additional details and information on calculating this setting value for applications on series compensated lines.
- **GND DIST Z1 DELAY:** This setting enables the user to delay operation of the distance elements and implement a stepped distance backup protection. The distance element timer applies a short drop out delay to cope with faults located close to the boundary of the zone when small oscillations in the voltages or currents could inadvertently reset the timer.
- **GND DIST Z1 BLK:** This setting enables the user to select a FlexLogic™ operand to block the given distance element. VT fuse fail detection is one of the applications for this setting.

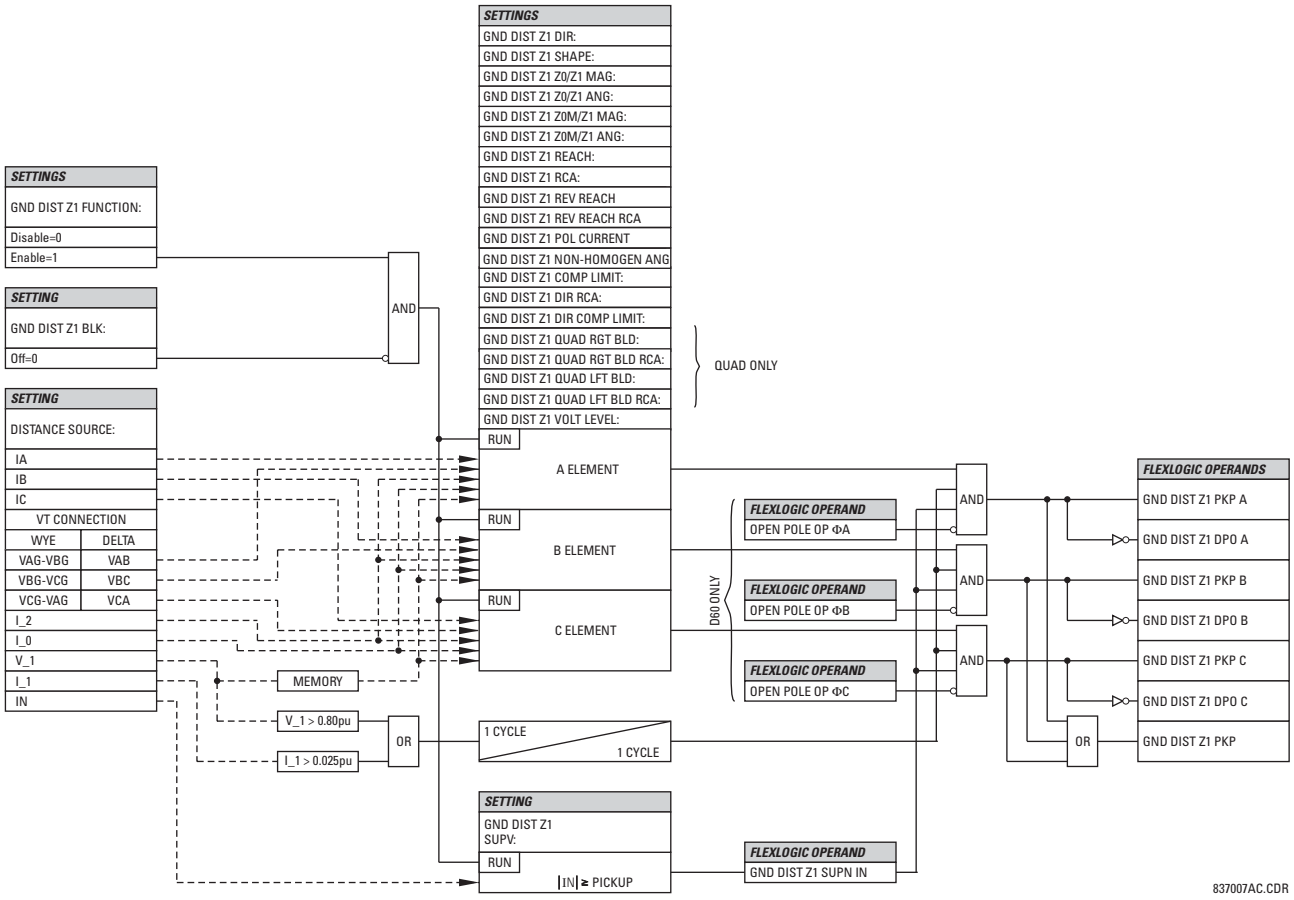


Figure 5–61: GROUND DISTANCE Z1 SCHEME LOGIC

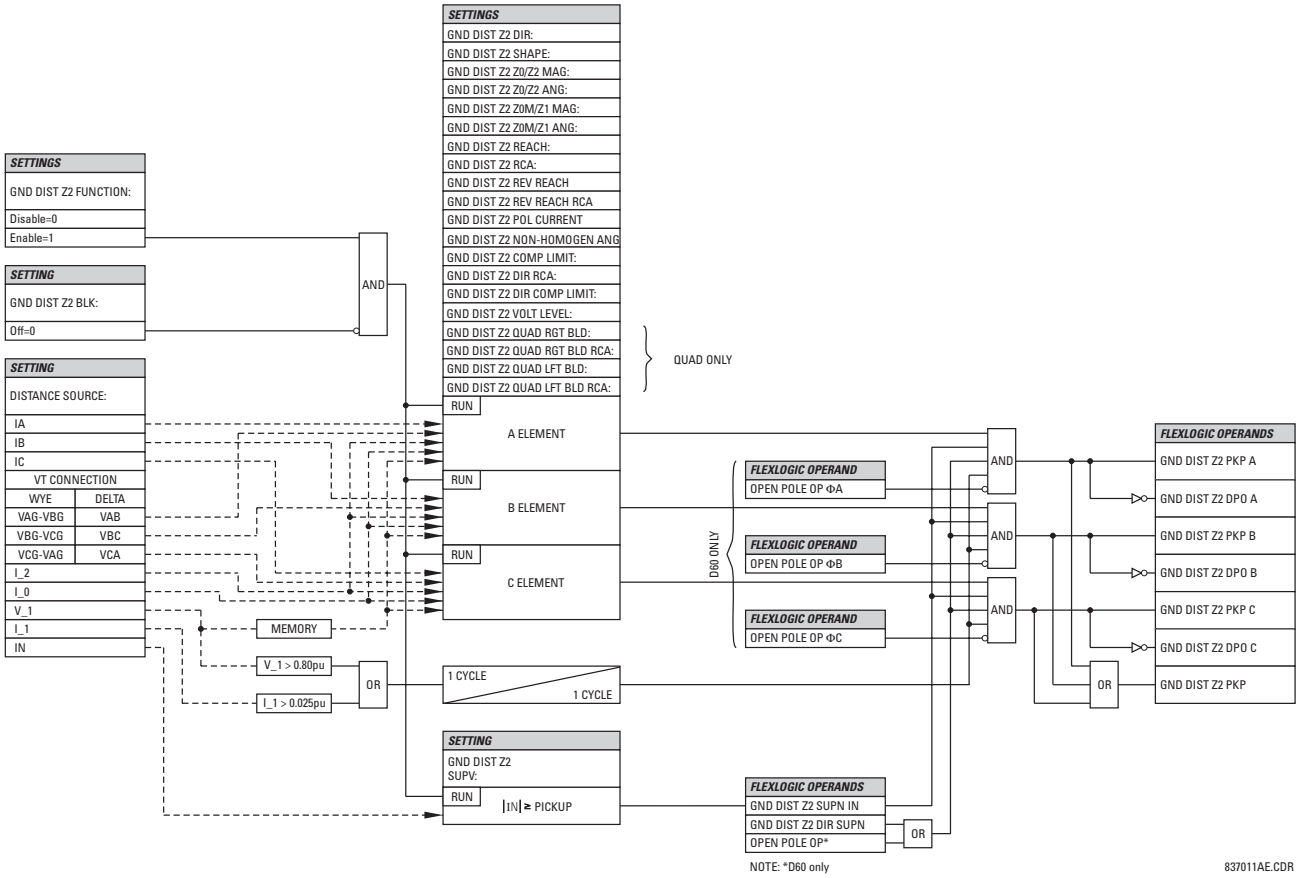


Figure 5–62: GROUND DISTANCE ZONE 2 TO ZONE 3 SCHEME LOGIC

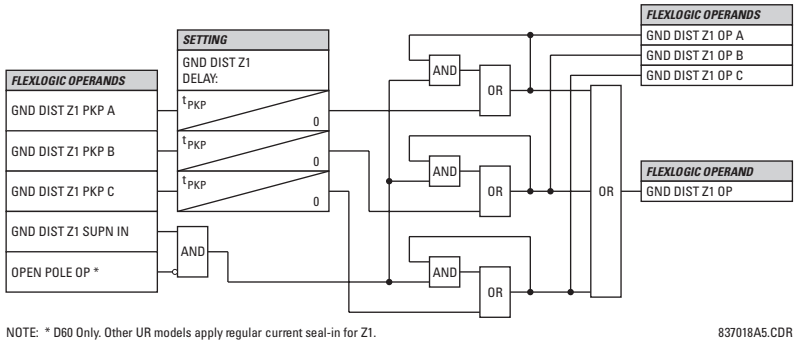


Figure 5–63: GROUND DISTANCE Z1 OP SCHEME

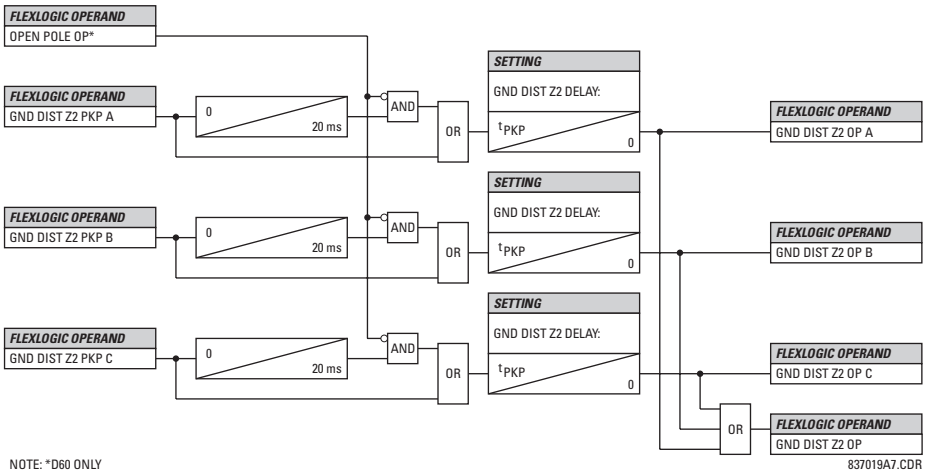


Figure 5–64: GROUND DISTANCE ZONE 2 TO ZONE 3 OP SCHEME

GROUND DIRECTIONAL SUPERVISION:

A dual (zero and negative-sequence) memory-polarized directional supervision applied to the ground distance protection elements has been shown to give good directional integrity. However, a reverse double-line-to-ground fault can lead to a maloperation of the ground element in a sound phase if the zone reach setting is increased to cover high resistance faults.

Ground distance zones 2 through 3 use an additional ground directional supervision to enhance directional integrity. The element's directional characteristic angle is used as a 'maximum torque angle' together with a 90° limit angle.

The supervision is biased toward operation in order to avoid compromising the sensitivity of ground distance elements at low signal levels. Otherwise, the reverse fault condition that generates concern will have high polarizing levels so that a correct reverse fault decision can be reliably made. The supervision for zones 2and 3 is removed during open pole conditions.

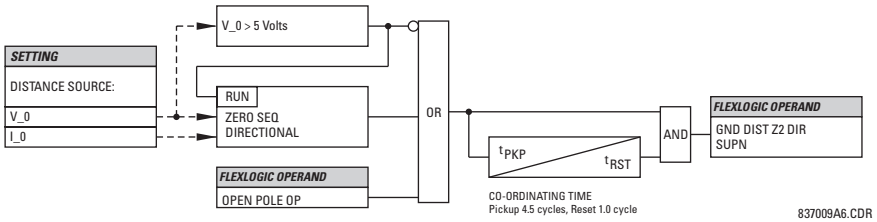


Figure 5–65: GROUND DIRECTIONAL SUPERVISION SCHEME LOGIC

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ POWER SWING DETECT

■ POWER SWING ■ DETECT		POWER SWING FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	POWER SWING SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	POWER SWING SHAPE: Mho Shape	Range: Mho Shape, Quad Shape
	MESSAGE	POWER SWING MODE: Two Step	Range: Two Step, Three Step
	MESSAGE	POWER SWING SUPV: 0.600 pu	Range: 0.050 to 30.000 pu in steps of 0.001
	MESSAGE	POWER SWING FWD REACH: 50.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING QUAD FWD REACH MID: 60.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING QUAD FWD REACH OUT: 70.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING FWD RCA: 75°	Range: 40 to 90° in steps of 1
	MESSAGE	POWER SWING REV REACH: 50.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING QUAD REV REACH MID: 60.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING QUAD REV REACH OUT: 70.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING REV RCA: 75°	Range: 40 to 90° in steps of 1
	MESSAGE	POWER SWING OUTER LIMIT ANGLE: 120°	Range: 40 to 140° in steps of 1
	MESSAGE	POWER SWING MIDDLE LIMIT ANGLE: 90°	Range: 40 to 140° in steps of 1
	MESSAGE	POWER SWING INNER LIMIT ANGLE: 60°	Range: 40 to 140° in steps of 1
	MESSAGE	POWER SWING OUTER RGT BLD: 100.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING OUTER LFT BLD: 100.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING MIDDLE RGT BLD: 100.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING MIDDLE LFT BLD: 100.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01
	MESSAGE	POWER SWING INNER RGT BLD: 100.00 Ω	Range: 0.10 to 500.00 Ω in steps of 0.01

MESSAGE
POWER SWING INNER LFT BLD: 100.00 Ω
Range: 0.10 to 500.00 Ω in steps of 0.01

MESSAGE
POWER SWING PICKUP DELAY 1: 0.030 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
POWER SWING RESET DELAY 1: 0.050 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
POWER SWING PICKUP DELAY 2: 0.017 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
POWER SWING PICKUP DELAY 3: 0.009 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
POWER SWING PICKUP DELAY 4: 0.017 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
POWER SWING SEAL-IN DELAY: 0.400 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
POWER SWING TRIP MODE: Delayed
Range: Early, Delayed

MESSAGE
POWER SWING BLK: Off
Range: Flexlogic™ operand

MESSAGE
POWER SWING TARGET: Self-Reset
Range: Self-Reset, Latched, Disabled

MESSAGE
POWER SWING EVENTS: Disabled
Range: Disabled, Enabled

The power swing detect element provides both power swing blocking and out-of-step tripping functions. The element measures the positive-sequence apparent impedance and traces its locus with respect to either two or three user-selectable operating characteristic boundaries. Upon detecting appropriate timing relations, the blocking and/or tripping indication is given through FlexLogic™ operands. The element incorporates an adaptive disturbance detector. This function does not trigger on power swings, but is capable of detecting faster disturbances – faults in particular – that may occur during power swings. Operation of this dedicated disturbance detector is signaled via the POWER SWING 50DD operand.

The power swing detect element asserts two outputs intended for blocking selected protection elements on power swings: POWER SWING BLOCK is a traditional signal that is safely asserted for the entire duration of the power swing, and POWER SWING UN/BLOCK is established in the same way, but resets when an extra disturbance is detected during the power swing. The POWER SWING UN/BLOCK operand may be used for blocking selected protection elements if the intent is to respond to faults during power swing conditions.

Different protection elements respond differently to power swings. If tripping is required for faults during power swing conditions, some elements may be blocked permanently (using the POWER SWING BLOCK operand), and others may be blocked and dynamically unblocked upon fault detection (using the POWER SWING UN/BLOCK operand).

The operating characteristic and logic figures should be viewed along with the following discussion to develop an understanding of the operation of the element.

The power swing detect element operates in three-step or two-step mode:

- **Three-step operation:** The power swing blocking sequence essentially times the passage of the locus of the positive-sequence impedance between the outer and the middle characteristic boundaries. If the locus enters the outer characteristic (indicated by the POWER SWING OUTER FlexLogic™ operand) but stays outside the middle characteristic (indicated by the POWER SWING MIDDLE FlexLogic™ operand) for an interval longer than **POWER SWING PICKUP DELAY 1**, the power swing blocking signal (POWER SWING BLOCK FlexLogic™ operand) is established and sealed-in. The blocking signal resets when the locus leaves the outer characteristic, but not sooner than the **POWER SWING RESET DELAY 1** time.
- **Two-step operation:** If the 2-step mode is selected, the sequence is identical, but it is the outer and inner characteristics that are used to time the power swing locus.

The out-of-step tripping feature operates as follows for three-step and two-step power swing detection modes:

- **Three-step operation:** The out-of-step trip sequence identifies unstable power swings by determining if the impedance locus spends a finite time between the outer and middle characteristics and then a finite time between the middle and inner characteristics. The first step is similar to the power swing blocking sequence. After timer **POWER SWING PICKUP DELAY 1** times out, latch 1 is set as long as the impedance stays within the outer characteristic.

  If afterwards, at any time (given the impedance stays within the outer characteristic), the locus enters the middle characteristic but stays outside the inner characteristic for a period of time defined as **POWER SWING PICKUP DELAY 2**, latch 2 is set as long as the impedance stays inside the outer characteristic. If afterwards, at any time (given the impedance stays within the outer characteristic), the locus enters the inner characteristic and stays there for a period of time defined as **POWER SWING PICKUP DELAY 3**, latch 2 is set as long as the impedance stays inside the outer characteristic; the element is now ready to trip.

  If the "Early" trip mode is selected, the POWER SWING TRIP operand is set immediately and sealed-in for the interval set by the **POWER SWING SEAL-IN DELAY**. If the "Delayed" trip mode is selected, the element waits until the impedance locus leaves the inner characteristic, then times out the **POWER SWING PICKUP DELAY 2** and sets Latch 4; the element is now ready to trip. The trip operand is set later, when the impedance locus leaves the outer characteristic.

- **Two-step operation:** The 2-step mode of operation is similar to the three-step mode with two exceptions. First, the initial stage monitors the time spent by the impedance locus between the outer and inner characteristics. Second, the stage involving the **POWER SWING PICKUP DELAY 2** timer is bypassed. It is up to the user to integrate the blocking (POWER SWING BLOCK) and tripping (POWER SWING TRIP) FlexLogic™ operands with other protection functions and output contacts in order to make this element fully operational.

The element can be set to use either lens (mho) or rectangular (quad) characteristics as illustrated below. When set to “Mho”, the element applies the right and left blinders as well. If the blinders are not required, their settings should be set high enough to effectively disable the blinders.

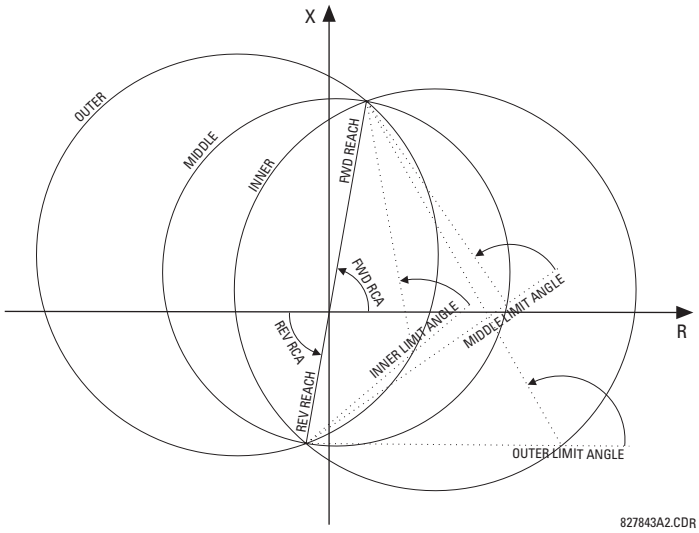


Figure 5–66: POWER SWING DETECT MHO OPERATING CHARACTERISTICS

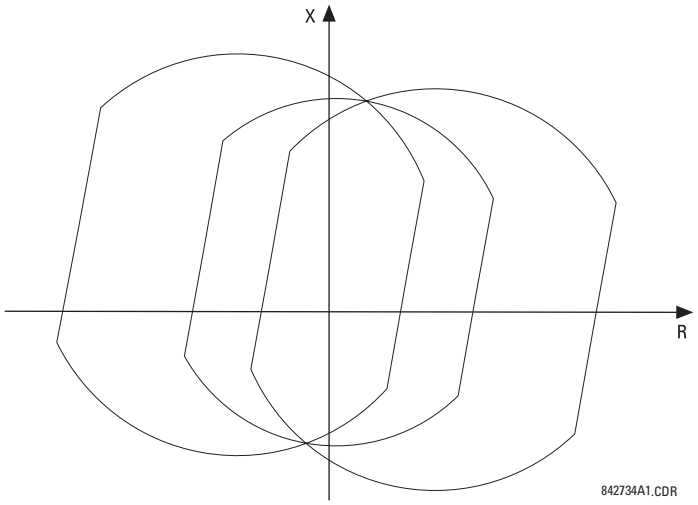


Figure 5–67: EFFECTS OF BLINDERS ON THE MHO CHARACTERISTICS

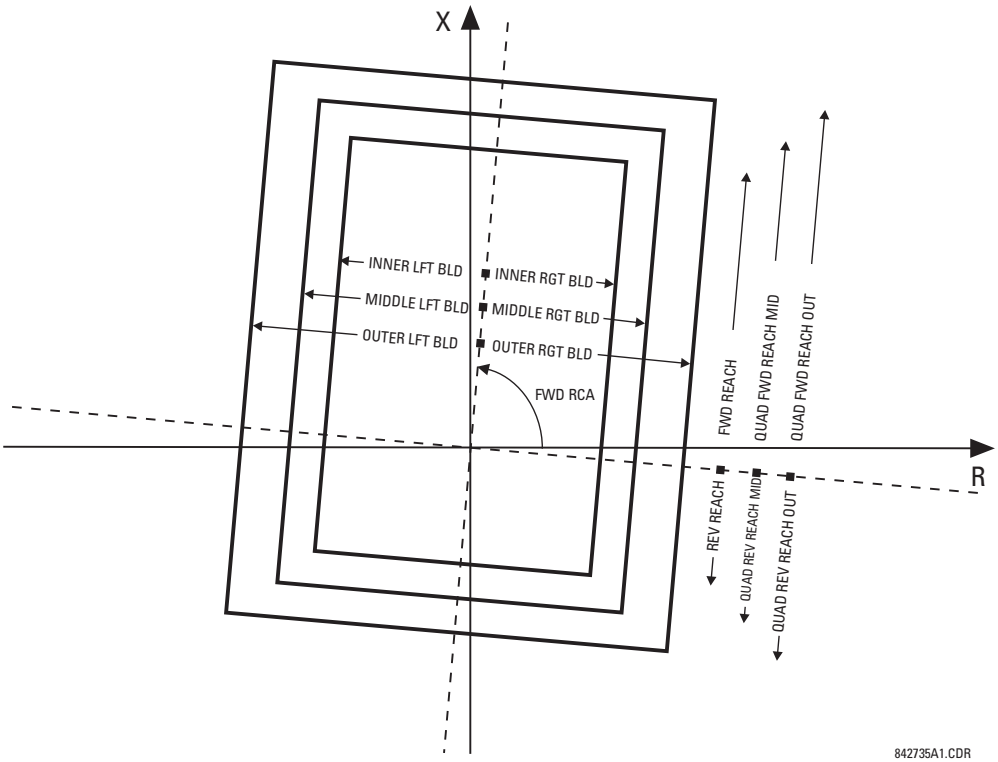


Figure 5–68: POWER SWING DETECT QUAD OPERATING CHARACTERISTICS

The FlexLogic™ output operands for the power swing detect element are described below:

- The POWER SWING OUTER, POWER SWING MIDDLE, POWER SWING INNER, POWER SWING TMR2 PKP, POWER SWING TMR3 PKP, and POWER SWING TMR4 PKP FlexLogic™ operands are auxiliary operands that could be used to facilitate testing and special applications.
- The POWER SWING BLOCK FlexLogic™ operand shall be used to block selected protection elements such as distance functions.

- The POWER SWING UN/BLOCK FlexLogic™ operand shall be used to block those protection elements that are intended to be blocked under power swings, but subsequently unblocked should a fault occur after the power swing blocking condition has been established.
- The POWER SWING 50DD FlexLogic™ operand indicates that an adaptive disturbance detector integrated with the element has picked up. This operand will trigger on faults occurring during power swing conditions. This includes both three-phase and single-pole-open conditions.
- The POWER SWING INCOMING FlexLogic™ operand indicates an unstable power swing with an incoming locus (the locus enters the inner characteristic).
- The POWER SWING OUTGOING FlexLogic™ operand indicates an unstable power swing with an outgoing locus (the locus leaving the outer characteristic). This operand can be used to count unstable swings and take certain action only after pre-defined number of unstable power swings.
- The POWER SWING TRIP FlexLogic™ operand is a trip command.

The settings for the power swing detect element are described below:

- **POWER SWING FUNCTION:** This setting enables/disables the entire power swing detection element. The setting applies to both power swing blocking and out-of-step tripping functions.
- **POWER SWING SOURCE:** The source setting identifies the signal source for both blocking and tripping functions.
- **POWER SWING SHAPE**: This setting selects the shapes (either “Mho” or “Quad”) of the outer, middle and, inner characteristics of the power swing detect element. The operating principle is not affected. The “Mho” characteristics use the left and right blinders.
- **POWER SWING MODE:** This setting selects between the two-step and three-step operating modes and applies to both power swing blocking and out-of-step tripping functions. The three-step mode applies if there is enough space between the maximum load impedances and distance characteristics of the relay that all three (outer, middle, and inner) characteristics can be placed between the load and the distance characteristics. Whether the spans between the outer and middle as well as the middle and inner characteristics are sufficient should be determined by analysis of the fastest power swings expected in correlation with settings of the power swing timers.

  The two-step mode uses only the outer and inner characteristics for both blocking and tripping functions. This leaves more space in heavily loaded systems to place two power swing characteristics between the distance characteristics and the maximum load, but allows for only one determination of the impedance trajectory.
- **POWER SWING SUPV:** A common overcurrent pickup level supervises all three power swing characteristics. The supervision responds to the positive sequence current.
- **POWER SWING FWD REACH:** This setting specifies the forward reach of all three mho characteristics and the inner quad characteristic. For a simple system consisting of a line and two equivalent sources, this reach should be higher than the sum of the line and remote source positive-sequence impedances. Detailed transient stability studies may be needed for complex systems in order to determine this setting. The angle of this reach impedance is specified by the **POWER SWING FWD RCA** setting.
- **POWER SWING QUAD FWD REACH MID**: This setting specifies the forward reach of the middle quad characteristic. The angle of this reach impedance is specified by the **POWER SWING FWD RCA** setting. The setting is not used if the shape setting is “Mho”.
- **POWER SWING QUAD FWD REACH OUT**: This setting specifies the forward reach of the outer quad characteristic. The angle of this reach impedance is specified by the **POWER SWING FWD RCA** setting. The setting is not used if the shape setting is “Mho”.
- **POWER SWING FWD RCA:** This setting specifies the angle of the forward reach impedance for the mho characteristics, angles of all the blinders, and both forward and reverse reach impedances of the quad characteristics.
- **POWER SWING REV REACH:** This setting specifies the reverse reach of all three mho characteristics and the inner quad characteristic. For a simple system of a line and two equivalent sources, this reach should be higher than the positive-sequence impedance of the local source. Detailed transient stability studies may be needed for complex systems to determine this setting. The angle of this reach impedance is specified by the **POWER SWING REV RCA** setting for “Mho”, and the **POWER SWING FWD RCA** setting for “Quad”.
- **POWER SWING QUAD REV REACH MID**: This setting specifies the reverse reach of the middle quad characteristic. The angle of this reach impedance is specified by the **POWER SWING FWD RCA** setting. The setting is not used if the shape setting is “Mho”.

- **POWER SWING QUAD REV REACH OUT**: This setting specifies the reverse reach of the outer quad characteristic. The angle of this reach impedance is specified by the **POWER SWING FWD RCA** setting. The setting is not used if the shape setting is “Mho”.
- **POWER SWING REV RCA:** This setting specifies the angle of the reverse reach impedance for the mho characteristics. This setting applies to mho shapes only.
- **POWER SWING OUTER LIMIT ANGLE:** This setting defines the outer power swing characteristic. The convention depicted in the *Power swing detect characteristic* diagram should be observed: values greater than 90° result in an apple-shaped characteristic; values less than 90° result in a lens shaped characteristic. This angle must be selected in consideration of the maximum expected load. If the maximum load angle is known, the outer limit angle should be coordinated with a 20° security margin. Detailed studies may be needed for complex systems to determine this setting. This setting applies to mho shapes only.
- **POWER SWING MIDDLE LIMIT ANGLE:** This setting defines the middle power swing detect characteristic. It is relevant only for the 3-step mode. A typical value would be close to the average of the outer and inner limit angles. This setting applies to mho shapes only.
- **POWER SWING INNER LIMIT ANGLE:** This setting defines the inner power swing detect characteristic. The inner characteristic is used by the out-of-step tripping function: beyond the inner characteristic out-of-step trip action is definite (the actual trip may be delayed as per the **TRIP MODE** setting). Therefore, this angle must be selected in consideration to the power swing angle beyond which the system becomes unstable and cannot recover.

  The inner characteristic is also used by the power swing blocking function in the two-step mode. In this case, set this angle large enough so that the characteristics of the distance elements are safely enclosed by the inner characteristic. This setting applies to mho shapes only.
- **POWER SWING OUTER**, **MIDDLE**, and **INNER RGT BLD**: These settings specify the resistive reach of the right blinder. The blinder applies to both “Mho” and “Quad” characteristics. Set these value high if no blinder is required for the “Mho” characteristic.
- **POWER SWING OUTER**, **MIDDLE**, and **INNER LFT BLD**: These settings specify the resistive reach of the left blinder. Enter a positive value; the relay automatically uses a negative value. The blinder applies to both “Mho” and “Quad” characteristics. Set this value high if no blinder is required for the “Mho” characteristic.
- **POWER SWING PICKUP DELAY 1:** All the coordinating timers are related to each other and should be set to detect the fastest expected power swing and produce out-of-step tripping in a secure manner. The timers should be set in consideration to the power swing detect characteristics, mode of power swing detect operation and mode of out-of-step tripping. This timer defines the interval that the impedance locus must spend between the outer and inner characteristics (two-step operating mode), or between the outer and middle characteristics (three-step operating mode) before the power swing blocking signal is established. This time delay must be set shorter than the time required for the impedance locus to travel between the two selected characteristics during the fastest expected power swing. This setting is relevant for both power swing blocking and out-of-step tripping.
- **POWER SWING RESET DELAY 1:** This setting defines the dropout delay for the power swing blocking signal. Detection of a condition requiring a block output sets latch 1 after **PICKUP DELAY 1** time. When the impedance locus leaves the outer characteristic, timer **POWER SWING RESET DELAY 1** is started. When the timer times-out the latch is reset. This setting should be selected to give extra security for the power swing blocking action.
- **POWER SWING PICKUP DELAY 2:** Controls the out-of-step tripping function in the three-step mode only. This timer defines the interval the impedance locus must spend between the middle and inner characteristics before the second step of the out-of-step tripping sequence is completed. This time delay must be set shorter than the time required for the impedance locus to travel between the two characteristics during the fastest expected power swing.
- **POWER SWING PICKUP DELAY 3:** Controls the out-of-step tripping function only. It defines the interval the impedance locus must spend within the inner characteristic before the last step of the out-of-step tripping sequence is completed and the element is armed to trip. The actual moment of tripping is controlled by the **TRIP MODE** setting. This time delay is provided for extra security before the out-of-step trip action is executed.
- **POWER SWING PICKUP DELAY 4:** Controls the out-of-step tripping function in “Delayed” trip mode only. This timer defines the interval the impedance locus must spend outside the inner characteristic but within the outer characteristic before the element is armed for the delayed trip. The delayed trip occurs when the impedance leaves the outer characteristic. This time delay is provided for extra security and should be set considering the fastest expected power swing.

- **POWER SWING SEAL-IN DELAY:** The out-of-step trip FlexLogic™ operand (POWER SWING TRIP) is sealed-in for the specified period of time. The sealing-in is crucial in the delayed trip mode, as the original trip signal is a very short pulse occurring when the impedance locus leaves the outer characteristic after the out-of-step sequence is completed.
- **POWER SWING TRIP MODE:** Selection of the "Early" trip mode results in an instantaneous trip after the last step in the out-of-step tripping sequence is completed. The early trip mode will stress the circuit breakers as the currents at that moment are high (the electromotive forces of the two equivalent systems are approximately 180° apart). Selection of the "Delayed" trip mode results in a trip at the moment when the impedance locus leaves the outer characteristic. delayed trip mode will relax the operating conditions for the breakers as the currents at that moment are low. The selection should be made considering the capability of the breakers in the system.
- **POWER SWING BLK:** This setting specifies the FlexLogic™ operand used for blocking the out-of-step function only. The power swing blocking function is operational all the time as long as the element is enabled. The blocking signal resets the output POWER SWING TRIP operand but does not stop the out-of-step tripping sequence.

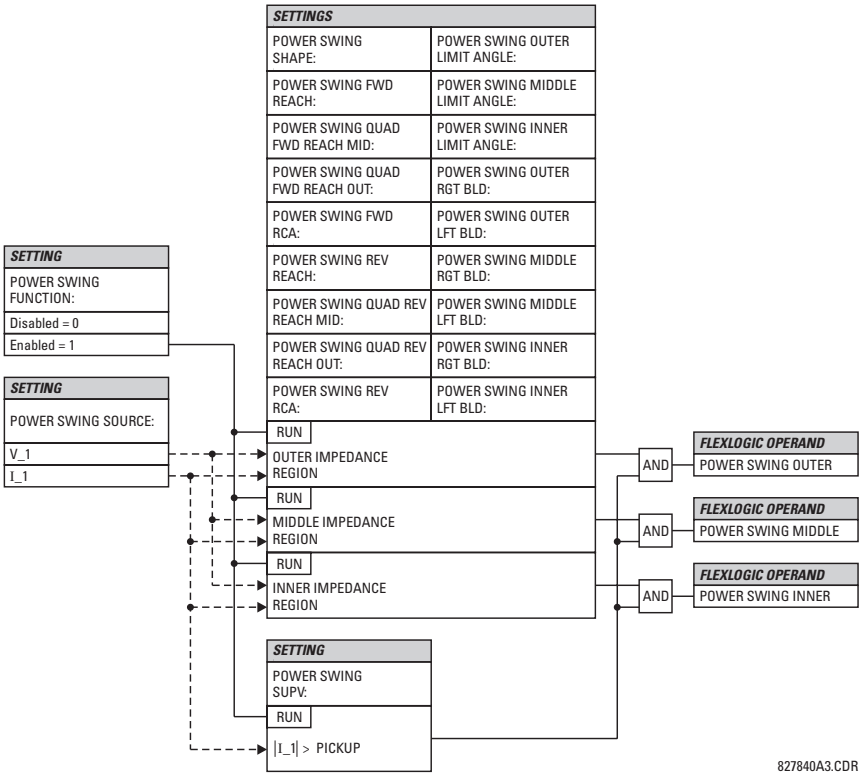


Figure 5–69: POWER SWING DETECT SCHEME LOGIC (1 of 3)

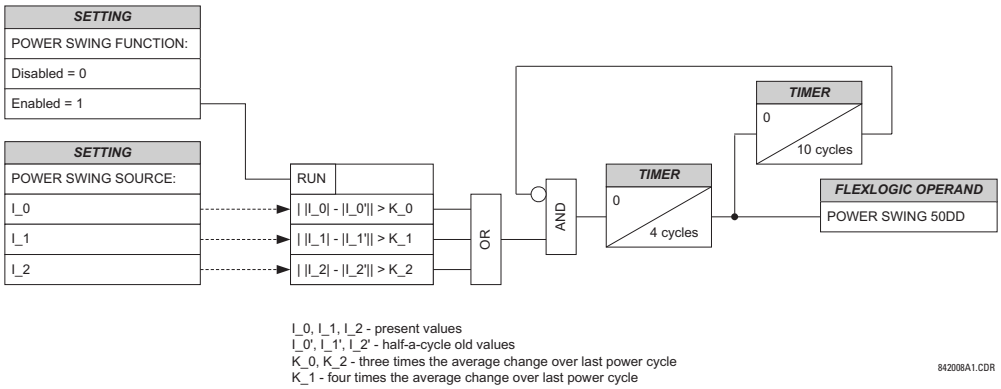


Figure 5–70: POWER SWING DETECT SCHEME LOGIC (2 of 3)

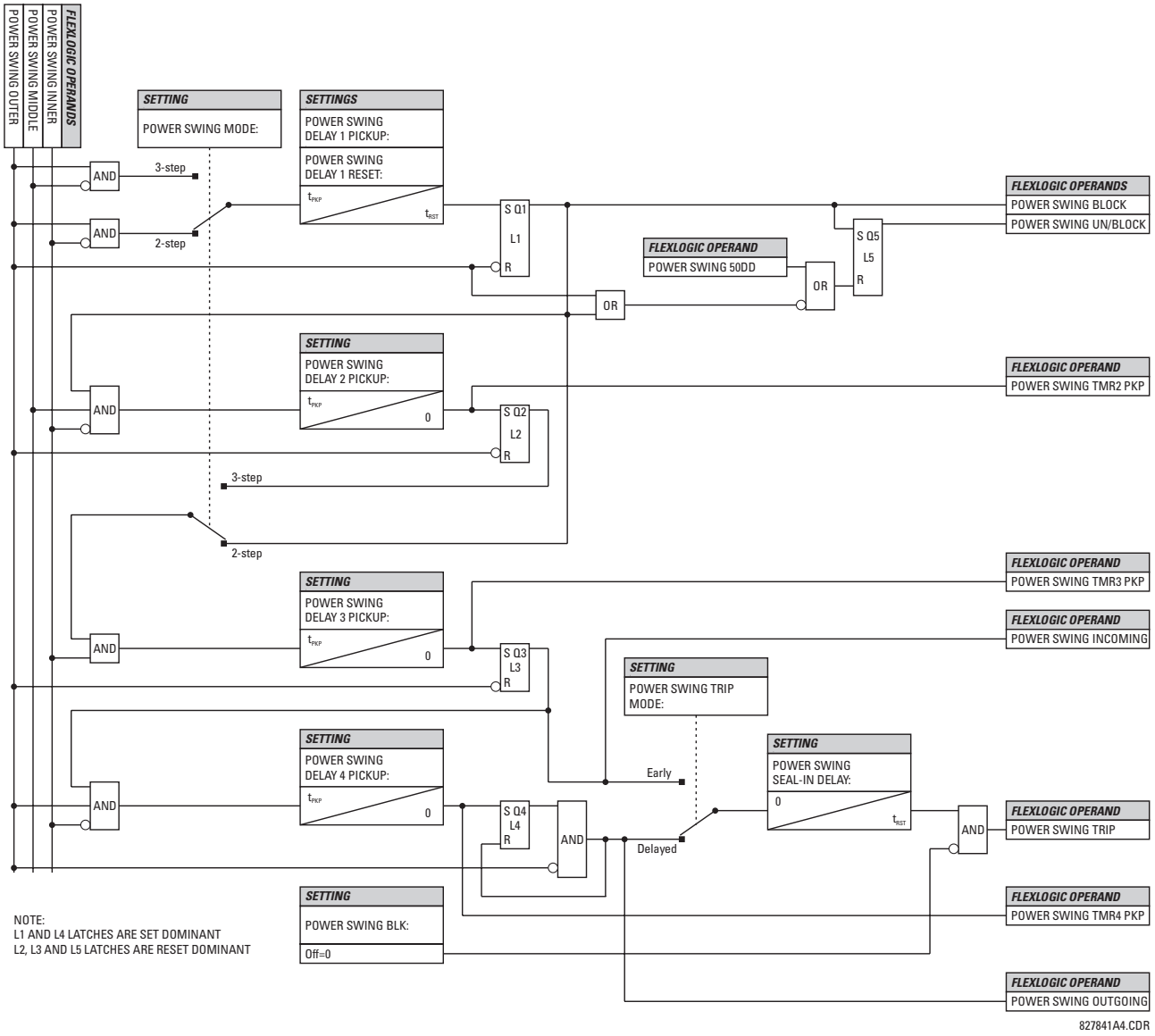


Figure 5–71: POWER SWING DETECT SCHEME LOGIC (3 of 3)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ LOAD ENCROACHMENT

■ LOAD ENCROACHMENT ■		LOAD ENCROACHMENT FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	LOAD ENCROACHMENT SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	LOAD ENCROACHMENT MIN VOLT: 0.250 pu	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	LOAD ENCROACHMENT REACH: 1.00 Ω	Range: 0.02 to 250.00 ohms in steps of 0.01
	MESSAGE	LOAD ENCROACHMENT ANGLE: 30°	Range: 5 to 50° in steps of 1
	MESSAGE	LOAD ENCROACHMENT PKP DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	LOAD ENCROACHMENT RST DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	LOAD ENCRMNT BLK: Off	Range: Flexlogic™ operand
	MESSAGE	LOAD ENCROACHMENT TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	LOAD ENCROACHMENT EVENTS: Disabled	Range: Disabled, Enabled

The load encroachment element responds to the positive-sequence voltage and current and applies a characteristic shown in the figure below.

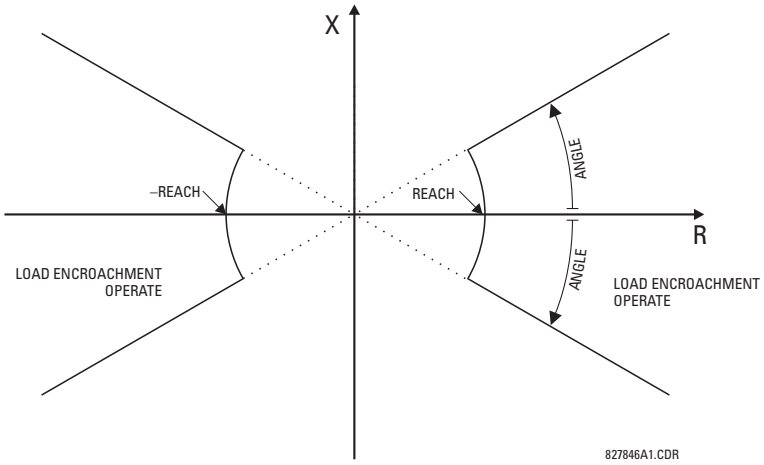


Figure 5–72: LOAD ENCROACHMENT CHARACTERISTIC

The element operates if the positive-sequence voltage is above a settable level and asserts its output signal that can be used to block selected protection elements such as distance or phase overcurrent. The following figure shows an effect of the load encroachment characteristics used to block the quadrilateral distance element.

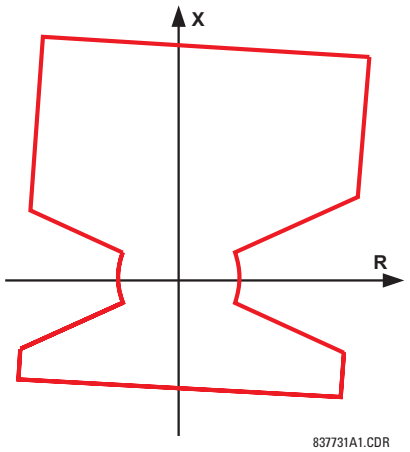


Figure 5–73: LOAD ENCROACHMENT APPLIED TO DISTANCE ELEMENT

- **LOAD ENCROACHMENT MIN VOLT:** This setting specifies the minimum positive-sequence voltage required for operation of the element. If the voltage is below this threshold a blocking signal will not be asserted by the element. When selecting this setting one must remember that the L60 measures the phase-to-ground sequence voltages regardless of the VT connection.

  The nominal VT secondary voltage as specified with the **SYSTEM SETUP ⇨⇩ AC INPUTS ⇨ VOLTAGE BANK X5 ⇨⇩ PHASE VT SECONDARY** setting is the per-unit base for this setting.

- **LOAD ENCROACHMENT REACH:** This setting specifies the resistive reach of the element as shown in the *Load encroachment characteristic* diagram. This setting should be entered in secondary ohms and be calculated as the positive-sequence resistance seen by the relay under maximum load conditions and unity power factor.

- **LOAD ENCROACHMENT ANGLE:** This setting specifies the size of the blocking region as shown on the *Load encroachment characteristic* diagram and applies to the positive-sequence impedance.

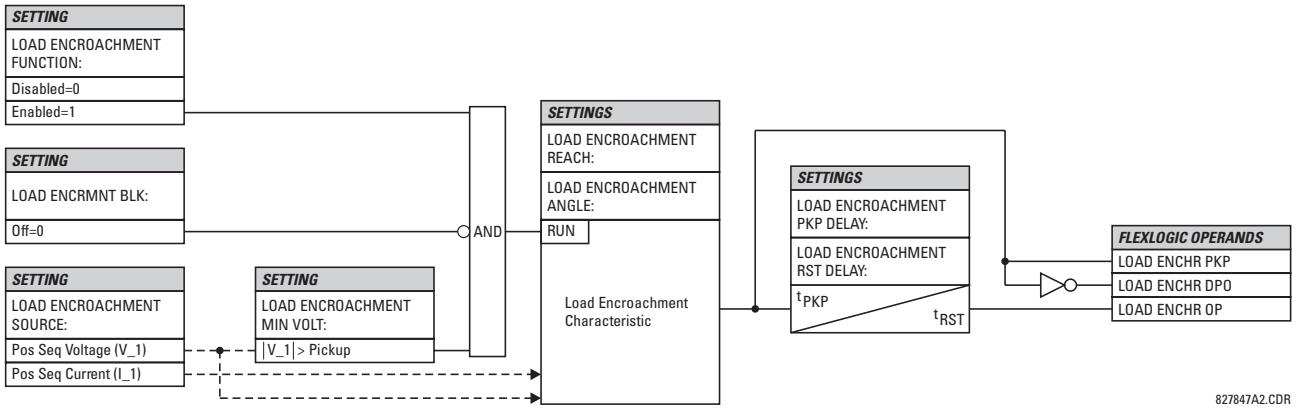
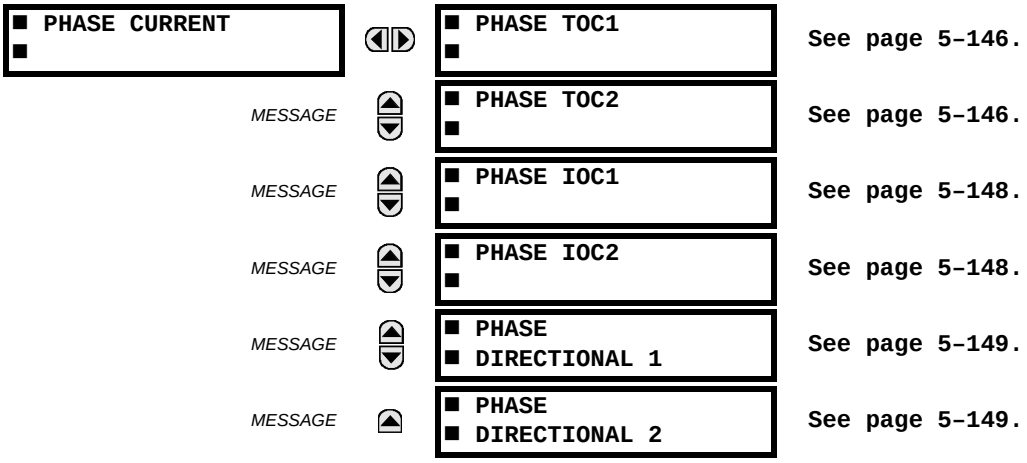


Figure 5–74: LOAD ENCROACHMENT SCHEME LOGIC

a) MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ PHASE CURRENT



The L60 Line Phase Comparison System has two (2) Phase Time Overcurrent, two (2) Phase Instantaneous Overcurrent, and two (2) Phase Directional Overcurrent elements. These are described in the following sub-sections.

b) INVERSE TIME OVERCURRENT CURVE CHARACTERISTICS

The inverse time overcurrent curves used by the time overcurrent elements are the IEEE, IEC, GE Type IAC, and I^2t standard curve shapes. This allows for simplified coordination with downstream devices.

If none of these curve shapes is adequate, FlexCurves™ may be used to customize the inverse time curve characteristics. The Definite Time curve is also an option that may be appropriate if only simple protection is required.

Table 5–14: OVERCURRENT CURVE TYPES

IEEE	IEC	GE TYPE IAC	OTHER
IEEE Extremely Inverse	IEC Curve A (BS142)	IAC Extremely Inverse	I^2t
IEEE Very Inverse	IEC Curve B (BS142)	IAC Very Inverse	FlexCurves™ A, B, C, and D
IEEE Moderately Inverse	IEC Curve C (BS142)	IAC Inverse	Recloser Curves
	IEC Short Inverse	IAC Short Inverse	Definite Time

A time dial multiplier setting allows selection of a multiple of the base curve shape (where the time dial multiplier = 1) with the curve shape (**CURVE**) setting. Unlike the electromechanical time dial equivalent, operate times are directly proportional to the time multiplier (**TD MULTIPLIER**) setting value. For example, all times for a multiplier of 10 are 10 times the multiplier 1 or base curve values. Setting the multiplier to zero results in an instantaneous response to all current levels above pickup.

Time overcurrent time calculations are made with an internal 'energy capacity' memory variable. When this variable indicates that the energy capacity has reached 100%, a time overcurrent element will operate. If less than 100% energy capacity is accumulated in this variable and the current falls below the dropout threshold of 97 to 98% of the pickup value, the variable must be reduced. Two methods of this resetting operation are available: "Instantaneous" and "Timed". The "Instantaneous" selection is intended for applications with other relays, such as most static relays, which set the energy capacity directly to zero when the current falls below the reset threshold. The "Timed" selection can be used where the relay must coordinate with electromechanical relays.

IEEE CURVES:

The IEEE time overcurrent curve shapes conform to industry standards and the IEEE C37.112-1996 curve classifications for extremely, very, and moderately inverse. The IEEE curves are derived from the formulae:

$$T = TDM \times \left[\frac{A}{\left(\frac{I}{I_{pickup}} \right)^{p} - 1} + B \right], T_{RESET} = TDM \times \left[\frac{t_r}{1 - \left(\frac{I}{I_{pickup}} \right)^{2}} \right] \quad \textbf{(EQ 5.10)}$$

where: T = operate time (in seconds), TDM = Multiplier setting, I = input current, I_{pickup} = Pickup Current setting A, B, p = constants, T_{RESET} = reset time in seconds (assuming energy capacity is 100% and **RESET** is "Timed"), t_r = characteristic constant

Table 5–15: IEEE INVERSE TIME CURVE CONSTANTS

IEEE CURVE SHAPE	A	B	P	T_R
IEEE Extremely Inverse	28.2	0.1217	2.0000	29.1
IEEE Very Inverse	19.61	0.491	2.0000	21.6
IEEE Moderately Inverse	0.0515	0.1140	0.02000	4.85

Table 5–16: IEEE CURVE TRIP TIMES (IN SECONDS)

MULTIPLIER (TDM)	CURRENT (I / I_{pickup})									
	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
IEEE EXTREMELY INVERSE										
0.5	11.341	4.761	1.823	1.001	0.648	0.464	0.355	0.285	0.237	0.203
1.0	22.682	9.522	3.647	2.002	1.297	0.927	0.709	0.569	0.474	0.407
2.0	45.363	19.043	7.293	4.003	2.593	1.855	1.418	1.139	0.948	0.813
4.0	90.727	38.087	14.587	8.007	5.187	3.710	2.837	2.277	1.897	1.626
6.0	136.090	57.130	21.880	12.010	7.780	5.564	4.255	3.416	2.845	2.439
8.0	181.454	76.174	29.174	16.014	10.374	7.419	5.674	4.555	3.794	3.252
10.0	226.817	95.217	36.467	20.017	12.967	9.274	7.092	5.693	4.742	4.065
IEEE VERY INVERSE										
0.5	8.090	3.514	1.471	0.899	0.654	0.526	0.450	0.401	0.368	0.345
1.0	16.179	7.028	2.942	1.798	1.308	1.051	0.900	0.802	0.736	0.689
2.0	32.358	14.055	5.885	3.597	2.616	2.103	1.799	1.605	1.472	1.378
4.0	64.716	28.111	11.769	7.193	5.232	4.205	3.598	3.209	2.945	2.756
6.0	97.074	42.166	17.654	10.790	7.849	6.308	5.397	4.814	4.417	4.134
8.0	129.432	56.221	23.538	14.387	10.465	8.410	7.196	6.418	5.889	5.513
10.0	161.790	70.277	29.423	17.983	13.081	10.513	8.995	8.023	7.361	6.891
IEEE MODERATELY INVERSE										
0.5	3.220	1.902	1.216	0.973	0.844	0.763	0.706	0.663	0.630	0.603
1.0	6.439	3.803	2.432	1.946	1.688	1.526	1.412	1.327	1.260	1.207
2.0	12.878	7.606	4.864	3.892	3.377	3.051	2.823	2.653	2.521	2.414
4.0	25.756	15.213	9.729	7.783	6.753	6.102	5.647	5.307	5.041	4.827
6.0	38.634	22.819	14.593	11.675	10.130	9.153	8.470	7.960	7.562	7.241
8.0	51.512	30.426	19.458	15.567	13.507	12.204	11.294	10.614	10.083	9.654
10.0	64.390	38.032	24.322	19.458	16.883	15.255	14.117	13.267	12.604	12.068

IEC CURVES

For European applications, the relay offers three standard curves defined in IEC 255-4 and British standard BS142. These are defined as IEC Curve A, IEC Curve B, and IEC Curve C. The formulae for these curves are:

$$T = TDM \times \left[\frac{K}{(I/I_{pickup})^{E} - 1} \right], \quad T_{RESET} = TDM \times \left[\frac{t_r}{1 - (I/I_{pickup})^{2}} \right] \qquad \textbf{(EQ 5.11)}$$

where: T = operate time (in seconds), TDM = Multiplier setting, I = input current, I_{pickup} = Pickup Current setting, K, E = constants, t_r = characteristic constant, and T_{RESET} = reset time in seconds (assuming energy capacity is 100% and **RESET** is "Timed")

Table 5–17: IEC (BS) INVERSE TIME CURVE CONSTANTS

IEC (BS) CURVE SHAPE	K	E	T_R
IEC Curve A (BS142)	0.140	0.020	9.7
IEC Curve B (BS142)	13.500	1.000	43.2
IEC Curve C (BS142)	80.000	2.000	58.2
IEC Short Inverse	0.050	0.040	0.500

Table 5–18: IEC CURVE TRIP TIMES (IN SECONDS)

MULTIPLIER (TDM)	CURRENT (I / I_{pickup})									
	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
IEC CURVE A										
0.05	0.860	0.501	0.315	0.249	0.214	0.192	0.176	0.165	0.156	0.149
0.10	1.719	1.003	0.630	0.498	0.428	0.384	0.353	0.330	0.312	0.297
0.20	3.439	2.006	1.260	0.996	0.856	0.767	0.706	0.659	0.623	0.594
0.40	6.878	4.012	2.521	1.992	1.712	1.535	1.411	1.319	1.247	1.188
0.60	10.317	6.017	3.781	2.988	2.568	2.302	2.117	1.978	1.870	1.782
0.80	13.755	8.023	5.042	3.984	3.424	3.070	2.822	2.637	2.493	2.376
1.00	17.194	10.029	6.302	4.980	4.280	3.837	3.528	3.297	3.116	2.971
IEC CURVE B										
0.05	1.350	0.675	0.338	0.225	0.169	0.135	0.113	0.096	0.084	0.075
0.10	2.700	1.350	0.675	0.450	0.338	0.270	0.225	0.193	0.169	0.150
0.20	5.400	2.700	1.350	0.900	0.675	0.540	0.450	0.386	0.338	0.300
0.40	10.800	5.400	2.700	1.800	1.350	1.080	0.900	0.771	0.675	0.600
0.60	16.200	8.100	4.050	2.700	2.025	1.620	1.350	1.157	1.013	0.900
0.80	21.600	10.800	5.400	3.600	2.700	2.160	1.800	1.543	1.350	1.200
1.00	27.000	13.500	6.750	4.500	3.375	2.700	2.250	1.929	1.688	1.500
IEC CURVE C										
0.05	3.200	1.333	0.500	0.267	0.167	0.114	0.083	0.063	0.050	0.040
0.10	6.400	2.667	1.000	0.533	0.333	0.229	0.167	0.127	0.100	0.081
0.20	12.800	5.333	2.000	1.067	0.667	0.457	0.333	0.254	0.200	0.162
0.40	25.600	10.667	4.000	2.133	1.333	0.914	0.667	0.508	0.400	0.323
0.60	38.400	16.000	6.000	3.200	2.000	1.371	1.000	0.762	0.600	0.485
0.80	51.200	21.333	8.000	4.267	2.667	1.829	1.333	1.016	0.800	0.646
1.00	64.000	26.667	10.000	5.333	3.333	2.286	1.667	1.270	1.000	0.808
IEC SHORT TIME										
0.05	0.153	0.089	0.056	0.044	0.038	0.034	0.031	0.029	0.027	0.026
0.10	0.306	0.178	0.111	0.088	0.075	0.067	0.062	0.058	0.054	0.052
0.20	0.612	0.356	0.223	0.175	0.150	0.135	0.124	0.115	0.109	0.104
0.40	1.223	0.711	0.445	0.351	0.301	0.269	0.247	0.231	0.218	0.207
0.60	1.835	1.067	0.668	0.526	0.451	0.404	0.371	0.346	0.327	0.311
0.80	2.446	1.423	0.890	0.702	0.602	0.538	0.494	0.461	0.435	0.415
1.00	3.058	1.778	1.113	0.877	0.752	0.673	0.618	0.576	0.544	0.518

IAC CURVES:

The curves for the General Electric type IAC relay family are derived from the formulae:

$$T = \text{TDM} \times \left(A + \frac{B}{(I/I_{pkp}) - C} + \frac{D}{((I/I_{pkp}) - C)^2} + \frac{E}{((I/I_{pkp}) - C)^3} \right), \; T_{RESET} = TDM \times \left[\frac{t_r}{1 - (I/I_{pkp})^2} \right] \quad \textbf{(EQ 5.12)}$$

where: T = operate time (in seconds), TDM = Multiplier setting, I = Input current, I_{pkp} = Pickup Current setting, A *to* E = constants, t_r = characteristic constant, and T_{RESET} = reset time in seconds (assuming energy capacity is 100% and **RESET** is "Timed")

Table 5–19: GE TYPE IAC INVERSE TIME CURVE CONSTANTS

IAC CURVE SHAPE	A	B	C	D	E	T_R
IAC Extreme Inverse	0.0040	0.6379	0.6200	1.7872	0.2461	6.008
IAC Very Inverse	0.0900	0.7955	0.1000	–1.2885	7.9586	4.678
IAC Inverse	0.2078	0.8630	0.8000	–0.4180	0.1947	0.990
IAC Short Inverse	0.0428	0.0609	0.6200	–0.0010	0.0221	0.222

Table 5–20: IAC CURVE TRIP TIMES

MULTIPLIER (TDM)	CURRENT (I / I_{pickup})									
	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
IAC EXTREMELY INVERSE										
0.5	1.699	0.749	0.303	0.178	0.123	0.093	0.074	0.062	0.053	0.046
1.0	3.398	1.498	0.606	0.356	0.246	0.186	0.149	0.124	0.106	0.093
2.0	6.796	2.997	1.212	0.711	0.491	0.372	0.298	0.248	0.212	0.185
4.0	13.591	5.993	2.423	1.422	0.983	0.744	0.595	0.495	0.424	0.370
6.0	20.387	8.990	3.635	2.133	1.474	1.115	0.893	0.743	0.636	0.556
8.0	27.183	11.987	4.846	2.844	1.966	1.487	1.191	0.991	0.848	0.741
10.0	33.979	14.983	6.058	3.555	2.457	1.859	1.488	1.239	1.060	0.926
IAC VERY INVERSE										
0.5	1.451	0.656	0.269	0.172	0.133	0.113	0.101	0.093	0.087	0.083
1.0	2.901	1.312	0.537	0.343	0.266	0.227	0.202	0.186	0.174	0.165
2.0	5.802	2.624	1.075	0.687	0.533	0.453	0.405	0.372	0.349	0.331
4.0	11.605	5.248	2.150	1.374	1.065	0.906	0.810	0.745	0.698	0.662
6.0	17.407	7.872	3.225	2.061	1.598	1.359	1.215	1.117	1.046	0.992
8.0	23.209	10.497	4.299	2.747	2.131	1.813	1.620	1.490	1.395	1.323
10.0	29.012	13.121	5.374	3.434	2.663	2.266	2.025	1.862	1.744	1.654
IAC INVERSE										
0.5	0.578	0.375	0.266	0.221	0.196	0.180	0.168	0.160	0.154	0.148
1.0	1.155	0.749	0.532	0.443	0.392	0.360	0.337	0.320	0.307	0.297
2.0	2.310	1.499	1.064	0.885	0.784	0.719	0.674	0.640	0.614	0.594
4.0	4.621	2.997	2.128	1.770	1.569	1.439	1.348	1.280	1.229	1.188
6.0	6.931	4.496	3.192	2.656	2.353	2.158	2.022	1.921	1.843	1.781
8.0	9.242	5.995	4.256	3.541	3.138	2.878	2.695	2.561	2.457	2.375
10.0	11.552	7.494	5.320	4.426	3.922	3.597	3.369	3.201	3.072	2.969
IAC SHORT INVERSE										
0.5	0.072	0.047	0.035	0.031	0.028	0.027	0.026	0.026	0.025	0.025
1.0	0.143	0.095	0.070	0.061	0.057	0.054	0.052	0.051	0.050	0.049
2.0	0.286	0.190	0.140	0.123	0.114	0.108	0.105	0.102	0.100	0.099
4.0	0.573	0.379	0.279	0.245	0.228	0.217	0.210	0.204	0.200	0.197
6.0	0.859	0.569	0.419	0.368	0.341	0.325	0.314	0.307	0.301	0.296
8.0	1.145	0.759	0.559	0.490	0.455	0.434	0.419	0.409	0.401	0.394
10.0	1.431	0.948	0.699	0.613	0.569	0.542	0.524	0.511	0.501	0.493

I2t CURVES:

The curves for the I^2t are derived from the formulae:

$$T = \text{TDM} \times \left[\frac{100}{\left(\frac{I}{I_{pickup}} \right)^2} \right], \quad T_{RESET} = \text{TDM} \times \left[\frac{100}{\left(\frac{I}{I_{pickup}} \right)^{-2}} \right] \qquad \textbf{(EQ 5.13)}$$

where: T = Operate Time (sec.); TDM = Multiplier Setting; I = Input Current; I_{pickup} = Pickup Current Setting; T_{RESET} = Reset Time in sec. (assuming energy capacity is 100% and RESET: Timed)

Table 5–21: I^2T CURVE TRIP TIMES

MULTIPLIER (TDM)	CURRENT (I / I_{pickup})									
	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
0.01	0.44	0.25	0.11	0.06	0.04	0.03	0.02	0.02	0.01	0.01
0.10	4.44	2.50	1.11	0.63	0.40	0.28	0.20	0.16	0.12	0.10
1.00	44.44	25.00	11.11	6.25	4.00	2.78	2.04	1.56	1.23	1.00
10.00	444.44	250.00	111.11	62.50	40.00	27.78	20.41	15.63	12.35	10.00
100.00	4444.4	2500.0	1111.1	625.00	400.00	277.78	204.08	156.25	123.46	100.00
600.00	26666.7	15000.0	6666.7	3750.0	2400.0	1666.7	1224.5	937.50	740.74	600.00

FLEXCURVES™:

The custom FlexCurves™ are described in detail in the FlexCurves™ section of this chapter. The curve shapes for the FlexCurves™ are derived from the formulae:

$$T = \text{TDM} \times \left[\text{FlexCurve Time at } \left(\frac{I}{I_{pickup}} \right) \right] \text{ when } \left(\frac{I}{I_{pickup}} \right) \geq 1.00 \qquad \textbf{(EQ 5.14)}$$

$$T_{RESET} = \text{TDM} \times \left[\text{FlexCurve Time at } \left(\frac{I}{I_{pickup}} \right) \right] \text{ when } \left(\frac{I}{I_{pickup}} \right) \leq 0.98 \qquad \textbf{(EQ 5.15)}$$

where: T = Operate Time (sec.), TDM = Multiplier setting
I = Input Current, I_{pickup} = Pickup Current setting
T_{RESET} = Reset Time in seconds (assuming energy capacity is 100% and RESET: Timed)

DEFINITE TIME CURVE:

The Definite Time curve shape operates as soon as the pickup level is exceeded for a specified period of time. The base definite time curve delay is in seconds. The curve multiplier of 0.00 to 600.00 makes this delay adjustable from instantaneous to 600.00 seconds in steps of 10 ms.

$$T = \text{TDM in seconds, when } I > I_{pickup} \qquad \textbf{(EQ 5.16)}$$

$$T_{RESET} = \text{TDM in seconds} \qquad \textbf{(EQ 5.17)}$$

where: T = Operate Time (sec.), TDM = Multiplier setting
I = Input Current, I_{pickup} = Pickup Current setting
T_{RESET} = Reset Time in seconds (assuming energy capacity is 100% and RESET: Timed)

RECLOSER CURVES:

The L60 uses the FlexCurve™ feature to facilitate programming of 41 recloser curves. Please refer to the FlexCurve™ section in this chapter for additional details.

c) PHASE TIME OVERCURRENT (ANSI 51P)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨ PHASE CURRENT ⇨ PHASE TOC1(2)

■ PHASE TOC1 ■		PHASE TOC1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	PHASE TOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	PHASE TOC1 INPUT: Phasor	Range: Phasor, RMS
	MESSAGE	PHASE TOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu in steps of 0.001
	MESSAGE	PHASE TOC1 CURVE: IEEE Mod Inv	Range: See Overcurrent Curve Types table
	MESSAGE	PHASE TOC1 TD MULTIPLIER: 1.00	Range: 0.00 to 600.00 in steps of 0.01
	MESSAGE	PHASE TOC1 RESET: Instantaneous	Range: Instantaneous, Timed
	MESSAGE	PHASE TOC1 VOLTAGE RESTRAINT: Disabled	Range: Disabled, Enabled
	MESSAGE	PHASE TOC1 BLOCK A: Off	Range: FlexLogic™ operand
	MESSAGE	PHASE TOC1 BLOCK B: Off	Range: FlexLogic™ operand
	MESSAGE	PHASE TOC1 BLOCK C: Off	Range: FlexLogic™ operand
	MESSAGE	PHASE TOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	PHASE TOC1 EVENTS: Disabled	Range: Disabled, Enabled

The phase time overcurrent element can provide a desired time-delay operating characteristic versus the applied current or be used as a simple Definite Time element. The phase current input quantities may be programmed as fundamental phasor magnitude or total waveform RMS magnitude as required by the application.

Two methods of resetting operation are available: “Timed” and “Instantaneous” (refer to the Inverse *TOC Curves Characteristic* sub-section earlier for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to “Instantaneous” and the element is blocked, the time accumulator will be cleared immediately.

The **PHASE TOC1 PICKUP** setting can be dynamically reduced by a voltage restraint feature (when enabled). This is accomplished via the multipliers (Mvr) corresponding to the phase-phase voltages of the voltage restraint characteristic curve (see the figure below); the pickup level is calculated as ‘Mvr’ times the **PHASE TOC1 PICKUP** setting. If the voltage restraint feature is disabled, the pickup level always remains at the setting value.

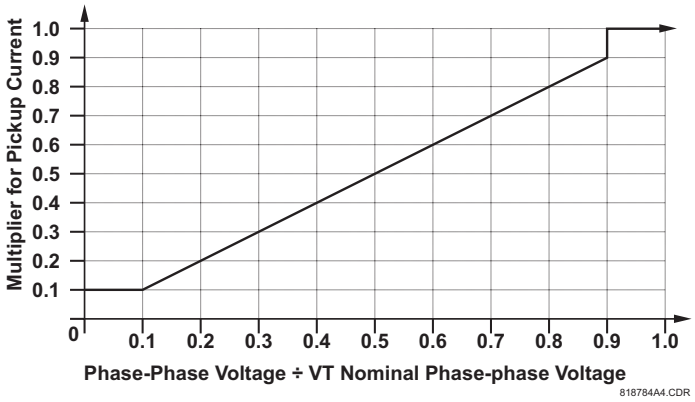


Figure 5–75: PHASE TOC VOLTAGE RESTRAINT CHARACTERISTIC

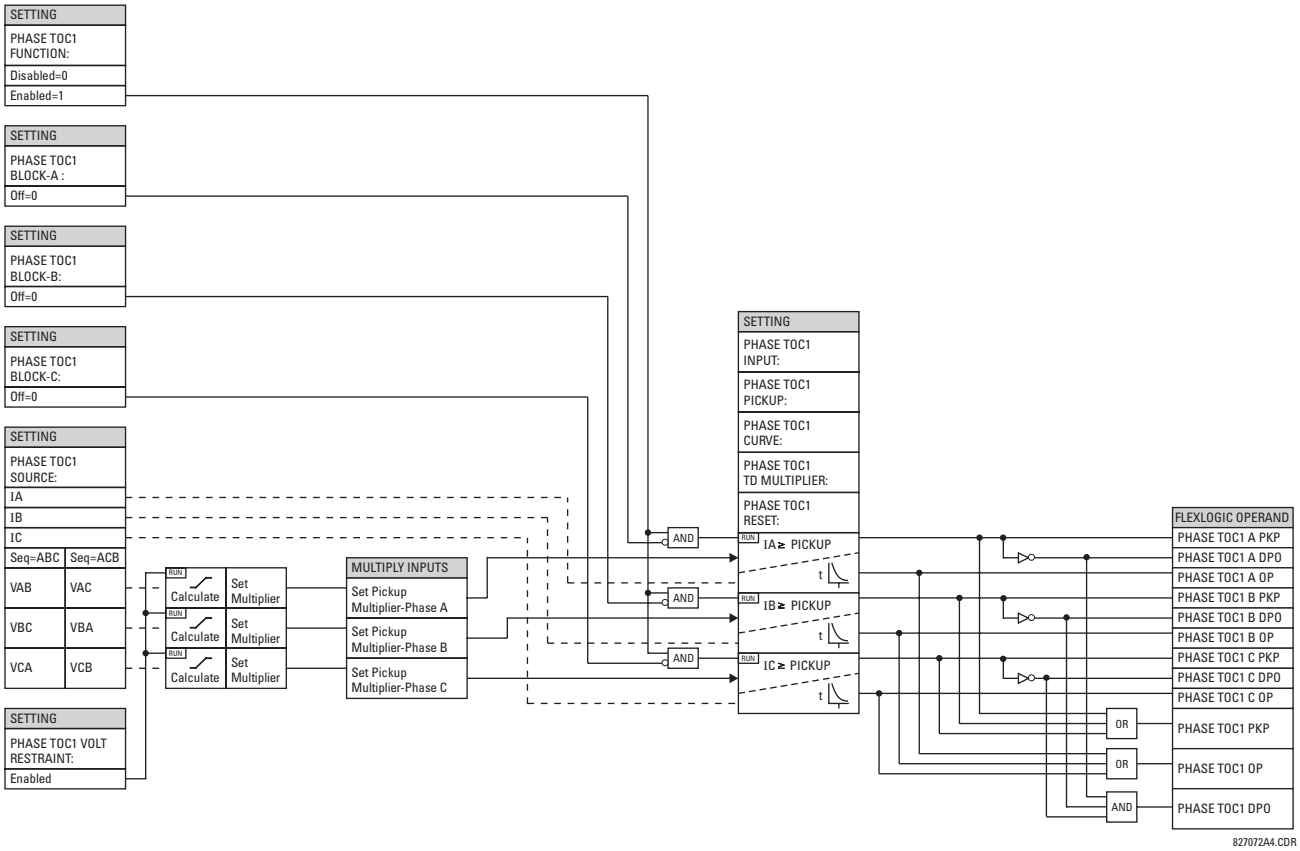


Figure 5–76: PHASE TOC1 SCHEME LOGIC

d) PHASE INSTANTANEOUS OVERCURRENT (ANSI 50P)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨ PHASE CURRENT ⇨ PHASE IOC 1(2)

■ PHASE IOC1 ■	PHASE IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	PHASE IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
MESSAGE	PHASE IOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu in steps of 0.001
MESSAGE	PHASE IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 to 600.00 s in steps of 0.01
MESSAGE	PHASE IOC1 RESET DELAY: 0.00 s	Range: 0.00 to 600.00 s in steps of 0.01
MESSAGE	PHASE IOC1 BLOCK A: Off	Range: FlexLogic™ operand
MESSAGE	PHASE IOC1 BLOCK B: Off	Range: FlexLogic™ operand
MESSAGE	PHASE IOC1 BLOCK C: Off	Range: FlexLogic™ operand
MESSAGE	PHASE IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	PHASE IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The phase instantaneous overcurrent element may be used as an instantaneous element with no intentional delay or as a Definite Time element. The input current is the fundamental phasor magnitude.

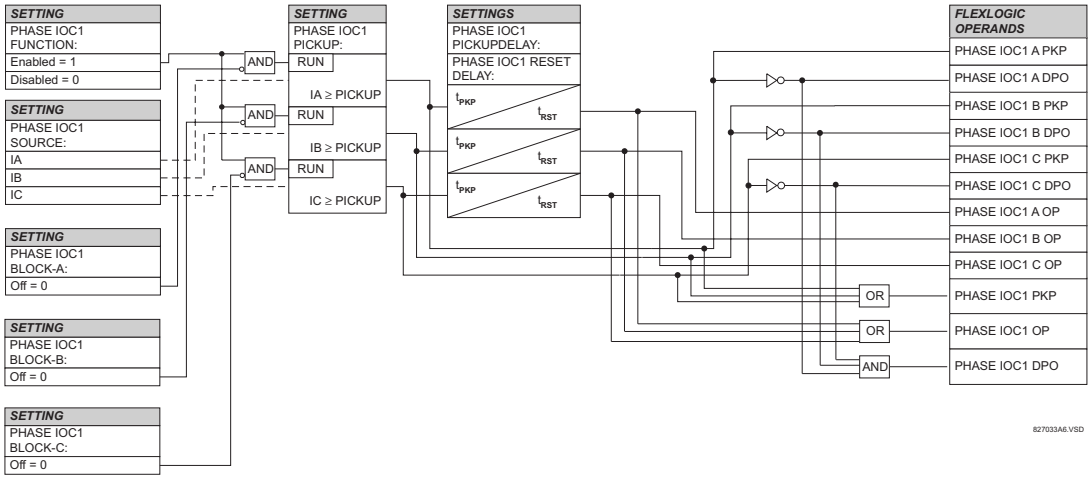


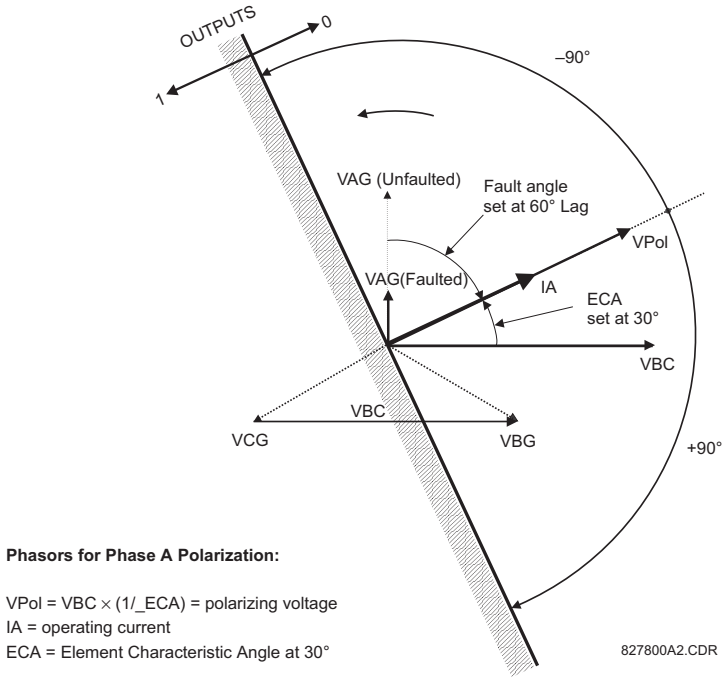
Figure 5–77: PHASE IOC1 SCHEME LOGIC

e) PHASE DIRECTIONAL OVERCURRENT (ANSI 51P)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨ PHASE CURRENT ⇨ PHASE DIRECTIONAL 1(2)

■ PHASE ■ DIRECTIONAL 1		PHASE DIR 1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	PHASE DIR 1 SIGNAL SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	PHASE DIR 1 BLOCK: Off	*Range: FlexLogic™ operand*
	MESSAGE	PHASE DIR 1 ECA: 30	*Range: 0 to 359° in steps of 1*
	MESSAGE	PHASE DIR POL V1 THRESHOLD: 0.700 pu	*Range: 0.000 to 3.000 pu in steps of 0.001*
	MESSAGE	PHASE DIR 1 BLOCK WHEN V MEM EXP: No	*Range: No, Yes*
	MESSAGE	PHASE DIR 1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	PHASE DIR 1 EVENTS: Disabled	*Range: Disabled, Enabled*

The phase directional elements (one for each of phases A, B, and C) determine the phase current flow direction for steady state and fault conditions and can be used to control the operation of the phase overcurrent elements via the **BLOCK** inputs of these elements.



Phasors for Phase A Polarization:

VPol = VBC × (1/_ECA) = polarizing voltage
IA = operating current
ECA = Element Characteristic Angle at 30°

Figure 5–78: PHASE A DIRECTIONAL POLARIZATION

This element is intended to apply a block signal to an overcurrent element to prevent an operation when current is flowing in a particular direction. The direction of current flow is determined by measuring the phase angle between the current from the phase CTs and the line-line voltage from the VTs, based on the 90° or quadrature connection. If there is a requirement to supervise overcurrent elements for flows in opposite directions, such as can happen through a bus-tie breaker, two phase directional elements should be programmed with opposite element characteristic angle (ECA) settings.

To increase security for three phase faults very close to the VTs used to measure the polarizing voltage, a voltage memory feature is incorporated. This feature stores the polarizing voltage the moment before the voltage collapses, and uses it to determine direction. The voltage memory remains valid for one second after the voltage has collapsed.

The main component of the phase directional element is the phase angle comparator with two inputs: the operating signal (phase current) and the polarizing signal (the line voltage, shifted in the leading direction by the characteristic angle, ECA).

The following table shows the operating and polarizing signals used for phase directional control:

PHASE	OPERATING SIGNAL	POLARIZING SIGNAL V_{pol}	
		ABC PHASE SEQUENCE	ACB PHASE SEQUENCE
A	angle of IA	angle of VBC × (1∠ECA)	angle of VCB × (1∠ECA)
B	angle of IB	angle of VCA × (1∠ECA)	angle of VAC × 1∠ECA)
C	angle of IC	angle of VAB × (1∠ECA)	angle of VBA × (1∠ECA)

MODE OF OPERATION:

- When the function is “Disabled”, or the operating current is below 5% × CT nominal, the element output is “0”.
- When the function is “Enabled”, the operating current is above 5% × CT nominal, and the polarizing voltage is above the **PRODUCT SETUP ⇨⇩ DISPLAY PROPERTIES ⇨⇩ VOLTAGE CUT-OFF LEVEL** value, the element output is dependent on the phase angle between the operating and polarizing signals:
  – The element output is logic “0” when the operating current is within polarizing voltage ±90°.
  – For all other angles, the element output is logic “1”.
- Once the voltage memory has expired, the phase overcurrent elements under directional control can be set to block or trip on overcurrent as follows:
  – When **BLOCK WHEN V MEM EXP** is set to “Yes”, the directional element will block the operation of any phase overcurrent element under directional control when voltage memory expires.
  – When **BLOCK WHEN V MEM EXP** is set to “No”, the directional element allows tripping of phase overcurrent elements under directional control when voltage memory expires.

In all cases, directional blocking will be permitted to resume when the polarizing voltage becomes greater than the ‘polarizing voltage threshold’.

SETTINGS:

- **PHASE DIR 1 SIGNAL SOURCE:** This setting is used to select the source for the operating and polarizing signals. The operating current for the phase directional element is the phase current for the selected current source. The polarizing voltage is the line voltage from the phase VTs, based on the 90° or ‘quadrature’ connection and shifted in the leading direction by the element characteristic angle (ECA).
- **PHASE DIR 1 ECA:** This setting is used to select the element characteristic angle, i.e. the angle by which the polarizing voltage is shifted in the leading direction to achieve dependable operation. In the design of the UR-series elements, a block is applied to an element by asserting logic 1 at the blocking input. This element should be programmed via the ECA setting so that the output is **logic 1 for current in the non-tripping direction**.
- **PHASE DIR 1 POL V THRESHOLD:** This setting is used to establish the minimum level of voltage for which the phase angle measurement is reliable. The setting is based on VT accuracy. The default value is “0.700 pu”.
- **PHASE DIR 1 BLOCK WHEN V MEM EXP:** This setting is used to select the required operation upon expiration of voltage memory. When set to "Yes", the directional element blocks the operation of any phase overcurrent element under directional control, when voltage memory expires; when set to "No", the directional element allows tripping of phase overcurrent elements under directional control.

NOTE

The phase directional element responds to the forward load current. In the case of a following reverse fault, the element needs some time – in the order of 8 ms – to establish a blocking signal. Some protection elements such as instantaneous overcurrent may respond to reverse faults before the blocking signal is established. Therefore, a coordination time of at least 10 ms must be added to all the instantaneous protection elements under the supervision of the phase directional element. If current reversal is of a concern, a longer delay – in the order of 20 ms – may be needed.

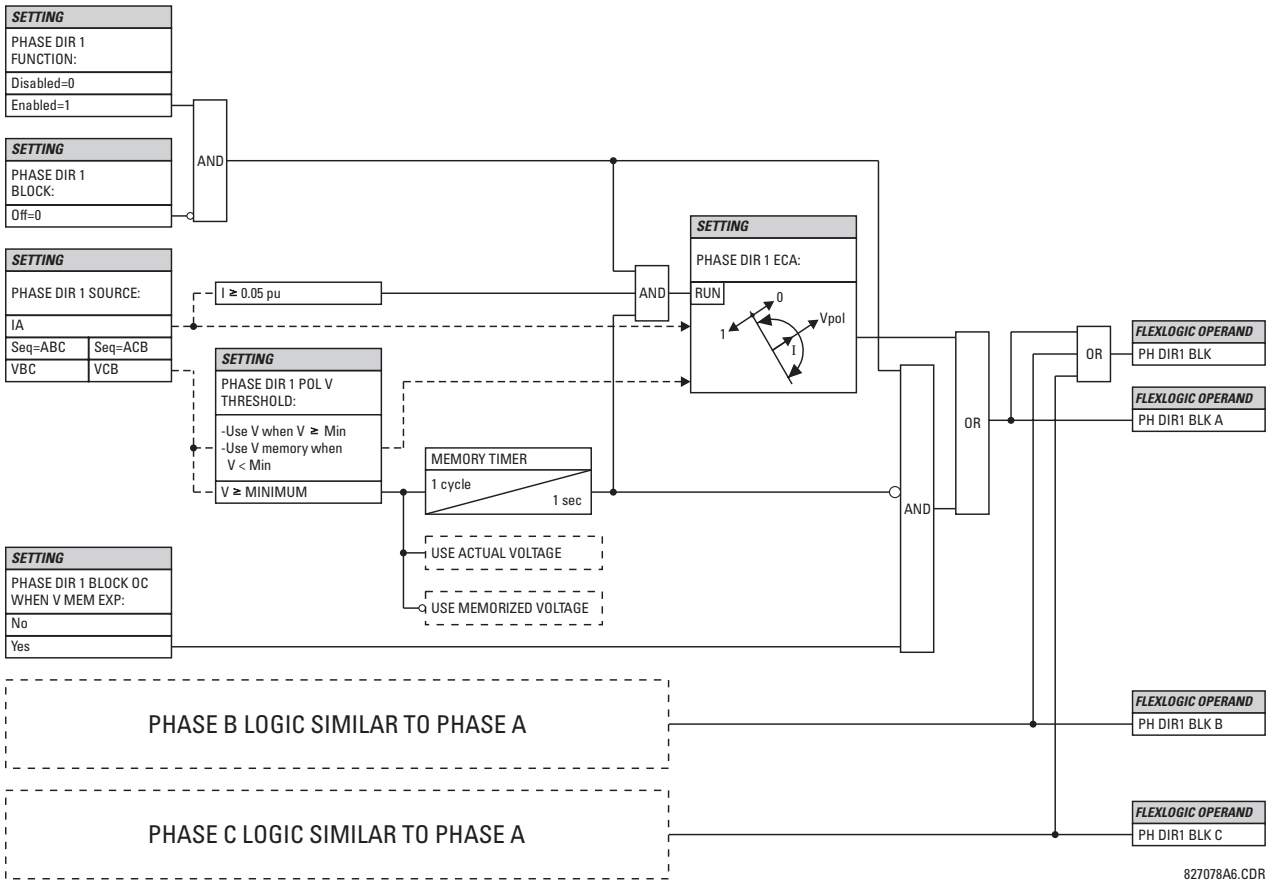


Figure 5–79: PHASE DIRECTIONAL SCHEME LOGIC

5.5.9 NEUTRAL CURRENT

a) MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ NEUTRAL CURRENT

■ NEUTRAL CURRENT ■	◀▶	■ NEUTRAL TOC1 ■	See page 5–152.
MESSAGE	▲▼	■ NEUTRAL TOC2 ■	See page 5–152.
MESSAGE	▲▼	■ NEUTRAL IOC1 ■	See page 5–153.
MESSAGE	▲▼	■ NEUTRAL IOC2 ■	See page 5–153.
MESSAGE	▲▼	■ NEUTRAL ■ DIRECTIONAL 1	See page 5–154.
MESSAGE	▲	■ NEUTRAL ■ DIRECTIONAL 2	See page 5–154.

The L60 Line Phase Comparison System has two (2) Neutral Time Overcurrent, two (2) Neutral Instantaneous Overcurrent, and two (2) Neutral Directional Overcurrent elements. These elements are described in the following sub-sections.

b) NEUTRAL TIME OVERCURRENT (ANSI 51N)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ NEUTRAL CURRENT ⇨ NEUTRAL TOC1(2)

■ NEUTRAL TOC1 ■	NEUTRAL TOC1 FUNCTION: Disabled	*Range: Disabled, Enabled*
MESSAGE	NEUTRAL TOC1 SIGNAL SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
MESSAGE	NEUTRAL TOC1 INPUT: Phasor	*Range: Phasor, RMS*
MESSAGE	NEUTRAL TOC1 PICKUP: 1.000 pu	*Range: 0.000 to 30.000 pu in steps of 0.001*
MESSAGE	NEUTRAL TOC1 CURVE: IEEE Mod Inv	*Range: See OVERCURRENT CURVE TYPES table*
MESSAGE	NEUTRAL TOC1 TD MULTIPLIER: 1.00	*Range: 0.00 to 600.00 in steps of 0.01*
MESSAGE	NEUTRAL TOC1 RESET: Instantaneous	*Range: Instantaneous, Timed*
MESSAGE	NEUTRAL TOC1 BLOCK: Off	*Range: FlexLogic™ operand*
MESSAGE	NEUTRAL TOC1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
MESSAGE	NEUTRAL TOC1 EVENTS: Disabled	*Range: Disabled, Enabled*

The neutral time overcurrent element can provide a desired time-delay operating characteristic versus the applied current or be used as a simple definite time element. The neutral current input value is a quantity calculated as 3Io from the phase currents and may be programmed as fundamental phasor magnitude or total waveform RMS magnitude as required by the application.

Two methods of resetting operation are available: “Timed” and “Instantaneous” (refer to the *Inverse TOC Curve Characteristics* section for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to “Instantaneous” and the element is blocked, the time accumulator will be cleared immediately.

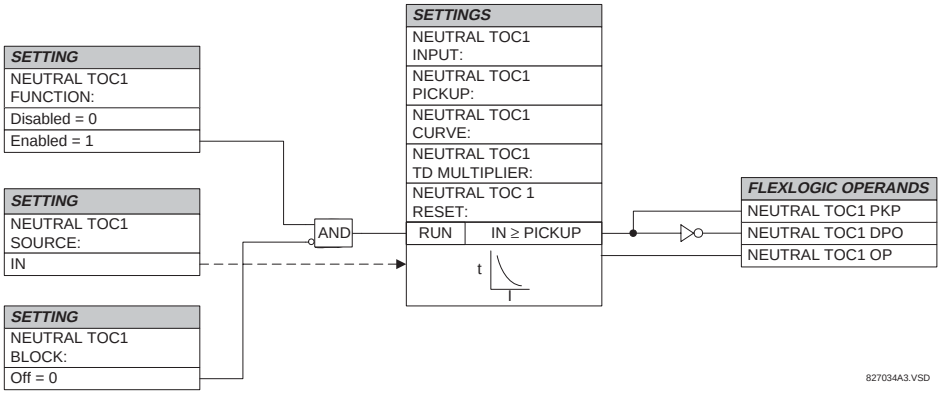


Figure 5–80: NEUTRAL TOC1 SCHEME LOGIC

c) NEUTRAL INSTANTANEOUS OVERCURRENT (ANSI 50N)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ NEUTRAL CURRENT ⇨⇩ NEUTRAL IOC1(2)

■ NEUTRAL IOC1 ■		NEUTRAL IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	NEUTRAL IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	NEUTRAL IOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu in steps of 0.001
	MESSAGE	NEUTRAL IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	NEUTRAL IOC1 RESET DELAY: 0.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	NEUTRAL IOC1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	NEUTRAL IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	NEUTRAL IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The neutral instantaneous overcurrent element may be used as an instantaneous function with no intentional delay or as a definite time function. The element essentially responds to the magnitude of a neutral current fundamental frequency phasor calculated from the phase currents. A positive-sequence restraint is applied for better performance. A small portion (6.25%) of the positive-sequence current magnitude is subtracted from the zero-sequence current magnitude when forming the operating quantity of the element as follows:

$$I_{op} = 3 \times (|I\_0| - K \cdot |I\_1|) \quad \text{where } K = 1/16 \qquad \textbf{(EQ 5.18)}$$

The positive-sequence restraint allows for more sensitive settings by counterbalancing spurious zero-sequence currents resulting from:

- system unbalances under heavy load conditions
- transformation errors of current transformers (CTs) during double-line and three-phase faults
- switch-off transients during double-line and three-phase faults

The positive-sequence restraint must be considered when testing for pickup accuracy and response time (multiple of pickup). The operating quantity depends on how test currents are injected into the relay (single-phase injection: $I_{op} = 0.9375 \cdot I_{injected}$; three-phase pure zero-sequence injection: $I_{op} = 3 \times I_{injected}$).

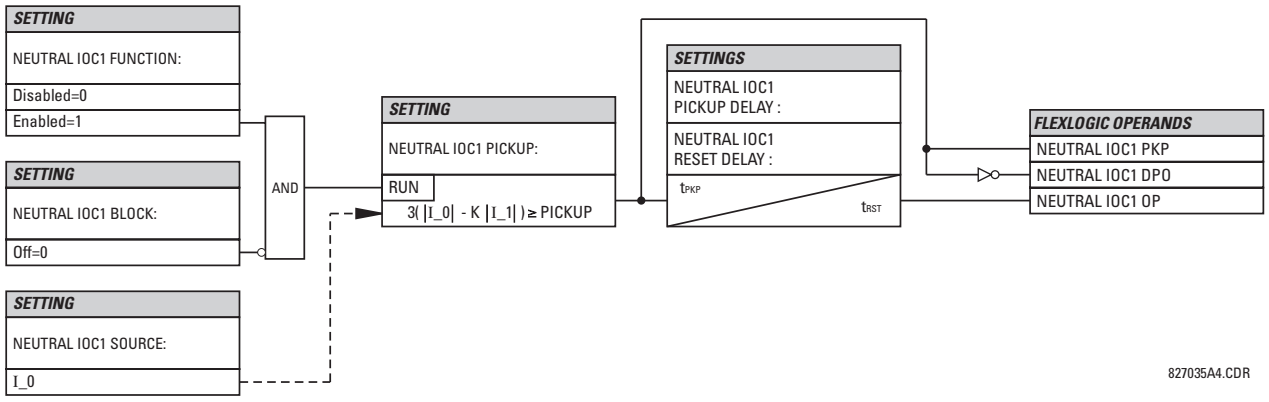


Figure 5–81: NEUTRAL IOC1 SCHEME LOGIC

d) NEUTRAL DIRECTIONAL OVERCURRENT (ANSI 67N)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨ NEUTRAL CURRENT ⇨⇩ NEUTRAL DIRECTIONAL OC1(2)

■ NEUTRAL ■ DIRECTIONAL OC1		NEUTRAL DIR OC1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	NEUTRAL DIR OC1 SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	NEUTRAL DIR OC1 POLARIZING: Voltage	*Range: Voltage, Current, Dual*
	MESSAGE	NEUTRAL DIR OC1 POL VOLT: Calculated V0	*Range: Calculated V0, Measured VX*
	MESSAGE	NEUTRAL DIR OC1 OP CURR: Calculated 3I0	*Range: Calculated 3I0, Measured IG*
	MESSAGE	NEUTRAL DIR OC1 POS- SEQ RESTRAINT: 0.063	*Range: 0.000 to 0.500 in steps of 0.001*
	MESSAGE	NEUTRAL DIR OC1 OFFSET: 0.00 Ω	*Range: 0.00 to 250.00 Ω in steps of 0.01*
	MESSAGE	NEUTRAL DIR OC1 FWD ECA: 75° Lag	*Range: –90 to 90° in steps of 1*
	MESSAGE	NEUTRAL DIR OC1 FWD LIMIT ANGLE: 90°	*Range: 40 to 90° in steps of 1*
	MESSAGE	NEUTRAL DIR OC1 FWD PICKUP: 0.050 pu	*Range: 0.002 to 30.000 pu in steps of 0.001*
	MESSAGE	NEUTRAL DIR OC1 REV LIMIT ANGLE: 90°	*Range: 40 to 90° in steps of 1*
	MESSAGE	NEUTRAL DIR OC1 REV PICKUP: 0.050 pu	*Range: 0.002 to 30.000 pu in steps of 0.001*
	MESSAGE	NEUTRAL DIR OC1 BLK: Off	*Range: FlexLogic™ operand*
	MESSAGE	NEUTRAL DIR OC1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	NEUTRAL DIR OC1 EVENTS: Disabled	*Range: Disabled, Enabled*

There are two Neutral Directional Overcurrent protection elements available. The element provides both forward and reverse fault direction indications the NEUTRAL DIR OC1 FWD and NEUTRAL DIR OC1 REV operands, respectively. The output operand is asserted if the magnitude of the operating current is above a pickup level (overcurrent unit) and the fault direction is seen as “forward or “reverse”, respectively (directional unit).

The **overcurrent unit** responds to the magnitude of a fundamental frequency phasor of the either the neutral current calculated from the phase currents or the ground current. There are two separate pickup settings for the forward- and reverse-looking functions, respectively. If set to use the calculated 3I_0, the element applies a “positive-sequence restraint” for better performance: a small user-programmable portion of the positive–sequence current magnitude is subtracted from the zero-sequence current magnitude when forming the operating quantity.

$$I_{op} = 3 \times (|I\_0| - K \times |I\_1|) \quad \textbf{(EQ 5.19)}$$

The positive-sequence restraint allows for more sensitive settings by counterbalancing spurious zero-sequence currents resulting from:

- System unbalances under heavy load conditions.

- Transformation errors of current transformers (CTs) during double-line and three-phase faults.
- Switch-off transients during double-line and three-phase faults.

The positive-sequence restraint must be considered when testing for pickup accuracy and response time (multiple of pickup). The operating quantity depends on the way the test currents are injected into the relay (single-phase injection: $I_{op} = (1 - K) \times I_{injected}$; three-phase pure zero-sequence injection: $I_{op} = 3 \times I_{injected}$).

The positive-sequence restraint is removed for low currents. If the positive-sequence current is below 0.8 pu, the restraint is removed by changing the constant *K* to zero. This facilitates better response to high-resistance faults when the unbalance is very small and there is no danger of excessive CT errors as the current is low.

The **directional unit** uses the zero-sequence current (I_0) or ground current (IG) for fault direction discrimination and may be programmed to use either zero-sequence voltage ("Calculated V0" or "Measured VX"), ground current (IG), or both for polarizing. The following tables define the neutral directional overcurrent element.

Table 5–22: QUANTITIES FOR "CALCULATED 3I0" CONFIGURATION

DIRECTIONAL UNIT				OVERCURRENT UNIT
POLARIZING MODE	DIRECTION	COMPARED PHASORS		
Voltage	Forward	–V_0 + Z_offset × I_0	I_0 × 1∠ECA	$I_{op} = 3 \times (\lvert I\_0\rvert - K \times \lvert I\_1\rvert)$ if $\lvert I_1\rvert > 0.8$ pu $I_{op} = 3 \times (\lvert I\_0\rvert)$ if $\lvert I_1\rvert \le 0.8$ pu
	Reverse	–V_0 + Z_offset × I_0	–I_0 × 1∠ECA	
Current	Forward	IG	I_0	
	Reverse	IG	–I_0	
Dual	Forward	–V_0 + Z_offset × I_0	I_0 × 1∠ECA	
		or		
		IG	I_0	
	Reverse	–V_0 + Z_offset × I_0	–I_0 × 1∠ECA	
		or		
		IG	–I_0	

Table 5–23: QUANTITIES FOR "MEASURED IG" CONFIGURATION

DIRECTIONAL UNIT				OVERCURRENT UNIT
POLARIZING MODE	DIRECTION	COMPARED PHASORS		
Voltage	Forward	–V_0 + Z_offset × IG/3	IG × 1∠ECA	$I_{op} = \lvert IG\rvert$
	Reverse	–V_0 + Z_offset × IG/3	–IG × 1∠ECA	

where: $V\_0 = \frac{1}{3}(VAG + VBG + VCG)$ = zero sequence voltage ,

$I\_0 = \frac{1}{3}IN = \frac{1}{3}(IA + IB + IC)$ = zero sequence current ,

ECA = element characteristic angle and IG = ground current

When **NEUTRAL DIR OC1 POL VOLT** is set to "Measured VX", one-third of this voltage is used in place of V_0. The following figure explains the usage of the voltage polarized directional unit of the element.

The figure below shows the voltage-polarized phase angle comparator characteristics for a phase A to ground fault, with:

ECA = 90° (element characteristic angle = centerline of operating characteristic)
FWD LA = 80° (forward limit angle = the ± angular limit with the ECA for operation)
REV LA = 80° (reverse limit angle = the ± angular limit with the ECA for operation)

The element incorporates a current reversal logic: if the reverse direction is indicated for at least 1.25 of a power system cycle, the prospective forward indication will be delayed by 1.5 of a power system cycle. The element is designed to emulate an electromechanical directional device. Larger operating and polarizing signals will result in faster directional discrimination bringing more security to the element operation.

The forward-looking function is designed to be more secure as compared to the reverse-looking function, and therefore, should be used for the tripping direction. The reverse-looking function is designed to be faster as compared to the forward-looking function and should be used for the blocking direction. This allows for better protection coordination.

The above bias should be taken into account when using the neutral directional overcurrent element to directionalize other protection elements.

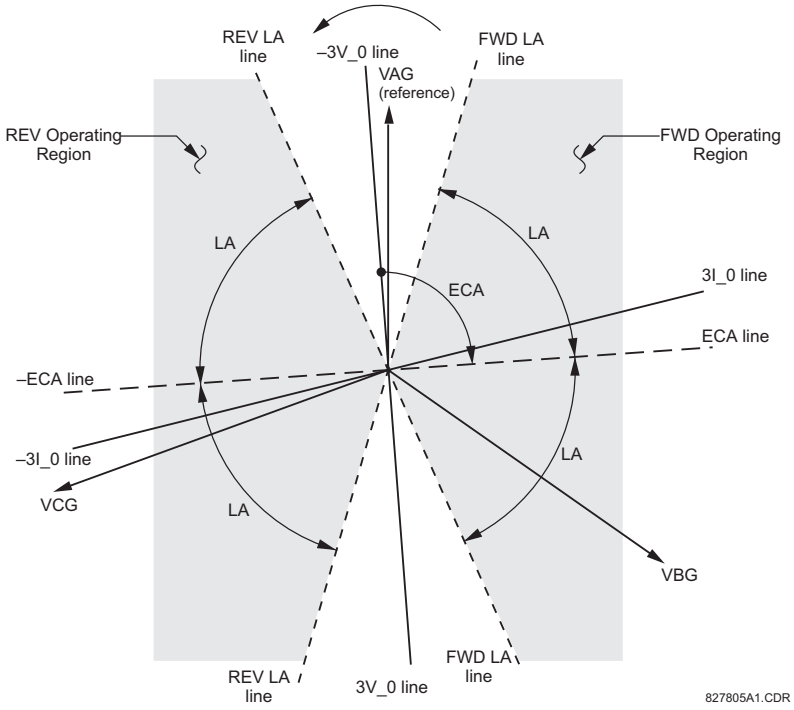


Figure 5–82: NEUTRAL DIRECTIONAL VOLTAGE-POLARIZED CHARACTERISTICS

- **NEUTRAL DIR OC1 POLARIZING:** This setting selects the polarizing mode for the directional unit.
  - If “Voltage” polarizing is selected, the element uses the zero-sequence voltage angle for polarization. The user can use either the zero-sequence voltage V_0 calculated from the phase voltages, or the zero-sequence voltage supplied externally as the auxiliary voltage Vx, both from the **NEUTRAL DIR OC1 SOURCE**.

    The calculated V_0 can be used as polarizing voltage only if the voltage transformers are connected in Wye. The auxiliary voltage can be used as the polarizing voltage provided **SYSTEM SETUP** ⇨ **AC INPUTS** ⇨⇩ **VOLTAGE BANK** ⇨⇩ **AUXILIARY VT CONNECTION** is set to “Vn” and the auxiliary voltage is connected to a zero-sequence voltage source (such as open delta connected secondary of VTs).

    The zero-sequence (V_0) or auxiliary voltage (Vx), accordingly, must be higher than the **PRODUCT SETUP** ⇨⇩ **DISPLAY PROPERTIES** ⇨⇩ **VOLTAGE CUT-OFF LEVEL** value to be validated for use as a polarizing signal. If the polarizing signal is invalid, neither forward nor reverse indication is given.
  - If “Current” polarizing is selected, the element uses the ground current angle connected externally and configured under **NEUTRAL OC1 SOURCE** for polarization. The Ground CT must be connected between the ground and neutral point of an adequate local source of ground current. The ground current must be higher than 0.05 pu to be validated as a polarizing signal. If the polarizing signal is not valid, neither forward nor reverse indication is given.

    For a choice of current polarizing, it is recommended that the polarizing signal be analyzed to ensure that a known direction is maintained irrespective of the fault location. For example, if using an autotransformer neutral current as a polarizing source, it should be ensured that a reversal of the ground current does not occur for a high-side fault. The low-side system impedance should be assumed minimal when checking for this condition. A similar situation arises for a Wye/Delta/Wye transformer, where current in one transformer winding neutral may reverse when faults on both sides of the transformer are considered.
  - If "Dual" polarizing is selected, the element performs both directional comparisons as described above. A given direction is confirmed if either voltage or current comparators indicate so. If a conflicting (simultaneous forward and reverse) indication occurs, the forward direction overrides the reverse direction.

- **NEUTRAL DIR OC1 POL VOLT:** Selects the polarizing voltage used by the directional unit when "Voltage" or "Dual" polarizing mode is set. The polarizing voltage can be programmed to be either the zero-sequence voltage calculated from the phase voltages ("Calculated V0") or supplied externally as an auxiliary voltage ("Measured VX").
- **NEUTRAL DIR OC1 OP CURR:** This setting indicates whether the 3I_0 current calculated from the phase currents, or the ground current shall be used by this protection. This setting acts as a switch between the neutral and ground modes of operation (67N and 67G). If set to “Calculated 3I0” the element uses the phase currents and applies the positive-sequence restraint; if set to “Measured IG” the element uses ground current supplied to the ground CT of the CT bank configured as **NEUTRAL DIR OC1 SOURCE**. If this setting is “Measured IG”, then the **NEUTRAL DIR OC1 POLARIZING** setting must be “Voltage”, as it is not possible to use the ground current as an operating and polarizing signal simultaneously.
- **NEUTRAL DIR OC1 POS-SEQ RESTRAINT**: This setting controls the amount of the positive-sequence restraint. Set to 0.063 for backward compatibility with firmware revision 3.40 and older. Set to zero to remove the restraint. Set higher if large system unbalances or poor CT performance are expected.
- **NEUTRAL DIR OC1 OFFSET:** This setting specifies the offset impedance used by this protection. The primary application for the offset impedance is to guarantee correct identification of fault direction on series compensated lines. See the Chapter 9 for information on how to calculate this setting. In regular applications, the offset impedance ensures proper operation even if the zero-sequence voltage at the relaying point is very small. If this is the intent, the offset impedance shall not be larger than the zero-sequence impedance of the protected circuit. Practically, it shall be several times smaller. See Chapter 8 for additional details. The offset impedance shall be entered in secondary ohms.
- **NEUTRAL DIR OC1 FWD ECA:** This setting defines the characteristic angle (ECA) for the forward direction in the "Voltage" polarizing mode. The "Current" polarizing mode uses a fixed ECA of 0°. The ECA in the reverse direction is the angle set for the forward direction shifted by 180°.
- **NEUTRAL DIR OC1 FWD LIMIT ANGLE:** This setting defines a symmetrical (in both directions from the ECA) limit angle for the forward direction.
- **NEUTRAL DIR OC1 FWD PICKUP:** This setting defines the pickup level for the overcurrent unit of the element in the forward direction. When selecting this setting it must be kept in mind that the design uses a ‘positive-sequence restraint’ technique for the “Calculated 3I0” mode of operation.
- **NEUTRAL DIR OC1 REV LIMIT ANGLE:** This setting defines a symmetrical (in both directions from the ECA) limit angle for the reverse direction.
- **NEUTRAL DIR OC1 REV PICKUP:** This setting defines the pickup level for the overcurrent unit of the element in the reverse direction. When selecting this setting it must be kept in mind that the design uses a ‘positive-sequence restraint’ technique for the “Calculated 3I0” mode of operation.

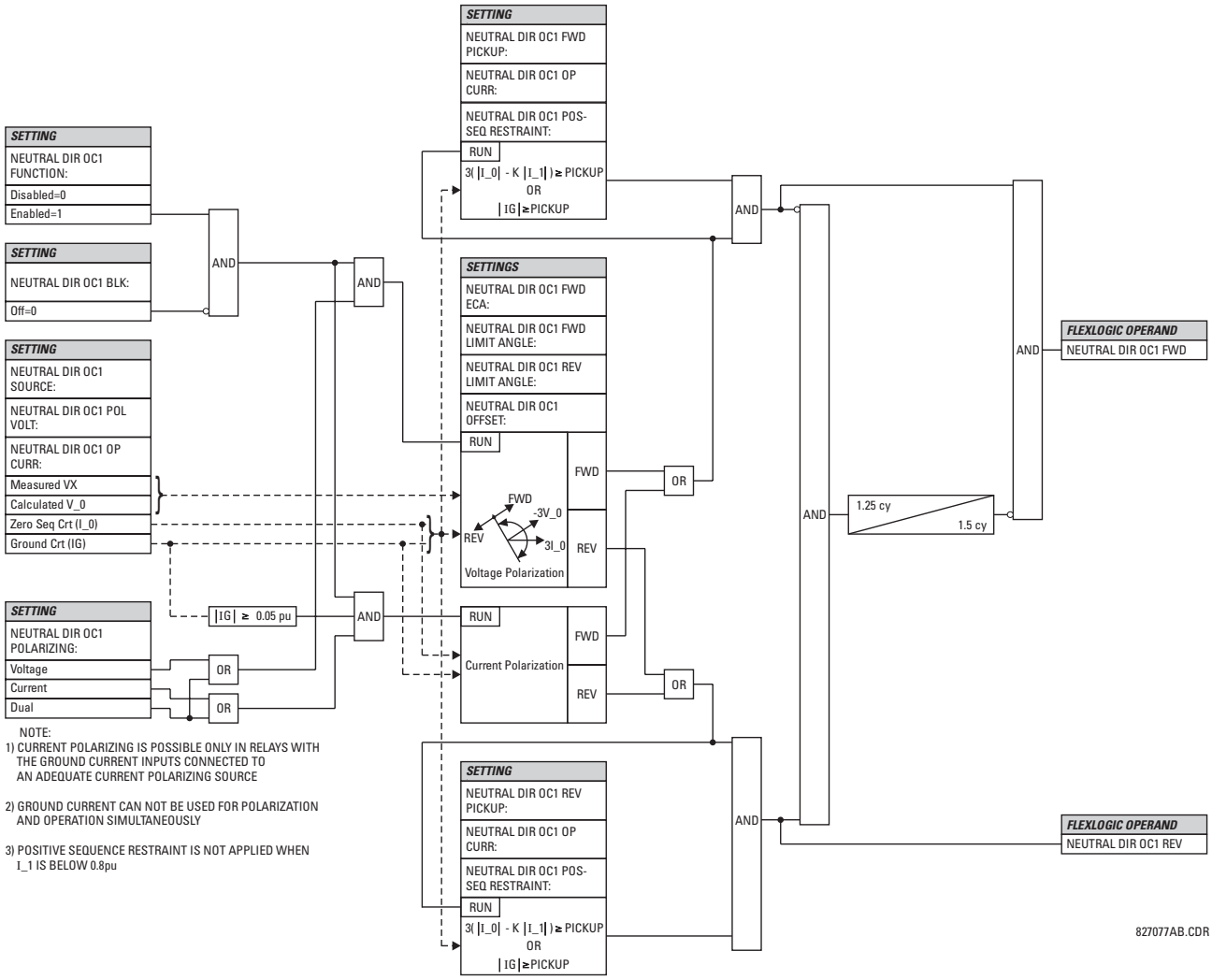


Figure 5–83: NEUTRAL DIRECTIONAL OVERCURRENT LOGIC

a) WATTMETRIC ZERO-SEQUENCE DIRECTIONAL (ANSI 32N)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨ WATTMETRIC... ⇨⇩ WATTMETRIC GROUND FAULT 1(2)

■ WATTMETRIC ■ GROUND FAULT 1		WATTMETRIC GND FLT 1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	WATTMETRIC GND FLT 1 SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	WATTMETRIC GND FLT 1 VOLT: Calculated VN	*Range: Calculated VN, Measured VX*
	MESSAGE	WATTMETRIC GND FLT 1 OV PKP: 0.20 pu	*Range: 0.02 to 3.00 pu in steps of 0.01*
	MESSAGE	WATTMETRIC GND FLT 1 CURR: Calculated IN	*Range: Calculated IN, Measured IG*
	MESSAGE	WATTMETRIC GND FLT 1 OC PKP: 0.060 pu	*Range: 0.002 to 30.000 pu in steps of 0.001*
	MESSAGE	WATTMETRIC GND FLT 1 OC PKP DEL: 0.20 s	*Range: 0.00 to 600.00 s in steps of 0.01*
	MESSAGE	WATTMETRIC GND FLT 1 PWR PKP: 0.100 pu	*Range: 0.001 to 1.200 pu in steps of 0.001*
	MESSAGE	WATTMETRIC GND FLT 1 REF PWR: 0.500 pu	*Range: 0.001 to 1.200 pu in steps of 0.001*
	MESSAGE	WATTMETRIC GND FLT 1 ECA: 0° Lag	*Range: 0 to 360° Lag in steps of 1*
	MESSAGE	WATTMETRIC GND FLT 1 PWR PKP DEL: 0.20 s	*Range: 0.00 to 600.00 s in steps of 0.01*
	MESSAGE	WATTMETRIC GND FLT 1 CURVE: Definite Time	*Range: Definite Time, Inverse, FlexCurves A through D*
	MESSAGE	WATTMETRIC GND FLT 1 MULTIPLIER: 1.00 s	*Range: 0.01 to 2.00 s in steps of 0.01*
	MESSAGE	WATT GND FLT 1 BLK: Off	*Range: FlexLogic™ operand*
	MESSAGE	WATTMETRIC GND FLT 1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	WATTMETRIC GND FLT 1 EVENTS: Disabled	*Range: Disabled, Enabled*

The wattmetric zero-sequence directional element responds to power derived from zero-sequence voltage and current in a direction specified by the element characteristic angle. The angle can be set within all four quadrants and the power can be active or reactive. Therefore, the element may be used to sense either forward or reverse ground faults in either inductive, capacitive or resistive networks. The inverse time characteristic allows time coordination of elements across the network.

Typical applications include ground fault protection in solidly grounded transmission networks, grounded/ungrounded/resistor-grounded/resonant-grounded distribution networks, or for directionalizing other non-directional ground elements.

- **WATTMETRIC GND FLT 1 VOLT**: The element uses neutral voltage (that is, three times the zero-sequence voltage). This setting allows selecting between the internally calculated neutral voltage, or externally supplied voltage (broken delta VT connected to the auxiliary channel bank of the relay). When the latter selection is made, the auxiliary channel

must be identified by the user as a neutral voltage under the VT bank settings. This element will operate only if the auxiliary voltage is configured as neutral.

- **WATTMETRIC GND FLT 1 OV PKP**: This setting specifies the minimum zero sequence voltage supervising the directional power measurement. This threshold should be higher than possible unbalance during normal operation of the system. Typically, this setting would be selected at 0.1 to 0.2 pu for the ungrounded or resonant grounded systems, and at 0.05 to 0.1 pu for solidly or resistor-grounded systems. When using externally supplied voltage via the auxiliary voltage channel, 1 pu is the nominal voltage of this channel as per VT bank settings. When using internally calculated neutral voltage, 1 pu is the nominal phase to ground voltage as per the VT bank settings.
- **WATTMETRIC GND FLT 1 CURR**: The element responds to the neutral current (that is, three times zero-sequence current), either calculated internally from the phase currents or supplied externally via the ground CT input from more accurate sources such as the core balanced CT. This setting allows selecting the source of the operating current.
- **WATTMETRIC GND FLT 1 OC PKP**: This setting specifies the current supervision level for the measurement of the zero-sequence power.
- **WATTMETRIC GND FLT 1 OC PKP DEL**: This setting specifies delay for the overcurrent portion of this element. The delay applies to the WATTMETRIC 1 PKP operand driven from the overcurrent condition.
- **WATTMETRIC GND FLT 1 PWR PKP**: This setting specifies the operating point of the element. A value of 1 pu is a product of the 1 pu voltage as specified for the overvoltage condition of this element, and 1 pu current as specified for the overcurrent condition of this element.
- **WATTMETRIC GND FLT 1 REF PWR**: This setting is used to calculate the inverse time characteristic delay (defined by S_{ref} in the following equations). A value of 1 pu represents the product of a 1 pu voltage (as specified in the overvoltage condition for this element) and a 1 pu current (as specified in the overcurrent condition for this element.
- **WATTMETRIC GND FLT 1 ECA**: This setting adjusts the maximum torque angle of the element. The operating power is calculated as:

$$\text{S\_op} = \text{Re}(V_n(I_n \times 1\angle \text{ECA})^*) \quad \textbf{(EQ 5.20)}$$

where * indicates complex conjugate. By varying the element characteristic angle (ECA), the element can be made to respond to forward or reverse direction in inductive, resistive, or capacitive networks as shown in the *Wattmetric characteristic angle response* diagram.

- **WATTMETRIC GND FLT 1 PWR PKP DEL**: This setting defines a definite time delay before the inverse time characteristic is activated. If the curve selection is set as “Definite Time”, the element would operate after this security time delay. If the curve selection is “Inverse” or one of the FlexCurves, the element uses both the definite and inverse time timers simultaneously. The definite time timer, specified by this setting, is used and when expires it releases the inverse time timer for operation (torque control).
- **WATTMETRIC GND FLT 1 CURVE**: This setting allows choosing one of three methods to delay operate signal once all conditions are met to discriminate fault direction.

  The “Definite Time” selection allows for a fixed time delay defined by the **WATTMETRIC GND FLT 1 PWR PKP DEL** setting.

  The “Inverse” selection allows for inverse time characteristics delay defined by the following formula:

$$t = m \times \frac{S_{ref}}{S_{op}} \quad \textbf{(EQ 5.21)}$$

where m is a multiplier defined by the multiplier setting, S_{ref} is the multiplier setting, and S_{op} is the operating power at the time. This timer starts after the definite time timer expires.

The four FlexCurves allow for custom user-programmable time characteristics. When working with FlexCurves, the element uses the operate to pickup ratio, and the multiplier setting is not applied:

$$t = \text{FlexCurve}\left(\frac{S_{op}}{S_{ref}}\right) \quad \textbf{(EQ 5.22)}$$

Again, the FlexCurve timer starts after the definite time timer expires.

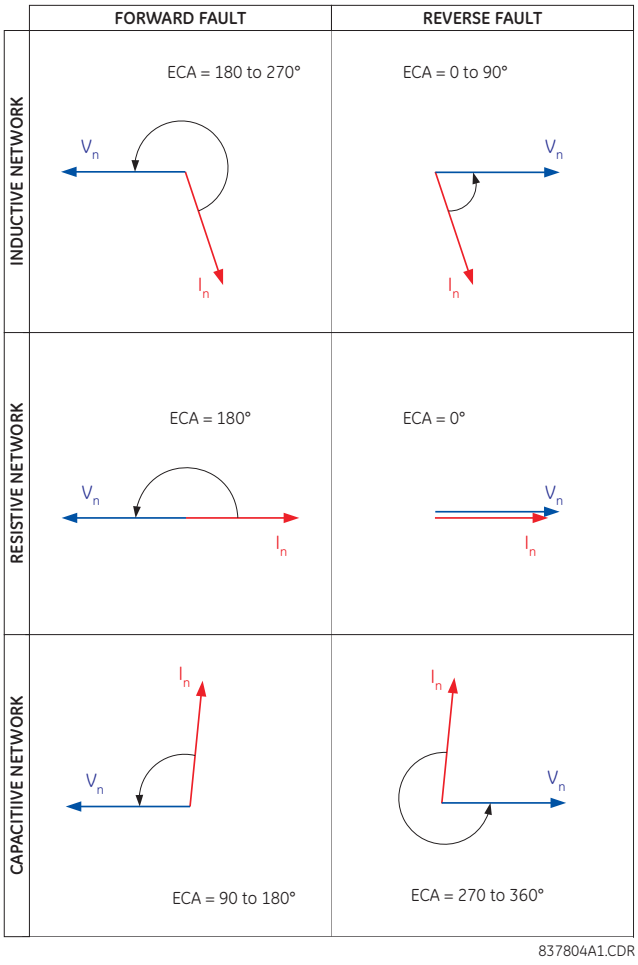


Figure 5–84: WATTMETRIC CHARACTERISTIC ANGLE RESPONSE

- **WATTMETRIC GND FLT 1 MULTIPLIER**: This setting is applicable if **WATTMETRIC GND FLT 1 CURVE** above is selected to Inverse and defines the multiplier factor for the inverse time delay.

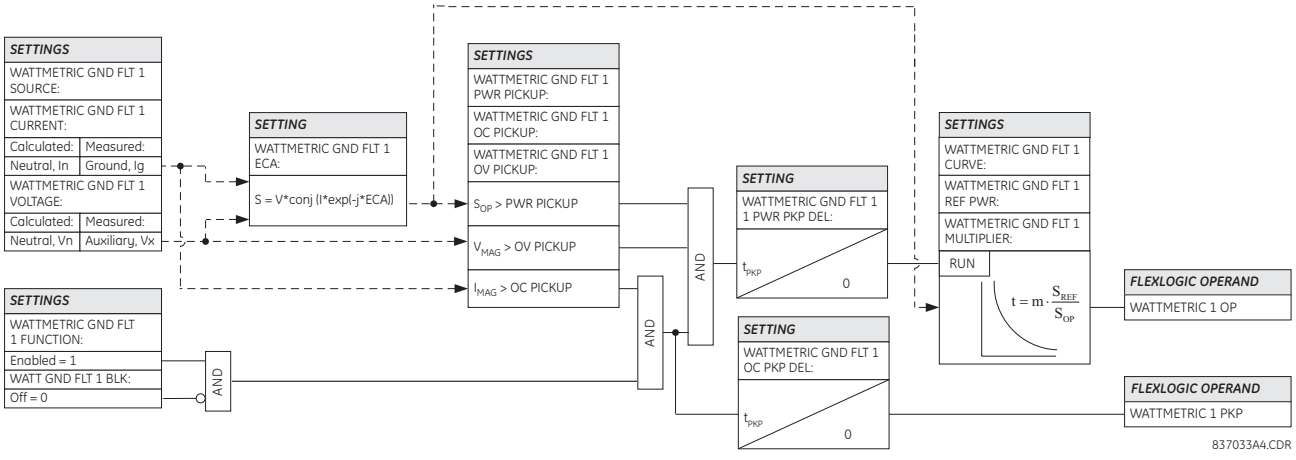


Figure 5–85: WATTMETRIC ZERO-SEQUENCE DIRECTIONAL LOGIC

a) GROUND TIME OVERCURRENT (ANSI 51G)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ GROUND CURRENT ⇨ GROUND TOC1(2)

■ GROUND TOC1 ■		GROUND TOC1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	GROUND TOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	GROUND TOC1 INPUT: Phasor	Range: Phasor, RMS
	MESSAGE	GROUND TOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu in steps of 0.001
	MESSAGE	GROUND TOC1 CURVE: IEEE Mod Inv	Range: see the Overcurrent Curve Types table
	MESSAGE	GROUND TOC1 TD MULTIPLIER: 1.00	Range: 0.00 to 600.00 in steps of 0.01
	MESSAGE	GROUND TOC1 RESET: Instantaneous	Range: Instantaneous, Timed
	MESSAGE	GROUND TOC1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	GROUND TOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	GROUND TOC1 EVENTS: Disabled	Range: Disabled, Enabled

This element can provide a desired time-delay operating characteristic versus the applied current or be used as a simple definite time element. The ground current input value is the quantity measured by the ground input CT and is the fundamental phasor or RMS magnitude. Two methods of resetting operation are available: “Timed” and “Instantaneous” (refer to the *Inverse time overcurrent curve characteristics* section for details). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to “Instantaneous” and the element is blocked, the time accumulator will be cleared immediately.

NOTE These elements measure the current that is connected to the ground channel of a CT/VT module. The conversion range of a standard channel is from 0.02 to 46 times the CT rating.

NOTE This channel may be also equipped with a sensitive input. The conversion range of a sensitive channel is from 0.002 to 4.6 times the CT rating.

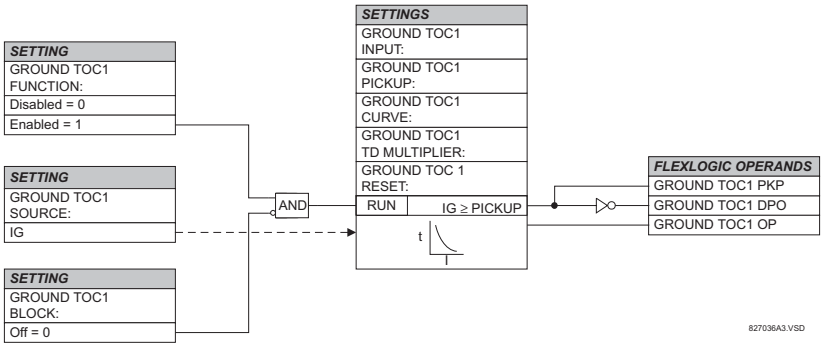


Figure 5–86: GROUND TOC1 SCHEME LOGIC

b) GROUND INSTANTANEOUS OVERCURRENT (ANSI 50G)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ GROUND CURRENT ⇨⇩ GROUND IOC1(2)

■ GROUND IOC1 ■	GROUND IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	GROUND IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
MESSAGE	GROUND IOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu in steps of 0.001
MESSAGE	GROUND IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 to 600.00 s in steps of 0.01
MESSAGE	GROUND IOC1 RESET DELAY: 0.00 s	Range: 0.00 to 600.00 s in steps of 0.01
MESSAGE	GROUND IOC1 BLOCK: Off	Range: FlexLogic™ operand
MESSAGE	GROUND IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	GROUND IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The ground instantaneous overcurrent element may be used as an instantaneous element with no intentional delay or as a definite time element. The ground current input is the quantity measured by the ground input CT and is the fundamental phasor magnitude.

NOTE

These elements measure the current that is connected to the ground channel of a CT/VT module. The conversion range of a standard channel is from 0.02 to 46 times the CT rating.

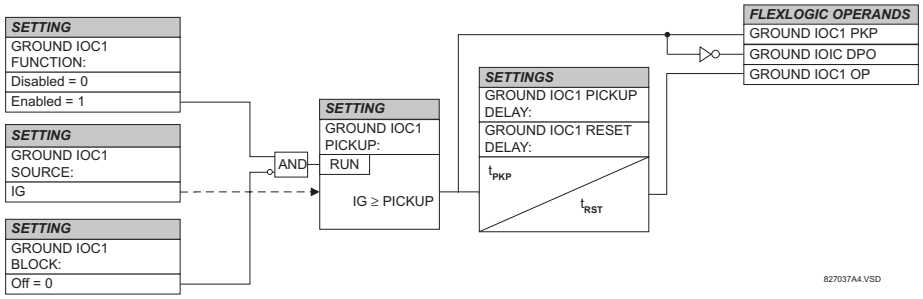


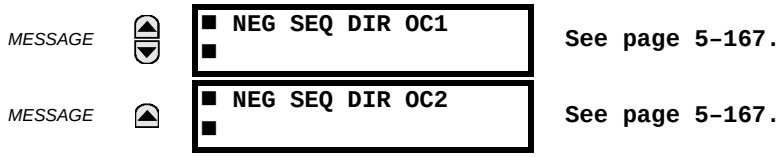
Figure 5–87: GROUND IOC1 SCHEME LOGIC

5.5.12 NEGATIVE SEQUENCE CURRENT

a) MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ NEGATIVE SEQUENCE CURRENT

■ NEGATIVE SEQUENCE ■ CURRENT	■ NEG SEQ TOC1 ■	See page 5–165.
MESSAGE	■ NEG SEQ TOC2 ■	See page 5–165.
MESSAGE	■ NEG SEQ IOC1 ■	See page 5–166.
MESSAGE	■ NEG SEQ IOC2 ■	See page 5–166.



The L60 Line Phase Comparison System has two (2) Negative Sequence Time Overcurrent, two (2) Negative Sequence Instantaneous Overcurrent, and two (2) Negative Sequence Directional Overcurrent elements. These are described in the following sub-sections.

b) NEGATIVE SEQUENCE TIME OVERCURRENT (ANSI 51_2)

PATH: SETTINGS ⇩ GROUPED ELEMENTS ⇨⇩ SETTING GROUP 1(6) ⇨⇩ NEGATIVE SEQUENCE CURRENT ⇨ NEG SEQ TOC1(2)

■ NEG SEQ TOC1 ■		NEG SEQ TOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE		NEG SEQ TOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
MESSAGE		NEG SEQ TOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu in steps of 0.001
MESSAGE		NEG SEQ TOC1 CURVE: IEEE Mod Inv	Range: see OVERCURRENT CURVE TYPES table
MESSAGE		NEG SEQ TOC1 TD MULTIPLIER: 1.00	Range: 0.00 to 600.00 in steps of 0.01
MESSAGE		NEG SEQ TOC1 RESET: Instantaneous	Range: Instantaneous, Timed
MESSAGE		NEG SEQ TOC1 BLOCK: Off	Range: FlexLogic™ operand
MESSAGE		NEG SEQ TOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE		NEG SEQ TOC1 EVENTS: Disabled	Range: Disabled, Enabled

The negative-sequence time overcurrent element may be used to determine and clear unbalance in the system. The input for calculating negative-sequence current is the fundamental phasor value.

Two methods of resetting operation are available; “Timed” and “Instantaneous” (refer to the *Inverse Time Overcurrent Characteristics* sub-section for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to “Instantaneous” and the element is blocked, the time accumulator will be cleared immediately.

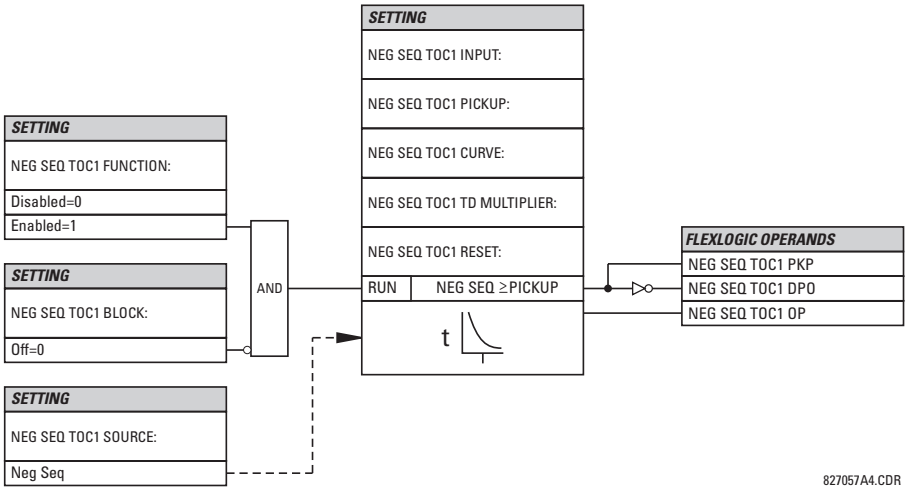


Figure 5–88: NEGATIVE SEQUENCE TOC1 SCHEME LOGIC

c) NEGATIVE SEQUENCE INSTANTANEOUS OVERCURRENT (ANSI 50_2)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ NEGATIVE SEQUENCE CURRENT ⇨⇩ NEG SEQ OC1(2)

■ NEG SEQ IOC1 ■		NEG SEQ IOC1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	NEG SEQ IOC1 SIGNAL SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	NEG SEQ IOC1 PICKUP: 1.000 pu	*Range: 0.000 to 30.000 pu in steps of 0.001*
	MESSAGE	NEG SEQ IOC1 PICKUP DELAY: 0.00 s	*Range: 0.00 to 600.00 s in steps of 0.01*
	MESSAGE	NEG SEQ IOC1 RESET DELAY: 0.00 s	*Range: 0.00 to 600.00 s in steps of 0.01*
	MESSAGE	NEG SEQ IOC1 BLOCK: Off	*Range: FlexLogic™ operand*
	MESSAGE	NEG SEQ IOC1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	NEG SEQ IOC1 EVENTS: Disabled	*Range: Disabled, Enabled*

5

The negative-sequence instantaneous overcurrent element may be used as an instantaneous function with no intentional delay or as a definite time function. The element responds to the negative-sequence current fundamental frequency phasor magnitude (calculated from the phase currents) and applies a positive-sequence restraint for better performance: a small portion (12.5%) of the positive-sequence current magnitude is subtracted from the negative-sequence current magnitude when forming the operating quantity:

$$I_{op} = |I\_2| - K \cdot |I\_1| \quad \text{where } K = 1/8 \qquad \textbf{(EQ 5.23)}$$

The positive-sequence restraint allows for more sensitive settings by counterbalancing spurious negative-sequence currents resulting from:

- system unbalances under heavy load conditions
- transformation errors of current transformers (CTs) during three-phase faults
- fault inception and switch-off transients during three-phase faults

The positive-sequence restraint must be considered when testing for pickup accuracy and response time (multiple of pickup). The operating quantity depends on the way the test currents are injected into the relay (single-phase injection: $I_{op} = 0.2917 \cdot I_{injected}$; three-phase injection, opposite rotation: $I_{op} = I_{injected}$).

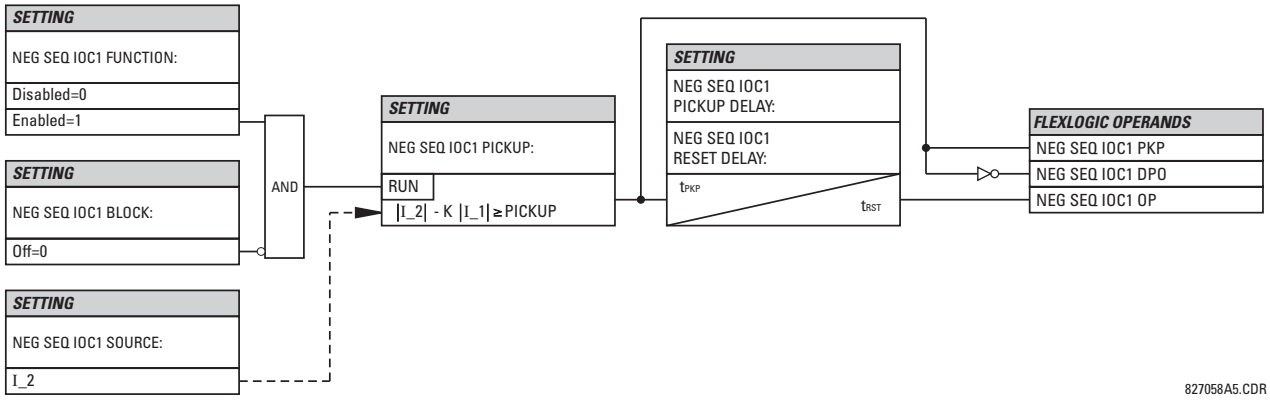


Figure 5–89: NEGATIVE SEQUENCE IOC1 SCHEME LOGIC

d) NEGATIVE SEQUENCE DIRECTIONAL OVERCURRENT (ANSI 67_2)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ NEGATIVE SEQUENCE CURRENT ⇨⇩ NEG SEQ DIR OC1(2)

■ NEG SEQ DIR OC1 ■		NEG SEQ DIR OC1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	NEG SEQ DIR OC1 SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	NEG SEQ DIR OC1 OFFSET: 0.00 Ω	*Range: 0.00 to 250.00 Ω in steps of 0.01*
	MESSAGE	NEG SEQ DIR OC1 TYPE: Neg Sequence	*Range: Neg Sequence, Zero Sequence*
	MESSAGE	NEG SEQ DIR OC1 POS-SEQ RESTRAINT: 0.063	*Range: 0.000 to 0.500 in steps of 0.001*
	MESSAGE	NEG SEQ DIR OC1 FWD ECA: 75° Lag	*Range: 0 to 90° Lag in steps of 1*
	MESSAGE	NEG SEQ DIR OC1 FWD LIMIT ANGLE: 90°	*Range: 40 to 90° in steps of 1*
	MESSAGE	NEG SEQ DIR OC1 FWD PICKUP: 0.05 pu	*Range: 0.05 to 30.00 pu in steps of 0.01*
	MESSAGE	NEG SEQ DIR OC1 REV LIMIT ANGLE: 90°	*Range: 40 to 90° in steps of 1*
	MESSAGE	NEG SEQ DIR OC1 REV PICKUP: 0.05 pu	*Range: 0.05 to 30.00 pu in steps of 0.01*
	MESSAGE	NEG SEQ DIR OC1 BLK: Off	*Range: FlexLogic™ operand*
	MESSAGE	NEG SEQ DIR OC1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	NEG SEQ DIR OC1 EVENTS: Disabled	*Range: Disabled, Enabled*

There are two negative-sequence directional overcurrent protection elements available. The element provides both forward and reverse fault direction indications through its output operands NEG SEQ DIR OC1 FWD and NEG SEQ DIR OC1 REV, respectively. The output operand is asserted if the magnitude of the operating current is above a pickup level (overcurrent unit) and the fault direction is seen as 'forward' or 'reverse', respectively (directional unit).

The **overcurrent unit** of the element essentially responds to the magnitude of a fundamental frequency phasor of either the negative-sequence or zero-sequence current as per user selection. The zero-sequence current should not be mistaken with the neutral current (factor 3 difference).

A positive-sequence restraint is applied for better performance: a small user-programmable portion of the positive–sequence current magnitude is subtracted from the negative- or zero-sequence current magnitude, respectively, when forming the element operating quantity.

$$I_{op} = |I\_2| - K \times |I\_1| \quad \text{or} \quad I_{op} = |I\_0| - K \times |I\_1| \qquad \textbf{(EQ 5.24)}$$

The positive-sequence restraint allows for more sensitive settings by counterbalancing spurious negative- and zero-sequence currents resulting from:

- System unbalances under heavy load conditions.
- Transformation errors of current transformers (CTs).
- Fault inception and switch-off transients.

The positive-sequence restraint must be considered when testing for pick-up accuracy and response time (multiple of pickup). The operating quantity depends on the way the test currents are injected into the relay:

- single-phase injection: $I_{op} = 1/3 \times (1 - K) \times I_{injected}$
- three-phase pure zero- or negative-sequence injection, respectively: $I_{op} = I_{injected}$.
- the directional unit uses the negative-sequence current and voltage for fault direction discrimination

The following table defines the negative-sequence directional overcurrent element.

OVERCURRENT UNIT		DIRECTIONAL UNIT		
MODE	OPERATING CURRENT	DIRECTION	COMPARED PHASORS	
Negative-sequence	$I_{op} = \|I\_2\| - K \times \|I\_1\|$	Forward	–V_2 + Z_offset × I_2	I_2 × 1∠ECA
		Reverse	–V_2 + Z_offset × I_2	–(I_2 × 1∠ECA)
Zero-sequence	$I_{op} = \|I\_0\| - K \times \|I\_1\|$	Forward	–V_2 + Z_offset × I_2	I_2 × 1∠ECA
		Reverse	–V_2 + Z_offset × I_2	–(I_2 × 1∠ECA)

The negative-sequence voltage must be higher than the **PRODUCT SETUP ⇨⇩ DISPLAY PROPERTIES ⇨⇩ VOLTAGE CUT-OFF LEVEL** value to be validated for use as a polarizing signal. If the polarizing signal is not validated neither forward nor reverse indication is given. The following figure explains the usage of the voltage polarized directional unit of the element.

The figure below shows the phase angle comparator characteristics for a Phase A to ground fault, with settings of:

ECA = 75° (Element characteristic angle = centerline of operating characteristic)
FWD LA = 80° (Forward limit angle = ± the angular limit with the ECA for operation)
REV LA = 80° (Reverse limit angle = ± the angular limit with the ECA for operation)

The element incorporates a current reversal logic: if the reverse direction is indicated for at least 1.25 of a power system cycle, the prospective forward indication will be delayed by 1.5 of a power system cycle. The element is designed to emulate an electromechanical directional device. Larger operating and polarizing signals will result in faster directional discrimination bringing more security to the element operation.

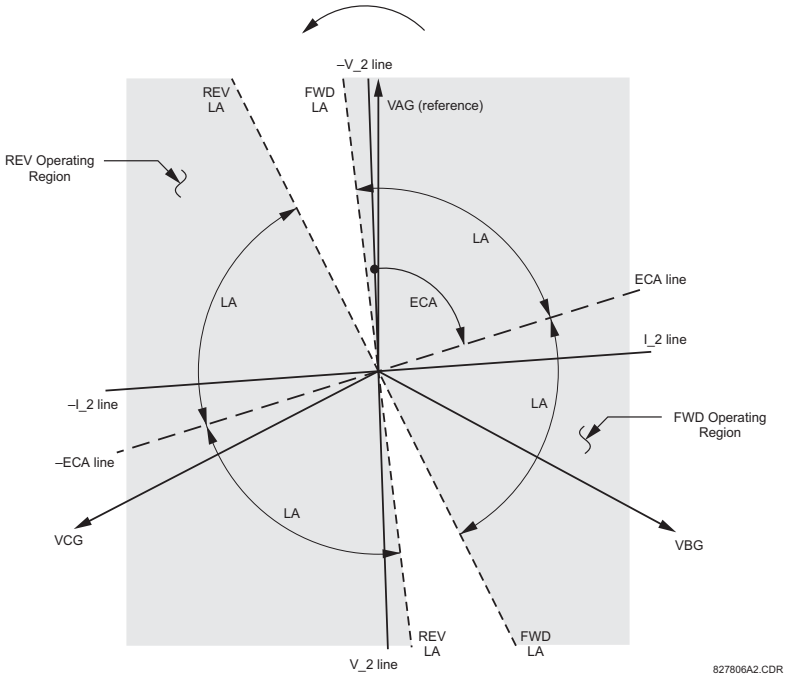


Figure 5–90: NEG SEQ DIRECTIONAL CHARACTERISTICS

The forward-looking function is designed to be more secure as compared to the reverse-looking function, and therefore, should be used for the tripping direction. The reverse-looking function is designed to be faster as compared to the forward-looking function and should be used for the blocking direction. This allows for better protection coordination. The above bias should be taken into account when using the negative-sequence directional overcurrent element to directionalize other protection elements.

- **NEG SEQ DIR OC1 OFFSET:** This setting specifies the offset impedance used by this protection. The primary application for the offset impedance is to guarantee correct identification of fault direction on series compensated lines (see the *Application of Settings* chapter for information on how to calculate this setting). In regular applications, the offset impedance ensures proper operation even if the negative-sequence voltage at the relaying point is very small. If this is the intent, the offset impedance shall not be larger than the negative-sequence impedance of the protected circuit. Practically, it shall be several times smaller. The offset impedance shall be entered in secondary ohms. See the *Theory of Operation* chapter for additional details.
- **NEG SEQ DIR OC1 TYPE:** This setting selects the operating mode for the overcurrent unit of the element. The choices are "Neg Sequence" and "Zero Sequence". In some applications it is advantageous to use a directional negative-sequence overcurrent function instead of a directional zero-sequence overcurrent function as inter-circuit mutual effects are minimized.
- **NEG SEQ DIR OC1 POS-SEQ RESTRAINT**: This setting controls the amount of the positive-sequence restraint. Set to 0.063 (in "Zero Sequence" mode) or 0.125 (in "Neg Sequence" mode) for backward compatibility with firmware revision 3.40 and older. Set to zero to remove the restraint. Set higher if large system unbalances or poor CT performance are expected.
- **NEG SEQ DIR OC1 FWD ECA:** This setting select the element characteristic angle (ECA) for the forward direction. The element characteristic angle in the reverse direction is the angle set for the forward direction shifted by 180°.
- **NEG SEQ DIR OC1 FWD LIMIT ANGLE:** This setting defines a symmetrical (in both directions from the ECA) limit angle for the forward direction.
- **NEG SEQ DIR OC1 FWD PICKUP:** This setting defines the pickup level for the overcurrent unit in the forward direction. Upon **NEG SEQ DIR OC1 TYPE** selection, this pickup threshold applies to zero- or negative-sequence current. When selecting this setting it must be kept in mind that the design uses a 'positive-sequence restraint' technique.
- **NEG SEQ DIR OC1 REV LIMIT ANGLE:** This setting defines a symmetrical (in both directions from the ECA) limit angle for the reverse direction.
- **NEG SEQ DIR OC1 REV PICKUP:** This setting defines the pickup level for the overcurrent unit in the reverse direction. Upon **NEG SEQ DIR OC1 TYPE** selection, this pickup threshold applies to zero- or negative-sequence current. When selecting this setting it must be kept in mind that the design uses a 'positive-sequence restraint' technique.

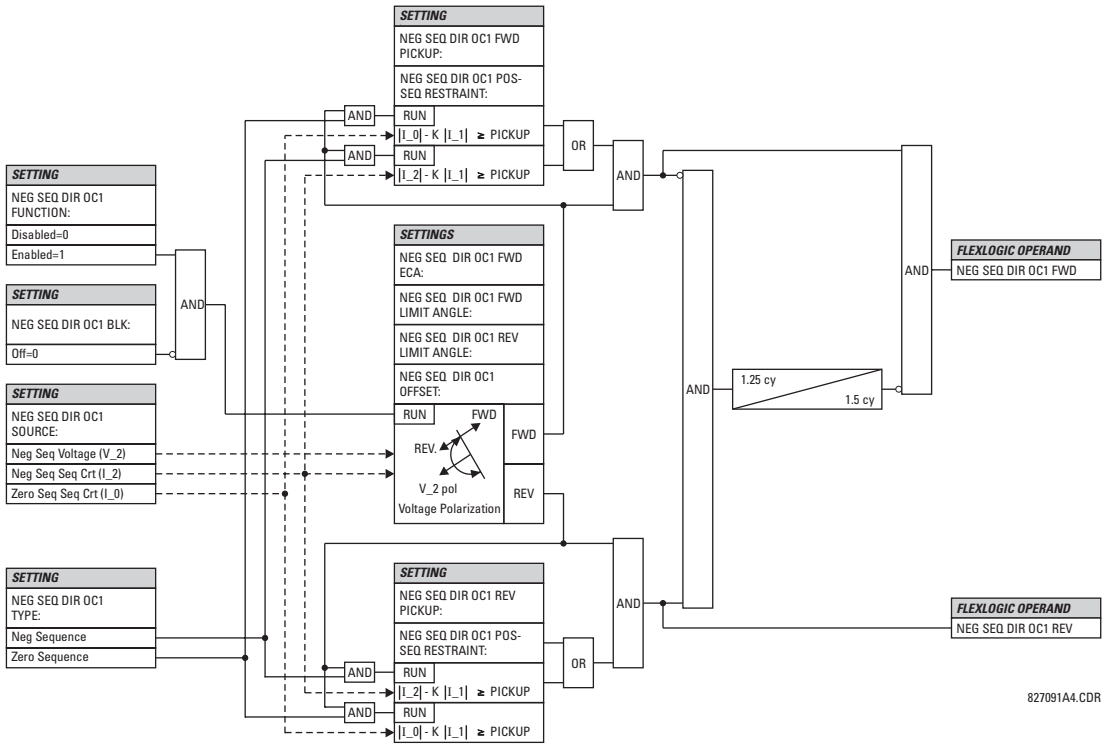
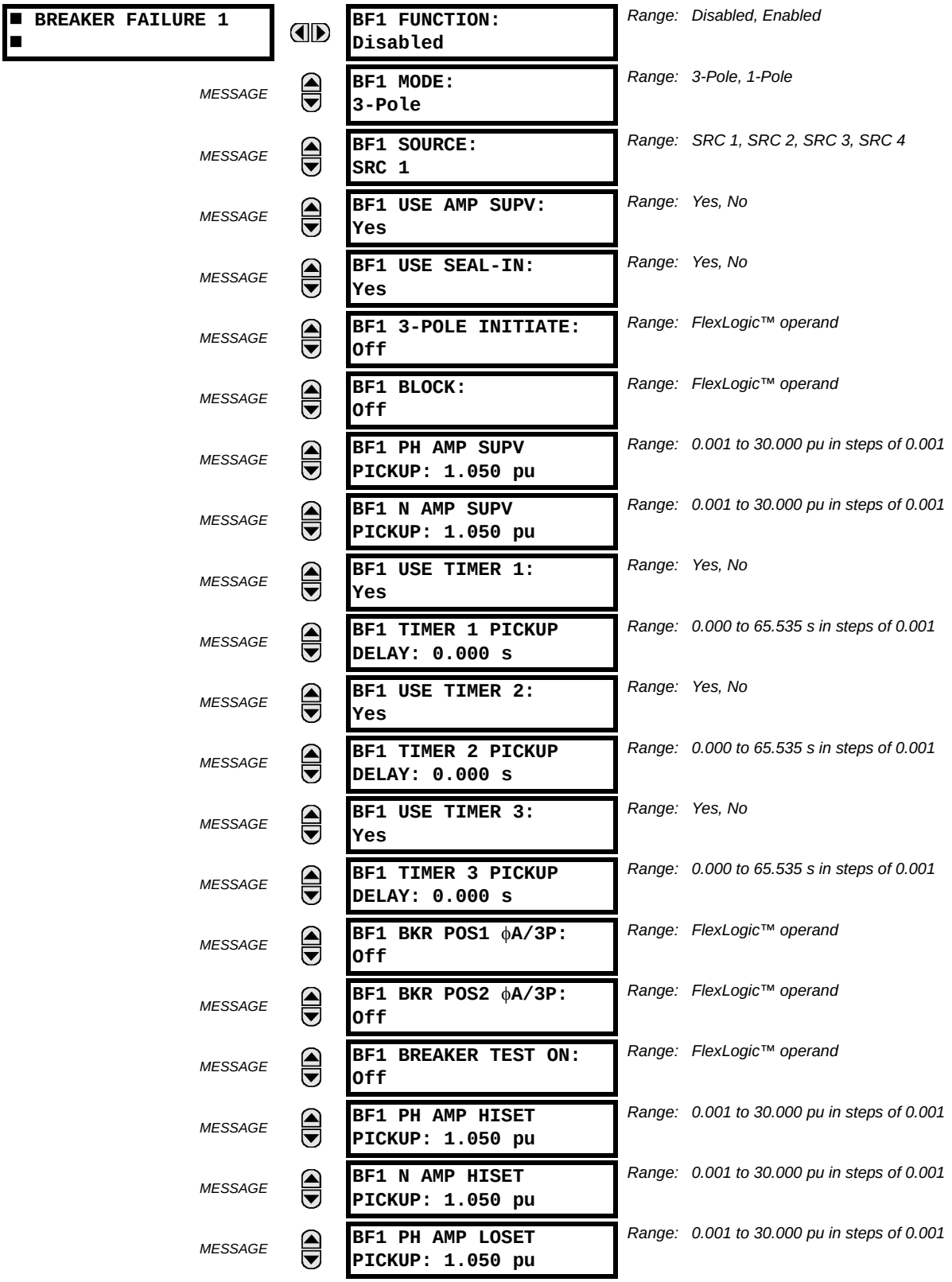


Figure 5–91: NEGATIVE SEQUENCE DIRECTIONAL OC1 SCHEME LOGIC

5.5.13 BREAKER FAILURE

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ BREAKER FAILURE ⇨ BREAKER FAILURE 1(2)



MESSAGE
BF1 N AMP LOSET
PICKUP: 1.050 pu
Range: 0.001 to 30.000 pu in steps of 0.001

MESSAGE
BF1 LOSET TIME
DELAY: 0.000 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
BF1 TRIP DROPOUT
DELAY: 0.000 s
Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE
BF1 TARGET
Self-Reset
Range: Self-reset, Latched, Disabled

MESSAGE
BF1 EVENTS
Disabled
Range: Disabled, Enabled

MESSAGE
BF1 PH A INITIATE:
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

MESSAGE
BF1 PH B INITIATE:
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

MESSAGE
BF1 PH C INITIATE:
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

MESSAGE
BF1 BKR POS1 ϕB
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

MESSAGE
BF1 BKR POS1 ϕC
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

MESSAGE
BF1 BKR POS2 ϕB
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

MESSAGE
BF1 BKR POS2 ϕC
Off
Range: FlexLogic™ operand
Valid only for 1-Pole breaker failure schemes.

In general, a breaker failure scheme determines that a breaker signaled to trip has not cleared a fault within a definite time, so further tripping action must be performed. Tripping from the breaker failure scheme should trip all breakers, both local and remote, that can supply current to the faulted zone. Usually operation of a breaker failure element will cause clearing of a larger section of the power system than the initial trip. Because breaker failure can result in tripping a large number of breakers and this affects system safety and stability, a very high level of security is required.

Two schemes are provided: one for three-pole tripping only (identified by the name "3BF") and one for three pole plus single-pole operation (identified by the name "1BF"). The philosophy used in these schemes is identical. The operation of a breaker failure element includes three stages: initiation, determination of a breaker failure condition, and output.

INITIATION STAGE:

A FlexLogic™ operand representing the protection trip signal initially sent to the breaker must be selected to initiate the scheme, except for the L60 relay were this is already programmed as a trip output (the protection trip signal does not include other breaker commands that are not indicative of a fault in the protected zone). The initiating signal should be sealed-in if primary fault detection can reset before the breaker failure timers have finished timing. The seal-in is supervised by current level, so it is reset when the fault is cleared. If desired, an incomplete sequence seal-in reset can be implemented by using the initiating operand to also initiate a FlexLogic™ timer, set longer than any breaker failure timer, whose output operand is selected to block the breaker failure scheme.

Schemes can be initiated either directly or with current level supervision. It is particularly important in any application to decide if a current-supervised initiate is to be used. The use of a current-supervised initiate results in the breaker failure element not being initiated for a breaker that has very little or no current flowing through it, which may be the case for transformer faults. For those situations where it is required to maintain breaker fail coverage for fault levels below the **BF1 PH AMP SUPV PICKUP** or the **BF1 N AMP SUPV PICKUP** setting, a current supervised initiate should *not* be used. This feature should be utilized for those situations where coordinating margins may be reduced when high speed reclosing is used. Thus, if this choice is made, fault levels must always be above the supervision pickup levels for dependable operation of

the breaker fail scheme. This can also occur in breaker-and-a-half or ring bus configurations where the first breaker closes into a fault; the protection trips and attempts to initiate breaker failure for the second breaker, which is in the process of closing, but does not yet have current flowing through it.

When the scheme is initiated, it immediately sends a trip signal to the breaker initially signaled to trip (this feature is usually described as re-trip). This reduces the possibility of widespread tripping that results from a declaration of a failed breaker.

DETERMINATION OF A BREAKER FAILURE CONDITION:

The schemes determine a breaker failure condition via three 'paths'. Each of these paths is equipped with a time delay, after which a failed breaker is declared and trip signals are sent to all breakers required to clear the zone. The delayed paths are associated with breaker failure timers 1, 2, and 3, which are intended to have delays increasing with increasing timer numbers. These delayed paths are individually enabled to allow for maximum flexibility.

Timer 1 logic (early path) is supervised by a fast-operating breaker auxiliary contact. If the breaker is still closed (as indicated by the auxiliary contact) and fault current is detected after the delay interval, an output is issued. Operation of the breaker auxiliary switch indicates that the breaker has mechanically operated. The continued presence of current indicates that the breaker has failed to interrupt the circuit.

Timer 2 logic (main path) is not supervised by a breaker auxiliary contact. If fault current is detected after the delay interval, an output is issued. This path is intended to detect a breaker that opens mechanically but fails to interrupt fault current; the logic therefore does not use a breaker auxiliary contact.

The timer 1 and 2 paths provide two levels of current supervision, high-set and low-set, that allow the supervision level to change from a current which flows before a breaker inserts an opening resistor into the faulted circuit to a lower level after resistor insertion. The high-set detector is enabled after timeout of timer 1 or 2, along with a timer that will enable the low-set detector after its delay interval. The delay interval between high-set and low-set is the expected breaker opening time. Both current detectors provide a fast operating time for currents at small multiples of the pickup value. The overcurrent detectors are required to operate after the breaker failure delay interval to eliminate the need for very fast resetting overcurrent detectors.

Timer 3 logic (slow path) is supervised by a breaker auxiliary contact and a control switch contact used to indicate that the breaker is in or out-of-service, disabling this path when the breaker is out-of-service for maintenance. There is no current level check in this logic as it is intended to detect low magnitude faults and it is therefore the slowest to operate.

OUTPUT:

The outputs from the schemes are:

- FlexLogic™ operands that report on the operation of portions of the scheme
- FlexLogic™ operand used to re-trip the protected breaker
- FlexLogic™ operands that initiate tripping required to clear the faulted zone. The trip output can be sealed-in for an adjustable period.
- Target message indicating a failed breaker has been declared
- Illumination of the faceplate Trip LED (and the Phase A, B or C LED, if applicable)

MAIN PATH SEQUENCE:

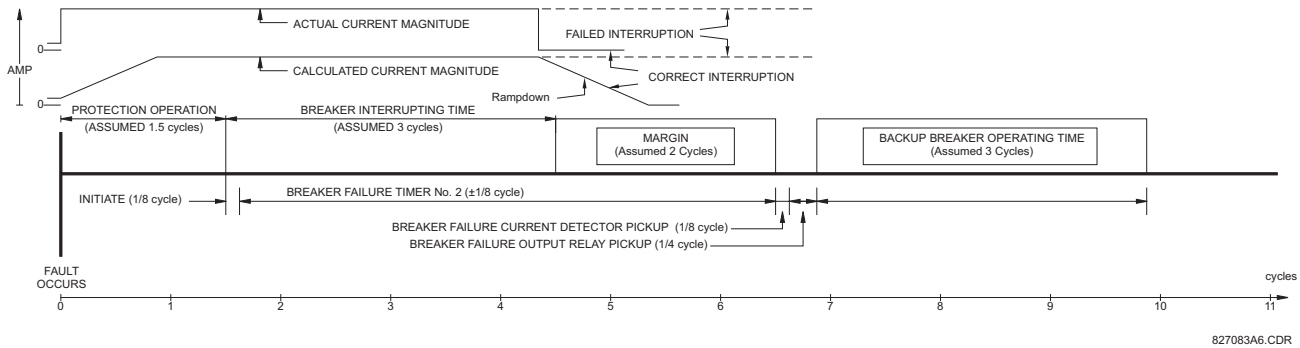


Figure 5–92: BREAKER FAILURE MAIN PATH SEQUENCE

The current supervision elements reset in less than 0.7 of a power cycle up to the multiple of pickup of 100 (threshold set at 0.01 of the actual fault current) as shown below.

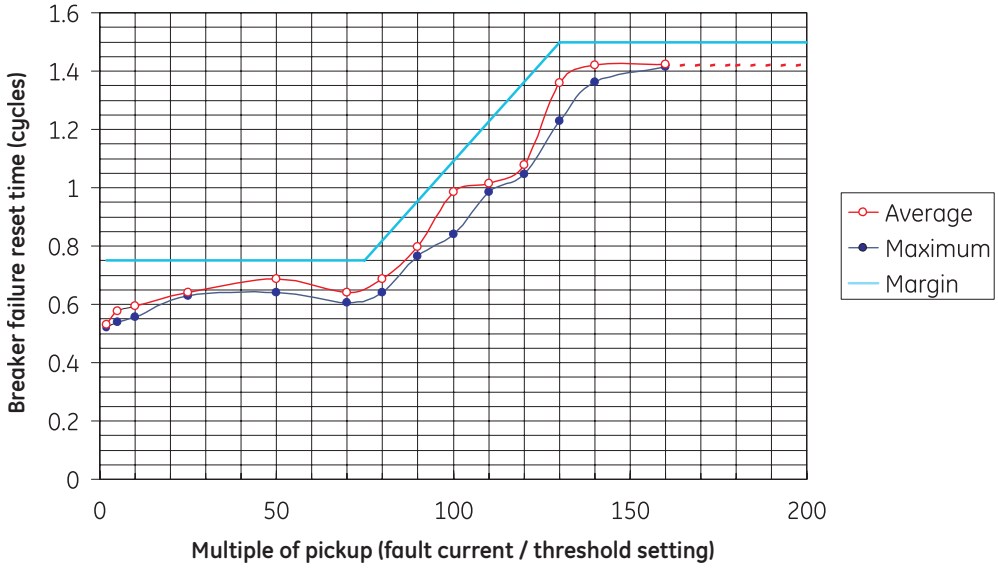


Figure 5–93: BREAKER FAILURE OVERCURRENT SUPERVISION RESET TIME

SETTINGS:

- **BF1 MODE:** This setting is used to select the breaker failure operating mode: single or three pole.
- **BF1 USE AMP SUPV:** If set to "Yes", the element will only be initiated if current flowing through the breaker is above the supervision pickup level.
- **BF1 USE SEAL-IN:** If set to "Yes", the element will only be sealed-in if current flowing through the breaker is above the supervision pickup level.
- **BF1 3-POLE INITIATE:** This setting selects the FlexLogic™ operand that will initiate 3-pole tripping of the breaker.
- **BF1 PH AMP SUPV PICKUP:** This setting is used to set the phase current initiation and seal-in supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker. It can be set as low as necessary (lower than breaker resistor current or lower than load current) - Hiset and Loset current supervision will guarantee correct operation.
- **BF1 N AMP SUPV PICKUP:** This setting is used to set the neutral current initiate and seal-in supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker. Neutral current supervision is used only in the three phase scheme to provide increased sensitivity. This setting is valid only for three-pole tripping schemes.
- **BF1 USE TIMER 1:** If set to "Yes", the Early Path is operational.
- **BF1 TIMER 1 PICKUP DELAY:** Timer 1 is set to the shortest time required for breaker auxiliary contact Status-1 to open, from the time the initial trip signal is applied to the breaker trip circuit, plus a safety margin.
- **BF1 USE TIMER 2:** If set to "Yes", the Main Path is operational.
- **BF1 TIMER 2 PICKUP DELAY:** Timer 2 is set to the expected opening time of the breaker, plus a safety margin. This safety margin was historically intended to allow for measuring and timing errors in the breaker failure scheme equipment. In microprocessor relays this time is not significant. In L60 relays, which use a Fourier transform, the calculated current magnitude will ramp-down to zero one power frequency cycle after the current is interrupted, and this lag should be included in the overall margin duration, as it occurs after current interruption. The *Breaker Failure Main Path Sequence* diagram below shows a margin of two cycles; this interval is considered the minimum appropriate for most applications.

  Note that in bulk oil circuit breakers, the interrupting time for currents less than 25% of the interrupting rating can be significantly longer than the normal interrupting time.
- **BF1 USE TIMER 3:** If set to "Yes", the Slow Path is operational.

- **BF1 TIMER 3 PICKUP DELAY:** Timer 3 is set to the same interval as Timer 2, plus an increased safety margin. Because this path is intended to operate only for low level faults, the delay can be in the order of 300 to 500 ms.
- **BF1 BKR POS1 ϕA/3P:** This setting selects the FlexLogic™ operand that represents the protected breaker early-type auxiliary switch contact (52/a). When using 1-Pole breaker failure scheme, this operand represents the protected breaker early-type auxiliary switch contact on pole A. This is normally a non-multiplied Form-A contact. The contact may even be adjusted to have the shortest possible operating time.
- **BF1 BKR POS2 ϕA/3P:** This setting selects the FlexLogic™ operand that represents the breaker normal-type auxiliary switch contact (52/a). When using 1-Pole breaker failure scheme, this operand represents the protected breaker auxiliary switch contact on pole A. This may be a multiplied contact.
- **BF1 BREAKER TEST ON:** This setting is used to select the FlexLogic™ operand that represents the breaker In-Service/Out-of-Service switch set to the Out-of-Service position.
- **BF1 PH AMP HISET PICKUP:** This setting sets the phase current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, before a breaker opening resistor is inserted.
- **BF1 N AMP HISET PICKUP:** This setting sets the neutral current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, before a breaker opening resistor is inserted. Neutral current supervision is used only in the three pole scheme to provide increased sensitivity. *This setting is valid only for 3-pole breaker failure schemes*.
- **BF1 PH AMP LOSET PICKUP:** This setting sets the phase current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, after a breaker opening resistor is inserted (approximately 90% of the resistor current).
- **BF1 N AMP LOSET PICKUP:** This setting sets the neutral current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, after a breaker opening resistor is inserted (approximately 90% of the resistor current). *This setting is valid only for 3-pole breaker failure schemes*.
- **BF1 LOSET TIME DELAY:** Sets the pickup delay for current detection after opening resistor insertion.
- **BF1 TRIP DROPOUT DELAY:** This setting is used to set the period of time for which the trip output is sealed-in. This timer must be coordinated with the automatic reclosing scheme of the failed breaker, to which the breaker failure element sends a cancel reclosure signal. Reclosure of a remote breaker can also be prevented by holding a Transfer Trip signal on longer than the "reclaim" time.
- **BF1 PH A INITIATE / BF1 PH B INITIATE / BF 1 PH C INITIATE:** These settings select the FlexLogic™ operand to initiate phase A, B, or C single-pole tripping of the breaker and the phase A, B, or C portion of the scheme, accordingly. *This setting is only valid for 1-pole breaker failure schemes*.
- **BF1 BKR POS1 ϕB / BF1 BKR POS 1 ϕC:** These settings select the FlexLogic™ operand to represents the protected breaker early-type auxiliary switch contact on poles B or C, accordingly. This contact is normally a non-multiplied Form-A contact. The contact may even be adjusted to have the shortest possible operating time. *This setting is valid only for 1-pole breaker failure schemes*.
- **BF1 BKR POS2 ϕB:** Selects the FlexLogic™ operand that represents the protected breaker normal-type auxiliary switch contact on pole B (52/a). This may be a multiplied contact. *This setting is valid only for 1-pole breaker failure schemes*.
- **BF1 BKR POS2 ϕC:** This setting selects the FlexLogic™ operand that represents the protected breaker normal-type auxiliary switch contact on pole C (52/a). This may be a multiplied contact. For single-pole operation, the scheme has the same overall general concept except that it provides re-tripping of each single pole of the protected breaker. The approach shown in the following single pole tripping diagram uses the initiating information to determine which pole is supposed to trip. The logic is segregated on a per-pole basis. The overcurrent detectors have ganged settings. *This setting is valid only for 1-pole breaker failure schemes*.

  Upon operation of the breaker failure element for a single pole trip command, a 3-pole trip command should be given via output operand BKR FAIL 1 TRIP OP.

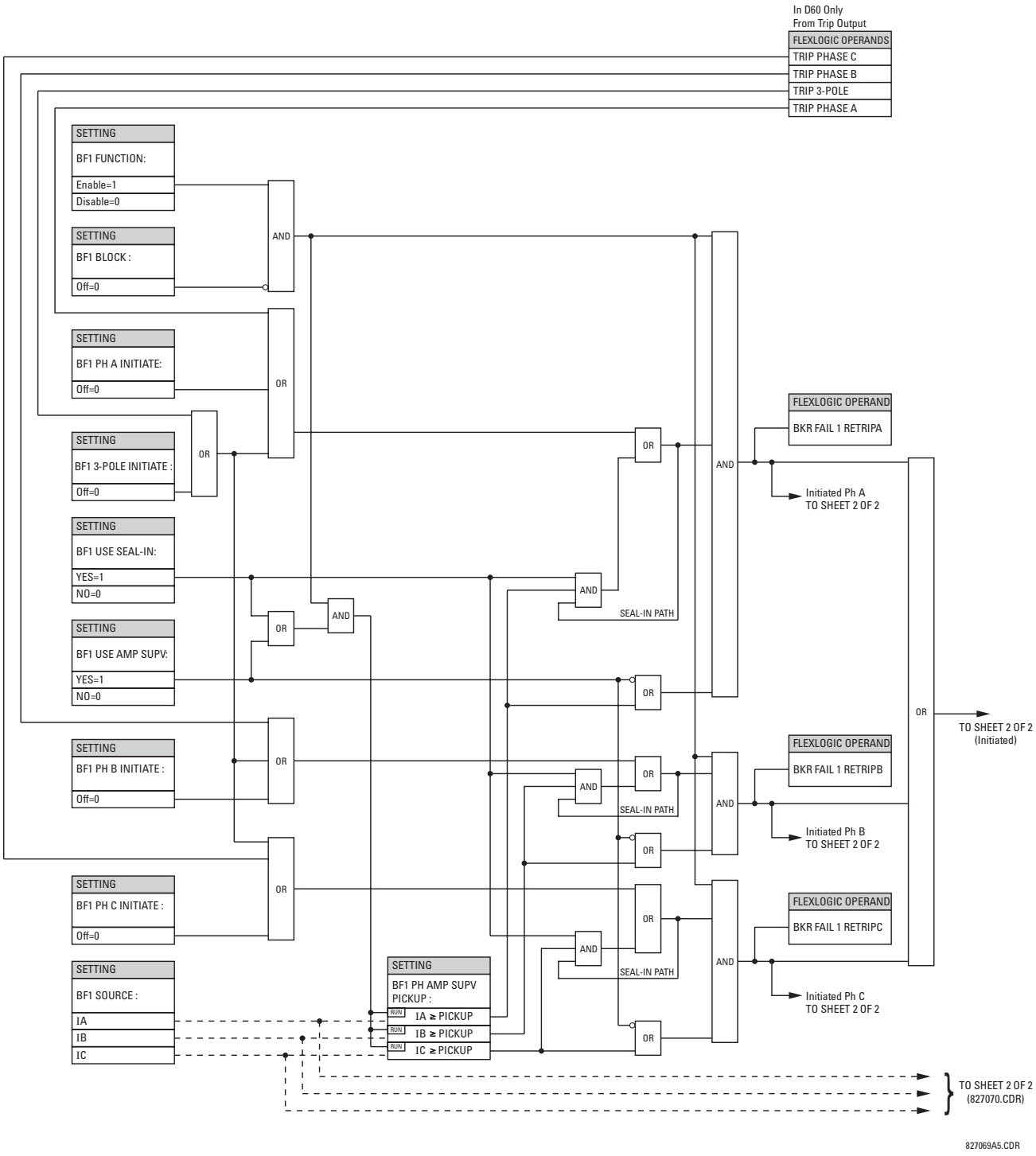


Figure 5–94: BREAKER FAILURE 1-POLE [INITIATE] (Sheet 1 of 2)

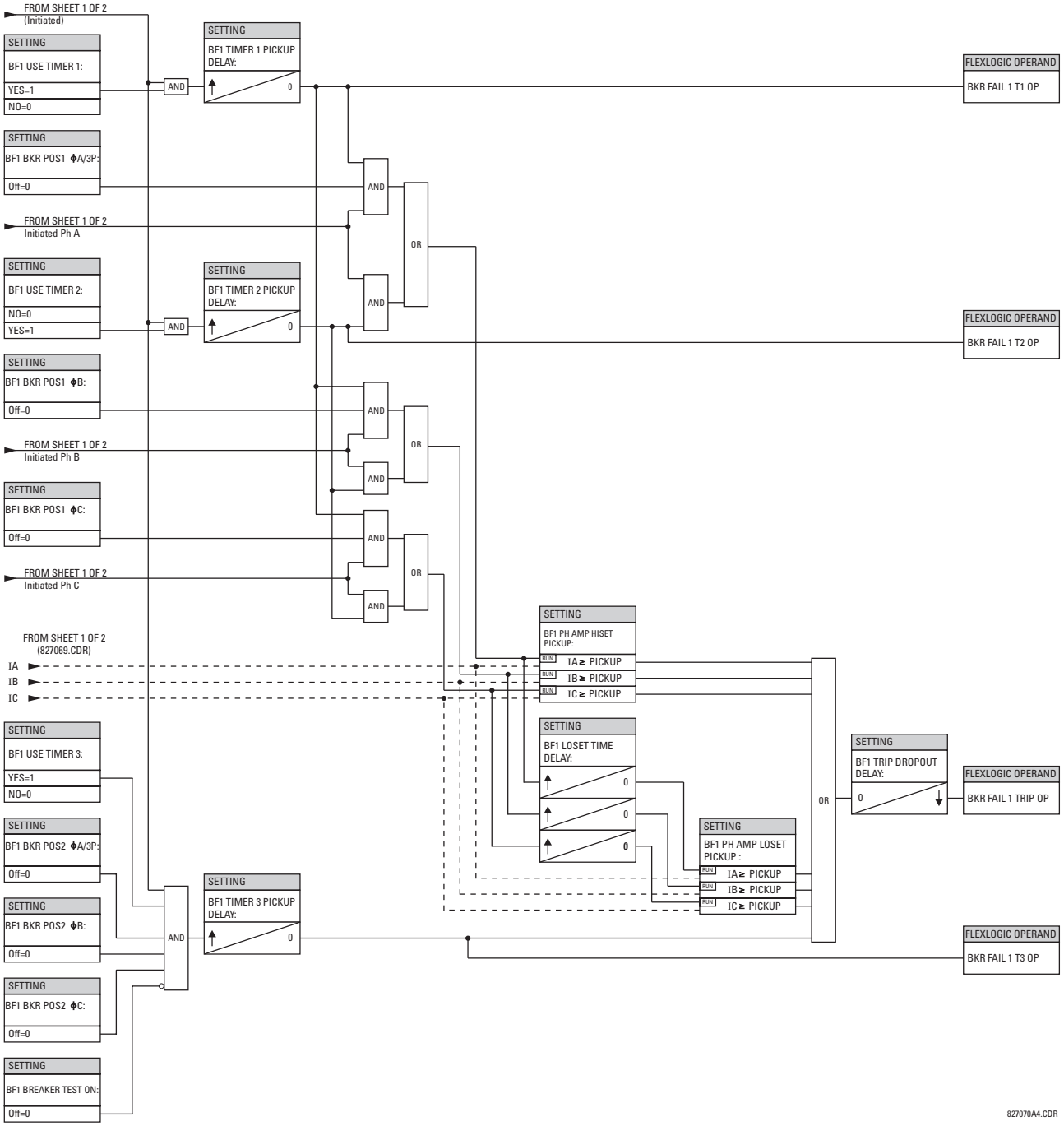


Figure 5–95: BREAKER FAILURE 1-POLE [TIMERS] (Sheet 2 of 2)

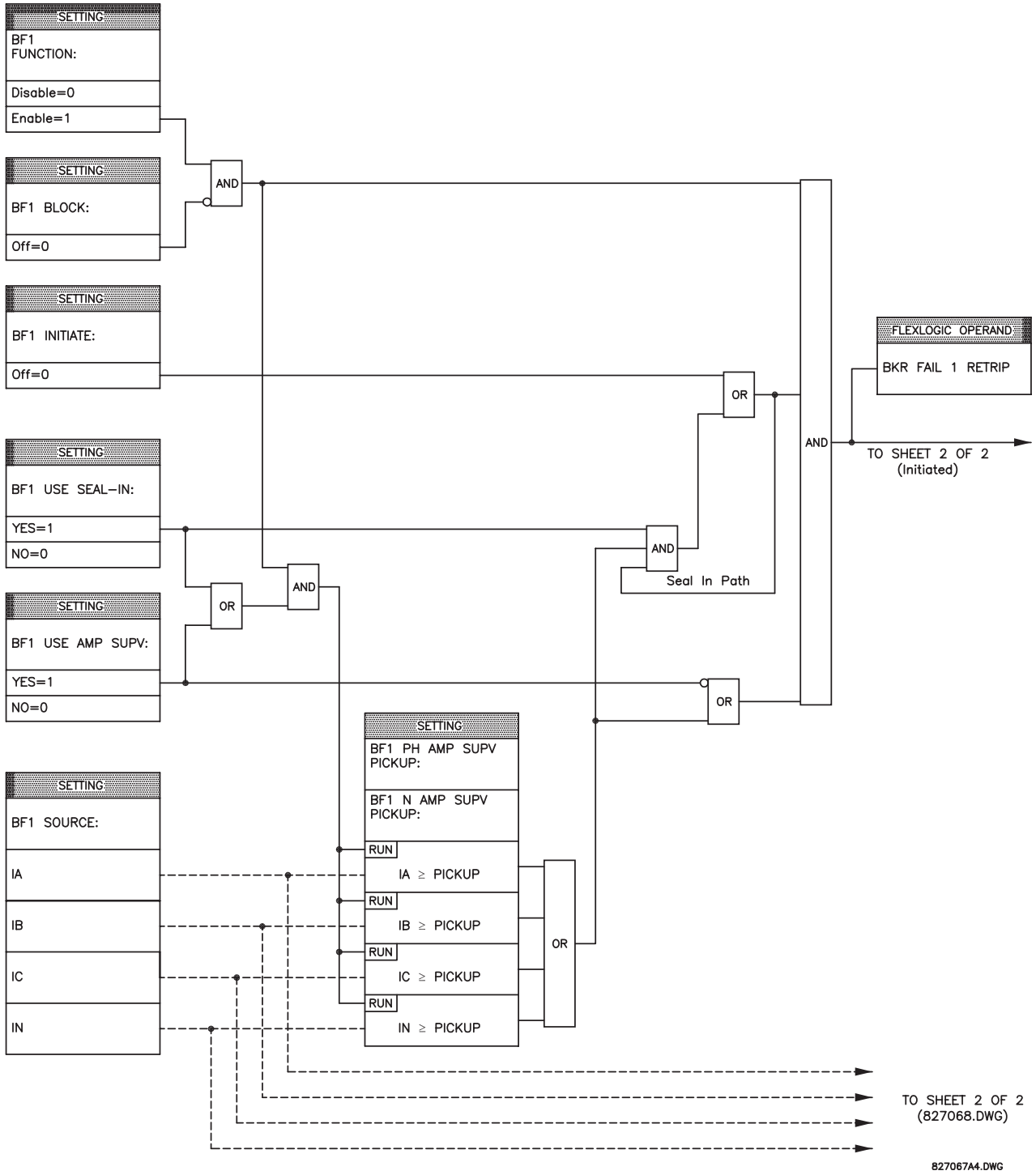


Figure 5–96: BREAKER FAILURE 3-POLE [INITIATE] (Sheet 1 of 2)

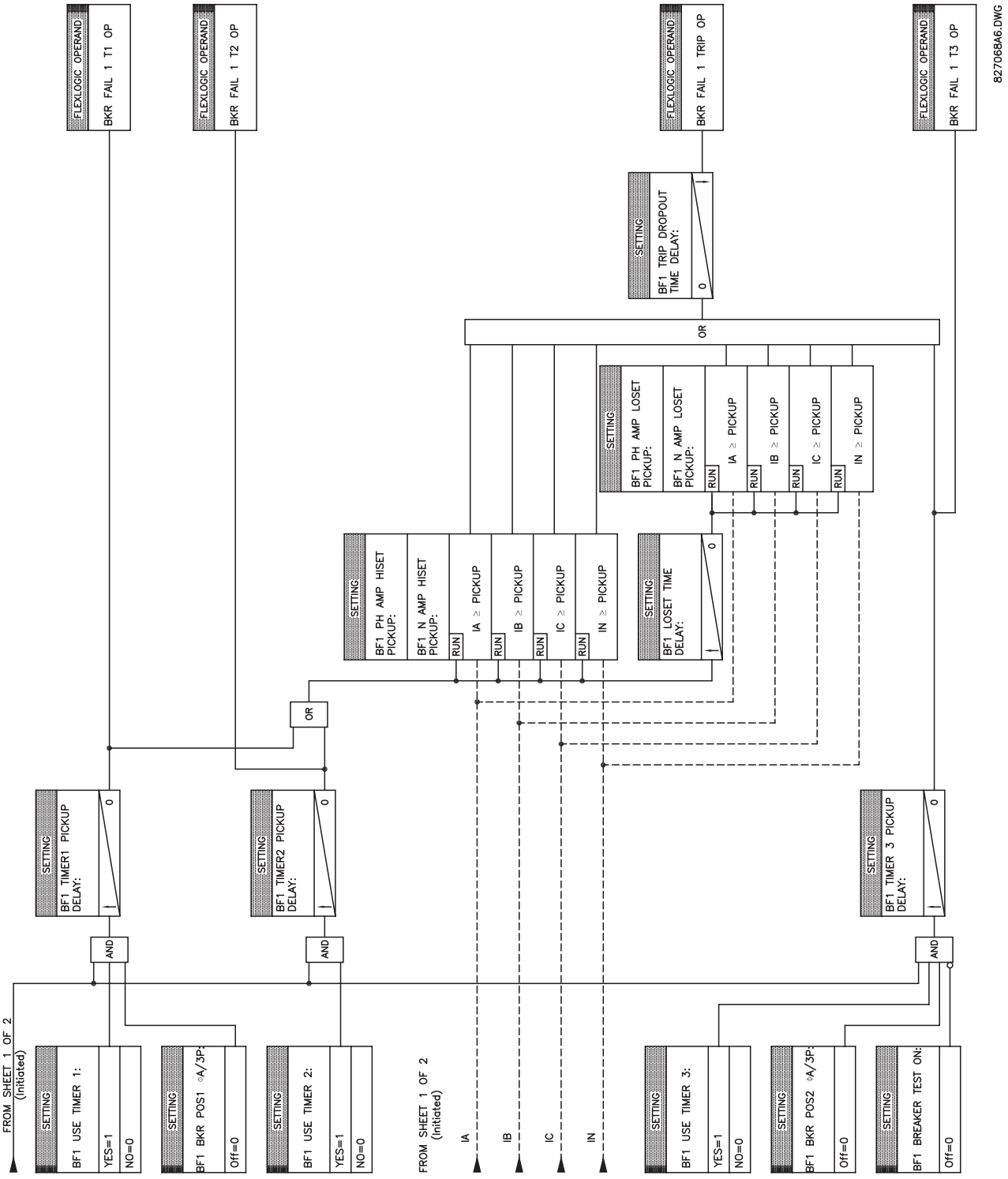
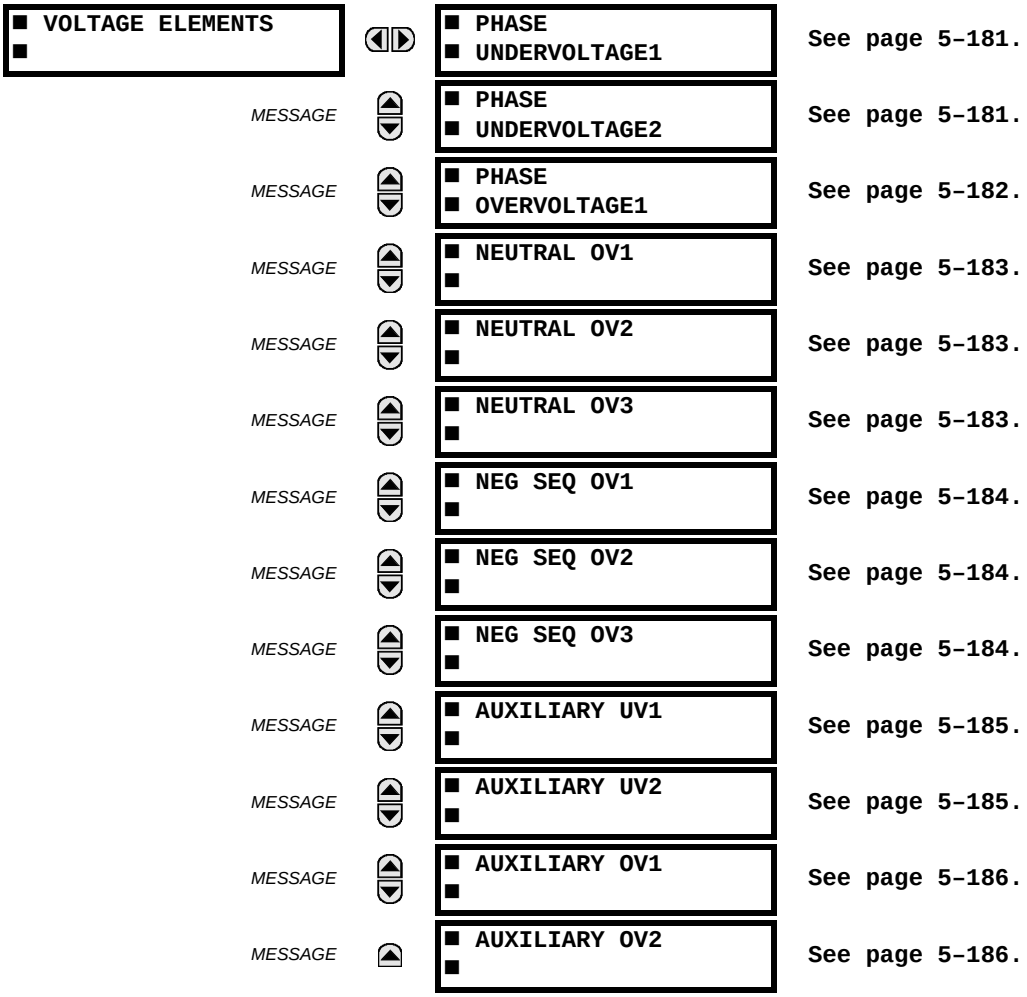


Figure 5–97: BREAKER FAILURE 3-POLE [TIMERS] (Sheet 2 of 2)

a) MAIN MENU

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS



These protection elements can be used for a variety of applications such as:

- ***Undervoltage Protection:*** For voltage sensitive loads, such as induction motors, a drop in voltage increases the drawn current which may cause dangerous overheating in the motor. The undervoltage protection feature can be used to either cause a trip or generate an alarm when the voltage drops below a specified voltage setting for a specified time delay.
- ***Permissive Functions:*** The undervoltage feature may be used to block the functioning of external devices by operating an output relay when the voltage falls below the specified voltage setting. The undervoltage feature may also be used to block the functioning of other elements through the block feature of those elements.
- ***Source Transfer Schemes:*** In the event of an undervoltage, a transfer signal may be generated to transfer a load from its normal source to a standby or emergency power source.

The undervoltage elements can be programmed to have a definite time delay characteristic. The definite time curve operates when the voltage drops below the pickup level for a specified period of time. The time delay is adjustable from 0 to 600.00 seconds in steps of 0.01. The undervoltage elements can also be programmed to have an inverse time delay characteristic.

The undervoltage delay setting defines the family of curves shown below.

$$T = \frac{D}{\left(1 - \frac{V}{V_{pickup}}\right)} \quad \text{(EQ 5.25)}$$

where: T = operating time
D = undervoltage delay setting (D = 0.00 operates instantaneously)
V = secondary voltage applied to the relay
V_{pickup} = pickup level

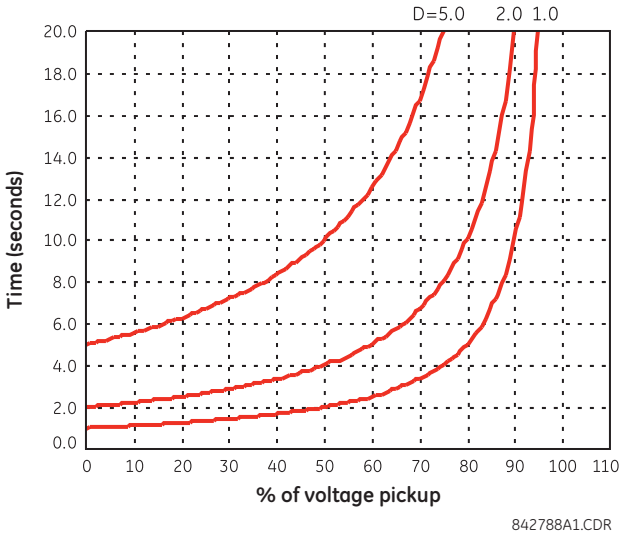


Figure 5–98: INVERSE TIME UNDERVOLTAGE CURVES

NOTE

At 0% of pickup, the operating time equals the UNDERVOLTAGE DELAY setting.

b) PHASE UNDERVOLTAGE (ANSI 27P)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS ⇨ PHASE UNDERVOLTAGE1(2)

■ PHASE ■ UNDERVOLTAGE1		PHASE UV1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE		PHASE UV1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
MESSAGE		PHASE UV1 MODE: Phase to Ground	Range: Phase to Ground, Phase to Phase
MESSAGE		PHASE UV1 PICKUP: 1.000 pu	Range: 0.000 to 3.000 pu in steps of 0.001
MESSAGE		PHASE UV1 CURVE: Definite Time	Range: Definite Time, Inverse Time
MESSAGE		PHASE UV1 DELAY: 1.00 s	Range: 0.00 to 600.00 s in steps of 0.01
MESSAGE		PHASE UV1 MINIMUM VOLTAGE: 0.100 pu	Range: 0.000 to 3.000 pu in steps of 0.001
MESSAGE		PHASE UV1 BLOCK: Off	Range: FlexLogic™ operand
MESSAGE		PHASE UV1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE		PHASE UV1 EVENTS: Disabled	Range: Disabled, Enabled

This element may be used to give a desired time-delay operating characteristic versus the applied fundamental voltage (phase-to-ground or phase-to-phase for Wye VT connection, or phase-to-phase for Delta VT connection) or as a Definite Time element. The element resets instantaneously if the applied voltage exceeds the dropout voltage. The delay setting selects the minimum operating time of the phase undervoltage. The minimum voltage setting selects the operating voltage below which the element is blocked (a setting of "0" will allow a dead source to be considered a fault condition).

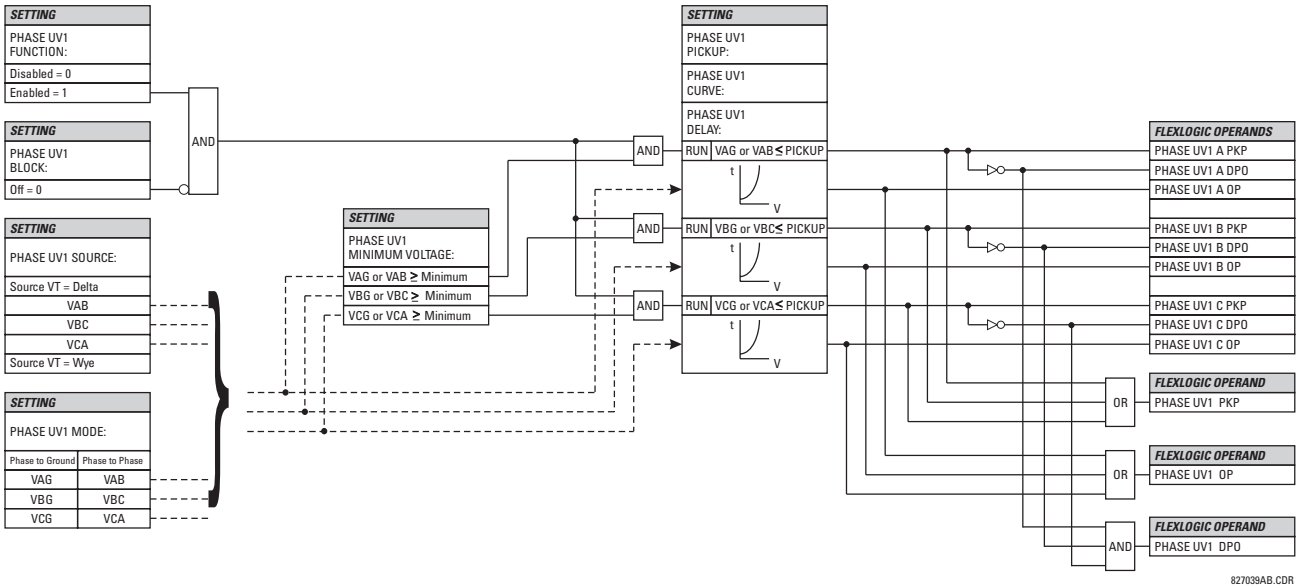


Figure 5–99: PHASE UNDERVOLTAGE1 SCHEME LOGIC

c) PHASE OVERVOLTAGE (ANSI 59P)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS ⇨⇩ PHASE OVERVOLTAGE1

■ PHASE ■ OVERVOLTAGE1		PHASE OV1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	PHASE OV1 SIGNAL SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	PHASE OV1 PICKUP: 1.000 pu	*Range: 0.000 to 3.000 pu in steps of 0.001*
	MESSAGE	PHASE OV1 PICKUP DELAY: 1.00 s	*Range: 0.00 to 600.00 s in steps of 0.01*
	MESSAGE	PHASE OV1 RESET DELAY: 1.00 s	*Range: 0.00 to 600.00 s in steps of 0.01*
	MESSAGE	PHASE OV1 BLOCK: Off	*Range: FlexLogic™ Operand*
	MESSAGE	PHASE OV1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	PHASE OV1 EVENTS: Disabled	*Range: Disabled, Enabled*

5

The phase overvoltage element may be used as an instantaneous element with no intentional time delay or as a definite time element. The input voltage is the phase-to-phase voltage, either measured directly from delta-connected VTs or as calculated from phase-to-ground (wye) connected VTs. The specific voltages to be used for each phase are shown below.

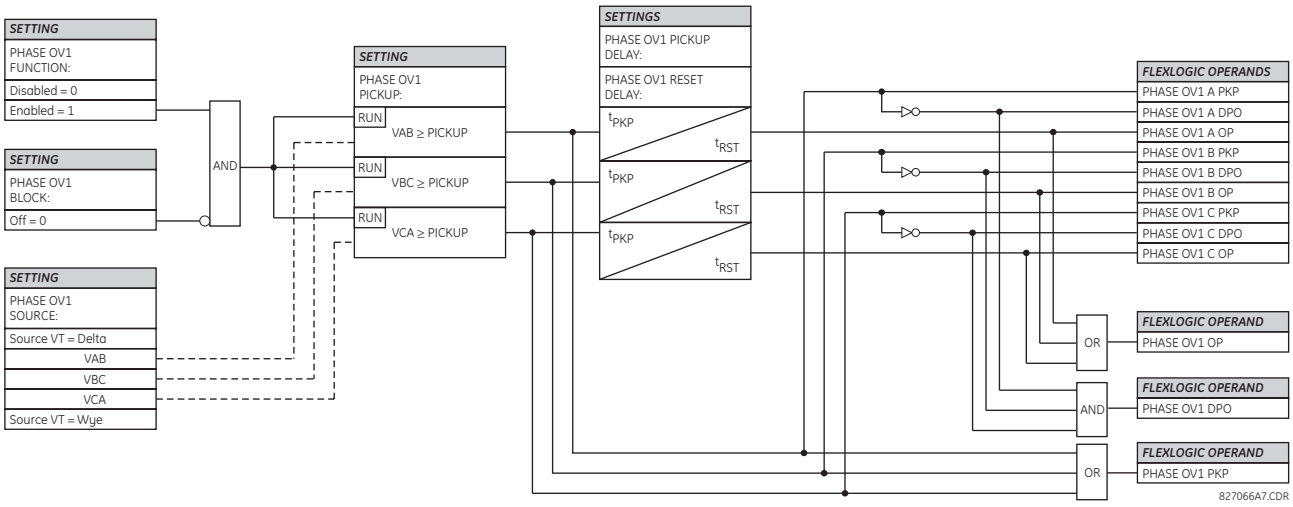


Figure 5–100: PHASE OVERVOLTAGE SCHEME LOGIC

d) NEUTRAL OVERVOLTAGE (ANSI 59N)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS ⇨⇩ NEUTRAL OV1(3)

■ NEUTRAL OV1 ■		NEUTRAL OV1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	NEUTRAL OV1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	NEUTRAL OV1 PICKUP: 0.300 pu	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	NEUTRAL OV1 CURVE: Definite time	Range: Definite time, FlexCurve A, FlexCurve B, FlexCurve C
	MESSAGE	NEUTRAL OV1 PICKUP DELAY: 1.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	NEUTRAL OV1 RESET DELAY: 1.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	NEUTRAL OV1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	NEUTRAL OV1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	NEUTRAL OV1 EVENTS: Disabled	Range: Disabled, Enabled

There are three neutral overvoltage elements available. The neutral overvoltage element can be used to detect asymmetrical system voltage condition due to a ground fault or to the loss of one or two phases of the source. The element responds to the system neutral voltage (3V_0), calculated from the phase voltages. The nominal secondary voltage of the phase voltage channels entered under SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨⇩ VOLTAGE BANK ⇨ PHASE VT SECONDARY is the p.u. base used when setting the pickup level.

The neutral overvoltage element can provide a time-delayed operating characteristic versus the applied voltage (initialized from FlexCurves A, B, or C) or be used as a definite time element. The **NEUTRAL OV1(3) PICKUP DELAY** setting applies only if the **NEUTRAL OV1(3) CURVE** setting is “Definite time”. The source assigned to this element must be configured for a phase VT.

VT errors and normal voltage unbalance must be considered when setting this element. This function requires the VTs to be wye-connected.

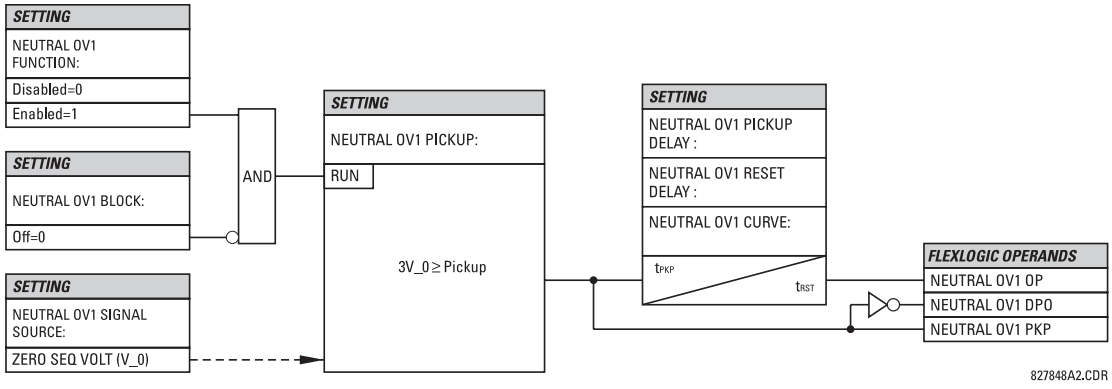


Figure 5–101: NEUTRAL OVERVOLTAGE1 SCHEME LOGIC

e) NEGATIVE SEQUENCE OVERVOLTAGE (ANSI 59_2)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS ⇨⇩ NEG SEQ OV1(3)

■ NEG SEQ OV1 ■		NEG SEQ OV1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	NEG SEQ OV1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	NEG SEQ OV1 PICKUP: 0.300 pu	Range: 0.000 to 1.250 pu in steps of 0.001
	MESSAGE	NEG SEQ OV1 PICKUP DELAY: 0.50 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	NEG SEQ OV1 RESET DELAY: 0.50 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	NEG SEQ OV1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	NEG SEQ OV1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	NEG SEQ OV1 EVENTS: Disabled	Range: Disabled, Enabled

5

There are three negative-sequence overvoltage elements available.

The negative-sequence overvoltage element may be used to detect loss of one or two phases of the source, a reversed phase sequence of voltage, or a non-symmetrical system voltage condition.

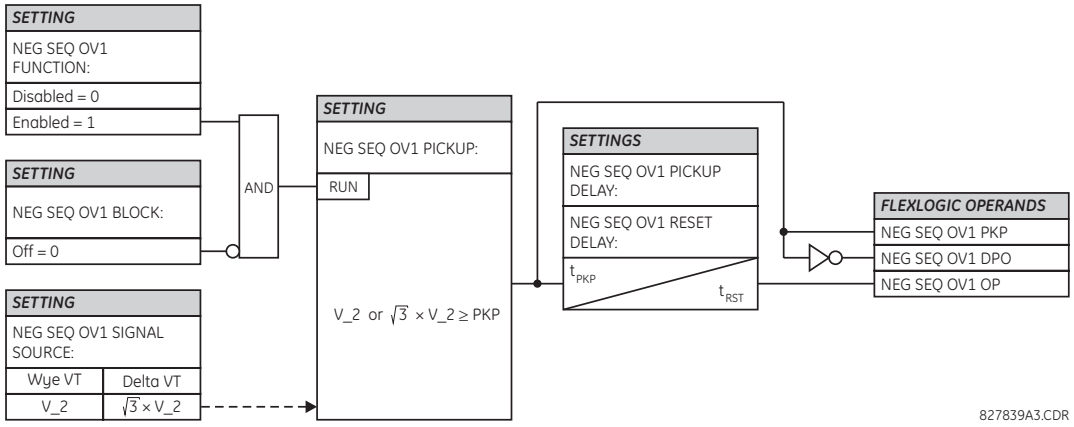


Figure 5–102: NEGATIVE-SEQUENCE OVERVOLTAGE SCHEME LOGIC

f) AUXILIARY UNDERVOLTAGE (ANSI 27X)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS ⇨⇩ AUXILIARY UV1(2)

■ AUXILIARY UV1 ■		AUX UV1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	AUX UV1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	AUX UV1 PICKUP: 0.700 pu	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	AUX UV1 CURVE: Definite Time	Range: Definite Time, Inverse Time
	MESSAGE	AUX UV1 DELAY: 1.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	AUX UV1 MINIMUM: VOLTAGE: 0.100 pu	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	AUX UV1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	AUX UV1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	AUX UV1 EVENTS: Disabled	Range: Disabled, Enabled

The L60 contains one auxiliary overvoltage element for each VT bank. This element is intended for monitoring undervoltage conditions of the auxiliary voltage. The **AUX UV1 PICKUP** selects the voltage level at which the time undervoltage element starts timing. The nominal secondary voltage of the auxiliary voltage channel entered under **SETTINGS ⇨⇩ SYSTEM SETUP ⇨ AC INPUTS ⇨⇩ VOLTAGE BANK X5 ⇨⇩ AUXILIARY VT X5 SECONDARY** is the per-unit base used when setting the pickup level.

The **AUX UV1 DELAY** setting selects the minimum operating time of the auxiliary undervoltage element. Both **AUX UV1 PICKUP** and **AUX UV1 DELAY** settings establish the operating curve of the undervoltage element. The auxiliary undervoltage element can be programmed to use either definite time delay or inverse time delay characteristics. The operating characteristics and equations for both definite and inverse time delay are as for the phase undervoltage element.

The element resets instantaneously. The minimum voltage setting selects the operating voltage below which the element is blocked.

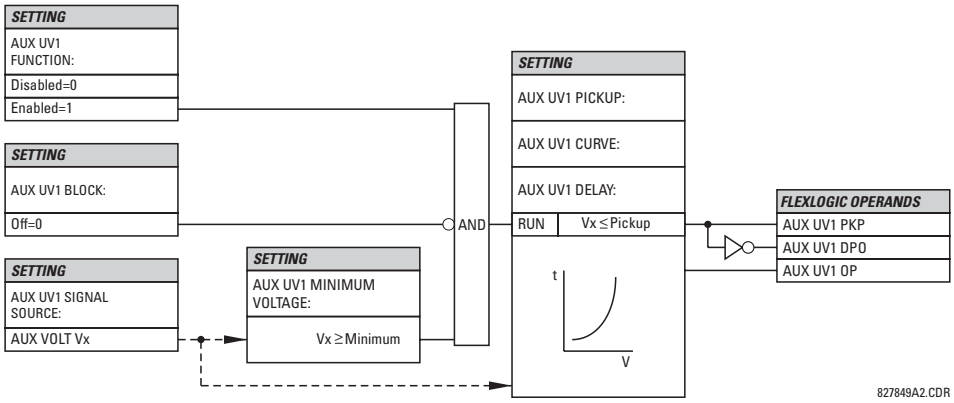


Figure 5–103: AUXILIARY UNDERVOLTAGE SCHEME LOGIC

g) AUXILIARY OVERVOLTAGE (ANSI 59X)

PATH: SETTINGS ⇨⇩ GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ VOLTAGE ELEMENTS ⇨⇩ AUXILIARY OV1(2)

■ AUXILIARY OV1 ■		AUX OV1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	AUX OV1 SIGNAL SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	AUX OV1 PICKUP: 0.300 pu	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	AUX OV1 PICKUP DELAY: 1.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	AUX OV1 RESET DELAY: 1.00 s	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	AUX OV1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	AUX OV1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	AUX OV1 EVENTS: Disabled	Range: Disabled, Enabled

5

The L60 contains one auxiliary overvoltage element for each VT bank. This element is intended for monitoring overvoltage conditions of the auxiliary voltage. The nominal secondary voltage of the auxiliary voltage channel entered under SYSTEM SETUP ⇨ AC INPUTS ⇩⇨ VOLTAGE BANK X5 ⇩⇨ AUXILIARY VT X5 SECONDARY is the per-unit (pu) base used when setting the pickup level.

A typical application for this element is monitoring the zero-sequence voltage (3V_0) supplied from an open-corner-delta VT connection.

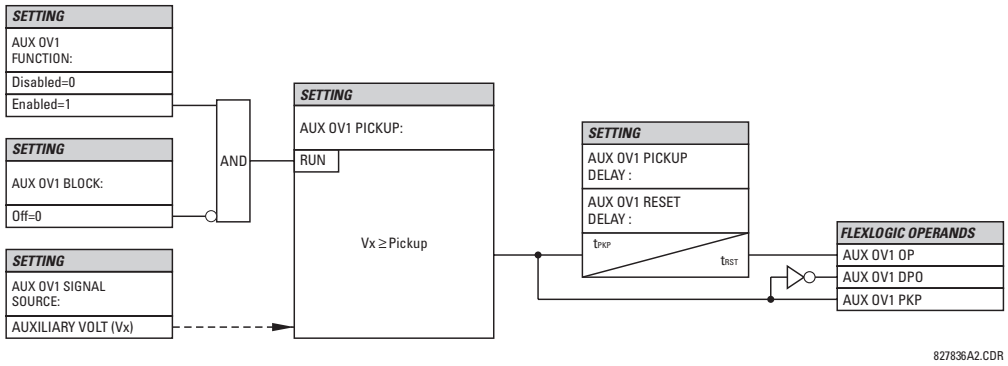


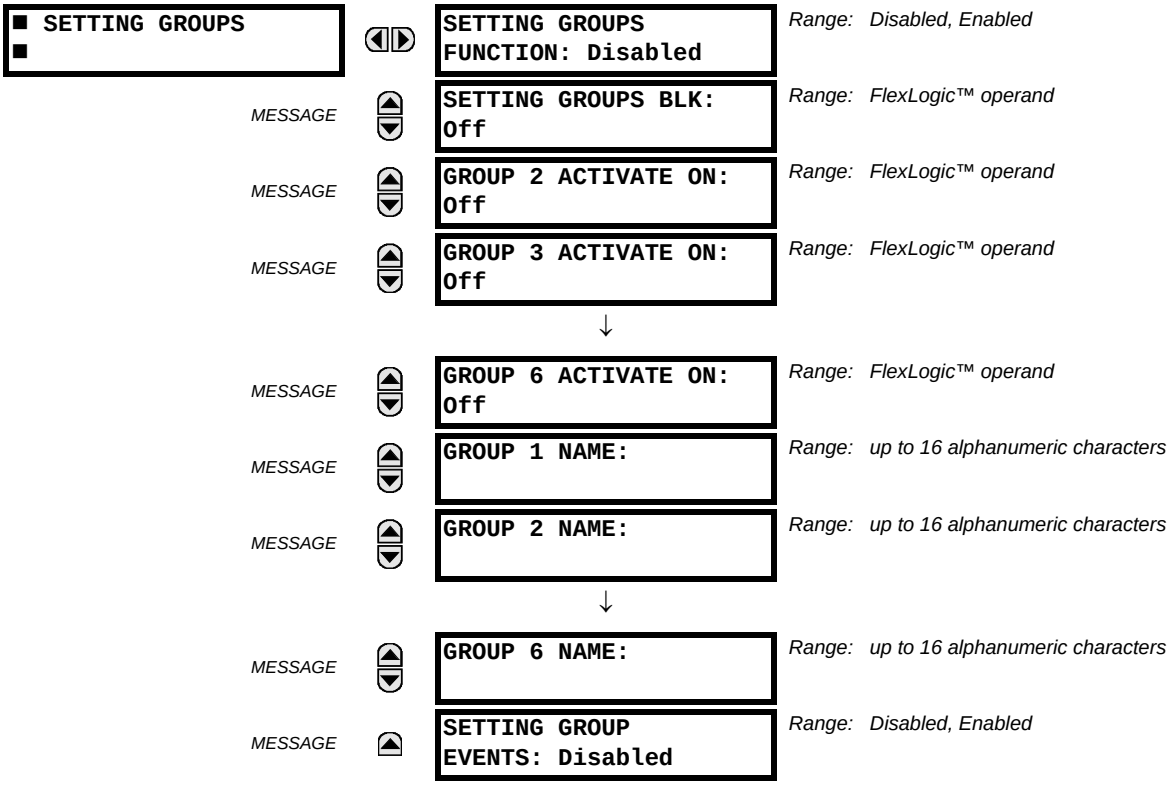
Figure 5–104: AUXILIARY OVERVOLTAGE SCHEME LOGIC

5.6.1 OVERVIEW

Control elements are generally used for control rather than protection. See the *Introduction to Elements* section at the beginning of this chapter for further information.

5.6.2 SETTING GROUPS

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨ SETTINGS GROUPS



The Setting Groups menu controls the activation/deactivation of up to six possible groups of settings in the **GROUPED ELEMENTS** settings menu. The faceplate 'Settings In Use' LEDs indicate which active group (with a non-flashing energized LED) is in service.

The **SETTING GROUPS BLK** setting prevents the active setting group from changing when the FlexLogic™ parameter is set to "On". This can be useful in applications where it is undesirable to change the settings under certain conditions, such as the breaker being open.

Each **GROUP n ACTIVATE ON** setting selects a FlexLogic™ operand which, when set, will make the particular setting group active for use by any grouped element. A priority scheme ensures that only one group is active at a given time – the highest-numbered group which is activated by its **GROUP n ACTIVATE ON** parameter takes priority over the lower-numbered groups. There is no "activate on" setting for Group 1 (the default active group), because Group 1 automatically becomes active if no other group is active.

The **SETTING GROUP 1(6) NAME** settings allows to user to assign a name to each of the six settings groups. Once programmed, this name will appear on the second line of the **GROUPED ELEMENTS ⇨ SETTING GROUP 1(6)** menu display.

The relay can be set up via a FlexLogic™ equation to receive requests to activate or de-activate a particular non-default settings group. The following FlexLogic™ equation (see the figure below) illustrates requests via remote communications (e.g. VIRTUAL INPUT 1 ON) or from a local contact input (e.g. CONTACT IP 1 ON) to initiate the use of a particular settings group, and requests from several overcurrent pickup measuring elements to inhibit the use of the particular settings group. The assigned VIRTUAL OUTPUT 1 operand is used to control the "On" state of a particular settings group.

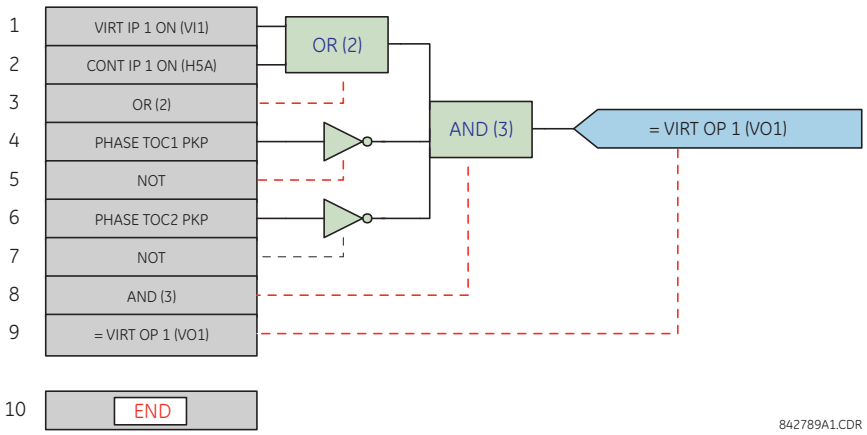


Figure 5–105: EXAMPLE FLEXLOGIC™ CONTROL OF A SETTINGS GROUP

5.6.3 SELECTOR SWITCH

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ SELECTOR SWITCH ⇨ SELECTOR SWITCH 1(2)

■ SELECTOR SWITCH 1 ■		SELECTOR 1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	SELECTOR 1 FULL RANGE: 7	Range: 1 to 7 in steps of 1
	MESSAGE	SELECTOR 1 TIME-OUT: 5.0 s	Range: 3.0 to 60.0 s in steps of 0.1
	MESSAGE	SELECTOR 1 STEP-UP: Off	Range: FlexLogic™ operand
	MESSAGE	SELECTOR 1 STEP-UP MODE: Time-out	Range: Time-out, Acknowledge
	MESSAGE	SELECTOR 1 ACK: Off	Range: FlexLogic™ operand
	MESSAGE	SELECTOR 1 3BIT A0: Off	Range: FlexLogic™ operand
	MESSAGE	SELECTOR 1 3BIT A1: Off	Range: FlexLogic™ operand
	MESSAGE	SELECTOR 1 3BIT A2: Off	Range: FlexLogic™ operand
	MESSAGE	SELECTOR 1 3BIT MODE: Time-out	Range: Time-out, Acknowledge
	MESSAGE	SELECTOR 1 3BIT ACK: Off	Range: FlexLogic™ operand
	MESSAGE	SELECTOR 1 POWER-UP MODE: Restore	Range: Restore, Synchronize, Sync/Restore
	MESSAGE	SELECTOR 1 TARGETS: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	SELECTOR 1 EVENTS: Disabled	Range: Disabled, Enabled

The Selector Switch element is intended to replace a mechanical selector switch. Typical applications include setting group control or control of multiple logic sub-circuits in user-programmable logic.

The element provides for two control inputs. The step-up control allows stepping through selector position one step at a time with each pulse of the control input, such as a user-programmable pushbutton. The 3-bit control input allows setting the selector to the position defined by a 3-bit word.

The element allows pre-selecting a new position without applying it. The pre-selected position gets applied either after time-out or upon acknowledgement via separate inputs (user setting). The selector position is stored in non-volatile memory. Upon power-up, either the previous position is restored or the relay synchronizes to the current 3-bit word (user setting). Basic alarm functionality alerts the user under abnormal conditions; e.g. the 3-bit control input being out of range.

- **SELECTOR 1 FULL RANGE**: This setting defines the upper position of the selector. When stepping up through available positions of the selector, the upper position wraps up to the lower position (Position 1). When using a direct 3-bit control word for programming the selector to a desired position, the change would take place only if the control word is within the range of 1 to the **SELECTOR FULL RANGE**. If the control word is outside the range, an alarm is established by setting the SELECTOR ALARM FlexLogic™ operand for 3 seconds.
- **SELECTOR 1 TIME-OUT:** This setting defines the time-out period for the selector. This value is used by the relay in the following two ways. When the **SELECTOR STEP-UP MODE** is “Time-out”, the setting specifies the required period of inactivity of the control input after which the pre-selected position is automatically applied. When the **SELECTOR STEP-UP MODE** is “Acknowledge”, the setting specifies the period of time for the acknowledging input to appear. The timer is re-started by any activity of the control input. The acknowledging input must come before the **SELECTOR 1 TIME-OUT** timer expires; otherwise, the change will not take place and an alarm will be set.
- **SELECTOR 1 STEP-UP**: This setting specifies a control input for the selector switch. The switch is shifted to a new position at each rising edge of this signal. The position changes incrementally, wrapping up from the last (**SELECTOR 1 FULL RANGE**) to the first (Position 1). Consecutive pulses of this control operand must not occur faster than every 50 ms. After each rising edge of the assigned operand, the time-out timer is restarted and the **SELECTOR SWITCH 1: POS Z CHNG INITIATED** target message is displayed, where ***Z*** the pre-selected position. The message is displayed for the time specified by the **FLASH MESSAGE TIME** setting. The pre-selected position is applied after the selector times out (“Time-out” mode), or when the acknowledging signal appears before the element times out (“Acknowledge” mode). When the new position is applied, the relay displays the **SELECTOR SWITCH 1: POSITION Z IN USE** message. Typically, a user-programmable pushbutton is configured as the stepping up control input.
- **SELECTOR 1 STEP-UP MODE**: This setting defines the selector mode of operation. When set to “Time-out”, the selector will change its position after a pre-defined period of inactivity at the control input. The change is automatic and does not require any explicit confirmation of the intent to change the selector's position. When set to “Acknowledge”, the selector will change its position only after the intent is confirmed through a separate acknowledging signal. If the acknowledging signal does not appear within a pre-defined period of time, the selector does not accept the change and an alarm is established by setting the SELECTOR STP ALARM output FlexLogic™ operand for 3 seconds.
- **SELECTOR 1 ACK**: This setting specifies an acknowledging input for the stepping up control input. The pre-selected position is applied on the rising edge of the assigned operand. This setting is active only under “Acknowledge” mode of operation. The acknowledging signal must appear within the time defined by the **SELECTOR 1 TIME-OUT** setting after the last activity of the control input. A user-programmable pushbutton is typically configured as the acknowledging input.
- **SELECTOR 1 3BIT A0, A1, and A2**: These settings specify a 3-bit control input of the selector. The 3-bit control word pre-selects the position using the following encoding convention:

A2	A1	A0	POSITION
0	0	0	rest
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The "rest" position (0, 0, 0) does not generate an action and is intended for situations when the device generating the 3-bit control word is having a problem. When **SELECTOR 1 3BIT MODE** is "Time-out", the pre-selected position is applied in **SELECTOR 1 TIME-OUT** seconds after the last activity of the 3-bit input. When **SELECTOR 1 3BIT MODE** is "Acknowledge", the pre-selected position is applied on the rising edge of the **SELECTOR 1 3BIT ACK** acknowledging input.

The stepping up control input (**SELECTOR 1 STEP-UP**) and the 3-bit control inputs (**SELECTOR 1 3BIT A0** through **A2**) lockout mutually: once the stepping up sequence is initiated, the 3-bit control input is inactive; once the 3-bit control sequence is initiated, the stepping up input is inactive.

- **SELECTOR 1 3BIT MODE**: This setting defines the selector mode of operation. When set to "Time-out", the selector changes its position after a pre-defined period of inactivity at the control input. The change is automatic and does not require explicit confirmation to change the selector position. When set to "Acknowledge", the selector changes its position only after confirmation via a separate acknowledging signal. If the acknowledging signal does not appear within a pre-defined period of time, the selector rejects the change and an alarm established by invoking the SELECTOR BIT ALARM FlexLogic™ operand for 3 seconds.
- **SELECTOR 1 3BIT ACK**: This setting specifies an acknowledging input for the 3-bit control input. The pre-selected position is applied on the rising edge of the assigned FlexLogic™ operand. This setting is active only under the "Acknowledge" mode of operation. The acknowledging signal must appear within the time defined by the **SELECTOR TIME-OUT** setting after the last activity of the 3-bit control inputs. Note that the stepping up control input and 3-bit control input have independent acknowledging signals (**SELECTOR 1 ACK** and **SELECTOR 1 3BIT ACK**, accordingly).
- **SELECTOR 1 POWER-UP MODE**: This setting specifies the element behavior on power up of the relay.

  When set to "Restore", the last position of the selector (stored in the non-volatile memory) is restored after powering up the relay. If the position restored from memory is out of range, position 0 (no output operand selected) is applied and an alarm is set (SELECTOR 1 PWR ALARM).

  When set to "Synchronize" selector switch acts as follows. For two power cycles, the selector applies position 0 to the switch and activates SELECTOR 1 PWR ALARM. After two power cycles expire, the selector synchronizes to the position dictated by the 3-bit control input. This operation does not wait for time-out or the acknowledging input. When the synchronization attempt is unsuccessful (i.e., the 3-bit input is not available (0,0,0) or out of range) then the selector switch output is set to position 0 (no output operand selected) and an alarm is established (SELECTOR 1 PWR ALARM).

  The operation of "Synch/Restore" mode is similar to the "Synchronize" mode. The only difference is that after an unsuccessful synchronization attempt, the switch will attempt to restore the position stored in the relay memory. The "Synch/Restore" mode is useful for applications where the selector switch is employed to change the setting group in redundant (two relay) protection schemes.
- **SELECTOR 1 EVENTS**: If enabled, the following events are logged:

EVENT NAME	DESCRIPTION
SELECTOR 1 POS Z	Selector 1 changed its position to Z.
SELECTOR 1 STP ALARM	The selector position pre-selected via the stepping up control input has not been confirmed before the time out.
SELECTOR 1 BIT ALARM	The selector position pre-selected via the 3-bit control input has not been confirmed before the time out.

The following figures illustrate the operation of the Selector Switch. In these diagrams, “T” represents a time-out setting.

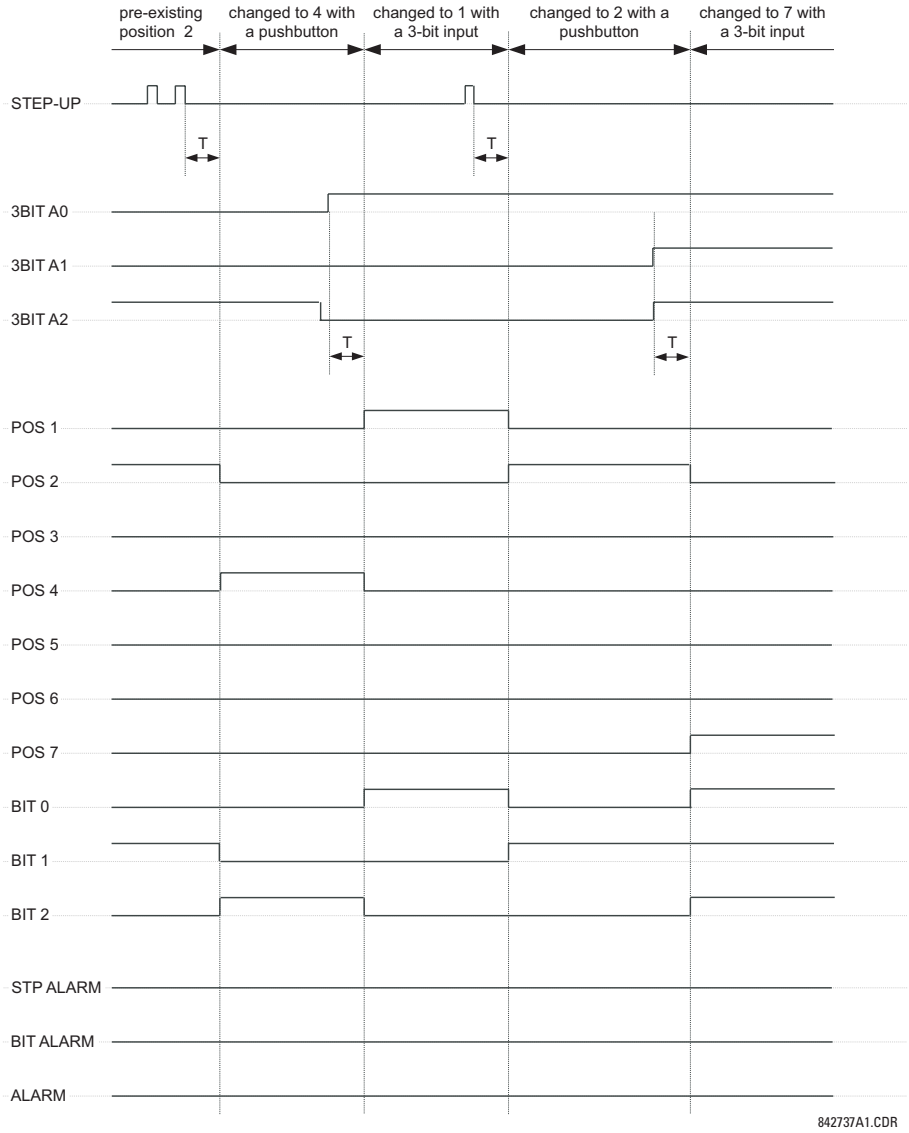


Figure 5–106: TIME-OUT MODE

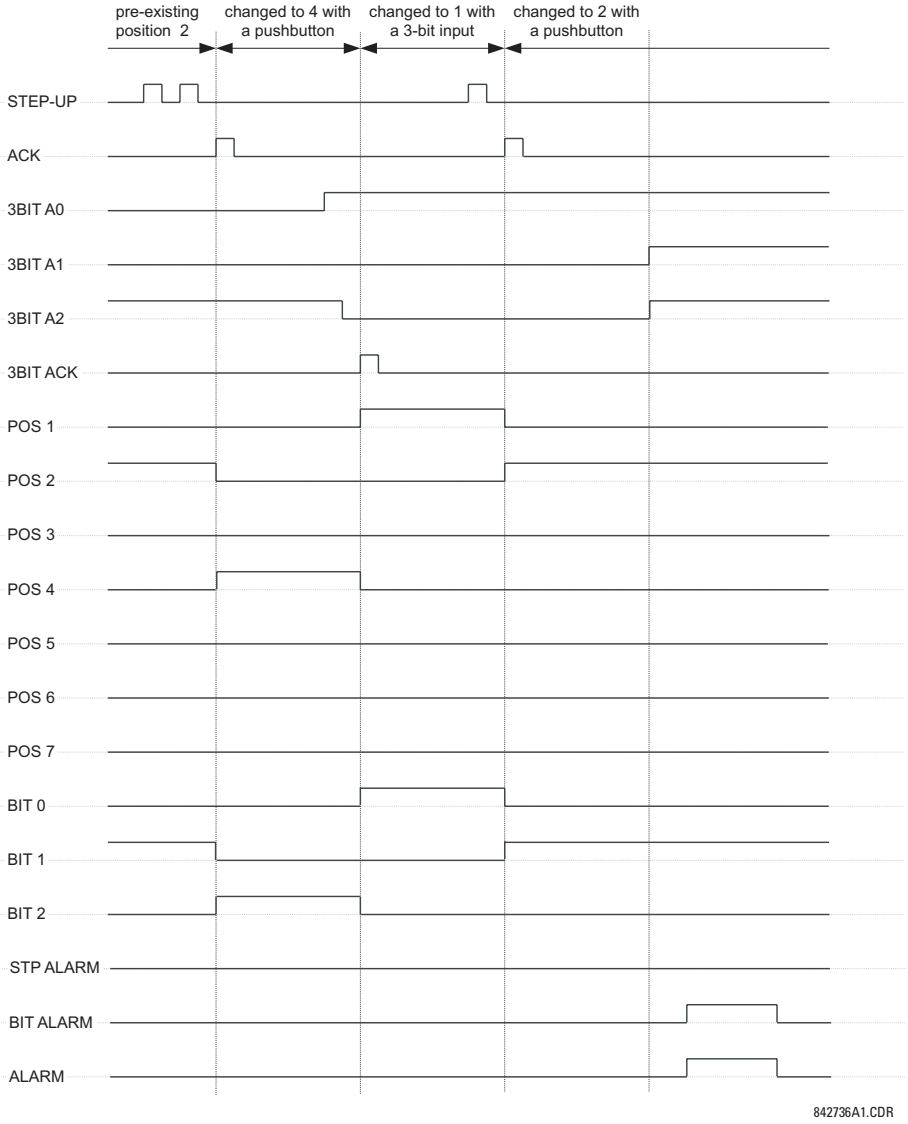


Figure 5–107: ACKNOWLEDGE MODE

APPLICATION EXAMPLE

Consider an application where the selector switch is used to control Setting Groups 1 through 4 in the relay. The setting groups are to be controlled from both User-Programmable Pushbutton 1 and from an external device via Contact Inputs 1 through 3. The active setting group shall be available as an encoded 3-bit word to the external device and SCADA via output contacts 1 through 3. The pre-selected setting group shall be applied automatically after 5 seconds of inactivity of the control inputs. When the relay powers up, it should synchronize the setting group to the 3-bit control input.

Make the following changes to Setting Group Control in the **SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨ SETTING GROUPS** menu:

SETTING GROUPS FUNCTION: "Enabled"
SETTING GROUPS BLK: "Off"
GROUP 2 ACTIVATE ON: "SELECTOR 1 POS 2"
GROUP 3 ACTIVATE ON: "SELECTOR 1 POS 3"
GROUP 4 ACTIVATE ON: "SELECTOR 1 POS 4"
GROUP 5 ACTIVATE ON: "Off"
GROUP 6 ACTIVATE ON: "Off"

Make the following changes to Selector Switch element in the **SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ SELECTOR SWITCH ⇨ SELECTOR SWITCH 1** menu to assign control to User Programmable Pushbutton 1 and Contact Inputs 1 through 3:

SELECTOR 1 FUNCTION: "Enabled"
SELECTOR 1 FULL-RANGE: "4"
SELECTOR 1 STEP-UP MODE: "Time-out"
SELECTOR 1 TIME-OUT: "5.0 s"
SELECTOR 1 STEP-UP: "PUSHBUTTON 1 ON"
SELECTOR 1 ACK: "Off"
SELECTOR 1 3BIT A0: "CONT IP 1 ON"
SELECTOR 1 3BIT A1: "CONT IP 2 ON"
SELECTOR 1 3BIT A2: "CONT IP 3 ON"
SELECTOR 1 3BIT MODE: "Time-out"
SELECTOR 1 3BIT ACK: "Off"
SELECTOR 1 POWER-UP MODE: "Synchronize"

Now, assign the contact output operation (assume the H6E module) to the Selector Switch element by making the following changes in the **SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS** menu:

OUTPUT H1 OPERATE: "SELECTOR 1 BIT 0"
OUTPUT H2 OPERATE: "SELECTOR 1 BIT 1"
OUTPUT H3 OPERATE: "SELECTOR 1 BIT 2"

Finally, assign configure User-Programmable Pushbutton 1 by making the following changes in the **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE PUSHBUTTONS ⇨ USER PUSHBUTTON 1** menu:

PUSHBUTTON 1 FUNCTION: "Self-reset"
PUSHBUTTON 1 DROP-OUT TIME: "0.10 s"

The logic for the selector switch is shown below:

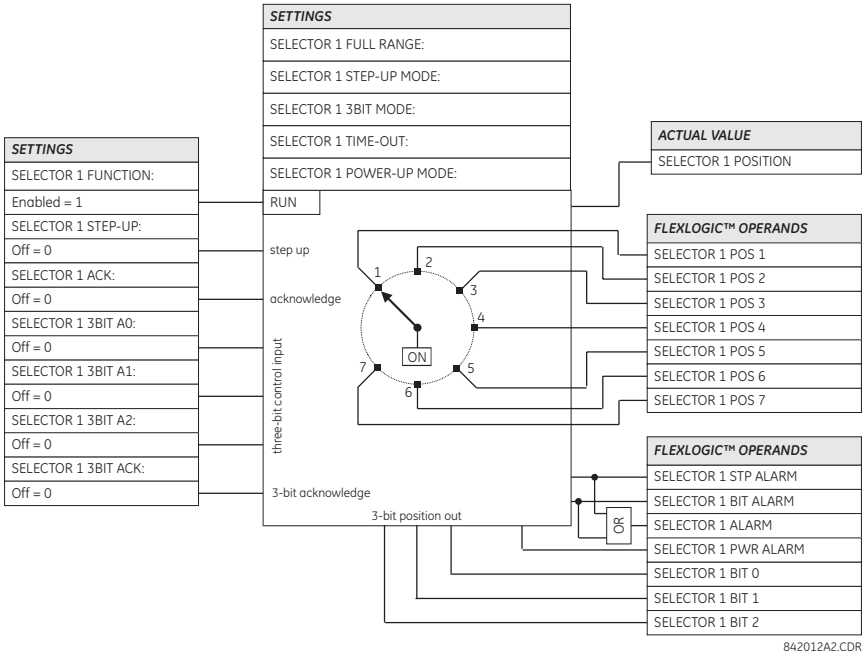


Figure 5–108: SELECTOR SWITCH LOGIC

5.6.4 TRIP OUTPUT

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ TRIP OUTPUT

■ TRIP OUTPUT ■		TRIP MODE: Disabled	*Range: Disabled, 3 Pole Only, 3 Pole & 1 Pole*
	MESSAGE	TRIP 3-POLE INPUT-1: Off	*Range: FlexLogic™ operand*
	MESSAGE	TRIP 3-POLE INPUT-2: Off	*Range: FlexLogic™ operand*
		↓	
	MESSAGE	TRIP 3-POLE INPUT-6: Off	*Range: FlexLogic™ operand*
	MESSAGE	TRIP 1-POLE INPUT-1: Off	*Range: FlexLogic™ operand*
	MESSAGE	TRIP 1-POLE INPUT-2: Off	*Range: FlexLogic™ operand*
		↓	
	MESSAGE	TRIP 1-POLE INPUT-6: Off	*Range: FlexLogic™ operand*
	MESSAGE	TRIP RECLOSE INPUT-1: Off	*Range: FlexLogic™ operand*
	MESSAGE	TRIP RECLOSE INPUT-2: Off	*Range: FlexLogic™ operand*
		↓	

MESSAGE
TRIP RECLOSE INPUT-6:
Off
Range: FlexLogic™ operand

MESSAGE
TRIP FORCE 3-POLE:
Off
Range: FlexLogic™ operand

MESSAGE
TRIP PILOT PRIORITY:
0.000 s
Range: 0 to 65.535 s in steps of 0.001

MESSAGE
REVERSE FAULT:
Off
Range: FlexLogic™ operand

MESSAGE
TRIP DELAY ON EVOLV FAULTS: 0.000 s
Range: 0 to 65.535 s in steps of 0.001

MESSAGE
BKR ΦA OPEN:
Off
Range: FlexLogic™ operand

MESSAGE
BKR ΦB OPEN:
Off
Range: FlexLogic™ operand

MESSAGE
BKR ΦC OPEN:
Off
Range: FlexLogic™ operand

MESSAGE
TRIP EVENTS:
Disabled
Range: Enabled, Disabled

The trip output element is primarily used to collect trip requests from protection elements and other inputs to generate output operands to initiate trip operations. Three pole trips will only initiate reclosure if programmed to do so, whereas single pole trips will always automatically initiate reclosure. The TRIP 3-POLE and TRIP 1-POLE output operands can also be used as inputs to a FlexLogic™ OR gate to operate the faceplate Trip indicator LED.

THREE POLE OPERATION:

In applications where single-pole tripping is not required this element provides a convenient method of collecting inputs to initiate tripping of circuit breakers, the reclose element and breaker failure elements.

SINGLE POLE OPERATION:

NOTE

This element *must* be used in single pole operation applications.

In these applications this element is used to:

- Determine if a single pole operation should be performed.
- Collect inputs to initiate three pole tripping, the recloser and breaker failure elements.
- Collect inputs to initiate single pole tripping, the recloser and breaker failure elements.
- Assign a higher priority to pilot aided scheme outputs than to exclusively local inputs.

The trip output element works in association with other L60 elements (refer to chapter 8 for a complete description of single pole operations) that must be programmed and in-service for successful operation. The necessary elements are: recloser, breaker control, open pole detector, and phase selector. The recloser must also be in the “Reset” state before a single pole trip can be issued. Outputs from this element are also directly connected as initiate signals to the breaker failure elements.

At least one internal protection element or digital input representing detection of a fault must be available as an input to this element. In pilot-aided scheme applications, a timer can be used to delay the output decision until data from a remote terminal is received from communications facilities, to prevent a three pole operation where a single pole operation is permitted.

- **TRIP MODE**: This setting is used to select the required mode of operation. If selected to “3 Pole Only” outputs for all three phases are always set simultaneously. If selected to “3 Pole & 1 Pole” outputs for all three phases are set simultaneously unless the phase selector or a pilot aided scheme determines the fault is single-phase-to-ground. If the fault is identified as being AG, BG or CG only the operands for the faulted phase will be asserted.

- **TRIP 3-POLE INPUT-1** to **TRIP 3-POLE INPUT-6**: These settings are used to select an operand representing a fault condition that is not desired to initiate a single pole operation (for example, phase undervoltage). Use a FlexLogic OR-gate if more than six inputs are required.
- **TRIP 1-POLE INPUT-1** to **TRIP 1-POLE INPUT-6**: These settings are used to select an operand representing a fault condition that is desired to initiate a single pole trip-and-reclose if the fault is single phase to ground (for example, distance zone 1). Use a FlexLogic™ OR-gate if more than six inputs are required. The inputs do not have to be phase-specific as the phase selector determines the fault type.

  The AR FORCE 3-P TRIP operand is asserted by the autorecloser 1.5 cycles after single-pole reclosing is initiated. This operand calls for a three-pole trip if any protection element configured under **TRIP 1-POLE INPUT** remains picked-up. The open pole detector provides blocking inputs to distance elements, and therefore the latter will reset immediately after the TRIP 1-POLE operand is asserted. For other protection elements used in single-pole tripping, the user must ensure they will reset immediately after tripping, otherwise the fact that they are still picked up will be detected as an evolving fault and the relay will trip three-poles. For example, if high-set phase instantaneous overcurrent is used (**TRIP 1-POLE INPUT X:** "PHASE IOC1 OP"), then OPEN POLE OP ΦA shall be used for blocking phase A of the instantaneous overcurrent element. In this way, after tripping phase A, the phase a instantaneous overcurrent element is forced to reset. Phases B and C are still operational and can detect an evolving fault as soon as 8 ms after tripping phase A. Neutral and negative-sequence instantaneous overcurrent elements shall be blocked from the OPEN POLE BLK N operand unless the pickup setting is high enough to prevent pickup during single-pole reclosing.
- **TRIP RECLOSE INPUT-1** to **TRIP RECLOSE INPUT-6**: These settings select an operand representing a fault condition that is desired to initiate three pole reclosing (for example, phase distance zone 1). Use a FlexLogic™ OR-gate if more than six inputs are required.
- **TRIP FORCE 3-POLE**: Selects an operand that will force an input selected for single pole operation to produce a three pole operation. The AR DISABLED FlexLogic™ operand is the recommended value for this setting. Power system configurations or conditions which require such operations may be considered as well.
- **TRIP PILOT PRIORITY**: This setting is used to set an interval equal to the inter-relay channel communications time, plus an appropriate margin, during which outputs are not asserted. This delay permits fault identification information from a remote terminal to be used instead of local data only.
- **REVERSE FAULT**: This setting should be used to guarantee accuracy of single-pole tripping under evolving external to internal faults. When a close-in external fault occurs, the relay is biased toward very fast operation on a following internal fault. This is primarily due to depressed voltages and elevated currents in response to the first, external fault. The phase selector may exhibit some time lag compared to the main protection elements. This may potentially result in a spurious three-pole operation on a single-line-to-ground internal fault. Delaying tripping on internal faults that follow detection of reverse faults solves the problem.

  As long as the operand indicated under this setting is asserted the trip action will be delayed by **TRIP DELAY ON EVOLV FAULTS** time. Typically this operand should combine reverse zone indications (such as zone 4 pickup) with a half-cycle pickup delay, and two-cycle dropout delay. This setting should be used only in single-pole tripping applications, when evolving faults are of importance, and slightly delayed operation on evolving faults could be traded for enhanced accuracy of single-pole tripping.
- **TRIP DELAY ON EVOLV FAULTS**: This setting should be used in conjunction with the **REVERSE FAULT** setting (see above). Typically this value should be set around half a power system cycle. This setting should be used only in single-pole tripping applications, when evolving faults are of importance, and slightly delayed operation on evolving faults could be traded for enhanced accuracy of single-pole tripping.

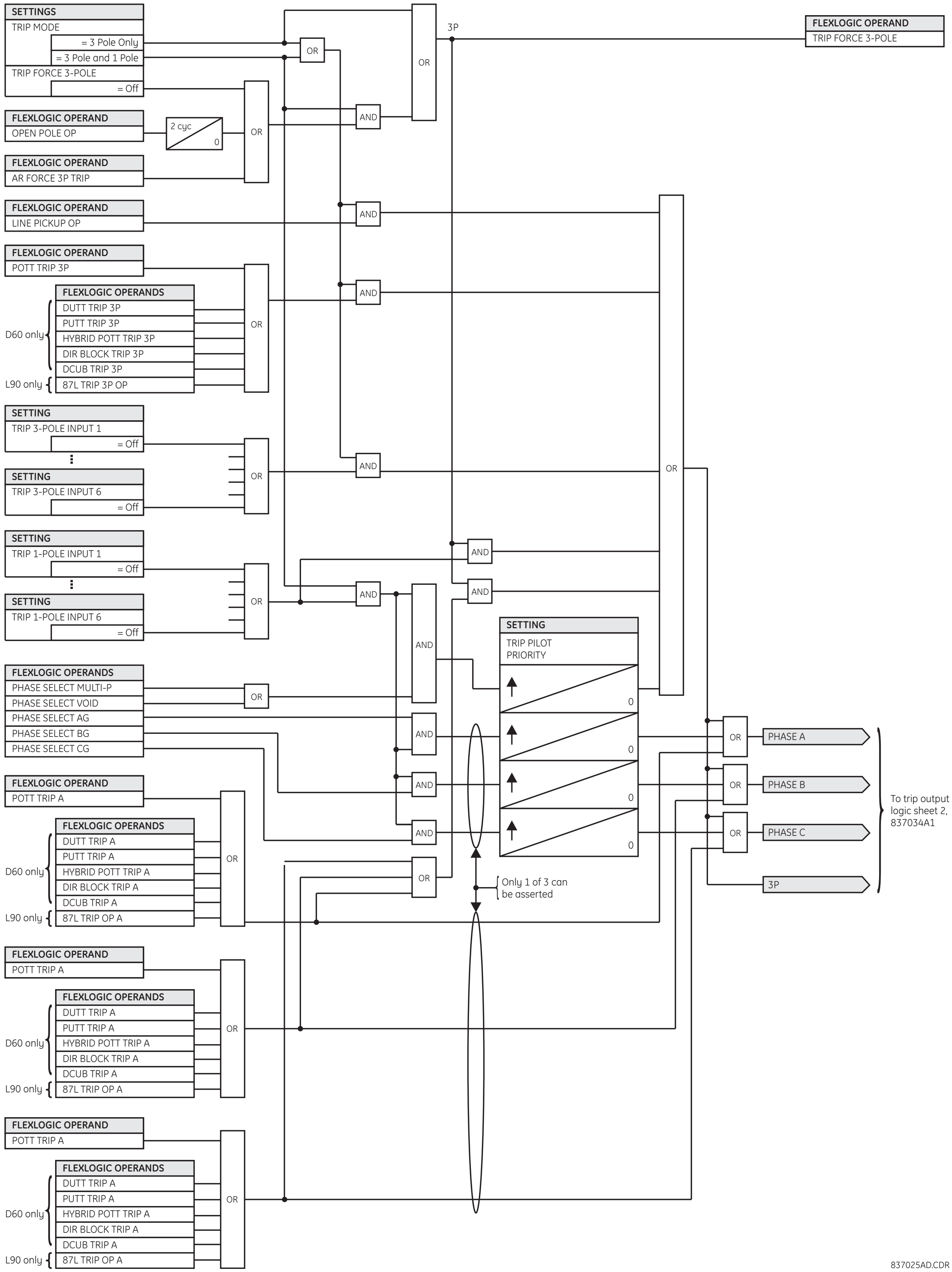


Figure 5–109: TRIP OUTPUT SCHEME LOGIC (Sheet 1 of 2)

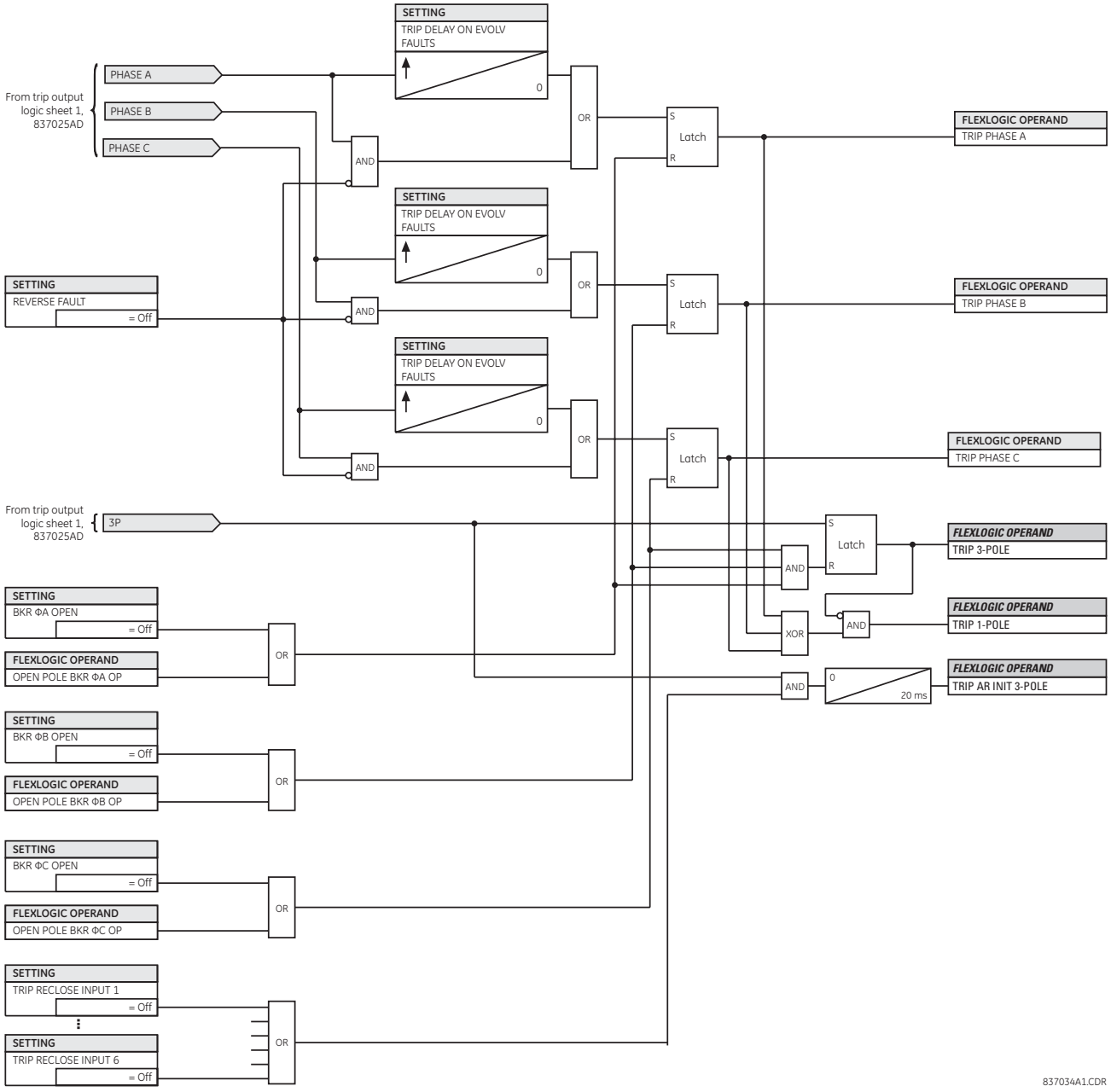


Figure 5–110: TRIP OUTPUT SCHEME LOGIC (Sheet 2 of 2)

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ SYNCHROCHECK ⇨ SYNCHROCHECK 1(2)

■ SYNCHROCHECK 1 ■		SYNCHK1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	SYNCHK1 BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	SYNCHK1 V1 SOURCE: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	SYNCHK1 V2 SOURCE: SRC 2	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	SYNCHK1 MAX VOLT DIFF: 10000 V	Range: 0 to 400000 V in steps of 1
	MESSAGE	SYNCHK1 MAX ANGLE DIFF: 30°	Range: 0 to 100° in steps of 1
	MESSAGE	SYNCHK1 MAX FREQ DIFF: 1.00 Hz	Range: 0.00 to 2.00 Hz in steps of 0.01
	MESSAGE	SYNCHK1 MAX FREQ HYSTERESIS: 0.06 Hz	Range: 0.00 to 0.10 Hz in steps of 0.01
	MESSAGE	SYNCHK1 DEAD SOURCE SELECT: LV1 and DV2	Range: None, LV1 and DV2, DV1 and LV2, DV1 or DV2, DV1 Xor DV2, DV1 and DV2
	MESSAGE	SYNCHK1 DEAD V1 MAX VOLT: 0.30 pu	Range: 0.00 to 1.25 pu in steps of 0.01
	MESSAGE	SYNCHK1 DEAD V2 MAX VOLT: 0.30 pu	Range: 0.00 to 1.25 pu in steps of 0.01
	MESSAGE	SYNCHK1 LIVE V1 MIN VOLT: 0.70 pu	Range: 0.00 to 1.25 pu in steps of 0.01
	MESSAGE	SYNCHK1 LIVE V2 MIN VOLT: 0.70 pu	Range: 0.00 to 1.25 pu in steps of 0.01
	MESSAGE	SYNCHK1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	SYNCHK1 EVENTS: Disabled	Range: Disabled, Enabled

The are two identical synchrocheck elements available, numbered 1 and 2.

The synchronism check function is intended for supervising the paralleling of two parts of a system which are to be joined by the closure of a circuit breaker. The synchrocheck elements are typically used at locations where the two parts of the system are interconnected through at least one other point in the system.

Synchrocheck verifies that the voltages (V1 and V2) on the two sides of the supervised circuit breaker are within set limits of magnitude, angle and frequency differences. The time that the two voltages remain within the admissible angle difference is determined by the setting of the phase angle difference $\Delta\Phi$ and the frequency difference ΔF (slip frequency). It can be defined as the time it would take the voltage phasor V1 or V2 to traverse an angle equal to $2 \times \Delta\Phi$ at a frequency equal to the frequency difference ΔF. This time can be calculated by:

$$T = \frac{1}{\frac{360^\circ}{2 \times \Delta\Phi} \times \Delta F} \quad \textbf{(EQ 5.26)}$$

where: $\Delta\Phi$ = phase angle difference in degrees; ΔF = frequency difference in Hz.

As an example; for the default values ($\Delta\Phi$ = 30°, ΔF = 0.1 Hz), the time while the angle between the two voltages will be less than the set value is:

$$T = \frac{1}{\frac{360^\circ}{2 \times \Delta\Phi} \times \Delta F} = \frac{1}{\frac{360^\circ}{2 \times 30^\circ} \times 0.1 \text{ Hz}} = 1.66 \text{ sec.} \quad \textbf{(EQ 5.27)}$$

If one or both sources are de-energized, the synchrocheck programming can allow for closing of the circuit breaker using undervoltage control to by-pass the synchrocheck measurements (Dead Source function).

- **SYNCHK1 V1 SOURCE**: This setting selects the source for voltage V1 (see NOTES below).
- **SYNCHK1 V2 SOURCE**: This setting selects the source for voltage V2, which must not be the same as used for the V1 (see NOTES below).
- **SYNCHK1 MAX VOLT DIFF**: This setting selects the maximum primary voltage difference in volts between the two sources. A primary voltage magnitude difference between the two input voltages below this value is within the permissible limit for synchronism.
- **SYNCHK1 MAX ANGLE DIFF:** This setting selects the maximum angular difference in degrees between the two sources. An angular difference between the two input voltage phasors below this value is within the permissible limit for synchronism.
- **SYNCHK1 MAX FREQ DIFF:** This setting selects the maximum frequency difference in 'Hz' between the two sources. A frequency difference between the two input voltage systems below this value is within the permissible limit for synchronism.
- **SYNCHK1 MAX FREQ HYSTERESIS**: This setting specifies the required hysteresis for the maximum frequency difference condition. The condition becomes satisfied when the frequency difference becomes lower than **SYNCHK1 MAX FREQ DIFF**. Once the Synchrocheck element has operated, the frequency difference must increase above the **SYNCHK1 MAX FREQ DIFF** + **SYNCHK1 MAX FREQ HYSTERESIS** sum to drop out (assuming the other two conditions, voltage and angle, remain satisfied).
- **SYNCHK1 DEAD SOURCE SELECT:** This setting selects the combination of dead and live sources that will by-pass synchronism check function and permit the breaker to be closed when one or both of the two voltages (V1 or/and V2) are below the maximum voltage threshold. A dead or live source is declared by monitoring the voltage level. Six options are available:

None:	Dead Source function is disabled
LV1 and DV2:	Live V1 and Dead V2
DV1 and LV2:	Dead V1 and Live V2
DV1 or DV2:	Dead V1 or Dead V2
DV1 Xor DV2:	Dead V1 exclusive-or Dead V2 (one source is Dead and the other is Live)
DV1 and DV2:	Dead V1 and Dead V2

- **SYNCHK1 DEAD V1 MAX VOLT:** This setting establishes a maximum voltage magnitude for V1 in 1 'pu'. Below this magnitude, the V1 voltage input used for synchrocheck will be considered "Dead" or de-energized.
- **SYNCHK1 DEAD V2 MAX VOLT**: This setting establishes a maximum voltage magnitude for V2 in 'pu'. Below this magnitude, the V2 voltage input used for synchrocheck will be considered "Dead" or de-energized.
- **SYNCHK1 LIVE V1 MIN VOLT**: This setting establishes a minimum voltage magnitude for V1 in 'pu'. Above this magnitude, the V1 voltage input used for synchrocheck will be considered "Live" or energized.
- **SYNCHK1 LIVE V2 MIN VOLT**: This setting establishes a minimum voltage magnitude for V2 in 'pu'. Above this magnitude, the V2 voltage input used for synchrocheck will be considered "Live" or energized.

NOTES ON THE SYNCHROCHECK FUNCTION:

1. The selected sources for synchrocheck inputs V1 and V2 (which must not be the same source) may include both a three-phase and an auxiliary voltage. The relay will automatically select the specific voltages to be used by the synchrocheck element in accordance with the following table.

NO.	V1 OR V2 (SOURCE Y)	V2 OR V1 (SOURCE Z)	AUTO-SELECTED COMBINATION		AUTO-SELECTED VOLTAGE
			SOURCE Y	SOURCE Z	
1	Phase VTs and Auxiliary VT	Phase VTs and Auxiliary VT	Phase	Phase	VAB
2	Phase VTs and Auxiliary VT	Phase VT	Phase	Phase	VAB
3	Phase VT	Phase VT	Phase	Phase	VAB
4	Phase VT and Auxiliary VT	Auxiliary VT	Phase	Auxiliary	V auxiliary (as set for Source z)
5	Auxiliary VT	Auxiliary VT	Auxiliary	Auxiliary	V auxiliary (as set for selected sources)

The voltages V1 and V2 will be matched automatically so that the corresponding voltages from the two sources will be used to measure conditions. A phase to phase voltage will be used if available in both sources; if one or both of the Sources have only an auxiliary voltage, this voltage will be used. For example, if an auxiliary voltage is programmed to VAG, the synchrocheck element will automatically select VAG from the other source. If the comparison is required on a specific voltage, the user can externally connect that specific voltage to auxiliary voltage terminals and then use this "Auxiliary Voltage" to check the synchronism conditions.

If using a single CT/VT module with both phase voltages and an auxiliary voltage, ensure that only the auxiliary voltage is programmed in one of the sources to be used for synchrocheck.

NOTE

Exception: Synchronism cannot be checked between Delta connected phase VTs and a Wye connected auxiliary voltage.

2. The relay measures frequency and Volts/Hz from an input on a given source with priorities as established by the configuration of input channels to the source. The relay will use the phase channel of a three-phase set of voltages if programmed as part of that source. The relay will use the auxiliary voltage channel only if that channel is programmed as part of the Source and a three-phase set is not.

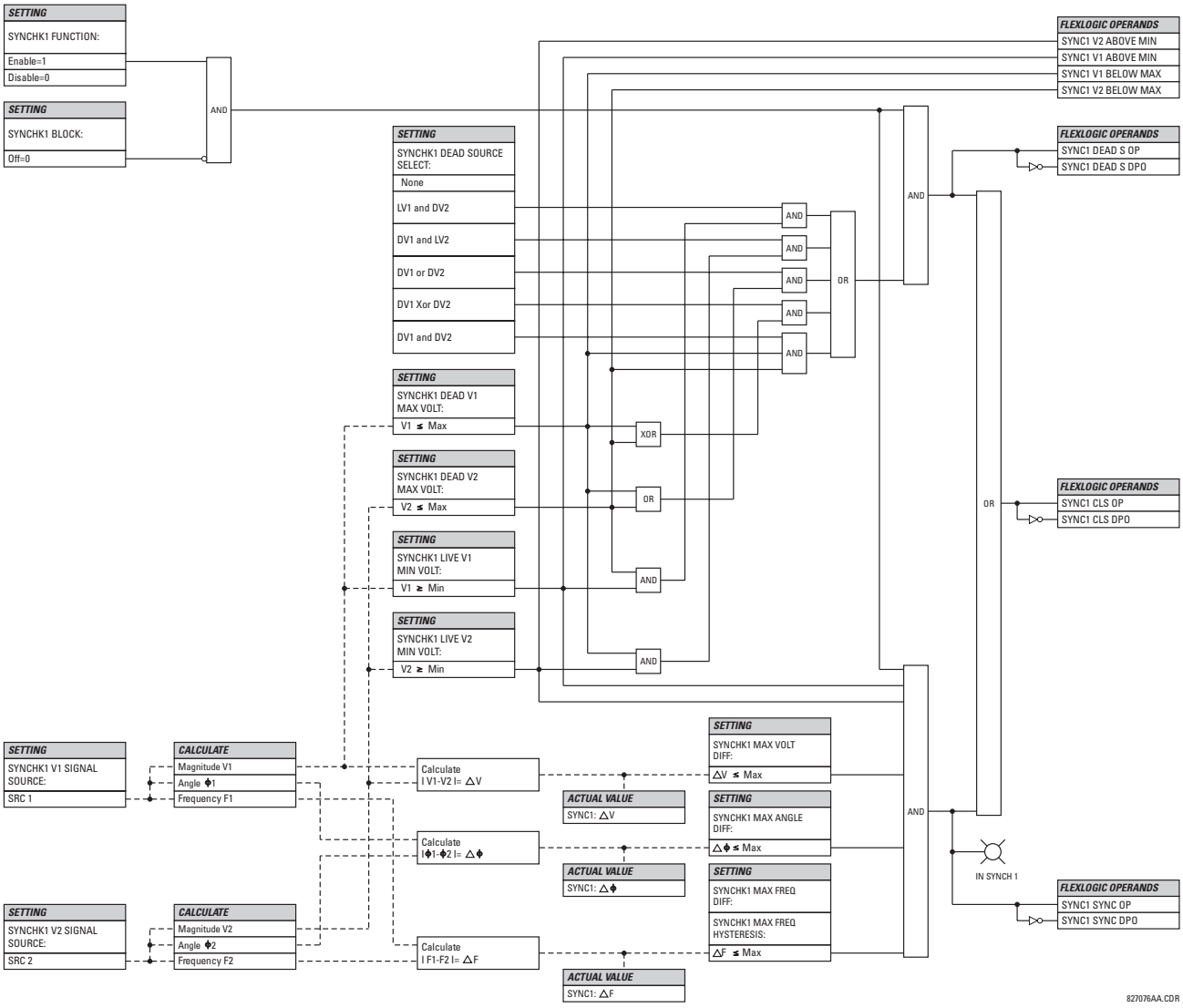


Figure 5–111: SYNCHROCHECK SCHEME LOGIC

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ DIGITAL ELEMENTS ⇨ DIGITAL ELEMENT 1(48)

■ DIGITAL ELEMENT 1 ■		DIGITAL ELEMENT 1 FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	DIG ELEM 1 NAME: Dig Element 1	*Range: 16 alphanumeric characters*
	MESSAGE	DIG ELEM 1 INPUT: Off	*Range: FlexLogic™ operand*
	MESSAGE	DIG ELEM 1 PICKUP DELAY: 0.000 s	*Range: 0.000 to 999999.999 s in steps of 0.001*
	MESSAGE	DIG ELEM 1 RESET DELAY: 0.000 s	*Range: 0.000 to 999999.999 s in steps of 0.001*
	MESSAGE	DIG ELEMENT 1 PICKUP LED: Enabled	*Range: Disabled, Enabled*
	MESSAGE	DIG ELEM 1 BLOCK: Off	*Range: FlexLogic™ operand*
	MESSAGE	DIGITAL ELEMENT 1 TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	DIGITAL ELEMENT 1 EVENTS: Disabled	*Range: Disabled, Enabled*

There are 48 identical digital elements available, numbered 1 to 48. A digital element can monitor any FlexLogic™ operand and present a target message and/or enable events recording depending on the output operand state. The digital element settings include a name which will be referenced in any target message, a blocking input from any selected FlexLogic™ operand, and a timer for pickup and reset delays for the output operand.

- **DIGITAL ELEMENT 1 INPUT:** Selects a FlexLogic™ operand to be monitored by the digital element.
- **DIGITAL ELEMENT 1 PICKUP DELAY:** Sets the time delay to pickup. If a pickup delay is not required, set to "0".
- **DIGITAL ELEMENT 1 RESET DELAY:** Sets the time delay to reset. If a reset delay is not required, set to “0”.
- **DIGITAL ELEMENT 1 PICKUP LED**: This setting enables or disabled the digital element pickup LED. When set to “Disabled”, the operation of the pickup LED is blocked.

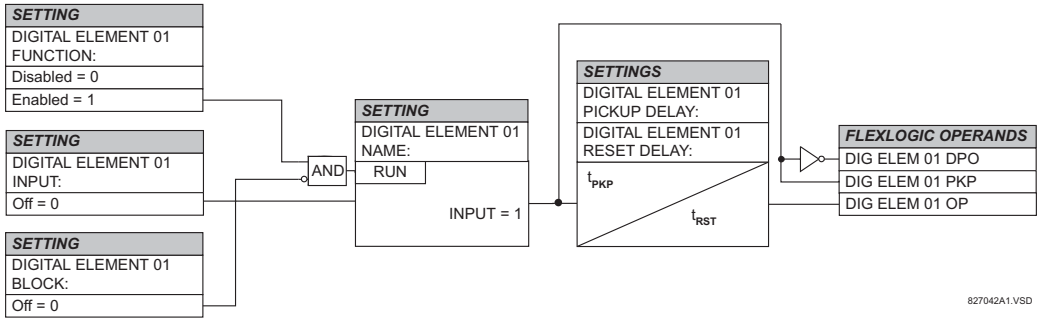


Figure 5–112: DIGITAL ELEMENT SCHEME LOGIC

CIRCUIT MONITORING APPLICATIONS:

Some versions of the digital input modules include an active voltage monitor circuit connected across form-A contacts. The voltage monitor circuit limits the trickle current through the output circuit (see technical specifications for form-A).

As long as the current through the voltage monitor is above a threshold (see technical specifications for form-A), the FlexLogic™ operand “Cont Op # VOn” will be set (# represents the output contact number). If the output circuit has a high resistance or the DC current is interrupted, the trickle current will drop below the threshold and the FlexLogic™ operand “Cont Op # VOff” will be set. Consequently, the state of these operands can be used as indicators of the integrity of the circuits in which Form-A contacts are inserted.

EXAMPLE 1: BREAKER TRIP CIRCUIT INTEGRITY MONITORING

In many applications it is desired to monitor the breaker trip circuit integrity so problems can be detected before a trip operation is required. The circuit is considered to be healthy when the voltage monitor connected across the trip output contact detects a low level of current, well below the operating current of the breaker trip coil. If the circuit presents a high resistance, the trickle current will fall below the monitor threshold and an alarm would be declared.

In most breaker control circuits, the trip coil is connected in series with a breaker auxiliary contact which is open when the breaker is open (see diagram below). To prevent unwanted alarms in this situation, the trip circuit monitoring logic must include the breaker position.

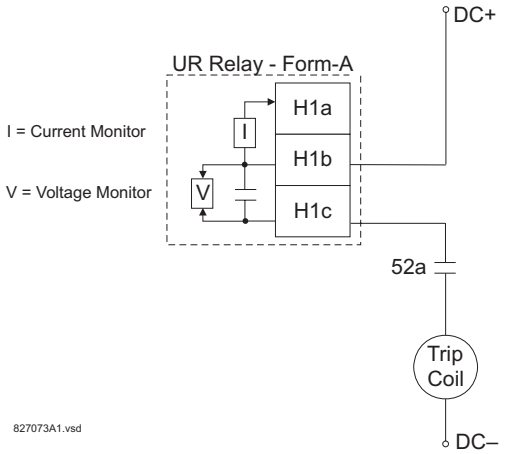
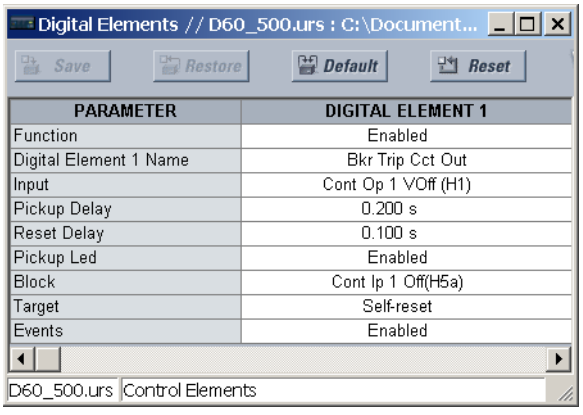


Figure 5–113: TRIP CIRCUIT EXAMPLE 1

Assume the output contact H1 is a trip contact. Using the contact output settings, this output will be given an ID name, e.g. “Cont Op 1". Assume a 52a breaker auxiliary contact is connected to contact input H7a to monitor breaker status. Using the contact input settings, this input will be given an ID name, e.g. “Cont Ip 1" and will be set “On” when the breaker is closed. The settings to use digital element 1 to monitor the breaker trip circuit are indicated below (EnerVista UR Setup example shown):

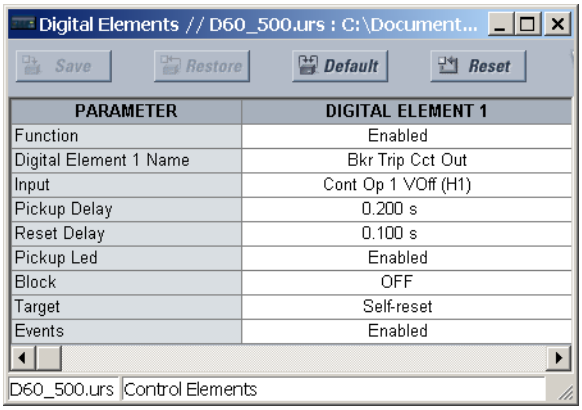


NOTE

The PICKUP DELAY setting should be greater than the operating time of the breaker to avoid nuisance alarms.

EXAMPLE 2: BREAKER TRIP CIRCUIT INTEGRITY MONITORING

If it is required to monitor the trip circuit continuously, independent of the breaker position (open or closed), a method to maintain the monitoring current flow through the trip circuit when the breaker is open must be provided (as shown in the figure below). This can be achieved by connecting a suitable resistor (see figure below) across the auxiliary contact in the trip circuit. In this case, it is not required to supervise the monitoring circuit with the breaker position – the **BLOCK** setting is selected to "Off". In this case, the settings are as follows (EnerVista UR Setup example shown).



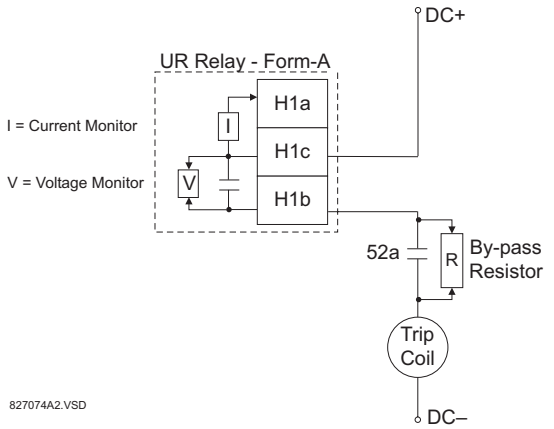
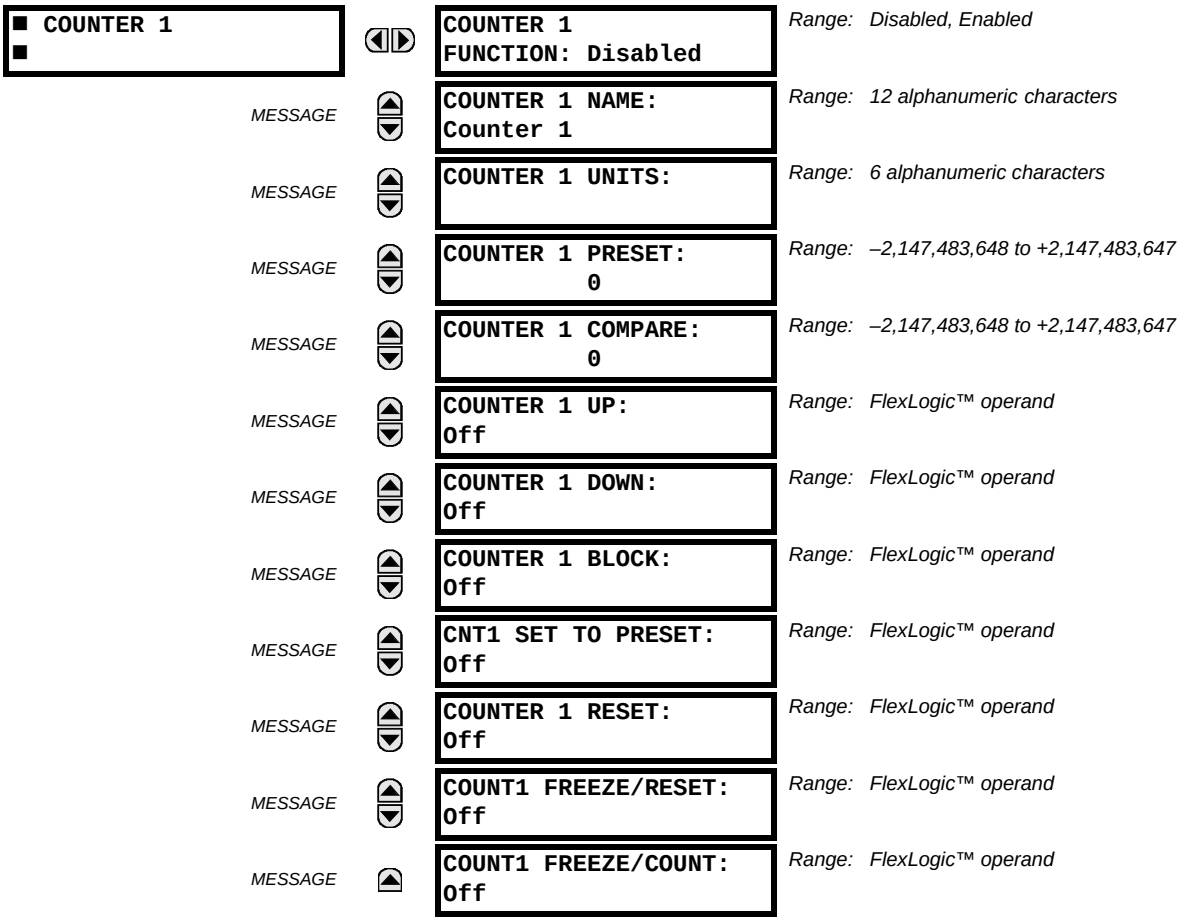


Table 5–24: VALUES OF RESISTOR 'R'

POWER SUPPLY (V DC)	RESISTANCE (OHMS)	POWER (WATTS)
24	1000	2
30	5000	2
48	10000	2
110	25000	5
125	25000	5
250	50000	5

Figure 5–114: TRIP CIRCUIT EXAMPLE 2

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ DIGITAL COUNTERS ⇨ COUNTER 1(8)



There are 8 identical digital counters, numbered from 1 to 8. A digital counter counts the number of state transitions from Logic 0 to Logic 1. The counter is used to count operations such as the pickups of an element, the changes of state of an external contact (e.g. breaker auxiliary switch), or pulses from a watt-hour meter.

- **COUNTER 1 UNITS:** Assigns a label to identify the unit of measure pertaining to the digital transitions to be counted. The units label will appear in the corresponding actual values status.
- **COUNTER 1 PRESET:** Sets the count to a required preset value before counting operations begin, as in the case where a substitute relay is to be installed in place of an in-service relay, or while the counter is running.
- **COUNTER 1 COMPARE:** Sets the value to which the accumulated count value is compared. Three FlexLogic™ output operands are provided to indicate if the present value is 'more than (HI)', 'equal to (EQL)', or 'less than (LO)' the set value.
- **COUNTER 1 UP:** Selects the FlexLogic™ operand for incrementing the counter. If an enabled UP input is received when the accumulated value is at the limit of +2,147,483,647 counts, the counter will rollover to –2,147,483,648.
- **COUNTER 1 DOWN:** Selects the FlexLogic™ operand for decrementing the counter. If an enabled DOWN input is received when the accumulated value is at the limit of –2,147,483,648 counts, the counter will rollover to +2,147,483,647.
- **COUNTER 1 BLOCK:** Selects the FlexLogic™ operand for blocking the counting operation. All counter operands are blocked.

- **CNT1 SET TO PRESET:** Selects the FlexLogic™ operand used to set the count to the preset value. The counter will be set to the preset value in the following situations:

  1. When the counter is enabled and the **CNT1 SET TO PRESET** operand has the value 1 (when the counter is enabled and **CNT1 SET TO PRESET** operand is 0, the counter will be set to 0).
  2. When the counter is running and the **CNT1 SET TO PRESET** operand changes the state from 0 to 1 (**CNT1 SET TO PRESET** changing from 1 to 0 while the counter is running has no effect on the count).
  3. When a reset or reset/freeze command is sent to the counter and the **CNT1 SET TO PRESET** operand has the value 1 (when a reset or reset/freeze command is sent to the counter and the **CNT1 SET TO PRESET** operand has the value 0, the counter will be set to 0).

- **COUNTER 1 RESET:** Selects the FlexLogic™ operand for setting the count to either "0" or the preset value depending on the state of the **CNT1 SET TO PRESET** operand.
- **COUNTER 1 FREEZE/RESET:** Selects the FlexLogic™ operand for capturing (freezing) the accumulated count value into a separate register with the date and time of the operation, and resetting the count to "0".
- **COUNTER 1 FREEZE/COUNT:** Selects the FlexLogic™ operand for capturing (freezing) the accumulated count value into a separate register with the date and time of the operation, and continuing counting. The present accumulated value and captured frozen value with the associated date/time stamp are available as actual values. If control power is interrupted, the accumulated and frozen values are saved into non-volatile memory during the power down operation.

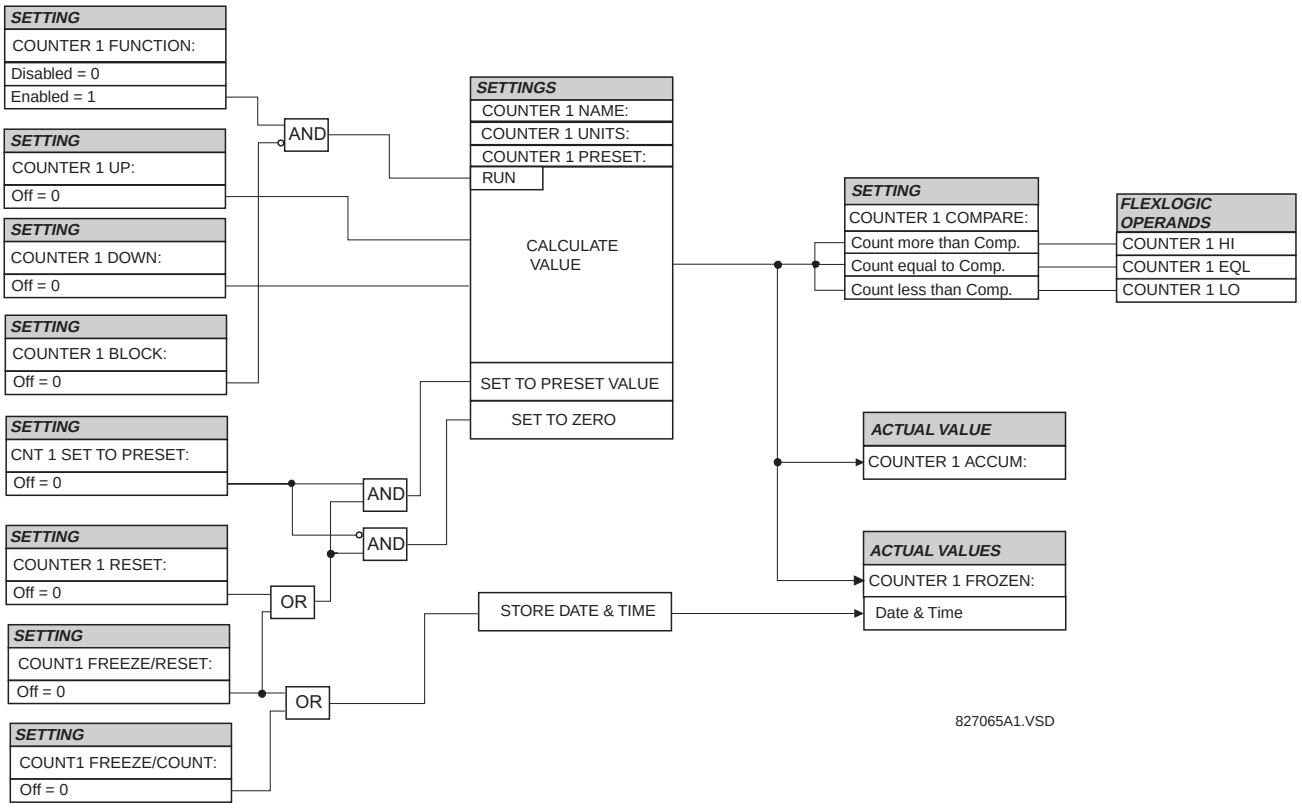


Figure 5–115: DIGITAL COUNTER SCHEME LOGIC

a) MAIN MENU

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ MONITORING ELEMENTS

■ MONITORING ■ ELEMENTS		■ BREAKER 1 ■ ARCING CURRENT	See below.
	MESSAGE	■ BREAKER 2 ■ ARCING CURRENT	See below.
	MESSAGE	■ BREAKER ■ FLASHOVER 1	See page 5–211.
	MESSAGE	■ BREAKER ■ FLASHOVER 2	See page 5–211.
	MESSAGE	■ CT FAILURE ■ DETECTOR	See page 5–215.
	MESSAGE	■ VT FUSE FAILURE 1 ■	See page 5–217.
	MESSAGE	■ VT FUSE FAILURE 2 ■	See page 5–217.
	MESSAGE	■ OPEN POLE ■	See page 5–218.

b) BREAKER ARCING CURRENT

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ MONITORING ELEMENTS ⇨ BREAKER 1(2) ARCING CURRENT

■ BREAKER 1 ■ ARCING CURRENT		BKR 1 ARC AMP FUNCTION: Disabled	*Range: Disabled, Enabled*
	MESSAGE	BKR 1 ARC AMP SOURCE: SRC 1	*Range: SRC 1, SRC 2, SRC 3, SRC 4*
	MESSAGE	BKR 1 ARC AMP INT-A: Off	*Range: FlexLogic™ operand*
	MESSAGE	BKR 1 ARC AMP INT-B: Off	*Range: FlexLogic™ operand*
	MESSAGE	BKR 1 ARC AMP INT-C: Off	*Range: FlexLogic™ operand*
	MESSAGE	BKR 1 ARC AMP DELAY: 0.000 s	*Range: 0.000 to 65.535 s in steps of 0.001*
	MESSAGE	BKR 1 ARC AMP LIMIT: 1000 kA2-cyc	*Range: 0 to 50000 kA^2-cycle in steps of 1*
	MESSAGE	BKR 1 ARC AMP BLOCK: Off	*Range: FlexLogic™ operand*
	MESSAGE	BKR 1 ARC AMP TARGET: Self-reset	*Range: Self-reset, Latched, Disabled*
	MESSAGE	BKR 1 ARC AMP EVENTS: Disabled	*Range: Disabled, Enabled*

There is one Breaker Arcing Current element available per CT bank, with a minimum of 2 elements. This element calculates an estimate of the per-phase wear on the breaker contacts by measuring and integrating the current squared passing through the breaker contacts as an arc. These per-phase values are added to accumulated totals for each phase and compared to a programmed threshold value. When the threshold is exceeded in any phase, the relay can set an output operand to "1". The accumulated value for each phase can be displayed as an actual value.

The operation of the scheme is shown in the following logic diagram. The same output operand that is selected to operate the output relay used to trip the breaker, indicating a tripping sequence has begun, is used to initiate this feature. A time delay is introduced between initiation and the starting of integration to prevent integration of current flow through the breaker before the contacts have parted. This interval includes the operating time of the output relay, any other auxiliary relays and the breaker mechanism. For maximum measurement accuracy, the interval between change-of-state of the operand (from 0 to 1) and contact separation should be measured for the specific installation. Integration of the measured current continues for 100 ms, which is expected to include the total arcing period.

The feature is programmed to perform fault duration calculations. Fault duration is defined as a time between operation of the disturbance detector occurring before initiation of this feature, and reset of an internal low-set overcurrent function. Correction is implemented to account for a non-zero reset time of the overcurrent function.

Breaker arcing currents and fault duration values are available under the **ACTUAL VALUES** ⇨⇩ **RECORDS** ⇨⇩ **MAINTENANCE** ⇨ **BREAKER 1(2)** menus.

- **BKR 1(2) ARC AMP INT-A(C):** Select the same output operands that are configured to operate the output relays used to trip the breaker. In three-pole tripping applications, the same operand should be configured to initiate arcing current calculations for poles A, B and C of the breaker. In single-pole tripping applications, per-pole tripping operands should be configured to initiate the calculations for the poles that are actually tripped.
- **BKR 1(2) ARC AMP DELAY:** This setting is used to program the delay interval between the time the tripping sequence is initiated and the time the breaker contacts are expected to part, starting the integration of the measured current.
- **BKR 1(2) ARC AMP LIMIT:** Selects the threshold value above which the output operand is set.

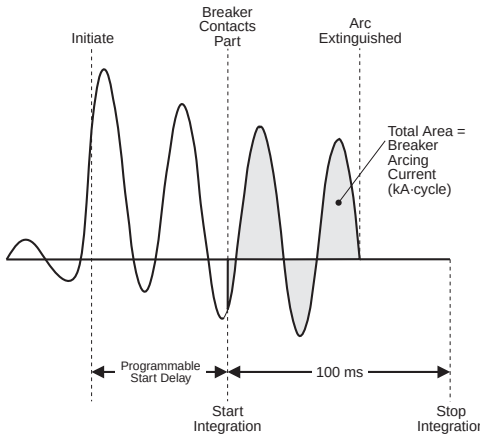


Figure 5–116: ARCING CURRENT MEASUREMENT

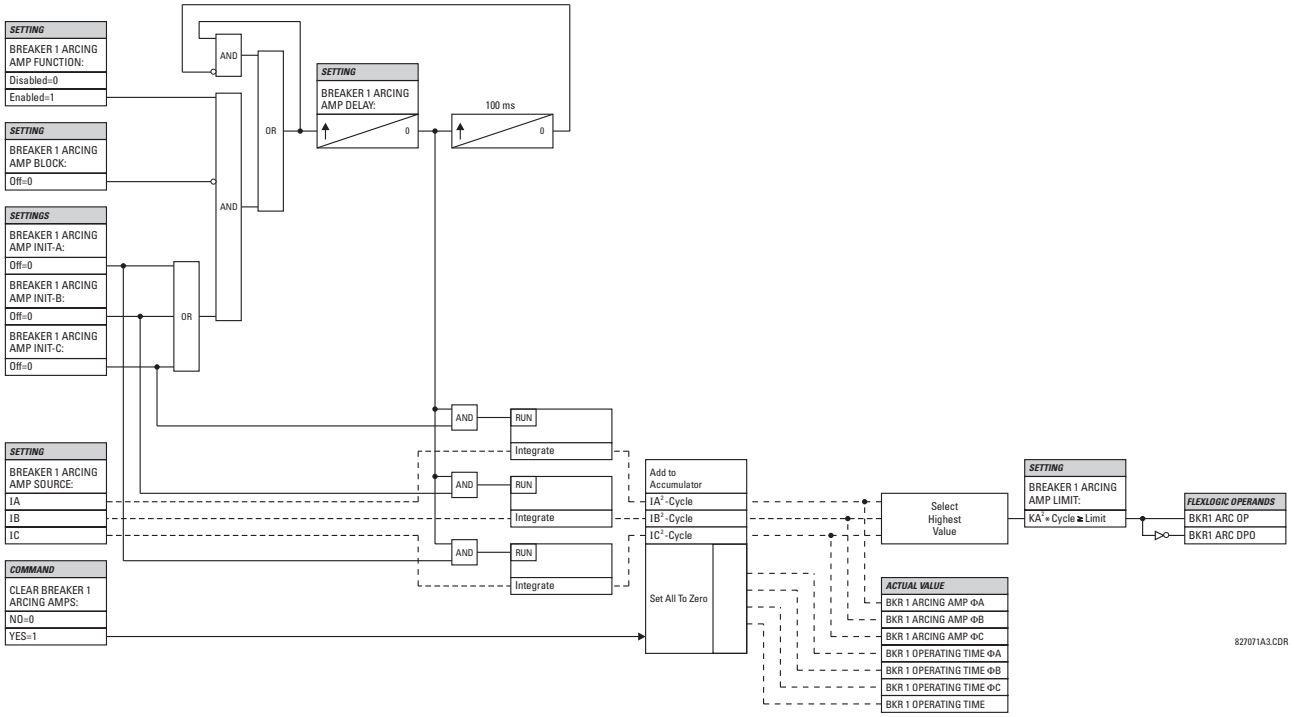


Figure 5–117: BREAKER ARCING CURRENT SCHEME LOGIC

c) BREAKER FLASHOVER

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ MONITORING ELEMENTS ⇨ BREAKER FLASHOVER 1(2)

■ BREAKER ■ FLASHOVER 1		BKR 1 FLSHOVR FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	BKR 1 FLSHOVR SIDE 1 SRC: SRC 1	Range: SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	BKR 1 FLSHOVR SIDE 2 SRC: None	Range: None, SRC 1, SRC 2, SRC 3, SRC 4
	MESSAGE	BKR 1 STATUS CLSD A: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 STATUS CLSD B: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 STATUS CLSD C: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 FLSHOVR V PKP: 0.850 pu	Range: 0.000 to 1.500 pu in steps of 0.001
	MESSAGE	BKR 1 FLSHOVR DIFF V PKP: 1000 V	Range: 0 to 100000 V in steps of 1
	MESSAGE	BKR 1 FLSHOVR AMP PKP: 0.600 pu	Range: 0.000 to 1.500 pu in steps of 0.001
	MESSAGE	BKR 1 FLSHOVR PKP DELAY: 0.100 s	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	BKR 1 FLSHOVR SPV A: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 FLSHOVR SPV B: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 FLSHOVR SPV C: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 FLSHOVR BLOCK: Off	Range: FlexLogic™ operand
	MESSAGE	BKR 1 FLSHOVR TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	BKR 1 FLSHOVR EVENTS: Disabled	Range: Disabled, Enabled

The detection of the breaker flashover is based on the following condition:

1. Breaker open,
2. Voltage drop measured from either side of the breaker during the flashover period,
3. Voltage difference drop, and
4. Measured flashover current through the breaker.

Furthermore, the scheme is applicable for cases where either one or two sets of three-phase voltages are available across the breaker.

THREE VT BREAKER FLASHOVER APPLICATION

When only one set of VTs is available across the breaker, the **BRK FLSHOVR SIDE 2 SRC** setting should be "None". To detect an open breaker condition in this application, the scheme checks if the per-phase voltages were recovered (picked up), the status of the breaker is open (contact input indicating the breaker status is off), and no flashover current is flowing. A contact showing the breaker status must be provided to the relay. The voltage difference will not be considered as a condition for open breaker in this part of the logic.

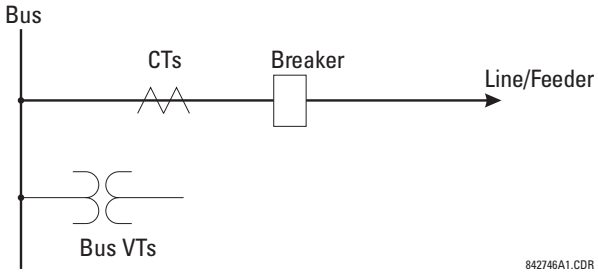
NOTE

Voltages must be present prior to flashover conditions. If the three VTs are placed after the breaker on the line (or feeder), and the downstream breaker is open, the measured voltage would be zero and the flashover element will not be initiated.

The flashover detection will reset if the current drops back to zero, the breaker closes, or the selected FlexLogic™ operand for supervision changes to high. Using supervision through the **BRK FLSHOVR SPV** setting is recommended by selecting a trip operand that will not allow the flashover element to pickup prior to the trip.

The flashover detection can be used for external alarm, re-tripping the breaker, or energizing the lockout relay.

Consider the following configuration:



The source 1 (SRC1) phase currents are feeder CTs and phase voltages are bus VTs, and Contact Input 1 is set as Breaker 52a contact. The conditions prior to flashover detection are:

1. 52a status = 0
2. VAg, VBg, or VCg is greater than the pickup setting
3. IA, IB, IC = 0; no current flows through the breaker
4. ΔVA is greater than pickup (not applicable in this scheme)

The conditions at flashover detection are:

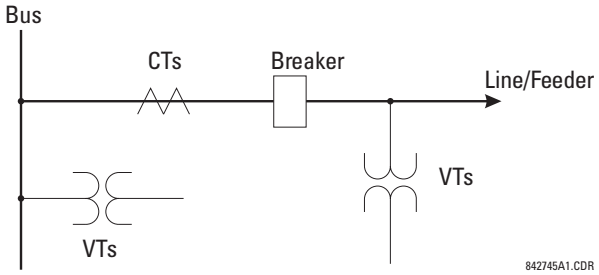
1. 52a status = 0
2. VAg, VBg, or VCg is lower than the pickup setting
3. IA, IB, or IC is greater than the pickup current flowing through the breaker
4. ΔVA is greater than pickup (not applicable in this scheme)

SIX VT BREAKER FLASHOVER APPLICATION

The per-phase voltage difference approaches zero when the breaker is closed. The is well below any typical minimum pickup voltage. Select the level of the **BRK 1(2) FLSHOVR DIFF V PKP** setting to be less than the voltage difference measured across the breaker when the close or open breaker resistors are left in service. Prior to flashover, the voltage difference is larger than **BRK 1(2) FLSHOVR DIFF V PKP**. This applies to either the difference between two live voltages per phase or when the voltage from one side of the breaker has dropped to zero (line de-energized), at least one per-phase voltage is larger than the **BRK 1(2) FLSHOVR V PKP** setting, and no current flows through the breaker poles. During breaker flashover, the per-phase voltages from both sides of the breaker drops below the pickup value defined by the **BRK 1(2) FLSHOVR V PKP** setting, the voltage difference drops below the pickup setting, and flashover current is detected. These flashover conditions initiate FlexLogic™ pickup operands and start the **BRK 1(2) FLSHOVR PKP DELAY** timer.

This application do not require detection of breaker status via a 52a contact, as it uses a voltage difference larger than the **BRK 1(2) FLSHOVR DIFF V PKP** setting. However, monitoring the breaker contact will ensure scheme stability.

Consider the following configuration:



The source 1 (SRC1) phase currents are CTs and phase voltages are bus VTs. The source 2 (SRC2) phase voltages are line VTs. Contact input 1 is set as the breaker 52a contact (optional).

The conditions prior to flashover detection are:

1. ΔVA is greater than pickup
2. VAg, VBg, or VCg is greater than the pickup setting
3. IA, IB, IC = 0; no current flows through the breaker
4. 52a status = 0 (optional)

The conditions at flashover detection are:

1. ΔVA is less than pickup
2. VAg, VBg, or VCg is lower than the pickup setting
3. IA, IB, or IC is greater than the pickup current flowing through the breaker
4. 52a status = 0 (optional)

NOTE

The element is operational only when phase-to-ground voltages are connected to relay terminals. The flashover element will not operate if delta voltages are applied.

The breaker flashover settings are described below.

- **BRK FLSHOVR SIDE 1 SRC**: This setting specifies a signal source used to provide three-phase voltages and three-phase currents from one side of the current breaker. The source selected as a setting and must be configured with breaker phase voltages and currents, even if only three (3) VTs are available across the breaker.
- **BRK FLSHOVR SIDE 2 SRC**: This setting specifies a signal source used to provide another set of three phase voltages whenever six (6) VTs are available across the breaker.
- **BRK STATUS CLSD A(C)**: These settings specify FlexLogic™ operands to indicate the open status of the breaker. A separate FlexLogic™ operand can be selected to detect individual breaker pole status and provide flashover detection. The recommended setting is 52a breaker contact or another operand defining the breaker poles open status.
- **BRK FLSHOVR V PKP**: This setting specifies a pickup level for the phase voltages from both sides of the breaker. If six VTs are available, opening the breaker leads to two possible combinations – live voltages from only one side of the breaker, or live voltages from both sides of the breaker. Either case will set the scheme ready for flashover detection upon detection of voltage above the selected value. Set **BRK FLSHOVR V PKP** to 85 to 90% of the nominal voltage.
- **BRK FLSHOVR DIFF V PKP**: This setting specifies a pickup level for the phase voltage difference when two VTs per phase are available across the breaker. The pickup voltage difference should be below the monitored voltage difference when close or open breaker resistors are left in service. The setting is selected as primary volts difference between the sources.
- **BRK FLSHOVR AMP PKP**: This setting specifies the normal load current which can flow through the breaker. Depending on the flashover protection application, the flashover current can vary from levels of the charging current when the line is de-energized (all line breakers open), to well above the maximum line (feeder) load (line/feeder connected to load).
- **BRK FLSHOVR SPV A(C)**: This setting specifies a FlexLogic™ operand (per breaker pole) that supervises the operation of the element per phase. Supervision can be provided by operation of other protection elements, breaker failure, and close and trip commands. A 6-cycle time delay applies after the selected FlexLogic™ operand resets.

- **BRK FLSHOVR PKP DELAY**: This setting specifies the time delay to operate after a pickup condition is detected.

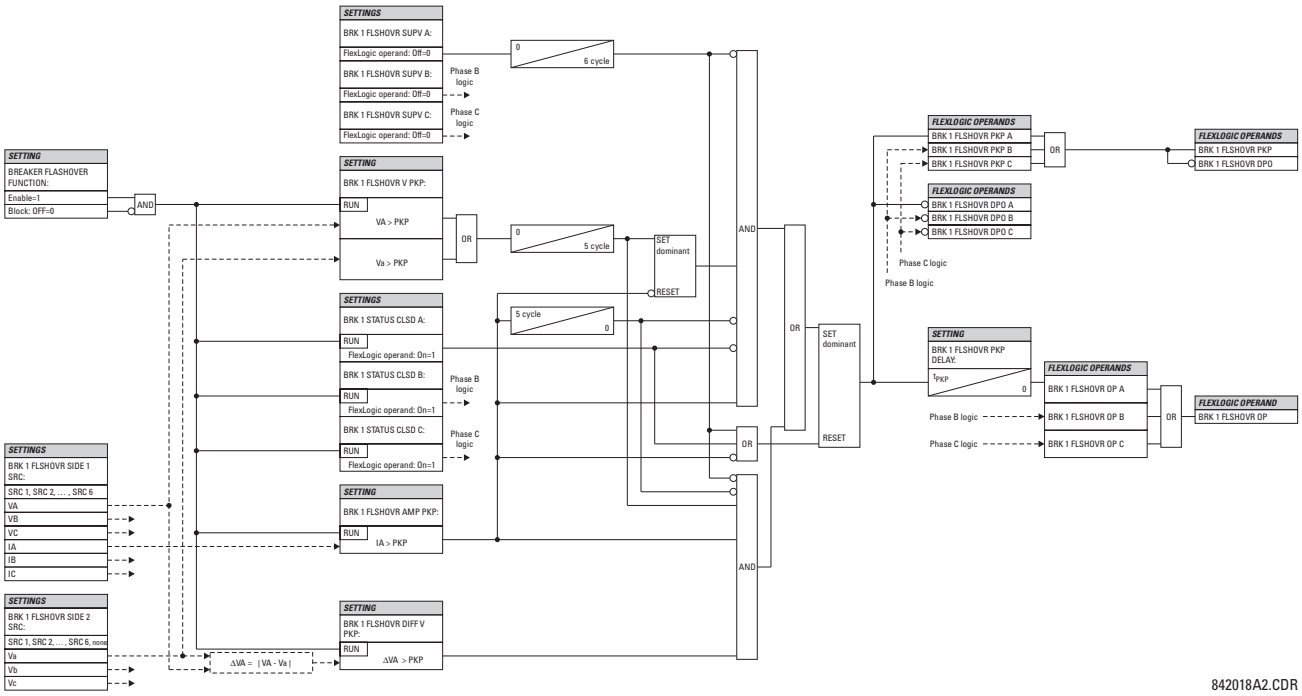
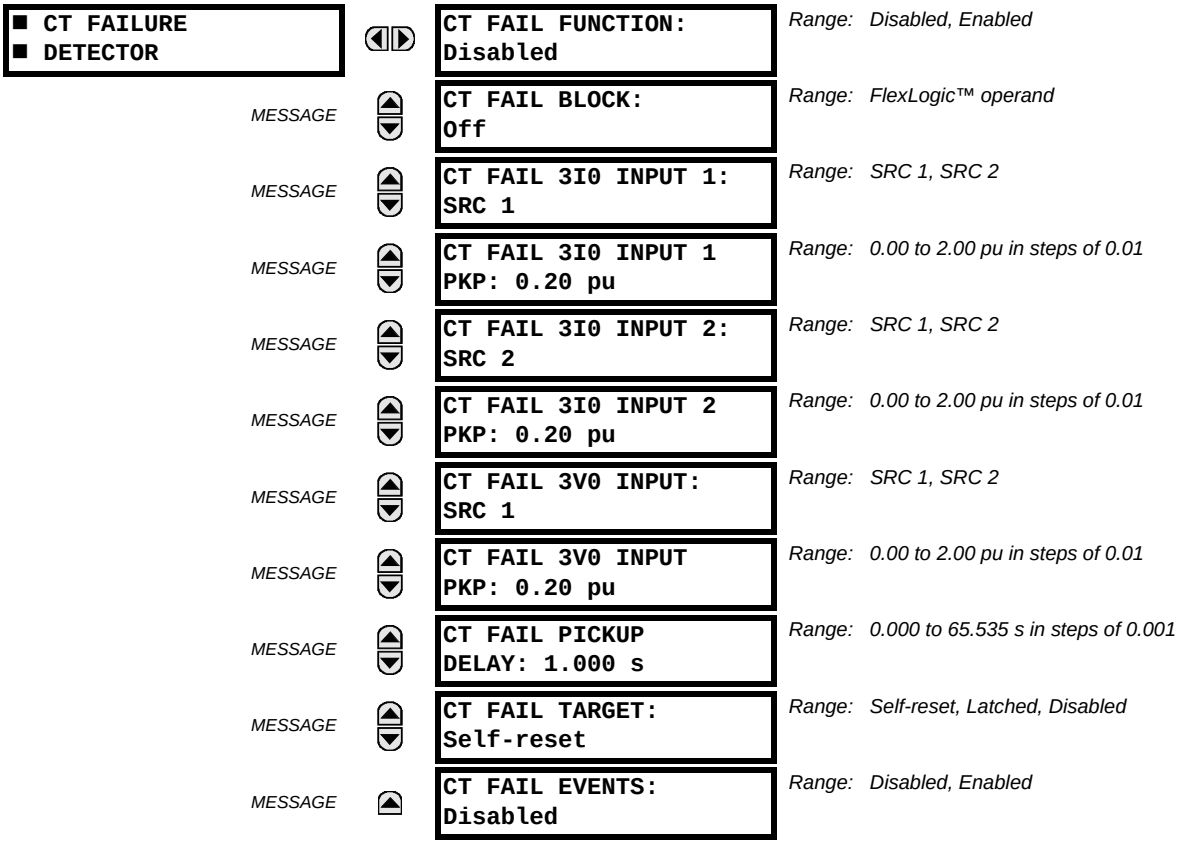


Figure 5–118: BREAKER FLASHOVER SCHEME LOGIC

d) CT FAILURE

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ MONITORING ELEMENTS ⇨⇩ CT FAILURE DETECTOR



The CT failure function is designed to detect problems with system current transformers used to supply current to the relay. This logic detects the presence of a zero-sequence current at the supervised source of current without a simultaneous zero-sequence current at another source, zero-sequence voltage, or some protection element condition.

The CT failure logic (see below) is based on the presence of the zero-sequence current in the supervised CT source and the absence of one of three or all of the three following conditions.

1. Zero-sequence current at different source current (may be different set of CTs or different CT core of the same CT).
2. Zero-sequence voltage at the assigned source.
3. Appropriate protection element or remote signal.

The CT failure settings are described below.

- **CT FAIL FUNCTION:** This setting enables or disables operation of the CT failure element.
- **CT FAIL BLOCK:** This setting selects a FlexLogic™ operand to block operation of the element during some condition (for example, an open pole in process of the single pole tripping-reclosing) when CT fail should be blocked. Local signals or remote signals representing operation of some remote current protection elements via communication channels can also be chosen.
- **CT FAIL 3I0 INPUT 1:** This setting selects the current source for input 1. The most critical protection element should also be assigned to the same source.
- **CT FAIL 3I0 INPUT 1 PICKUP:** This setting selects the 3I_0 pickup value for input 1 (the main supervised CT source).
- **CT FAIL 3I0 INPUT 2**: This setting selects the current source for input 2. Input 2 should use a different set of CTs or a different CT core of the same CT. If 3I_0 does not exist at source 2, then a CT failure is declared.
- **CT FAIL 3I0 INPUT 2 PICKUP**: This setting selects the 3I_0 pickup value for input 2 (different CT input) of the relay.
- **CT FAIL 3V0 INPUT:** This setting selects the voltage source.

- **CT FAIL 3V0 INPUT PICKUP:** This setting specifies the pickup value for the 3V_0 source.
- **CT FAIL PICKUP DELAY:** This setting specifies the pickup delay of the CT failure element.

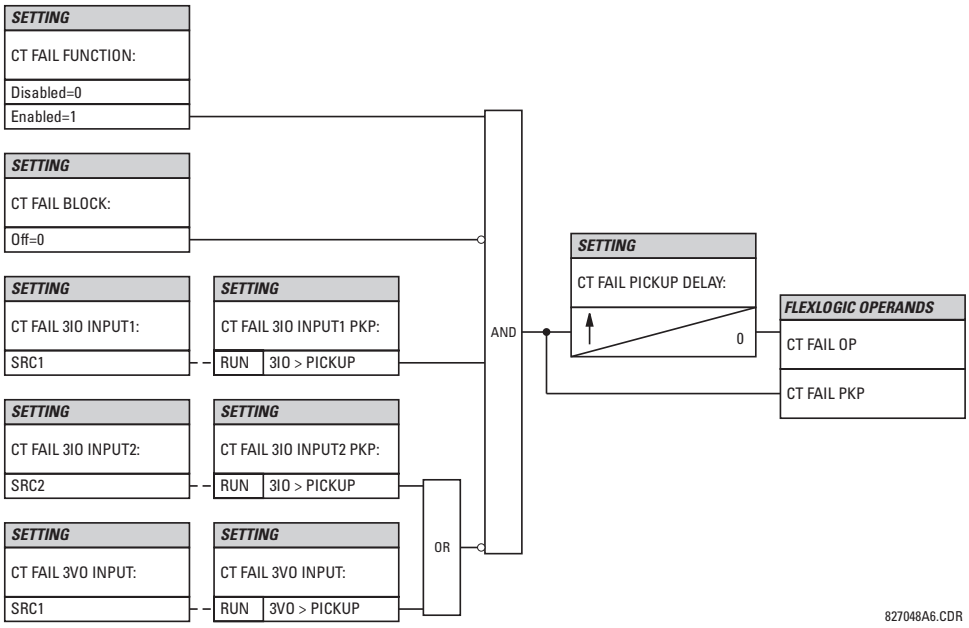


Figure 5–119: CT FAILURE DETECTOR SCHEME LOGIC

e) VT FUSE FAILURE

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ MONITORING ELEMENTS ⇨⇩ VT FUSE FAILURE 1(2)

```
■ VT FUSE FAILURE 1
■
```

⇔

```
VT FUSE FAILURE 1
FUNCTION: Disabled
```

Range: Disabled, Enabled

Every signal source includes a fuse failure scheme.

The VT fuse failure detector can be used to raise an alarm and/or block elements that may operate incorrectly for a full or partial loss of AC potential caused by one or more blown fuses. Some elements that might be blocked (via the BLOCK input) are distance, voltage restrained overcurrent, and directional current.

There are two classes of fuse failure that may occur:

- Class A: loss of one or two phases.
- Class B: loss of all three phases.

Different means of detection are required for each class. An indication of Class A failures is a significant level of negative sequence voltage, whereas an indication of class B failures is when positive sequence current is present and there is an insignificant amount of positive sequence voltage. These noted indications of fuse failure could also be present when faults are present on the system, so a means of detecting faults and inhibiting fuse failure declarations during these events is provided. Once the fuse failure condition is declared, it will be sealed-in until the cause that generated it disappears.

An additional condition is introduced to inhibit a fuse failure declaration when the monitored circuit is de-energized; positive sequence voltage and current are both below threshold levels.

The function setting enables and disables the fuse failure feature for each source.

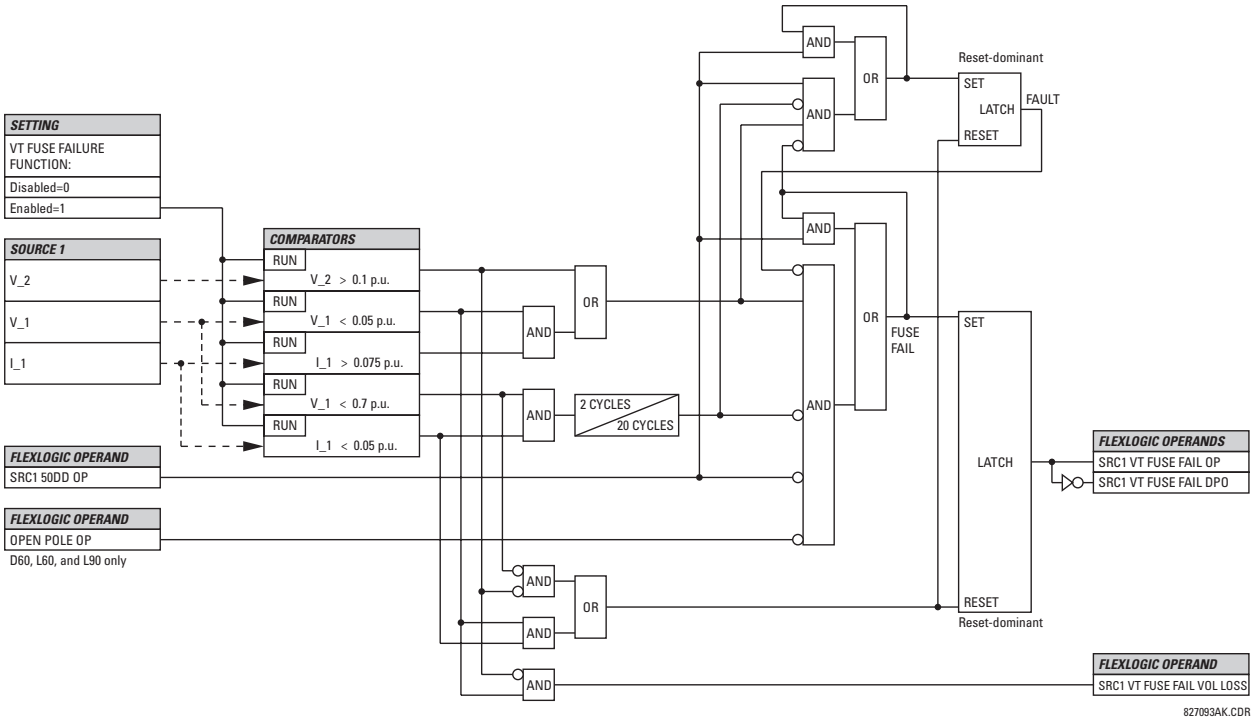
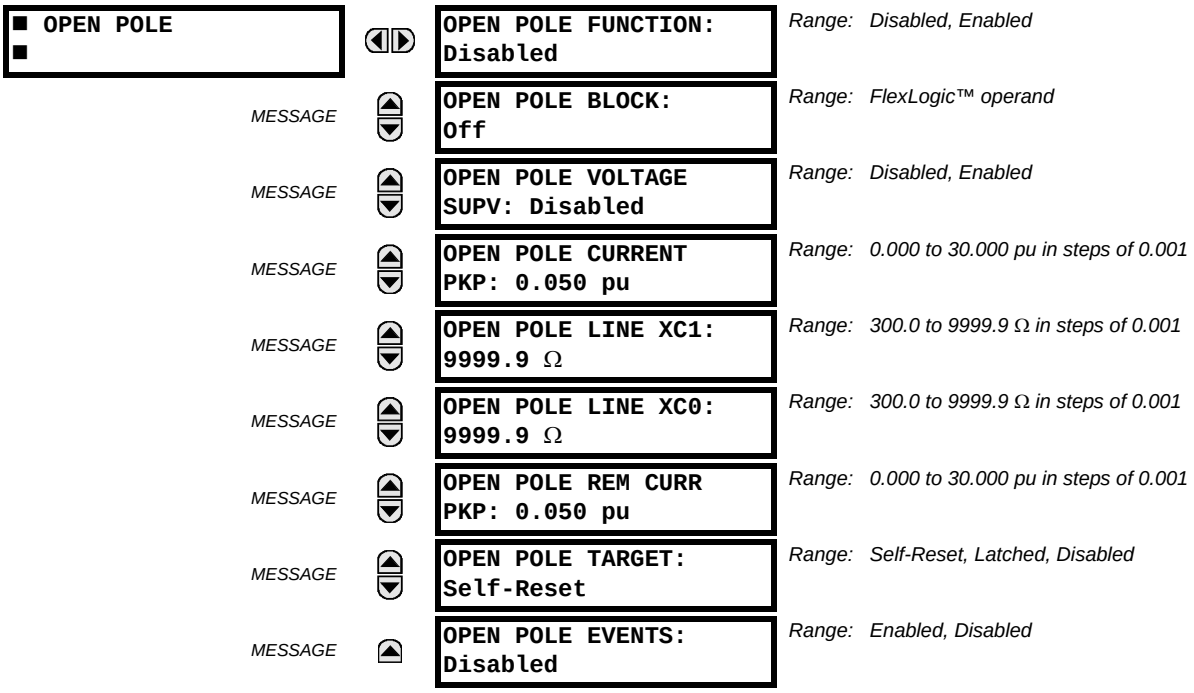


Figure 5–120: VT FUSE FAIL SCHEME LOGIC

f) OPEN POLE DETECTOR

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ MONITORING ELEMENTS ⇨⇩ OPEN POLE



The open pole detector is intended to identify an open pole of the line circuit breaker. The scheme monitors the breakers auxiliary contacts, current in the circuit and optionally voltage on the line. The scheme generates output operands used to block the phase selector and some specific protection elements, thus preventing maloperation during the dead time of a single pole autoreclose cycle or any other open pole conditions.

In two breaker and breaker and a half applications, an open pole condition is declared when:

- both breakers have an open pole on the same phase or
- the current on the line drops below a threshold or
- the current and voltage on the line drop below a threshold.

The Open Pole feature uses signals defined by the GROUPED ELEMENTS ⇨ SETTING GROUP 1(6) ⇨⇩ DISTANCE ⇨ DISTANCE SOURCE setting. Voltage supervision can be used only with wye VTs on the line side of the breaker(s).

The **OPEN POLE CURRENT PICKUP** setting establishes the current threshold below which an open pole is declared.

The **OPEN POLE LINE XC1** setting specifies positive-sequence reactance of the entire line. If shunt reactors are applied, this value should be a net capacitive reactance of the line and the reactors installed between the line breakers. The value is entered in secondary ohms. This setting is relevant if open pole condition at the remote end of the line is to be sensed and utilized by the relay.

The **OPEN POLE LINE XC0** setting specifies zero-sequence reactance of the entire line. If shunt reactors are applied, this value should be a net capacitive reactance of the line and the reactors installed between the line breakers. The value shall be entered in secondary ohms. This setting is relevant if open pole condition at the remote end of the line is to be sensed and utilized by the relay (OPEN POLE REM OP FlexLogic™ operand).

The **OPEN POLE REM CURR PKP** setting specifies pickup level for the remote-end current estimated by the relay as the local current compensated by the calculated charging current. The latter is calculated based on the local voltages and the capacitive reactances of the line. This setting is relevant if open pole condition at the remote end of the line is to be sensed and utilized by the relay (OPEN POLE REM OP FlexLogic™ operand).

For convenience, the position of the breaker poles defined in the Breaker Control feature and available as FlexLogic™ operand BREAKER 1/2 ΦA CLSD through BREAKER 1/2 ΦC CLSD and BREAKER 1/2 OOS are used by the Open Pole feature. For correct operation of the Open Pole Detector, the Breaker Control, Trip Output, and Single Pole Autoreclose features

must be enabled and configured properly. When used in configuration with only one breaker, the **BREAKER 2 FUNCTION** should be “Enabled” and the **BREAKER 2 OUT OF SV** setting should be “On” (see the Breaker Control section earlier in this Chapter for additional details).

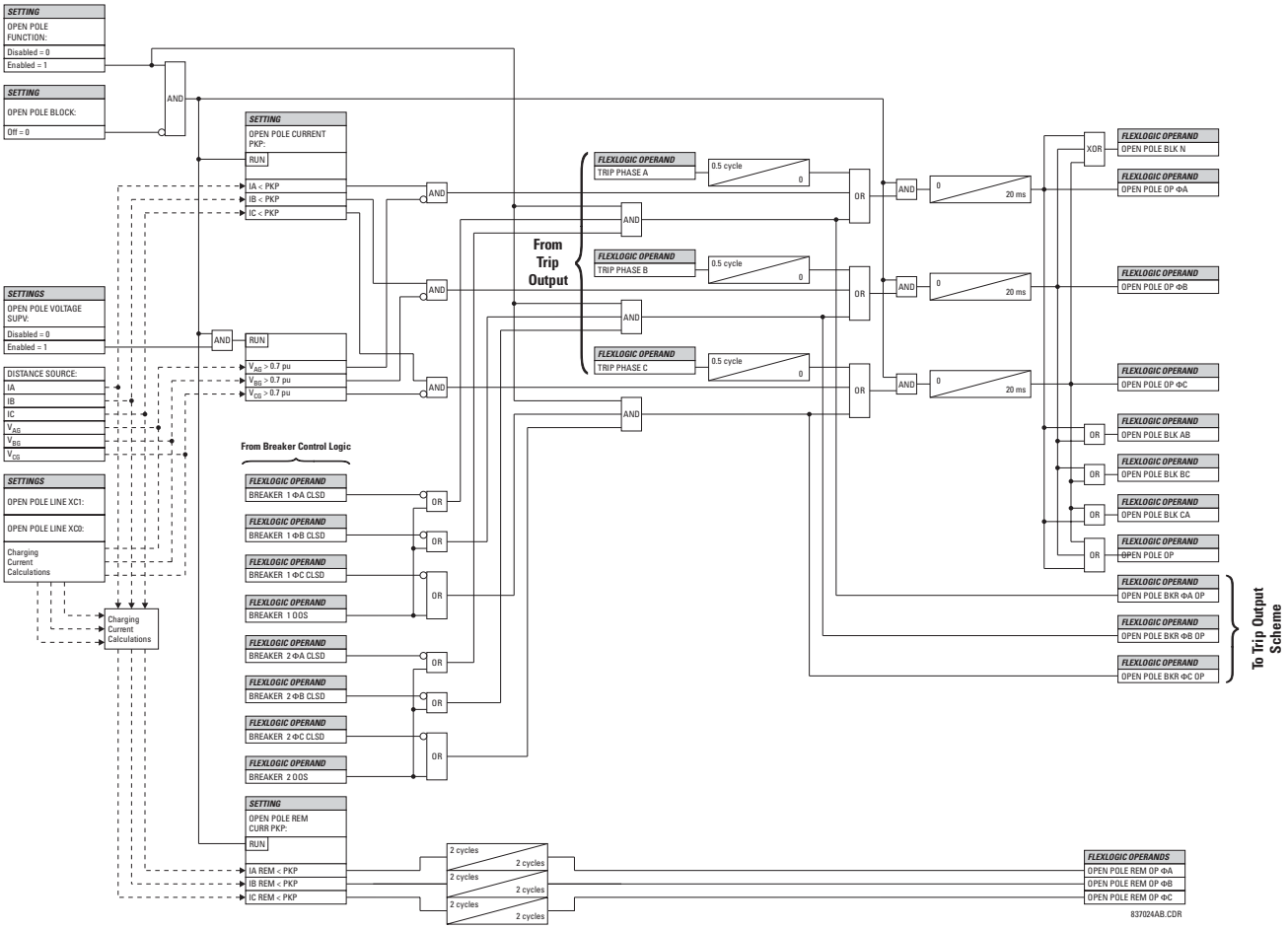
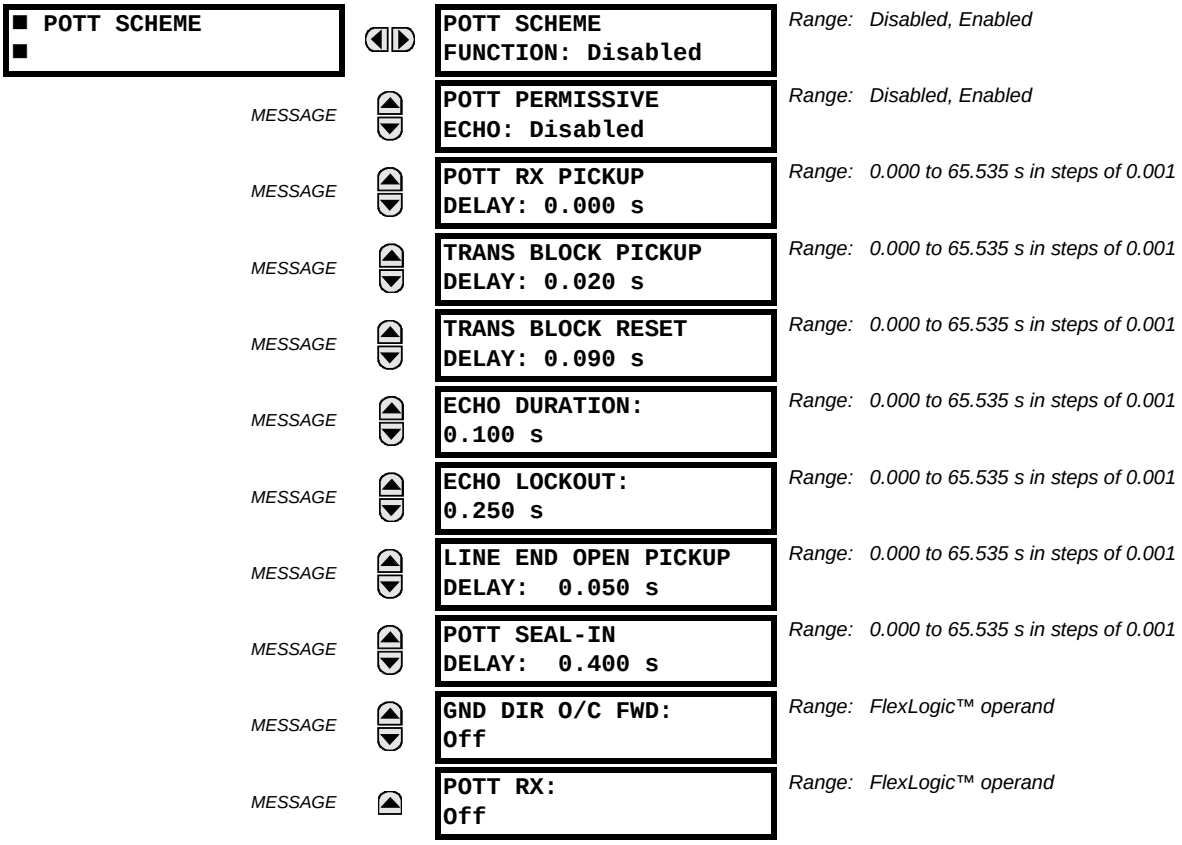


Figure 5–121: OPEN POLE DETECTOR LOGIC

a) PERMISSIVE OVERREACHING TRANSFER TRIP (POTT)

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ PILOT SCHEMES ⇨⇩ POTT SCHEME



This scheme is intended for two-terminal line applications only. It uses an over-reaching zone 2 distance element to essentially compare the direction to a fault at both the ends of the line. Ground directional overcurrent functions available in the relay can be used in conjunction with the zone 2 distance element to key the scheme and initiate its operation. This provides increased coverage for high resistance faults.

For proper scheme operation, the zone 2 phase and ground distance elements must be enabled, configured, and set per the rules of distance relaying. The line pickup element should be enabled, configured and set properly to detect line-end-open/weak-infeed conditions. If used by this scheme, the selected ground directional overcurrent function(s) must be enabled, configured, and set accordingly.

- **POTT PERMISSIVE ECHO:** If set to "Enabled" this setting will result in sending a permissive echo signal to the remote end. The permissive signal is echoed back upon receiving a reliable POTT RX signal from the remote end while the line-end-open condition is identified by the line pickup logic. The permissive echo is programmed as a one-shot logic. The echo is sent only once and then the echo logic locks out for a settable period of time (**ECHO LOCKOUT** setting). The duration of the echo pulse does not depend on the duration or shape of the received POTT RX signal but is settable as **ECHO DURATION**.
- **POTT RX PICKUP DELAY:** This setting enables the relay to cope with spurious receive signals. The delay should be set longer than the longest spurious TX signal that can occur simultaneously with the zone 2 pickup. The selected delay will increase the response time of the scheme.
- **TRANS BLOCK PICKUP DELAY:** This setting defines a transient blocking mechanism embedded in the POTT scheme for coping with the exposure of a ground directional overcurrent function (if used) to current reversal conditions. The transient blocking mechanism applies to the ground overcurrent path only as the reach settings for the zone 2 distance functions is not expected to be long for two-terminal applications, and the security of the distance functions is not endangered by the current reversal conditions. Upon receiving the POTT RX signal, the transient blocking mechanism allows the RX signal to be passed and aligned with the **GND DIR O/C FWD** indication only for a period of time

defined as **TRANS BLOCK PICKUP DELAY**. After that the ground directional overcurrent path will be virtually disabled for a period of time specified as **TRANS BLOCK RESET DELAY**.

The **TRANS BLOCK PICKUP DELAY** should be long enough to give the selected ground directional overcurrent function time to operate, but not longer than the fastest possible operation time of the protection system that can create current reversal conditions within the reach of the selected ground directional overcurrent function. This setting should take into account the **POTT RX PICKUP DELAY**. The POTT RX signal is shaped for aligning with the ground directional indication as follows: the original RX signal is delayed by the **POTT RX PICKUP DELAY**, then terminated at **TRANS BLOCK PICKUP DELAY** after the pickup of the original POTT TX signal, and eventually, locked-out for **TRANS BLOCK RESET DELAY**.

- **TRANS BLOCK RESET DELAY:** This setting defines a transient blocking mechanism embedded in the POTT scheme for coping with the exposure of a ground directional overcurrent function (if used) to current reversal conditions (see also the **TRANS BLOCK PICKUP DELAY**). This delay should be selected long enough to cope with transient conditions including not only current reversals but also spurious negative and zero-sequence currents occurring during breaker operations. The breaker failure time of the surrounding protection systems within the reach of the ground directional function used by the POTT scheme may be considered to make sure that the ground directional function is not jeopardized during delayed breaker operations.
- **ECHO DURATION:** This setting defines the guaranteed and exact duration of the echo pulse. The duration does not depend on the duration and shape of the received POTT RX signal. This setting enables the relay to avoid a permanent lock-up of the transmit/receive loop.
- **ECHO LOCKOUT:** This setting defines the lockout period for the echo logic after sending the echo pulse.
- **LINE END OPEN PICKUP DELAY:** This setting defines the pickup setting for validation of the line end open conditions as detected by the Line Pickup logic through the LINE PICKUP LEO PKP FlexLogic™ operand. The validated line end open condition is a requirement for the POTT scheme to return a received echo signal (if the echo feature is enabled). The value of this setting should take into account the principle of operation and settings of the line pickup element.
- **POTT SEAL-IN DELAY:** The output FlexLogic™ operand (POTT OP) is produced according to the POTT scheme logic. A seal-in time delay is applied to this operand for coping with noisy communication channels. This setting specifies a minimum guaranteed duration of the POTT OP pulse.
- **GND DIR O/C FWD:** This setting selectes the FlexLogic™ operand (if any) of a protection element used in addition to zone 2 for identifying faults on the protected line, and thus, for keying the communication channel and initiating operation of the scheme. Good directional integrity is the key requirement for an over-reaching forward-looking protection element used as **GND DIR O/C FWD**. Even though any FlexLogic™ operand could be used as **GND DIR O/C FWD** allowing the user to combine responses of various protection elements, or to apply extra conditions through FlexLogic™ equations, this extra signal is primarily meant to be the output operand from either the negative-sequence directional overcurrent or neutral directional overcurrent elements. Both of these elements have separate forward and reverse output operands. The forward indication should be used (**NEG SEQ DIR OC1 FWD** or **NEUTRAL DIR OC1 FWD**).
- **POTT RX:** This setting enables the user to select the FlexLogic™ operand that represents the receive signal (RX) for the scheme. Typically an input contact interfacing with a signaling system is used. Other choices include remote inputs and FlexLogic™ equations. The POTT transmit signal (TX) should be appropriately interfaced with the signaling system by assigning the output FlexLogic™ operand (POTT TX) to an output contact. The remote output mechanism is another choice.

  The output operand from the scheme (POTT OP) must be configured to interface with other relay functions, output contacts in particular, in order to make the scheme fully operational. Typically, the output operand should be programmed to initiate a trip, breaker fail, and autoreclose, and drive a user-programmable LED as per user application.

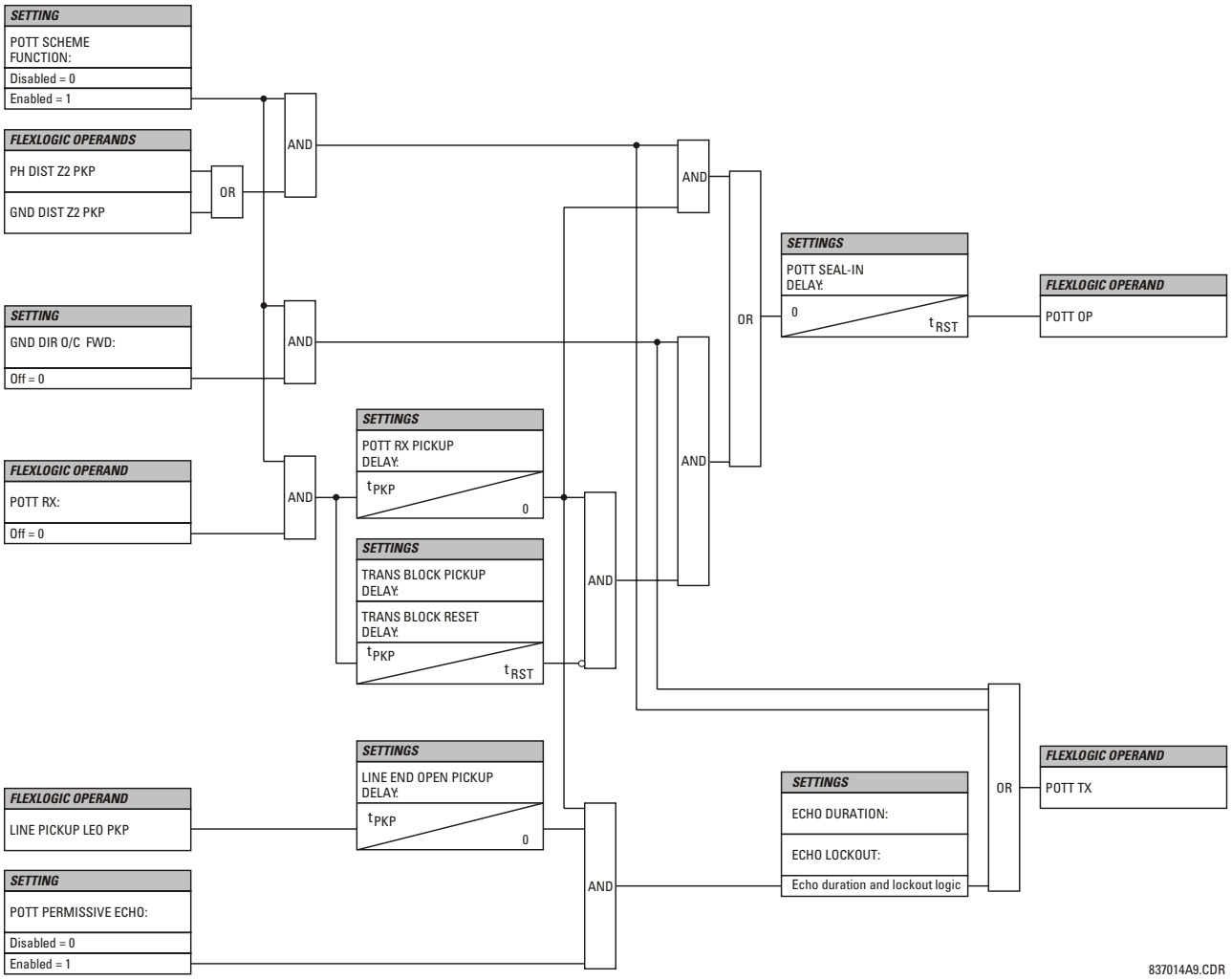
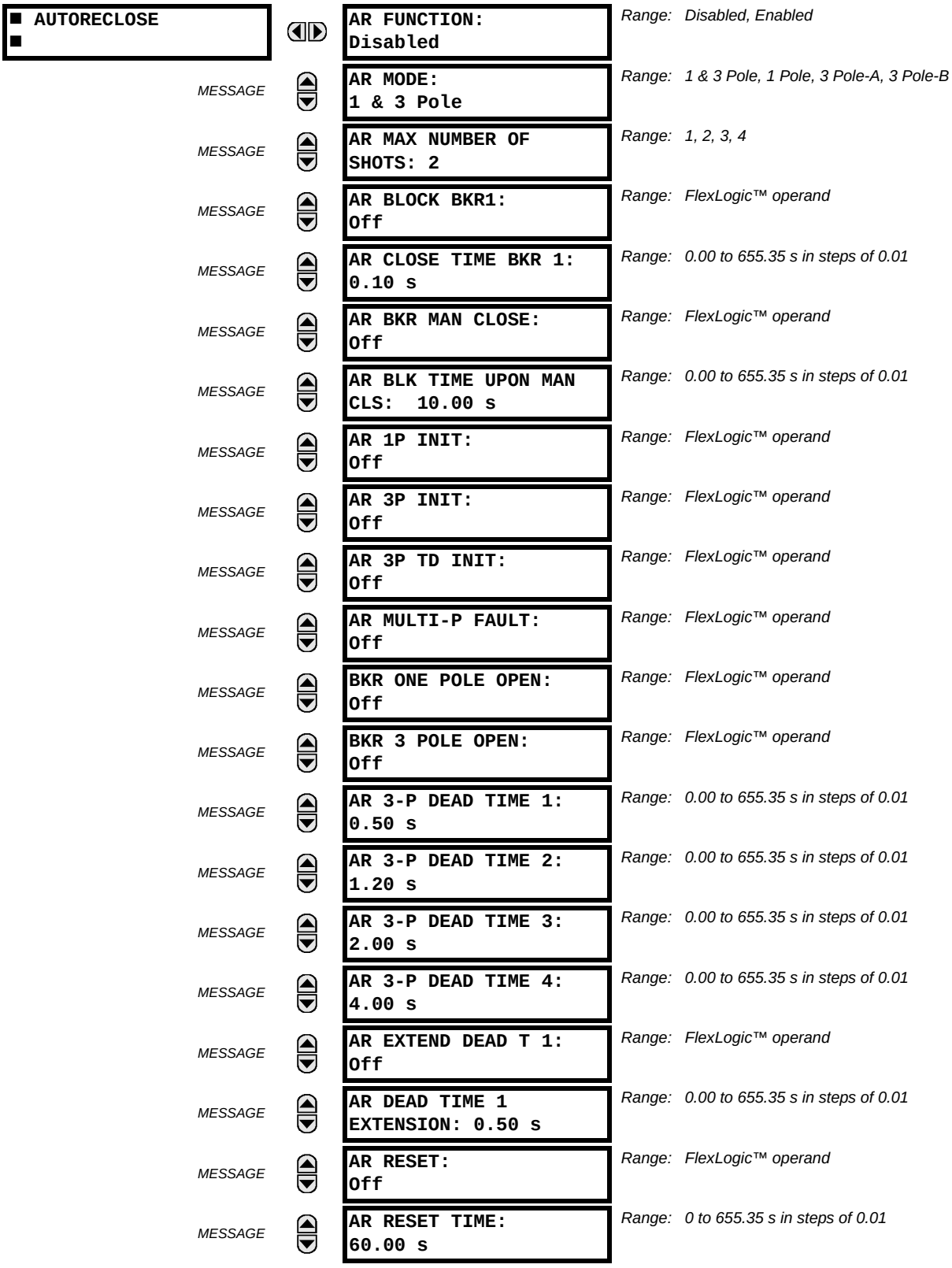
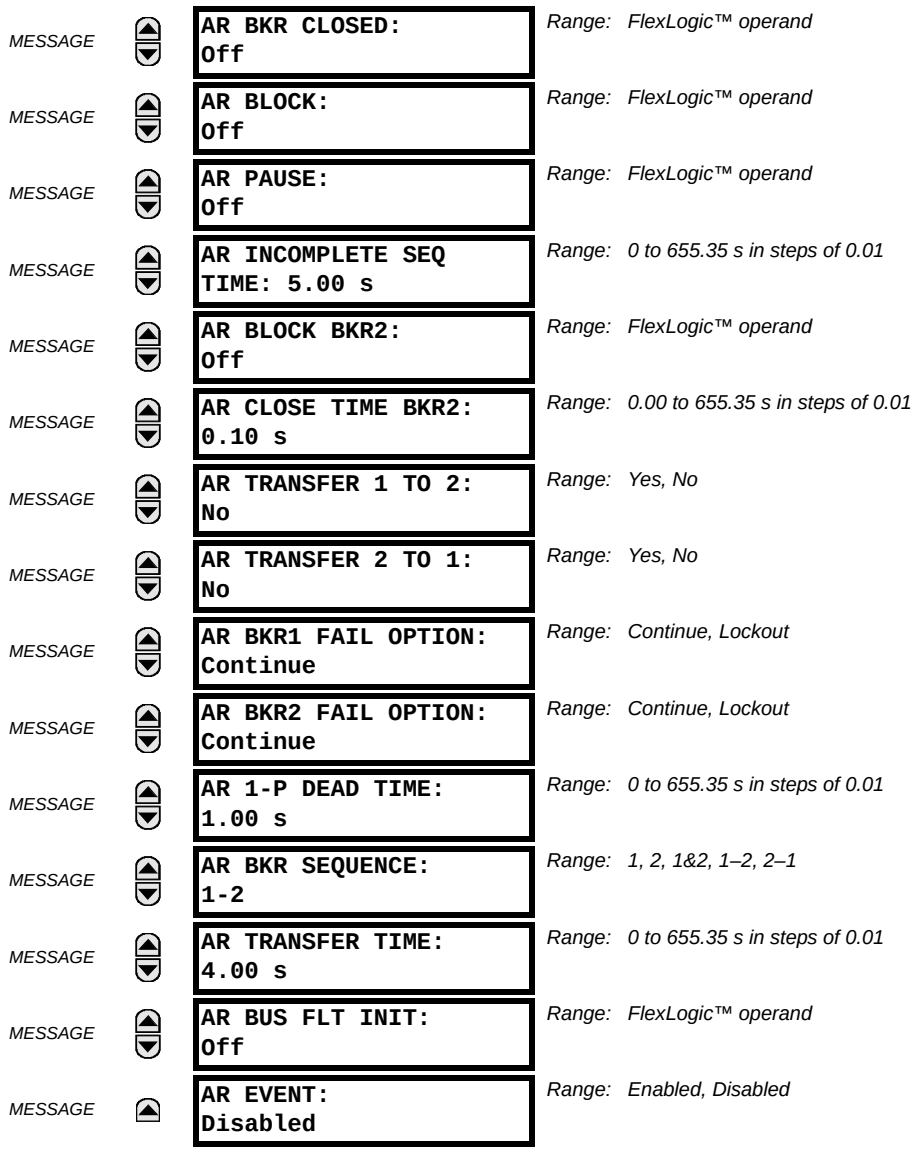


Figure 5–122: POTT SCHEME LOGIC

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ AUTORECLOSE ⇨ AUTORECLOSE





The autoreclose scheme is intended for use on transmission lines with circuit breakers operated in both the single pole and three pole modes, in one or two breaker arrangements. The autoreclose scheme provides four programs with different operating cycles, depending on the fault type. Each of the four programs can be set to trigger up to four reclosing attempts. The second, third, and fourth attempts always perform three-pole reclosing and have independent dead time delays.

When used in two breaker applications, the reclosing sequence is selectable. The reclose signal can be sent to one selected breaker only, to both breakers simultaneously or to both breakers in sequence (one breaker first and then, after a delay to check that the reclose was successful, to the second breaker). When reclosing in sequence, the first breaker should reclose with either the single-pole or three-pole dead time according to the fault type and reclose mode; the second breaker should follow the successful reclosure of the first breaker. When reclosing simultaneously, for the first shot both breakers should reclose with either the single-pole or three-pole dead time, according to the fault type and the reclose mode.

The signal used to initiate the autoreclose scheme is the trip output from protection. This signal can be single pole tripping for single phase faults and three phase tripping for multi-phase faults. The autoreclose scheme has five operating states.

STATE	CHARACTERISTICS
Enabled	Scheme is permitted to operate
Disabled	Scheme is not permitted to operate
Reset	Scheme is permitted to operate and shot count is reset to 0
Reclose in progress	Scheme has been initiated but the reclose cycle is not finished (successful or not)
Lockout	Scheme is not permitted to operate until reset received

AR PROGRAMS:

The autorecloser provides four programs that can cause from one to four reclose attempts (shots). After the first shot, all subsequent recloses will always be three-pole. If the maximum number of shots selected is "1" (only one reclose attempt) and the fault is persistent, after the first reclose the scheme will go to lockout upon another Initiate signal.

For the 3-pole reclose programs (modes 3 and 4), an AR FORCE 3-P FlexLogic™ operand is set. This operand can be used in connection with the tripping logic to cause a three-pole trip for single-phase faults.

Table 5–25: AUTORECLOSE PROGRAMS

MODE	AR MODE	FIRST SHOT		SECOND SHOT		THIRD SHOT		FOURTH SHOT	
		SINGLE-PHASE FAULT	MULTI-PHASE FAULT	SINGLE-PHASE FAULT	MULTI-PHASE FAULT	SINGLE-PHASE FAULT	MULTI-PHASE FAULT	SINGLE-PHASE FAULT	MULTI-PHASE FAULT
1	1 & 3 POLE	1 POLE	3 POLE	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO
2	1 POLE	1 POLE	LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO
3	3 POLE-A	3 POLE	LO	3 POLE or LO	LO	3 POLE or LO	LO	3 POLE or LO	LO
4	3 POLE-B	3 POLE	3 POLE	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO	3 POLE or LO

The four autoreclose modes are described below:

1. "1 & 3 Pole": In this mode, the autorecloser starts the **AR 1-P DEAD TIME** timer for the first shot if the autoreclose is single-phase initiated, the **AR 3-P DEAD TIME 1** timer if the autoreclose is three-pole initiated, and the **AR 3-P DEAD TIME 2** timer if the autoreclose is three-phase time delay initiated. If two or more shots are enabled, the second, third, and fourth shots are always three-pole and start the **AR 3-P DEAD TIME 2(4)** timers.
2. "1 Pole": In this mode, the autorecloser starts the **AR 1-P DEAD TIME** for the first shot if the fault is single phase. If the fault is three-phase *or a three-pole trip on the breaker occurred during the single-pole initiation*, the scheme goes to lockout without reclosing. If two or more shots are enabled, the second, third, and fourth shots are always three-pole and start the **AR 3-P DEAD TIME 2(4)** timers.
3. "3 Pole-A": In this mode, the autorecloser is initiated only for single phase faults, although the trip is three pole. The autorecloser uses the **AR 3-P DEAD TIME 1** for the first shot if the fault is single phase. If the fault is multi phase the scheme will go to Lockout without reclosing. If two or more shots are enabled, the second, third, and fourth shots are always three-phase and start the **AR 3-P DEAD TIME 2(4)** timers.
4. "3 Pole-B": In this mode, the autorecloser is initiated for any type of fault and starts the **AR 3-P DEAD TIME 1** for the first shot. If the initiating signal is **AR 3P TD INIT** the scheme starts **AR 3-P DEAD TIME 2** for the first shot. If two or more shots are enabled, the second, third, and fourth shots are always three-phase and start the **AR 3-P DEAD TIME 2(4)** timers.

BASIC RECLOSING OPERATION:

Reclosing operation is determined primarily by the **AR MODE** and **AR BKR SEQUENCE** settings. The reclosing sequences are started by the initiate inputs. A reclose initiate signal will send the scheme into the reclose-in-progress (RIP) state, asserting the AR RIP FlexLogic™ operand. The scheme is latched into the RIP state and resets only when an AR CLS BKR 1 (autoreclose breaker 1) or AR CLS BKR 2 (autoreclose breaker 2) operand is generated or the scheme goes to the Lockout state.

The dead time for the initial reclose operation will be determined by either the **AR 1-P DEAD TIME**, **AR 3-P DEAD TIME 1**, or **AR 3-P DEAD TIME 2** setting, depending on the fault type and the mode selected. After the dead time interval the scheme will assert the AR CLOSE BKR 1 or AR CLOSE BKR 2 operands, as determined by the sequence selected. These operands are latched until the breaker closes or the scheme goes to Reset or Lockout.

There are three initiate programs: single pole initiate, three pole initiate and three pole, time delay initiate. Any of these reclose initiate signals will start the reclose cycle and set the reclose-in-progress (AR RIP) operand. The reclose-in-progress operand is sealed-in until the Lockout or Reset signal appears.

The three-pole initiate and three-pole time delay initiate signals are latched until the CLOSE BKR1 OR BKR2 or Lockout or Reset signal appears.

AR PAUSE:

The pause input offers the possibility of freezing the autoreclose cycle until the pause signal disappears. This may be done when a trip occurs and simultaneously or previously, some conditions are detected such as out-of step or loss of guard frequency, or a remote transfer trip signal is received. The pause signal blocks all three dead timers. When the 'pause' signal disappears the autoreclose cycle is resumed by initiating **AR 3-P DEAD TIME 2**.

This feature can be also used when a transformer is tapped from the protected line and a reclose is not desirable until the transformer is removed from the line. In this case, the reclose scheme is 'paused' until the transformer is disconnected. The **AR PAUSE** input will force a three-pole trip through the **3-P DEADTIME 2** path.

EVOLVING FAULTS:

1.25 cycles after the single pole dead time has been initiated, the AR FORCE 3P TRIP operand is set and it will be reset only when the scheme is reset or goes to Lockout. This will ensure that when a fault on one phase evolves to include another phase during the single pole dead time of the auto-recloser the scheme will force a 3 pole trip and reclose.

RECLOSING SCHEME OPERATION FOR ONE BREAKER:

- **Permanent Fault**: Consider Mode 1, which calls for 1-Pole or 3-Pole Time Delay 1 for the first reclosure and 3-Pole Time Delay 2 for the second reclosure, and assume a permanent fault on the line. Also assume the scheme is in the Reset state. For the first single-phase fault the **AR 1-P DEAD TIME** timer will be started, while for the first multi-phase fault the **AR 3-P DEAD TIME 1** timer will be started. If the **AR 3P TD INIT** signal is high, the **AR 3-P DEAD TIME 2** will be started for the first shot.

  If **AR MAX NO OF SHOTS** is set to "1", upon the first reclose the shot counter is set to 1. Upon reclosing, the fault is again detected by protection and reclose is initiated. The breaker is tripped three-pole through the AR SHOT COUNT >0 operand that will set the AR FORCE 3P operand. Because the shot counter has reached the maximum number of shots permitted the scheme is sent to the Lockout state.

  If **AR MAX NO OF SHOTS** is set to "2", upon the first reclose the shot counter is set to 1. Upon reclosing, the fault is again detected by protection and reclose is initiated. The breaker is tripped three-pole through the AR SHOT COUNT >0 operand that will set the AR FORCE 3P operand. After the second reclose the shot counter is set to 2. Upon reclosing, the fault is again detected by protection, the breaker is tripped three-pole, and reclose is initiated again. Because the shot counter has reached the maximum number of shots permitted the scheme is sent to the lockout state.

- **Transient Fault**: When a reclose output signal is sent to close the breaker the reset timer is started. If the reclosure sequence is successful (there is no initiating signal and the breaker is closed) the reset timer will time out returning the scheme to the reset state with the shot counter set to "0" making it ready for a new reclose cycle.

RECLOSING SCHEME OPERATION FOR TWO BREAKERS:

- **Permanent Fault**: The general method of operation is the same as that outlined for the one breaker applications except for the following description, which assumes **AR BKR SEQUENCE** is "1-2" (reclose Breaker 1 before Breaker 2) The signal output from the dead time timers passes through the breaker selection logic to initiate reclosing of Breaker 1. The Close Breaker 1 signal will initiate the Transfer Timer. After the reclose of the first breaker the fault is again detected by the protection, the breaker is tripped three pole and the autoreclose scheme is initiated. The Initiate signal will stop the transfer timer. After the 3-P dead time times out the Close Breaker 1 signal will close first breaker again and will start the transfer timer. Since the fault is permanent the protection will trip again initiating the autoreclose scheme that will be sent to Lockout by the SHOT COUNT = MAX signal.

- **Transient Fault**: When the first reclose output signal is sent to close Breaker 1, the reset timer is started. The close Breaker 1 signal initiates the transfer timer that times out and sends the close signal to the second breaker. If the reclosure sequence is successful (both breakers closed and there is no initiating signal) the reset timer will time out, returning the scheme to the reset state with the shot counter set to 0. The scheme will be ready for a new reclose cycle.

AR BKR1(2) RECLS FAIL:

If the selected sequence is “1–2” or “2–1” and after the first or second reclose attempt the breaker fails to close, there are two options. If the **AR BKR 1(2) FAIL OPTION** is set to “Lockout”, the scheme will go to lockout state. If the **AR BKR 1(2) FAIL OPTION** is set to “Continue”, the reclose process will continue with Breaker 2. At the same time the shot counter will be decreased (since the closing process was not completed).

SCHEME RESET AFTER RECLOSURE:

When a reclose output signal is sent to close either breaker 1 or 2 the reset timer is started. If the reclosure sequence is successful (there is no initiating signal and the breakers are closed) the reset timer will time out, returning the scheme to the reset state, with the shot counter set to 0, making it ready for a new reclose cycle.

In two breaker schemes, if one breaker is in the out-of-service state and the other is closed at the end of the reset time, the scheme will also reset. If at the end of the reset time at least one breaker, which is not in the out-of-service state, is open the scheme will be sent to Lockout.

The reset timer is stopped if the reclosure sequence is not successful: an initiating signal present or the scheme is in Lockout state. The reset timer is also stopped if the breaker is manually closed or the scheme is otherwise reset from lockout.

LOCKOUT:

When a reclose sequence is started by an initiate signal the scheme moves into the reclose-in-progress state and starts the incomplete sequence timer. The setting of this timer determines the maximum time interval allowed for a single reclose shot. If a close breaker 1 or 2 signal is not present before this time expires, the scheme goes to “Lockout”.

There are four other conditions that can take the scheme to the Lockout state, as shown below:

- Receipt of ‘Block’ input while in the reclose-in-progress state
- The reclosing program logic: when a 3P Initiate is present and the autoreclose mode is either 1 Pole or 3Pole-A (3 pole autoreclose for single pole faults only)
- Initiation of the scheme when the count is at the maximum allowed
- If at the end of the reset time at least one breaker, which is not in the out-of-service state, is open the scheme will be sent to Lockout. The scheme will be also sent to Lockout if one breaker fails to reclose and the setting **AR BKR FAIL OPTION** is set to “Lockout”.

Once the Lockout state is set it will be latched until one or more of the following occurs:

- The scheme is intentionally reset from Lockout, employing the Reset setting of the Autorecloser;
- The Breaker(s) is(are) manually closed from panel switch, SCADA or other remote control through the **AR BRK MAN CLOSE** setting;
- 10 seconds after breaker control detects that breaker(s) were closed.

BREAKER OPEN BEFORE FAULT:

A logic circuit is provided that inhibits the close breaker 1 and close breaker 2 outputs if a reclose initiate (RIP) indicator is not present within 30 ms of the Breaker Any Phase Open input. This feature is intended to prevent reclosing if one of the breakers was open in advance of a reclose initiate input to the recloser. This logic circuit resets when the breaker is closed.

TRANSFER RECLOSE WHEN BREAKER IS BLOCKED:

1. When the reclosing sequence 1-2 is selected and Breaker 1 is blocked (AR BKR1 BLK operand is set) the reclose signal can be transferred direct to the Breaker 2 if **AR TRANSFER 1 TO 2** is set to “Yes”. If set to “No”, the scheme will be sent to Lockout by the incomplete sequence timer.
2. When the reclosing sequence 2-1 is selected and Breaker 2 is blocked (AR BKR2 BLK operand is set) the reclose signal can be transferred direct to the Breaker 1 if **AR TRANSFER 2 TO 1** is set to “Yes”. If set to “No” the scheme will be sent to Lockout by the incomplete sequence timer.

FORCE 3-POLE TRIPPING:

The reclosing scheme contains logic that is used to signal trip logic that three-pole tripping is required for certain conditions. This signal is activated by any of the following:

- Autoreclose scheme is paused after it was initiated.
- Autoreclose scheme is in the Lockout state.

- Autoreclose mode is programmed for three-pole operation
- The shot counter is not at 0, i.e. the scheme is not in the reset state. This ensures a second trip will be three-pole when reclosing onto a permanent single phase fault.
- 1.25 cycles after the single-pole reclose is initiated by the AR 1P INIT signal.

ZONE 1 EXTENT:

The Zone 1 extension philosophy here is to apply an overreaching zone permanently as long as the relay is ready to reclose, and reduce the reach when reclosing. Another Zone 1 extension approach is to operate normally from an underreaching zone, and use an overreaching distance zone when reclosing the line with the other line end open. This philosophy could be programmed via the Line Pickup scheme.

The “Extended Zone 1" is 0 when Autoreclose is in Lockout or Disabled and 1 when Autoreclose is in Reset.

1. When "Extended Zone 1" is 0, the distance functions shall be set to normal underreach Zone 1 setting.
2. When "Extended Zone 1" is 1, the distance functions may be set to Extended Zone 1 Reach, which is an overreaching setting.
3. During a reclose cycle, "Extended Zone 1" goes to 0 as soon as the first CLOSE BREAKER signal is issued (AR SHOT COUNT > 0) and remains 0 until the recloser goes back to Reset.

USE OF SETTINGS:

The single-phase autoreclose settings are described below.

- **AR MODE**: This setting selects the Autoreclose operating mode, which functions in conjunction with signals received at the initiation inputs as described previously.
- **AR MAX NUMBER OF SHOTS**: This setting specifies the number of reclosures that can be attempted before reclosure goes to Lockout when the fault is permanent.
- **AR BLOCK BKR1**: This input selects an operand that will block the reclose command for Breaker 1. This condition can be for example: breaker low air pressure, reclose in progress on another line (for the central breaker in a breaker and a half arrangement), or a sum of conditions combined in FlexLogic™.
- **AR CLOSE TIME BKR1**:This setting represents the closing time for the Breaker 1 from the moment the “Close” command is sent to the moment the contacts are closed.
- **AR BKR MAN CLOSE:** This setting selects a FlexLogic™ operand that represents manual close command to a breaker associated with the autoreclose scheme.
- **AR BLK TIME UPON MAN CLS**: The autoreclose scheme can be disabled for a programmable time delay after an associated circuit breaker is manually commanded to close, preventing reclosing onto an existing fault such as grounds on the line. This delay must be longer than the slowest expected trip from any protection not blocked after manual closing. If the autoreclose scheme is not initiated after a manual close and this time expires the autoreclose scheme is set to the Reset state.
- **AR 1P INIT**: This setting selects a FlexLogic™ operand that is intended to initiate single-pole autoreclosure.
- **AR 3P INIT**: This setting selects a FlexLogic™ operand that is intended to initiate three-pole autoreclosure, first timer (**AR 3P DEAD TIME 1**) that can be used for a high-speed autoreclosure.
- **AR 3P TD INIT**: This setting selects a FlexLogic™ operand intended to initiate three-pole autoreclosure. second timer (**AR 3P DEAD TIME 2**) can be used for a time-delay autoreclosure.
- **AR MULTI-P FAULT:** This setting selects a FlexLogic™ operand that indicates a multi-phase fault. The operand value should be zero for single-phase to ground faults.
- **BKR ONE POLE OPEN:** This setting selects a FlexLogic™ operand which indicates that the breaker(s) has opened correctly following a single phase to ground fault and the autoreclose scheme can start timing the single pole dead time (for 1-2 reclose sequence for example, Breaker 1 should trip single pole and Breaker 2 should trip 3 pole).

  The scheme has a pre-wired input that indicates breaker(s) status.
- **BKR 3 POLE OPEN:** This setting selects a FlexLogic™ operand which indicates that the breaker(s) has opened three pole and the autoreclose scheme can start timing the three pole dead time. The scheme has a pre-wired input that indicates breaker(s) status.

- **AR 3-P DEAD TIME 1**: This is the dead time following the first three pole trip. This intentional delay can be used for a high-speed three-pole autoreclose. However, it should be set longer than the estimated de-ionizing time following the three-pole trip.
- **AR 3-P DEAD TIME 2**: This is the dead time following the second three-pole trip or initiated by the AR 3P TD INIT input. This intentional delay is typically used for a time delayed three-pole autoreclose (as opposed to high speed three-pole autoreclose).
- **AR 3-P DEAD TIME 3(4)**: These settings represent the dead time following the third (fourth) three-pole trip.
- **AR EXTEND DEAD T 1**: This setting selects an operand that will adapt the duration of the dead time for the first shot to the possibility of non-simultaneous tripping at the two line ends. Typically this is the operand set when the communication channel is out of service
- **AR DEAD TIME 1 EXTENSION**: This timer is used to set the length of the dead time 1 extension for possible non-simultaneous tripping of the two ends of the line.
- **AR RESET**: This setting selects the operand that forces the autoreclose scheme from any state to Reset. Typically this is a manual reset from lockout, local or remote.
- **AR RESET TIME**: A reset timer output resets the recloser following a successful reclosure sequence. The setting is based on the breaker time which is the minimum time required between successive reclose sequences.
- **AR BKR CLOSED:** This setting selects an operand that indicates that the breaker(s) are closed at the end of the reset time and the scheme can reset.
- **AR BLOCK**: This setting selects the operand that blocks the Autoreclose scheme (it can be a sum of conditions such as: time delayed tripping, breaker failure, bus differential protection, etc.). If the block signal is present before autoreclose scheme initiation the AR DISABLED FlexLogic™ operand will be set. If the block signal occurs when the scheme is in the RIP state the scheme will be sent to Lockout.
- **AR PAUSE**: The pause input offers the ability to freeze the autoreclose cycle until the pause signal disappears. This may be done when a trip occurs and simultaneously or previously, some conditions are detected such as out-of step or loss of guard frequency, or a remote transfer trip signal is received. When the 'pause' signal disappears the autoreclose cycle is resumed. This feature can also be used when a transformer is tapped from the protected line and a reclose is not desirable until the it is disconnected from the line. In this situation, the reclose scheme is 'paused' until the transformer is disconnected.
- **AR INCOMPLETE SEQ TIME**: This timer is used to set the maximum time interval allowed for a single reclose shot. It is started whenever a reclosure is initiated and is active until the CLOSE BKR1 or CLOSE BKR2 signal is sent. If all conditions allowing a breaker closure are not satisfied when this time expires, the scheme goes to "Lockout". The minimum permissible setting is established by the **AR 3-P DEAD TIME 2** timer setting. Settings beyond this will determine the 'wait' time for the breaker to open so that the reclose cycle can continue and/or for the AR PAUSE signal to reset and allow the reclose cycle to continue and/or for the AR BKR1(2) BLK signal to disappear and allow the AR CLOSE BKR1(2) signal to be sent.
- **AR BLOCK BKR2**: This input selects an operand that will block the reclose command for Breaker 2. This condition can be for example: breaker low air pressure, reclose in progress on another line (for the central breaker in a breaker and a half arrangement), or a sum of conditions combined in FlexLogic™.
- **AR CLOSE TIME BKR2**: This setting represents the closing time for the Breaker 2 from the moment the 'Close' command is sent to the moment the contacts are closed.
- **AR TRANSFER 1 TO 2**: This setting establishes how the scheme performs when the breaker closing sequence is 1-2 and Breaker 1 is blocked. When set to "Yes" the closing command will be transferred direct to Breaker 2 without waiting the transfer time. When set to "No" the closing command will be blocked by the AR BKR1 BLK signal and the scheme will be sent to Lockout by the incomplete sequence timer.
- **AR TRANSFER 2 TO 1**: This setting establishes how the scheme performs when the breaker closing sequence is 2-1 and Breaker 2 is blocked. When set to "Yes" the closing command will be transferred direct to Breaker 1 without waiting the transfer time. When set to "No", the closing command will be blocked by the AR BKR2 BLK signal and the scheme will be sent to Lockout by the incomplete sequence timer.
- **AR BKR1 FAIL OPTION**: This setting establishes how the scheme performs when the breaker closing sequence is 1-2 and Breaker 1 has failed to close. When set to "Continue" the closing command will be transferred to Breaker 2 which will continue the reclosing cycle until successful (the scheme will reset) or unsuccessful (the scheme will go to Lockout). When set to "Lockout" the scheme will go to lockout without attempting to reclose Breaker 2.

- **AR BKR2 FAIL OPTION**: This setting establishes how the scheme performs when the breaker closing sequence is 2-1 and Breaker 2 has failed to close. When set to “Continue” the closing command will be transferred to Breaker 1 which will continue the reclosing cycle until successful (the scheme will reset) or unsuccessful (the scheme will go to Lockout). When set to “Lockout” the scheme will go to lockout without attempting to reclose Breaker 1.
- **AR 1-P DEAD TIME**: Set this intentional delay longer than the estimated de-ionizing time after the first single-pole trip.
- **AR BREAKER SEQUENCE**: This setting selects the breakers reclose sequence: Select “1” for reclose breaker 1 only, “2” for reclose breaker 2 only, “1&2” for reclose both breakers simultaneously, “1-2” for reclose breakers sequentially; Breaker 1 first, and “2-1” for reclose breakers sequentially; Breaker 2 first.
- **AR TRANSFER TIME**: The transfer time is used only for breaker closing sequence 1-2 or 2-1, when the two breakers are reclosed sequentially. The transfer timer is initiated by a close signal to the first breaker. The transfer timer transfers the reclose signal from the breaker selected to close first to the second breaker. The time delay setting is based on the maximum time interval between the autoreclose signal and the protection trip contact closure assuming a permanent fault (unsuccessful reclose). Therefore, the minimum setting is equal to the maximum breaker closing time plus the maximum line protection operating time plus a suitable margin. This setting will prevent the autoreclose scheme from transferring the close signal to the second breaker unless a successful reclose of the first breaker occurs.
- **AR BUS FLT INIT**: This setting is used in breaker-and-a-half applications to allow the autoreclose control function to perform reclosing with only *one* breaker previously opened by bus protection. For line faults, both breakers must open for the autoreclose reclosing cycles to take effect.

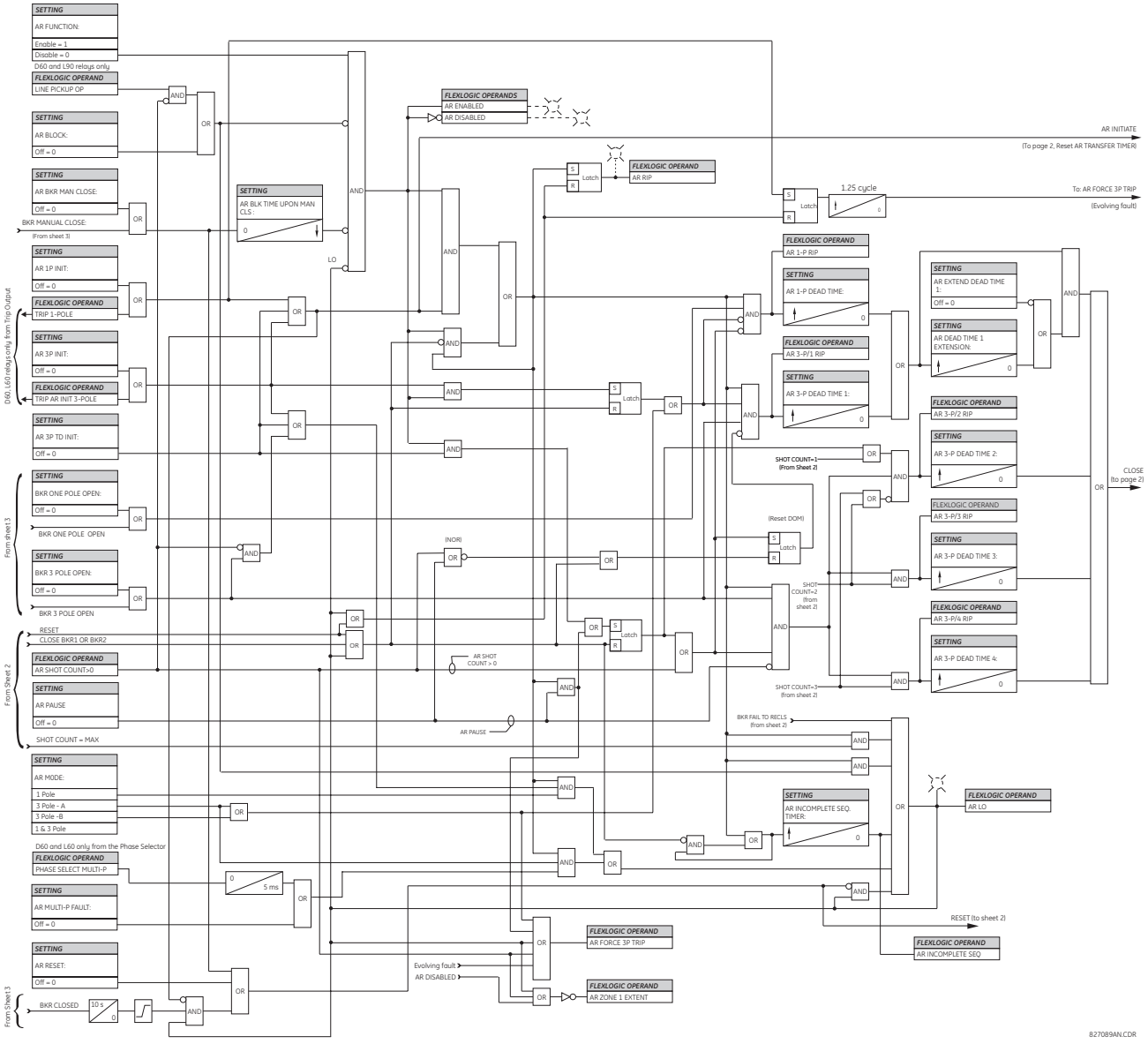


Figure 5–123: SINGLE-POLE AUTORECLOSE LOGIC (Sheet 1 of 3)

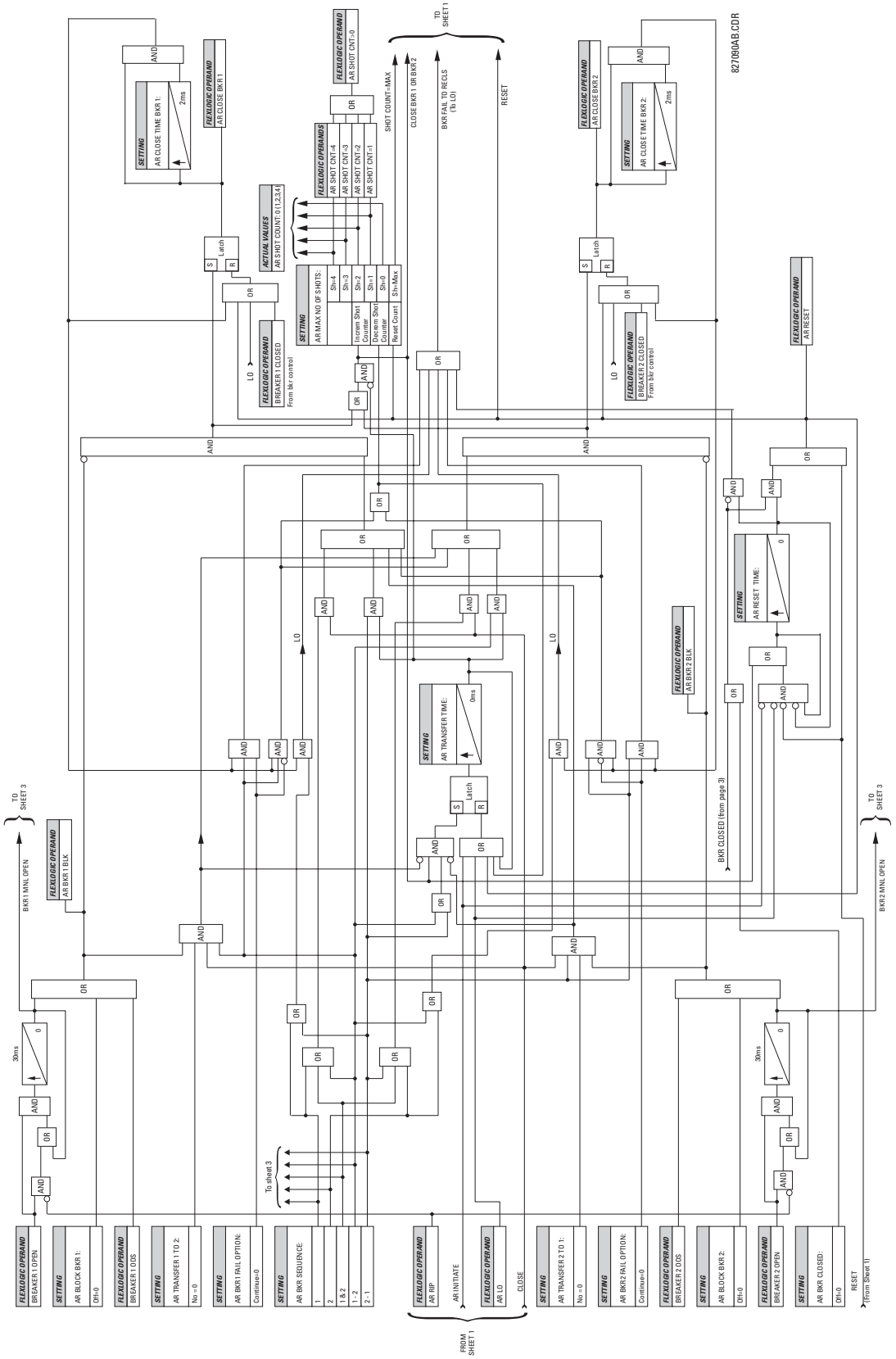


Figure 5–124: SINGLE-POLE AUTORECLOSE LOGIC (Sheet 2 of 3)

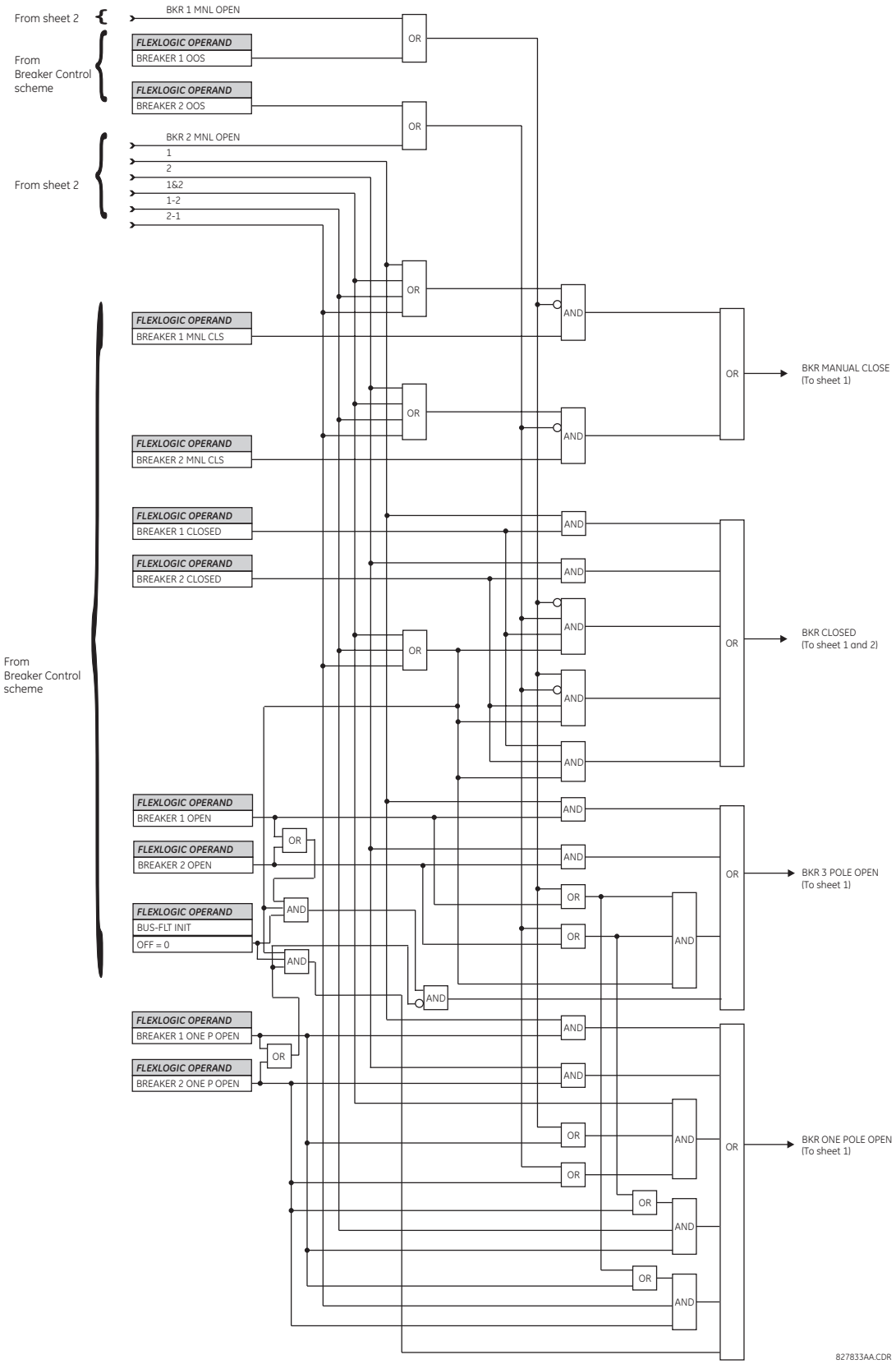


Figure 5–125: SINGLE-POLE AUTORECLOSE LOGIC (Sheet 3 of 3)

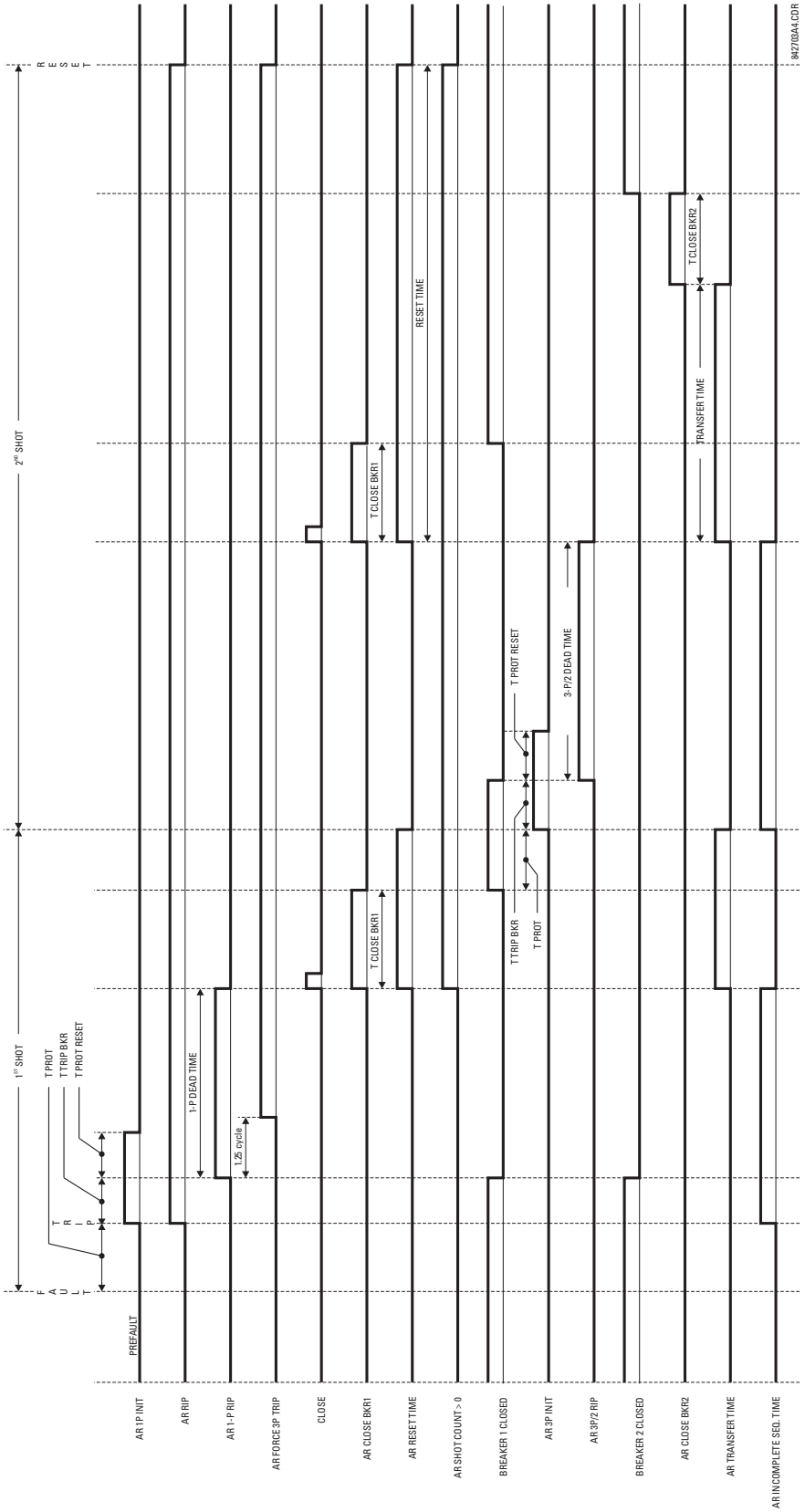
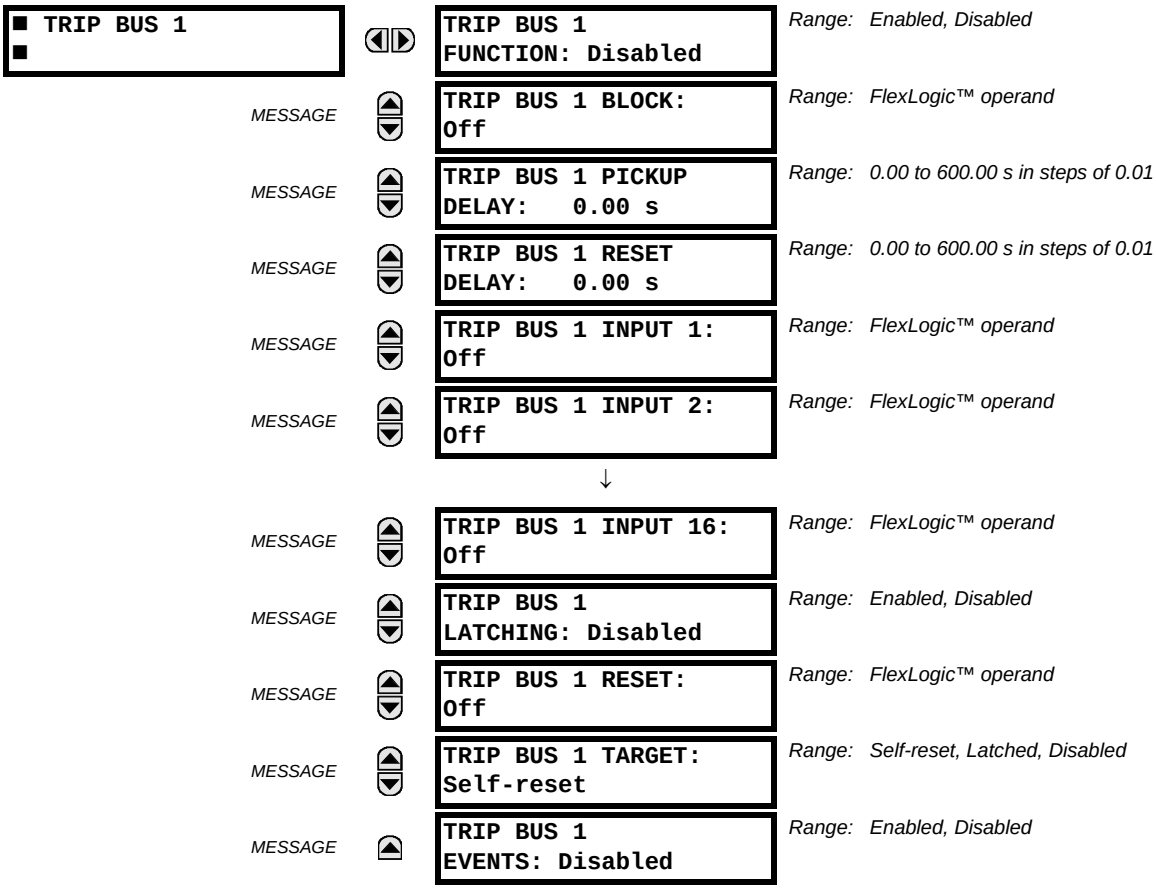


Figure 5–126: EXAMPLE RECLOSING SEQUENCE

PATH: SETTINGS ⇨⇩ CONTROL ELEMENTS ⇨⇩ TRIP BUS ⇨⇩ TRIP BUS 1(6))



The trip bus element allows aggregating outputs of protection and control elements without using FlexLogic™ and assigning them a simple and effective manner. Each trip bus can be assigned for either trip or alarm actions. Simple trip conditioning such as latch, delay, and seal-in delay are available.

The easiest way to assign element outputs to a trip bus is through the EnerVista UR Setup software A protection summary is displayed by navigating to a specific protection or control protection element and checking the desired bus box. Once the desired element is selected for a specific bus, a list of element operate-type operands are displayed and can be assigned to a trip bus. If more than one operate-type operand is required, it may be assigned directly from the trip bus menu.

Protection Summary // Quick Connect: Quick Connect Device: Settings

Save | Restore | Default | Reset | VIEW ALL mode

GROUPED ELEMENTS	TB1 TB2 TB3 TB4 TB5	GROUP 1	GROUP 2	GROUP 3	GROUP 4	GROUP 5	GROUP 6
Current Differential	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Stub Bus	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Line Pickup	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase Distance Z 1	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase Distance Z 2	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase Distance Z 3	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Ground Distance Z 1	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Ground Distance Z 2	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Ground Distance Z 3	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Power Swing	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Load Encroachment	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase TOC 1	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase TOC 2	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase TOC 3	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Phase TOC 4	☐ ☐ ☐ ☐ ☐	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled

Quick Connect Device

Figure 5–127: TRIP BUS FIELDS IN THE PROTECTION SUMMARY

The following settings are available.

- **TRIP BUS 1 BLOCK**: The trip bus output is blocked when the operand assigned to this setting is asserted.
- **TRIP BUS 1 PICKUP DELAY**: This setting specifies a time delay to produce an output depending on how output is used.
- **TRIP BUS 1 RESET DELAY**: This setting specifies a time delay to reset an output command. The time delay should be set long enough to allow the breaker or contactor to perform a required action.
- **TRIP BUS 1 INPUT 1** to **TRIP BUS 1 INPUT 16**: These settings select a FlexLogic™ operand to be assigned as an input to the trip bus.
- **TRIP BUS 1 LATCHING**: This setting enables or disables latching of the trip bus output. This is typically used when lockout is required or user acknowledgement of the relay response is required.
- **TRIP BUS 1 RESET**: The trip bus output is reset when the operand assigned to this setting is asserted. Note that the RESET OP operand is pre-wired to the reset gate of the latch, As such, a reset command the front panel interface or via communications will reset the trip bus output.

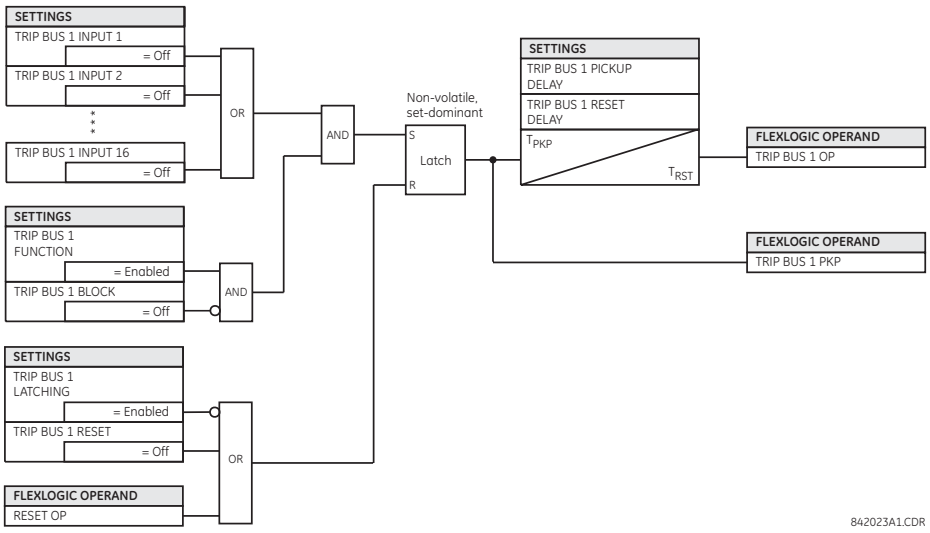
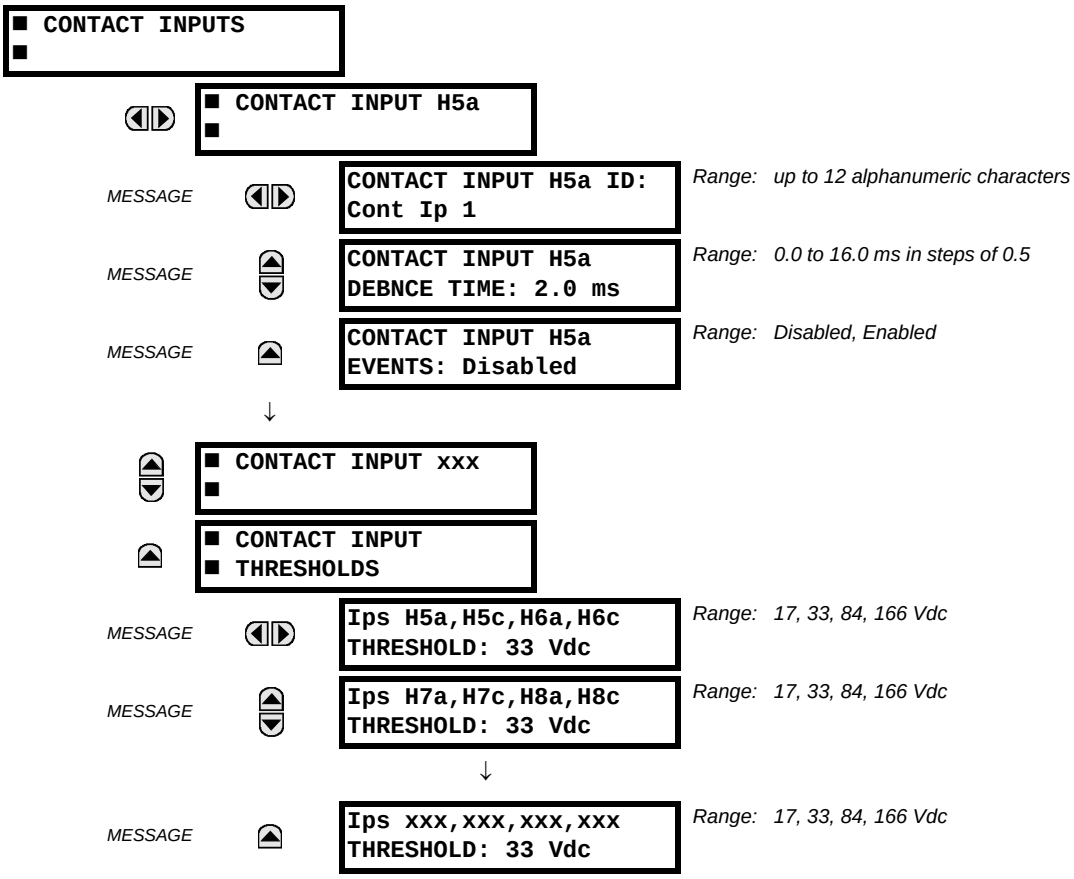


Figure 5–128: TRIP BUS LOGIC

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨ CONTACT INPUTS



The contact inputs menu contains configuration settings for each contact input as well as voltage thresholds for each group of four contact inputs. Upon startup, the relay processor determines (from an assessment of the installed modules) which contact inputs are available and then display settings for only those inputs.

An alphanumeric ID may be assigned to a contact input for diagnostic, setting, and event recording purposes. The CONTACT IP X On" (Logic 1) FlexLogic™ operand corresponds to contact input "X" being closed, while CONTACT IP X Off corresponds to contact input "X" being open. The **CONTACT INPUT DEBNCE TIME** defines the time required for the contact to overcome 'contact bouncing' conditions. As this time differs for different contact types and manufacturers, set it as a maximum contact debounce time (per manufacturer specifications) plus some margin to ensure proper operation. If **CONTACT INPUT EVENTS** is set to "Enabled", every change in the contact input state will trigger an event.

A raw status is scanned for all Contact Inputs synchronously at the constant rate of 0.5 ms as shown in the figure below. The DC input voltage is compared to a user-settable threshold. A new contact input state must be maintained for a user-settable debounce time in order for the L60 to validate the new contact state. In the figure below, the debounce time is set at 2.5 ms; thus the 6th sample in a row validates the change of state (mark no. 1 in the diagram). Once validated (debounced), the contact input asserts a corresponding FlexLogic™ operand and logs an event as per user setting.

A time stamp of the first sample in the sequence that validates the new state is used when logging the change of the contact input into the Event Recorder (mark no. 2 in the diagram).

Protection and control elements, as well as FlexLogic™ equations and timers, are executed eight times in a power system cycle. The protection pass duration is controlled by the frequency tracking mechanism. The FlexLogic™ operand reflecting the debounced state of the contact is updated at the protection pass following the validation (marks no. 3 and 4 on the figure below). The update is performed at the beginning of the protection pass so all protection and control functions, as well as FlexLogic™ equations, are fed with the updated states of the contact inputs.

The FlexLogic™ operand response time to the contact input change is equal to the debounce time setting plus up to one protection pass (variable and depending on system frequency if frequency tracking enabled). If the change of state occurs just after a protection pass, the recognition is delayed until the subsequent protection pass; that is, by the entire duration of the protection pass. If the change occurs just prior to a protection pass, the state is recognized immediately. Statistically a delay of half the protection pass is expected. Owing to the 0.5 ms scan rate, the time resolution for the input contact is below 1msec.

For example, 8 protection passes per cycle on a 60 Hz system correspond to a protection pass every 2.1 ms. With a contact debounce time setting of 3.0 ms, the FlexLogic™ operand-assert time limits are: 3.0 + 0.0 = 3.0 ms and 3.0 + 2.1 = 5.1 ms. These time limits depend on how soon the protection pass runs after the debouncing time.

Regardless of the contact debounce time setting, the contact input event is time-stamped with a 1 μs accuracy using the time of the first scan corresponding to the new state (mark no. 2 below). Therefore, the time stamp reflects a change in the DC voltage across the contact input terminals that was not accidental as it was subsequently validated using the debounce timer. Keep in mind that the associated FlexLogic™ operand is asserted/de-asserted later, after validating the change.

The debounce algorithm is symmetrical: the same procedure and debounce time are used to filter the LOW-HIGH (marks no.1, 2, 3, and 4 in the figure below) and HIGH-LOW (marks no. 5, 6, 7, and 8 below) transitions.

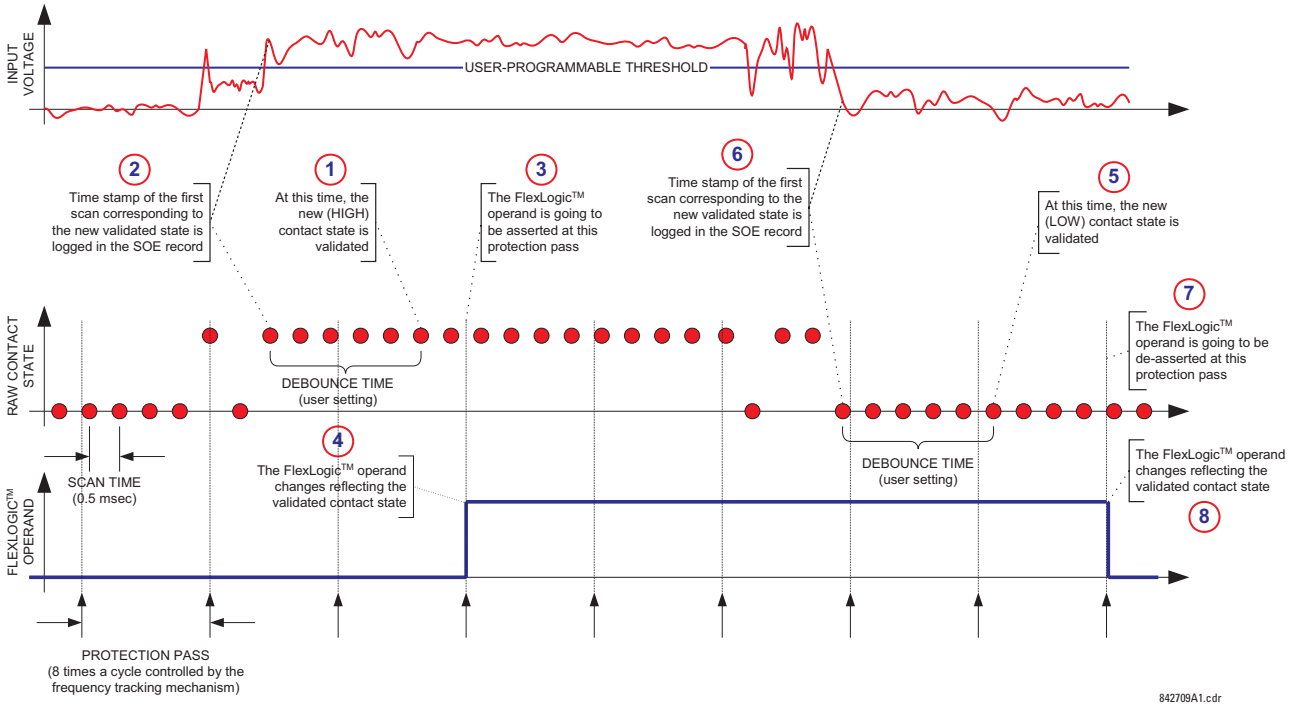


Figure 5–129: INPUT CONTACT DEBOUNCING MECHANISM AND TIME-STAMPING SAMPLE TIMING

Contact inputs are isolated in groups of four to allow connection of wet contacts from different voltage sources for each group. The **CONTACT INPUT THRESHOLDS** determine the minimum voltage required to detect a closed contact input. This value should be selected according to the following criteria: 17 for 24 V sources, 33 for 48 V sources, 84 for 110 to 125 V sources and 166 for 250 V sources.

For example, to use contact input H5a as a status input from the breaker 52b contact to seal-in the trip relay and record it in the Event Records menu, make the following settings changes:

CONTACT INPUT H5A ID: "Breaker Closed (52b)"
CONTACT INPUT H5A EVENTS: "Enabled"

Note that the 52b contact is closed when the breaker is open and open when the breaker is closed.

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ VIRTUAL INPUTS ⇨ VIRTUAL INPUT 1(64)

```
■ VIRTUAL INPUT  1
■
```

```
VIRTUAL INPUT  1
FUNCTION: Disabled
```

Range: Disabled, Enabled

MESSAGE

```
VIRTUAL INPUT  1 ID:
Virt Ip 1
```

Range: Up to 12 alphanumeric characters

MESSAGE

```
VIRTUAL INPUT  1
TYPE: Latched
```

Range: Self-Reset, Latched

MESSAGE

```
VIRTUAL INPUT  1
EVENTS: Disabled
```

Range: Disabled, Enabled

There are 64 virtual inputs that can be individually programmed to respond to input signals from the keypad (via the COMMANDS menu) and communications protocols. All virtual input operands are defaulted to "Off" (logic 0) unless the appropriate input signal is received.

If the **VIRTUAL INPUT x FUNCTION** is to "Disabled", the input will be forced to off (logic 0) regardless of any attempt to alter the input. If set to "Enabled", the input operates as shown on the logic diagram and generates output FlexLogic™ operands in response to received input signals and the applied settings.

There are two types of operation: self-reset and latched. If **VIRTUAL INPUT x TYPE** is "Self-Reset", when the input signal transits from off to on, the output operand will be set to on for only one evaluation of the FlexLogic™ equations and then return to off. If set to "Latched", the virtual input sets the state of the output operand to the same state as the most recent received input.

NOTE

The self-reset operating mode generates the output operand for a single evaluation of the FlexLogic™ equations. If the operand is to be used anywhere other than internally in a FlexLogic™ equation, it will likely have to be lengthened in time. A FlexLogic™ timer with a delayed reset can perform this function.

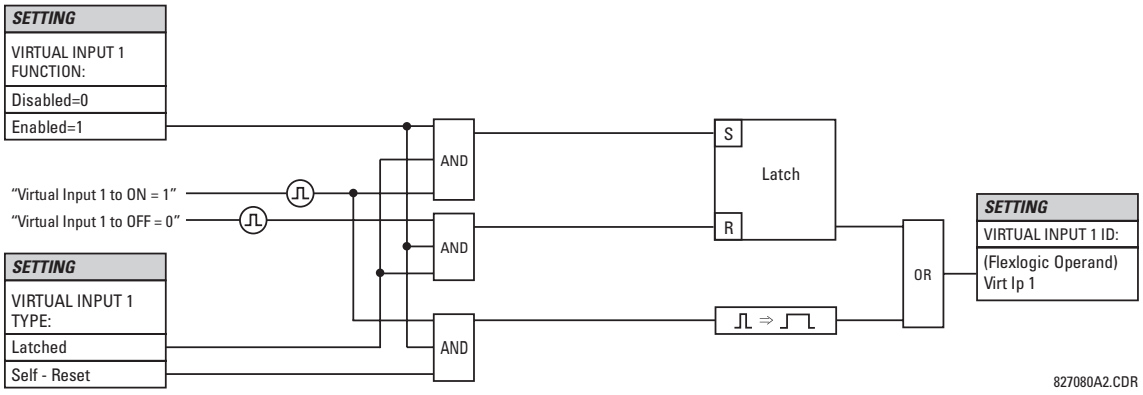
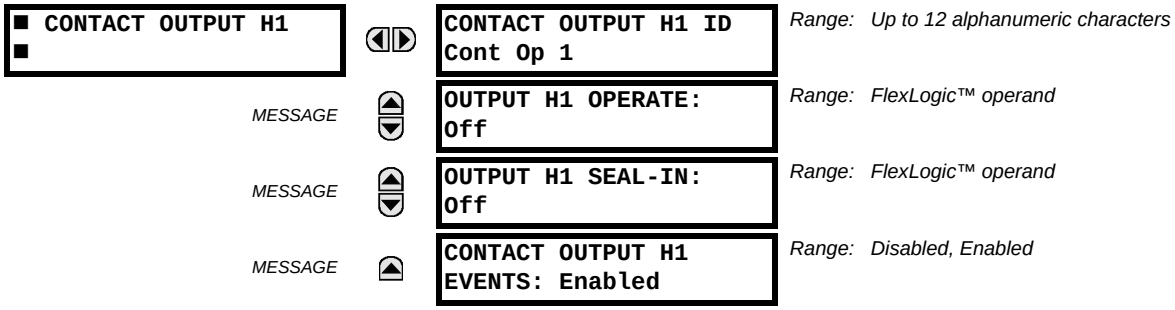


Figure 5–130: VIRTUAL INPUTS SCHEME LOGIC

a) DIGITAL OUTPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS ⇨ CONTACT OUTPUT H1



Upon startup of the relay, the main processor will determine from an assessment of the modules installed in the chassis which contact outputs are available and present the settings for only these outputs.

An ID may be assigned to each contact output. The signal that can **OPERATE** a contact output may be any FlexLogic™ operand (virtual output, element state, contact input, or virtual input). An additional FlexLogic™ operand may be used to **SEAL-IN** the relay. Any change of state of a contact output can be logged as an Event if programmed to do so.

For example, the trip circuit current is monitored by providing a current threshold detector in series with some Form-A contacts (see the trip circuit example in the *Digital Elements* section). The monitor will set a flag (see the specifications for Form-A). The name of the FlexLogic™ operand set by the monitor, consists of the output relay designation, followed by the name of the flag; e.g. 'Cont Op 1 IOn' or 'Cont Op 1 IOff'.

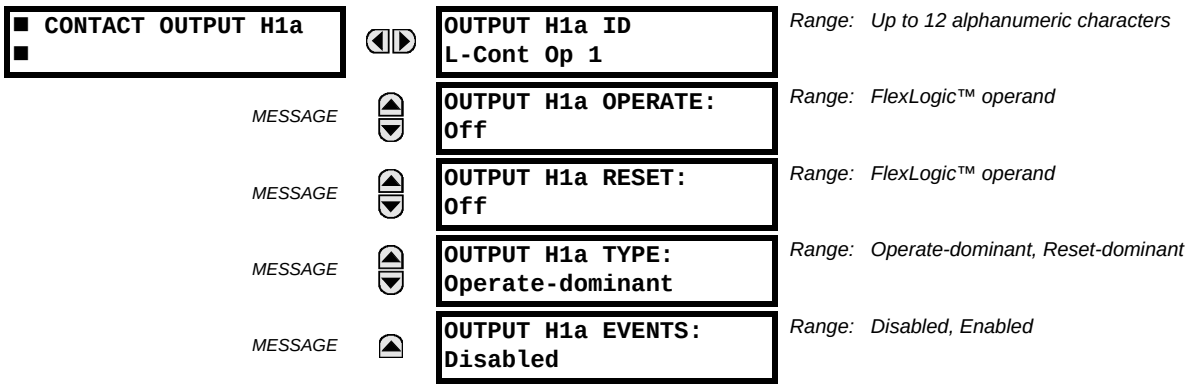
In most breaker control circuits, the trip coil is connected in series with a breaker auxiliary contact used to interrupt current flow after the breaker has tripped, to prevent damage to the less robust initiating contact. This can be done by monitoring an auxiliary contact on the breaker which opens when the breaker has tripped, but this scheme is subject to incorrect operation caused by differences in timing between breaker auxiliary contact change-of-state and interruption of current in the trip circuit. The most dependable protection of the initiating contact is provided by directly measuring current in the tripping circuit, and using this parameter to control resetting of the initiating relay. This scheme is often called 'trip seal-in'.

This can be realized in the L60 using the 'Cont Op 1 IOn' FlexLogic™ operand to seal-in the contact output as follows:

CONTACT OUTPUT H1 ID: "Cont Op 1"
OUTPUT H1 OPERATE: *any suitable FlexLogic™ operand*
OUTPUT H1 SEAL-IN: "Cont Op 1 IOn"
CONTACT OUTPUT H1 EVENTS: "Enabled"

b) LATCHING OUTPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS ⇨ CONTACT OUTPUT H1a



The L60 latching output contacts are mechanically bi-stable and controlled by two separate (open and close) coils. As such they retain their position even if the relay is not powered up. The relay recognizes all latching output contact cards and populates the setting menu accordingly. On power up, the relay reads positions of the latching contacts from the hardware before executing any other functions of the relay (such as protection and control features or FlexLogic™).

The latching output modules, either as a part of the relay or as individual modules, are shipped from the factory with all latching contacts opened. It is highly recommended to double-check the programming and positions of the latching contacts when replacing a module.

Since the relay asserts the output contact and reads back its position, it is possible to incorporate self-monitoring capabilities for the latching outputs. If any latching outputs exhibits a discrepancy, the **LATCHING OUTPUT ERROR** self-test error is declared. The error is signaled by the LATCHING OUT ERROR FlexLogic™ operand, event, and target message.

- **OUTPUT H1a OPERATE**: This setting specifies a FlexLogic™ operand to operate the 'close coil' of the contact. The relay will seal-in this input to safely close the contact. Once the contact is closed and the **RESET** input is logic 0 (off), any activity of the **OPERATE** input, such as subsequent chattering, will not have any effect. With both the **OPERATE** and **RESET** inputs active (logic 1), the response of the latching contact is specified by the **OUTPUT H1A TYPE** setting.
- **OUTPUT H1a RESET**: This setting specifies a FlexLogic™ operand to operate the 'trip coil' of the contact. The relay will seal-in this input to safely open the contact. Once the contact is opened and the **OPERATE** input is logic 0 (off), any activity of the **RESET** input, such as subsequent chattering, will not have any effect. With both the **OPERATE** and **RESET** inputs active (logic 1), the response of the latching contact is specified by the **OUTPUT H1A TYPE** setting.
- **OUTPUT H1a TYPE**: This setting specifies the contact response under conflicting control inputs; that is, when both the **OPERATE** and **RESET** signals are applied. With both control inputs applied simultaneously, the contact will close if set to "Operate-dominant" and will open if set to "Reset-dominant".

Application Example 1:

A latching output contact H1a is to be controlled from two user-programmable pushbuttons (buttons number 1 and 2). The following settings should be applied.

Program the Latching Outputs by making the following changes in the **SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS ⇨ CONTACT OUTPUT H1a** menu (assuming an H4L module):

OUTPUT H1a OPERATE: "PUSHBUTTON 1 ON"
OUTPUT H1a RESET: "PUSHBUTTON 2 ON"

Program the pushbuttons by making the following changes in the **PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE PUSHBUTTONS ⇨⇩ USER PUSHBUTTON 1** and **USER PUSHBUTTON 2** menus:

PUSHBUTTON 1 FUNCTION: "Self-reset"
PUSHBTN 1 DROP-OUT TIME: "0.00 s"

PUSHBUTTON 2 FUNCTION: "Self-reset"
PUSHBTN 2 DROP-OUT TIME: "0.00 s"

Application Example 2:

A relay, having two latching contacts H1a and H1c, is to be programmed. The H1a contact is to be a Type-a contact, while the H1c contact is to be a Type-b contact (Type-a means closed after exercising the operate input; Type-b means closed after exercising the reset input). The relay is to be controlled from virtual outputs: VO1 to operate and VO2 to reset.

Program the Latching Outputs by making the following changes in the **SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS ⇨ CONTACT OUTPUT H1a** and **CONTACT OUTPUT H1c** menus (assuming an H4L module):

OUTPUT H1a OPERATE: "VO1"
OUTPUT H1a RESET: "VO2"

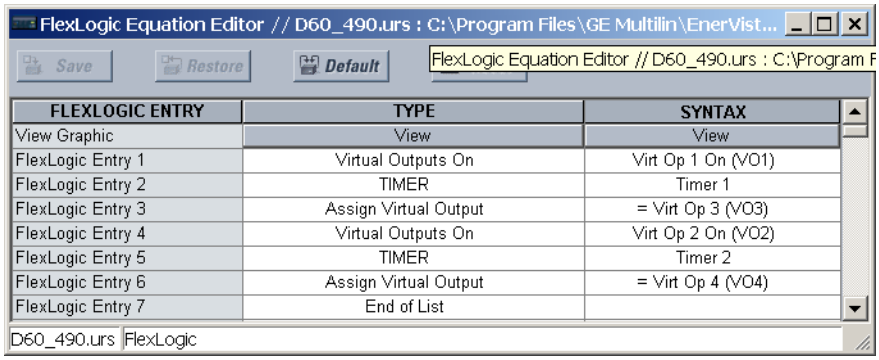
OUTPUT H1c OPERATE: "VO2"
OUTPUT H1c RESET: "VO1"

Since the two physical contacts in this example are mechanically separated and have individual control inputs, they will not operate at exactly the same time. A discrepancy in the range of a fraction of a maximum operating time may occur. Therefore, a pair of contacts programmed to be a multi-contact relay will not guarantee any specific sequence of operation (such as make before break). If required, the sequence of operation must be programmed explicitly by delaying some of the control inputs as shown in the next application example.

Application Example 3:

A make before break functionality must be added to the preceding example. An overlap of 20 ms is required to implement this functionality as described below:

Write the following FlexLogic™ equation (EnerVista UR Setup example shown):



Both timers (Timer 1 and Timer 2) should be set to 20 ms pickup and 0 ms dropout.

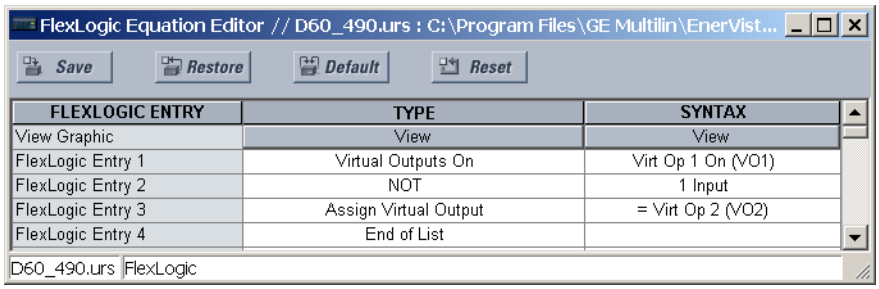
Program the Latching Outputs by making the following changes in the **SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS ⇨ CONTACT OUTPUT H1a** and **CONTACT OUTPUT H1c** menus (assuming an H4L module):

OUTPUT H1a OPERATE: "VO1"
OUTPUT H1a RESET: "VO4"
OUTPUT H1c OPERATE: "VO2"
OUTPUT H1c RESET: "VO3"

Application Example 4:

A latching contact H1a is to be controlled from a single virtual output VO1. The contact should stay closed as long as VO1 is high, and should stay opened when VO1 is low. Program the relay as follows.

Write the following FlexLogic™ equation (EnerVista UR Setup example shown):

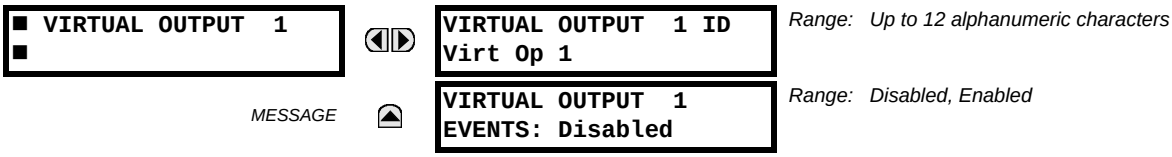


Program the Latching Outputs by making the following changes in the **SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ CONTACT OUTPUTS ⇨ CONTACT OUTPUT H1a** menu (assuming an H4L module):

OUTPUT H1a OPERATE: "VO1"
OUTPUT H1a RESET: "VO2"

5.7.4 VIRTUAL OUTPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ VIRTUAL OUTPUTS ⇨ VIRTUAL OUTPUT 1(96)



Range: Up to 12 alphanumeric characters

Range: Disabled, Enabled

There are 96 virtual outputs that may be assigned via FlexLogic™. If not assigned, the output will be forced to 'OFF' (Logic 0). An ID may be assigned to each virtual output. Virtual outputs are resolved in each pass through the evaluation of the FlexLogic™ equations. Any change of state of a virtual output can be logged as an event if programmed to do so.

For example, if Virtual Output 1 is the trip signal from FlexLogic™ and the trip relay is used to signal events, the settings would be programmed as follows:

VIRTUAL OUTPUT 1 ID: "Trip"
VIRTUAL OUTPUT 1 EVENTS: "Disabled"

5.7.5 REMOTE DEVICES

a) REMOTE INPUTS/OUTPUTS OVERVIEW

Remote inputs and outputs provide a means of exchanging digital state information between Ethernet-networked devices. The IEC 61850 GSSE (Generic Substation State Event) and GOOSE (Generic Object Oriented Substation Event) standards are used.

NOTE

The IEC 61850 specification requires that communications between devices be implemented on Ethernet. For UR-series relays, Ethernet communications is provided on all CPU modules except type 9E.

The sharing of digital point state information between GSSE/GOOSE equipped relays is essentially an extension to FlexLogic™, allowing distributed FlexLogic™ by making operands available to/from devices on a common communications network. In addition to digital point states, GSSE/GOOSE messages identify the originator of the message and provide other information required by the communication specification. All devices listen to network messages and capture data only from messages that have originated in selected devices.

IEC 61850 GSSE messages are compatible with UCA GOOSE messages and contain a fixed set of digital points. IEC 61850 GOOSE messages can, in general, contain any configurable data items. When used by the remote input/output feature, IEC 61850 GOOSE messages contain the same data as GSSE messages.

Both GSSE and GOOSE messages are designed to be short, reliable, and high priority. GOOSE messages have additional advantages over GSSE messages due to their support of VLAN (virtual LAN) and Ethernet priority tagging functionality. The GSSE message structure contains space for 128 bit pairs representing digital point state information. The IEC 61850 specification provides 32 “DNA” bit pairs that represent the state of two pre-defined events and 30 user-defined events. All remaining bit pairs are “UserSt” bit pairs, which are status bits representing user-definable events. The L60 implementation provides 32 of the 96 available UserSt bit pairs.

The IEC 61850 specification includes features that are used to cope with the loss of communication between transmitting and receiving devices. Each transmitting device will send a GSSE/GOOSE message upon a successful power-up, when the state of any included point changes, or after a specified interval (the *default update* time) if a change-of-state has not occurred. The transmitting device also sends a ‘hold time’ which is set greater than three times the programmed default time required by the receiving device.

Receiving devices are constantly monitoring the communications network for messages they require, as recognized by the identification of the originating device carried in the message. Messages received from remote devices include the message *time allowed to live*. The receiving relay sets a timer assigned to the originating device to this time interval, and if it has not received another message from this device at time-out, the remote device is declared to be non-communicating, so it will use the programmed default state for all points from that specific remote device. If a message is received from a remote device before the *time allowed to live* expires, all points for that device are updated to the states contained in the message and the hold timer is restarted. The status of a remote device, where “Offline” indicates non-communicating, can be displayed.

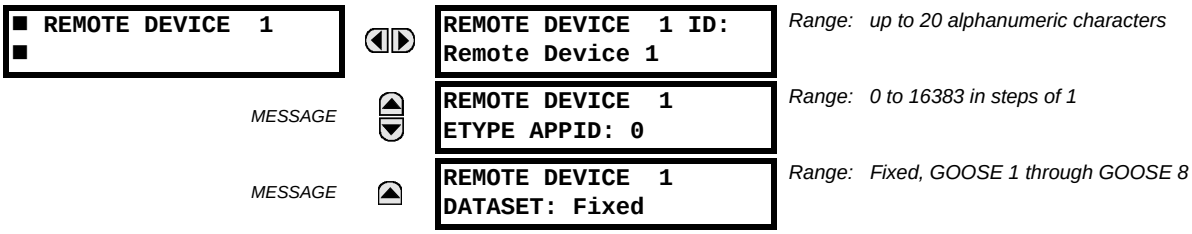
The remote input/output facility provides for 32 remote inputs and 64 remote outputs.

b) LOCAL DEVICES: DEVICE ID FOR TRANSMITTING GSSE MESSAGES

In a L60 relay, the device ID that identifies the originator of the message is programmed in the **SETTINGS ⇨ PRODUCT SETUP ⇨⇩ INSTALLATION ⇨⇩ RELAY NAME** setting.

c) REMOTE DEVICES: DEVICE ID FOR RECEIVING GSSE MESSAGES

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ REMOTE DEVICES ⇨ REMOTE DEVICE 1(16)



Remote devices are available for setting purposes. A receiving relay must be programmed to capture messages from only those originating remote devices of interest. This setting is used to select specific remote devices by entering (bottom row) the exact identification (ID) assigned to those devices.

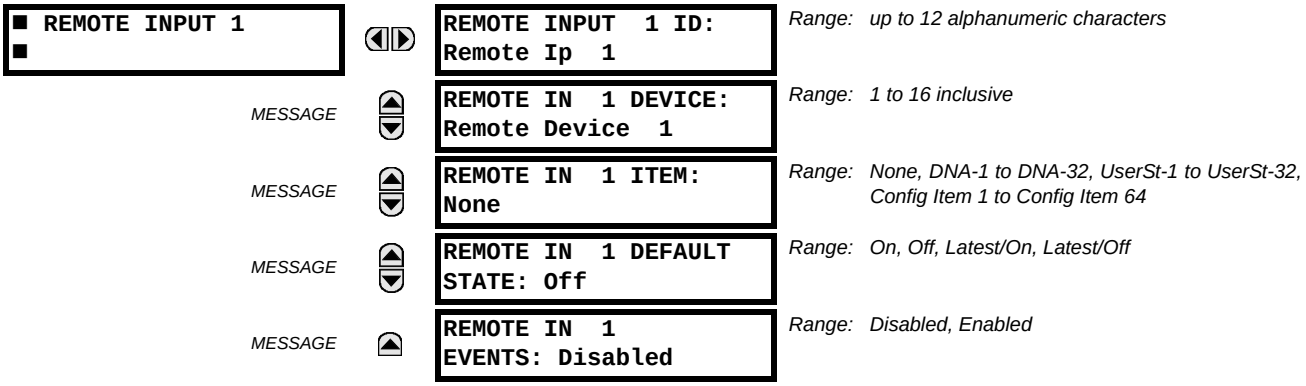
The **REMOTE DEVICE 1 ETYPE APPID** setting is only used with GOOSE messages; they are not applicable to GSSE messages. This setting identifies the Ethernet application identification in the GOOSE message. It should match the corresponding settings on the sending device.

The **REMOTE DEVICE 1 DATASET** setting provides for the choice of the L60 fixed (DNA/UserSt) dataset (that is, containing DNA and UserSt bit pairs), or one of the configurable datasets.

Note that the dataset for the received data items must be made up of existing items in an existing logical node. For this reason, logical node GGIO3 is instantiated to hold the incoming data items. GGIO3 is not necessary to make use of the received data. The remote input data item mapping takes care of the mapping of the inputs to remote input FlexLogic™ operands. However, GGIO3 data can be read by IEC 61850 clients.

5.7.6 REMOTE INPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ REMOTE INPUTS ⇨ REMOTE INPUT 1(32)



Remote Inputs that create FlexLogic™ operands at the receiving relay are extracted from GSSE/GOOSE messages originating in remote devices. Each remote input can be selected from a list consisting of 64 selections: DNA-1 through DNA-32 and UserSt-1 through UserSt-32. The function of DNA inputs is defined in the IEC 61850 specification and is presented in the IEC 61850 DNA Assignments table in the *Remote outputs* section. The function of UserSt inputs is defined by the user selection of the FlexLogic™ operand whose state is represented in the GSSE/GOOSE message. A user must program a DNA point from the appropriate FlexLogic™ operand.

Remote input 1 must be programmed to replicate the logic state of a specific signal from a specific remote device for local use. This programming is performed via the three settings shown above.

The **REMOTE INPUT 1 ID** setting allows the user to assign descriptive text to the remote input. The **REMOTE IN 1 DEVICE** setting selects the number (1 to 16) of the remote device which originates the required signal, as previously assigned to the remote device via the setting **REMOTE DEVICE 1(16) ID** (see the *Remote devices* section). The **REMOTE IN 1 ITEM** setting selects the specific bits of the GSSE/GOOSE message required.

The **REMOTE IN 1 DEFAULT STATE** setting selects the logic state for this point if the local relay has just completed startup or the remote device sending the point is declared to be non-communicating. The following choices are available:

- Setting **REMOTE IN 1 DEFAULT STATE** to "On" value defaults the input to logic 1.
- Setting **REMOTE IN 1 DEFAULT STATE** to "Off" value defaults the input to logic 0.
- Setting **REMOTE IN 1 DEFAULT STATE** to "Latest/On" freezes the input in case of lost communications. If the latest state is not known, such as after relay power-up but before the first communication exchange, the input will default to logic 1. When communication resumes, the input becomes fully operational.
- Setting **REMOTE IN 1 DEFAULT STATE** to "Latest/Off" freezes the input in case of lost communications. If the latest state is not known, such as after relay power-up but before the first communication exchange, the input will default to logic 0. When communication resumes, the input becomes fully operational.

NOTE

For additional information on GSSE/GOOOSE messaging, refer to the *Remote devices* section in this chapter.

5.7.7 REMOTE OUTPUTS

a) DNA BIT PAIRS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ REMOTE OUTPUTS DNA BIT PAIRS ⇨ REMOTE OUPUTS DNA- 1(32) BIT PAIR

```
■ REMOTE OUTPUTS
■ DNA- 1 BIT PAIR
```

MESSAGE

```
DNA- 1 OPERAND:
Off
```

Range: FlexLogic™ operand

```
DNA- 1 EVENTS:
Disabled
```

Range: Disabled, Enabled

Remote outputs (1 to 32) are FlexLogic™ operands inserted into GSSE/GOOSE messages that are transmitted to remote devices on a LAN. Each digital point in the message must be programmed to carry the state of a specific FlexLogic™ operand. The above operand setting represents a specific DNA function (as shown in the following table) to be transmitted.

Table 5–26: IEC 61850 DNA ASSIGNMENTS

DNA	IEC 61850 DEFINITION	FLEXLOGIC™ OPERAND
1	Test	IEC 61850 TEST MODE
2	ConfRev	IEC 61850 CONF REV

b) USERST BIT PAIRS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ REMOTE OUTPUTS UserSt BIT PAIRS ⇨ REMOTE OUTPUTS UserSt- 1(32) BIT PAIR

```
■ REMOTE OUTPUTS
■ UserSt- 1 BIT PAIR
```

MESSAGE

```
UserSt- 1 OPERAND:
Off
```

Range: FlexLogic™ operand

```
UserSt- 1 EVENTS:
Disabled
```

Range: Disabled, Enabled

Remote outputs 1 to 32 originate as GSSE/GOOSE messages to be transmitted to remote devices. Each digital point in the message must be programmed to carry the state of a specific FlexLogic™ operand. The setting above is used to select the operand which represents a specific UserSt function (as selected by the user) to be transmitted.

The following setting represents the time between sending GSSE/GOOSE messages when there has been no change of state of any selected digital point. This setting is located in the **PRODUCT SETUP ⇨⇩ COMMUNICATIONS ⇨⇩ IEC 61850 PROTOCOL ⇨⇩ GSSE/GOOSE CONFIGURATION** settings menu.

```
DEFAULT GSSE/GOOSE
UPDATE TIME: 60 s
```

Range: 1 to 60 s in steps of 1

NOTE

For more information on GSSE/GOOSE messaging, refer to *Remote Inputs/Outputs Overview* in the *Remote Devices* section.

5.7.8 RESETTING

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ RESETTING

Range: FlexLogic™ operand

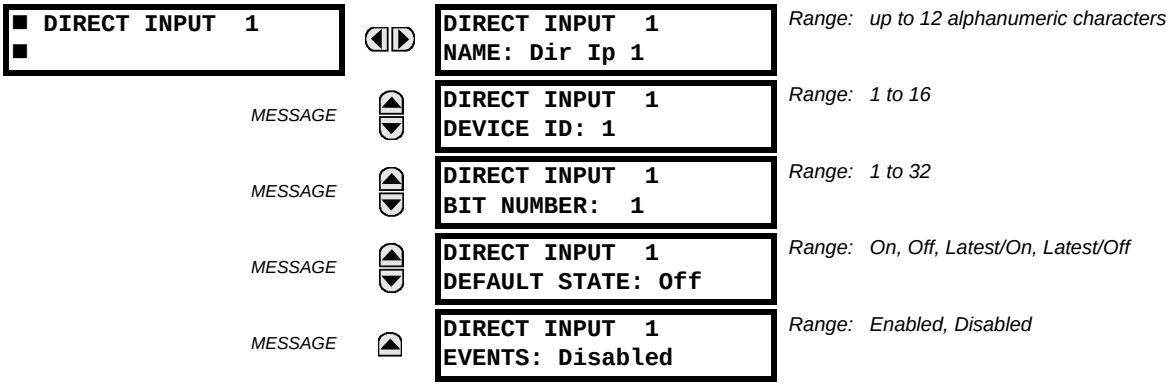
Some events can be programmed to latch the faceplate LED event indicators and the target message on the display. Once set, the latching mechanism will hold all of the latched indicators or messages in the set state after the initiating condition has cleared until a RESET command is received to return these latches (not including FlexLogic™ latches) to the reset state. The RESET command can be sent from the faceplate Reset button, a remote device via a communications channel, or any programmed operand.

When the RESET command is received by the relay, two FlexLogic™ operands are created. These operands, which are stored as events, reset the latches if the initiating condition has cleared. The three sources of RESET commands each create the RESET OP FlexLogic™ operand. Each individual source of a RESET command also creates its individual operand RESET OP (PUSHBUTTON), RESET OP (COMMS) or RESET OP (OPERAND) to identify the source of the command. The setting shown above selects the operand that will create the RESET OP (OPERAND) operand.

5.7.9 DIRECT INPUTS/OUTPUTS

a) DIRECT INPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ DIRECT INPUTS ⇨ DIRECT INPUT 1(32)



Range: up to 12 alphanumeric characters

Range: 1 to 16

Range: 1 to 32

Range: On, Off, Latest/On, Latest/Off

Range: Enabled, Disabled

These settings specify how the direct input information is processed. The **DIRECT INPUT 1 NAME** setting allows the user to assign a descriptive name to the direct input. The **DIRECT INPUT 1 DEVICE ID** represents the source of direct input 1. The specified direct input is driven by the device identified here.

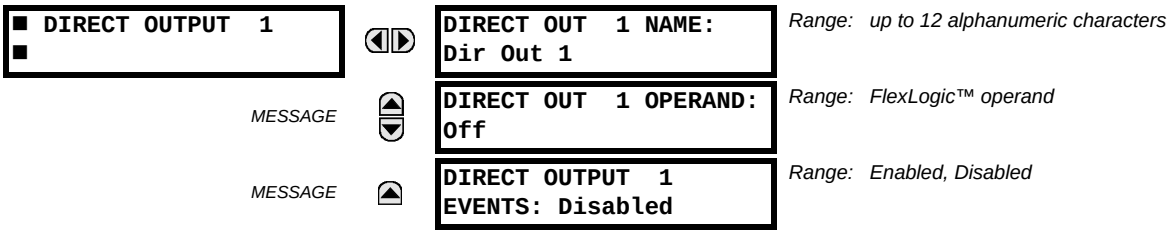
The **DIRECT INPUT 1 BIT NUMBER** is the bit number to extract the state for direct input 1. Direct Input 1 is driven by the bit identified as **DIRECT INPUT 1 BIT NUMBER**. This corresponds to the direct output number of the sending device.

The **DIRECT INPUT 1 DEFAULT STATE** represents the state of the direct input when the associated direct device is offline. The following choices are available:

- Setting **DIRECT INPUT 1 DEFAULT STATE** to "On" value defaults the input to Logic 1.
- Setting **DIRECT INPUT 1 DEFAULT STATE** to "Off" value defaults the input to Logic 0.
- Setting **DIRECT INPUT 1 DEFAULT STATE** to "Latest/On" freezes the input in case of lost communications. If the latest state is not known, such as after relay power-up but before the first communication exchange, the input will default to Logic 1. When communication resumes, the input becomes fully operational.
- Setting **DIRECT INPUT 1 DEFAULT STATE** to "Latest/Off" freezes the input in case of lost communications. If the latest state is not known, such as after relay power-up but before the first communication exchange, the input will default to Logic 0. When communication resumes, the input becomes fully operational.

b) DIRECT OUTPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ DIRECT OUTPUTS ⇨ DIRECT OUTPUT 1(32)



The **DIRECT OUT 1 NAME** setting allows the user to assign a descriptive name to the direct output. The **DIR OUT 1 OPERAND** is the FlexLogic™ operand that determines the state of this direct output.

c) APPLICATION EXAMPLES

The examples introduced in the earlier *Direct Inputs/Outputs* section (part of the *Product Setup* section) direct inputs/outputs are continued below to illustrate usage of the direct inputs and outputs.

EXAMPLE 1: EXTENDING INPUT/OUTPUT CAPABILITIES OF A L60 RELAY

Consider an application that requires additional quantities of digital inputs and/or output contacts and/or lines of programmable logic that exceed the capabilities of a single UR-series chassis. The problem is solved by adding an extra UR-series IED, such as the C30, to satisfy the additional inputs/outputs and programmable logic requirements. The two IEDs are connected via single-channel digital communication cards as shown below.

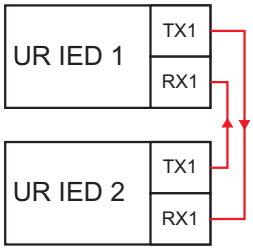


Figure 5–131: INPUT/OUTPUT EXTENSION VIA DIRECT INPUTS/OUTPUTS

Assume contact input 1 from UR IED 2 is to be used by UR IED 1. The following settings should be applied (Direct Input 5 and bit number 12 are used, as an example):

UR IED 1: **DIRECT INPUT 5 DEVICE ID** = "2"
DIRECT INPUT 5 BIT NUMBER = "12"

UR IED 2: **DIRECT OUT 12 OPERAND** = "Cont Ip 1 On"

The Cont Ip 1 On operand of UR IED 2 is now available in UR IED 1 as DIRECT INPUT 5 ON.

EXAMPLE 2: INTERLOCKING BUSBAR PROTECTION

A simple interlocking busbar protection scheme can be accomplished by sending a blocking signal from downstream devices, say 2, 3 and 4, to the upstream device that monitors a single incomer of the busbar, as shown in the figure below.

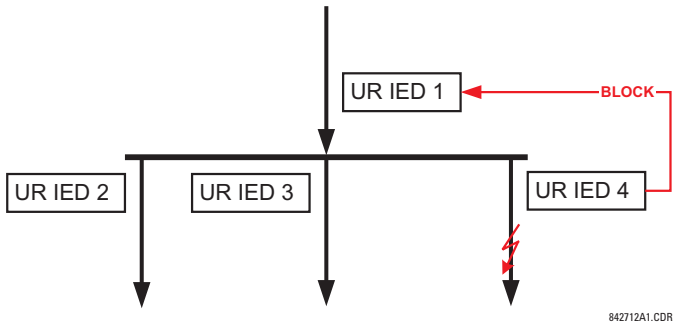


Figure 5–132: SAMPLE INTERLOCKING BUSBAR PROTECTION SCHEME

Assume that Phase Instantaneous Overcurrent 1 is used by Devices 2, 3, and 4 to block Device 1. If not blocked, Device 1 would trip the bus upon detecting a fault and applying a short coordination time delay.

The following settings should be applied (assume Bit 3 is used by all 3 devices to sent the blocking signal and Direct Inputs 7, 8, and 9 are used by the receiving device to monitor the three blocking signals):

UR IED 2: **DIRECT OUT 3 OPERAND**: "PHASE IOC1 OP"

UR IED 3: **DIRECT OUT 3 OPERAND**: "PHASE IOC1 OP"

UR IED 4: **DIRECT OUT 3 OPERAND**: "PHASE IOC1 OP"

UR IED 1: **DIRECT INPUT 7 DEVICE ID**: "2"
DIRECT INPUT 7 BIT NUMBER: "3"
DIRECT INPUT 7 DEFAULT STATE: select "On" for security, select "Off" for dependability

DIRECT INPUT 8 DEVICE ID: "3"
DIRECT INPUT 8 BIT NUMBER: "3"
DIRECT INPUT 8 DEFAULT STATE: select "On" for security, select "Off" for dependability

DIRECT INPUT 9 DEVICE ID: "4"
DIRECT INPUT 9 BIT NUMBER: "3"
DIRECT INPUT 9 DEFAULT STATE: select "On" for security, select "Off" for dependability

Now the three blocking signals are available in UR IED 1 as DIRECT INPUT 7 ON, DIRECT INPUT 8 ON, and DIRECT INPUT 9 ON. Upon losing communications or a device, the scheme is inclined to block (if any default state is set to “On”), or to trip the bus on any overcurrent condition (all default states set to “Off”).

5

EXAMPLE 2: PILOT-AIDED SCHEMES

Consider a three-terminal line protection application shown in the figure below.

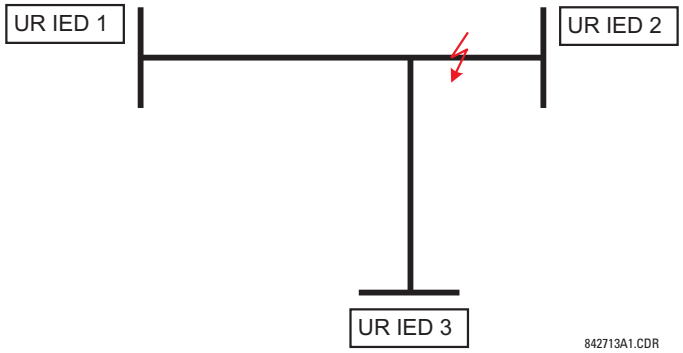


Figure 5–133: THREE-TERMINAL LINE APPLICATION

Assume the Hybrid Permissive Overreaching Transfer Trip (Hybrid POTT) scheme is applied using the architecture shown below. The scheme output operand HYB POTT TX1 is used to key the permission.

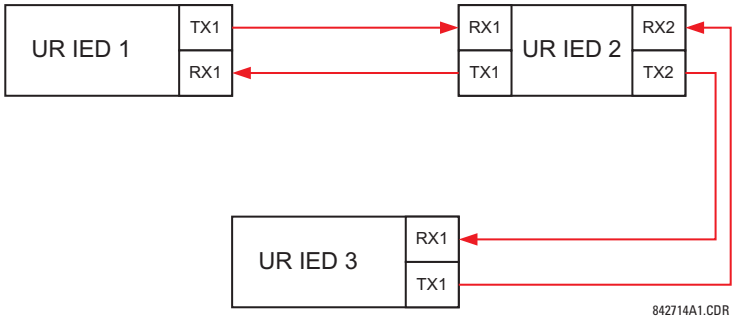


Figure 5–134: SINGLE-CHANNEL OPEN-LOOP CONFIGURATION

In the above architecture, Devices 1 and 3 do not communicate directly. Therefore, Device 2 must act as a 'bridge'. The following settings should be applied:

UR IED 1:
DIRECT OUT 2 OPERAND: "HYB POTT TX1"
DIRECT INPUT 5 DEVICE ID: "2"
DIRECT INPUT 5 BIT NUMBER: "2" (this is a message from IED 2)
DIRECT INPUT 6 DEVICE ID: "2"
DIRECT INPUT 6 BIT NUMBER: "4" (effectively, this is a message from IED 3)

UR IED 3:
DIRECT OUT 2 OPERAND: "HYB POTT TX1"
DIRECT INPUT 5 DEVICE ID: "2"
DIRECT INPUT 5 BIT NUMBER: "2" (this is a message from IED 2)
DIRECT INPUT 6 DEVICE ID: "2"
DIRECT INPUT 6 BIT NUMBER: "3" (effectively, this is a message from IED 1)

UR IED 2:
DIRECT INPUT 5 DEVICE ID: "1"
DIRECT INPUT 5 BIT NUMBER: "2"
DIRECT INPUT 6 DEVICE ID: "3"
DIRECT INPUT 6 BIT NUMBER: "2"
DIRECT OUT 2 OPERAND: "HYB POTT TX1"
DIRECT OUT 3 OPERAND: "DIRECT INPUT 5" (forward a message from 1 to 3)
DIRECT OUT 4 OPERAND: "DIRECT INPUT 6" (forward a message from 3 to 1)

Signal flow between the three IEDs is shown in the figure below:

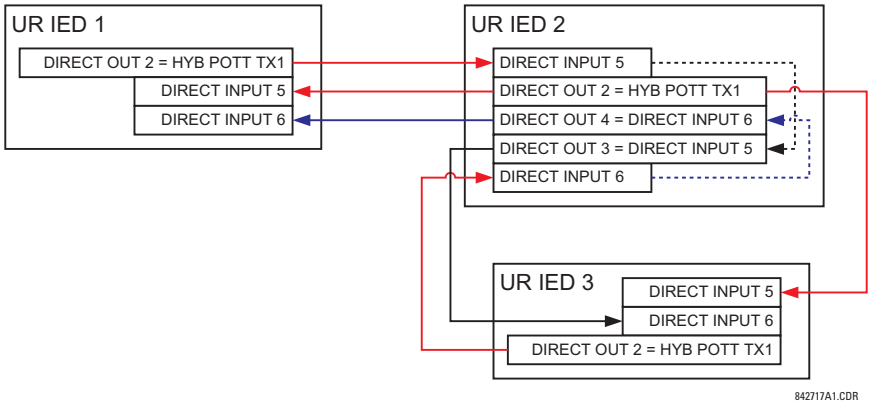


Figure 5–135: SIGNAL FLOW FOR DIRECT INPUT/OUTPUT EXAMPLE 3

In three-terminal applications, both the remote terminals must grant permission to trip. Therefore, at each terminal, Direct Inputs 5 and 6 should be ANDed in FlexLogic™ and the resulting operand configured as the permission to trip (**HYB POTT RX1** setting).

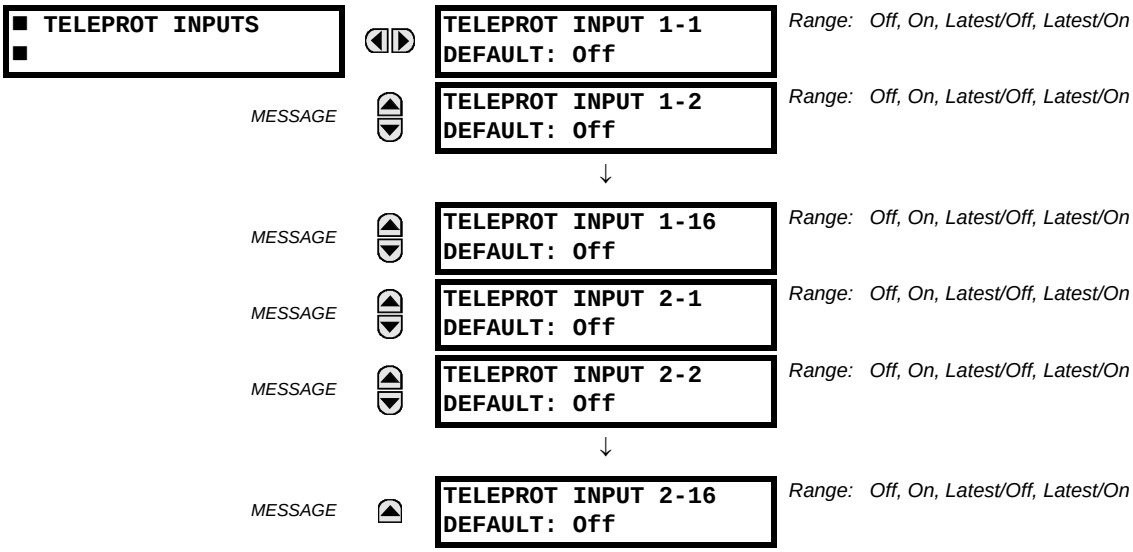
5.7.10 TELEPROTECTION INPUTS/OUTPUTS

a) OVERVIEW

The relay provides sixteen teleprotection inputs on communications channel 1 (numbered 1-1 through 1-16) and sixteen teleprotection inputs on communications channel 2 (on two-terminals two-channel and three-terminal systems only, numbered 2-1 through 2-16). The remote relay connected to channels 1 and 2 of the local relay is programmed by assigning FlexLogic™ operands to be sent via the selected communications channel. This allows the user to create distributed protection and control schemes via dedicated communications channels. Some examples are directional comparison pilot schemes and direct transfer tripping. It should be noted that failures of communications channels will affect teleprotection functionality. The teleprotection function must be enabled to utilize the inputs.

b) TELEPROTECTION INPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ TELEPROTECTION ⇨ TELEPROT INPUTS

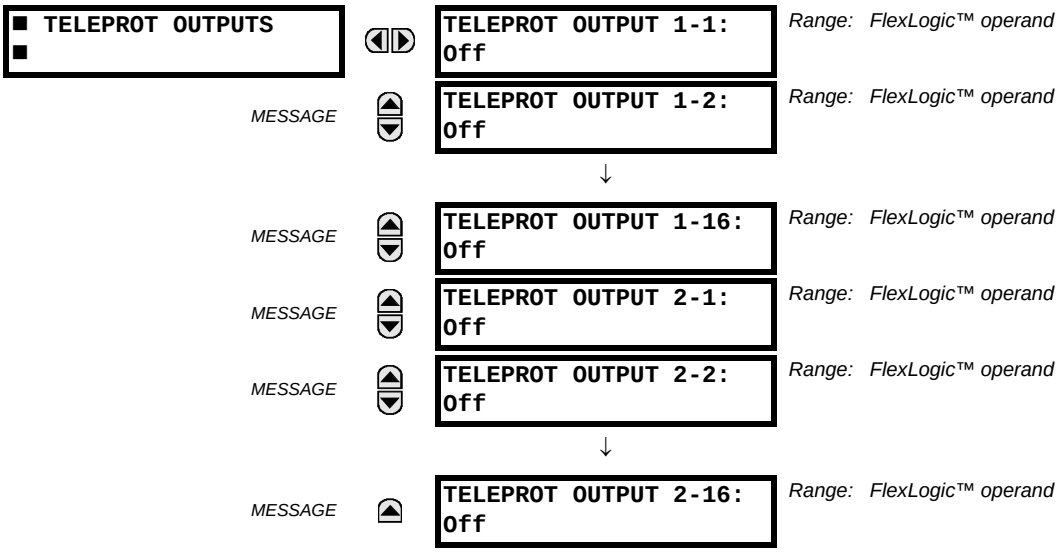


Setting the **TELEPROT INPUT ~~ DEFAULT** setting to "On" defaults the input to logic 1 when the channel fails. A value of "Off" defaults the input to logic 0 when the channel fails.

The "Latest/On" and "Latest/Off" values freeze the input in case of lost communications. If the latest state is not known, such as after relay power-up but before the first communication exchange, then the input defaults to logic 1 for "Latest/On" and logic 0 for "Latest/Off".

c) TELEPROTECTION OUTPUTS

PATH: SETTINGS ⇨⇩ INPUTS/OUTPUTS ⇨⇩ TELEPROTECTION ⇨⇩ TELEPROT OUTPUTS



As the following figure demonstrates, processing of the teleprotection inputs/outputs is dependent on the number of communication channels and terminals. On two-terminal two-channel systems, they are processed continuously on each channel and mapped separately per channel. Therefore, to achieve redundancy, the user must assign the same operand on both channels (teleprotection outputs at the sending end or corresponding teleprotection inputs at the receiving end). On three-terminal two-channel systems, redundancy is achieved by programming signal re-transmittal in the case of channel failure between any pair of relays.

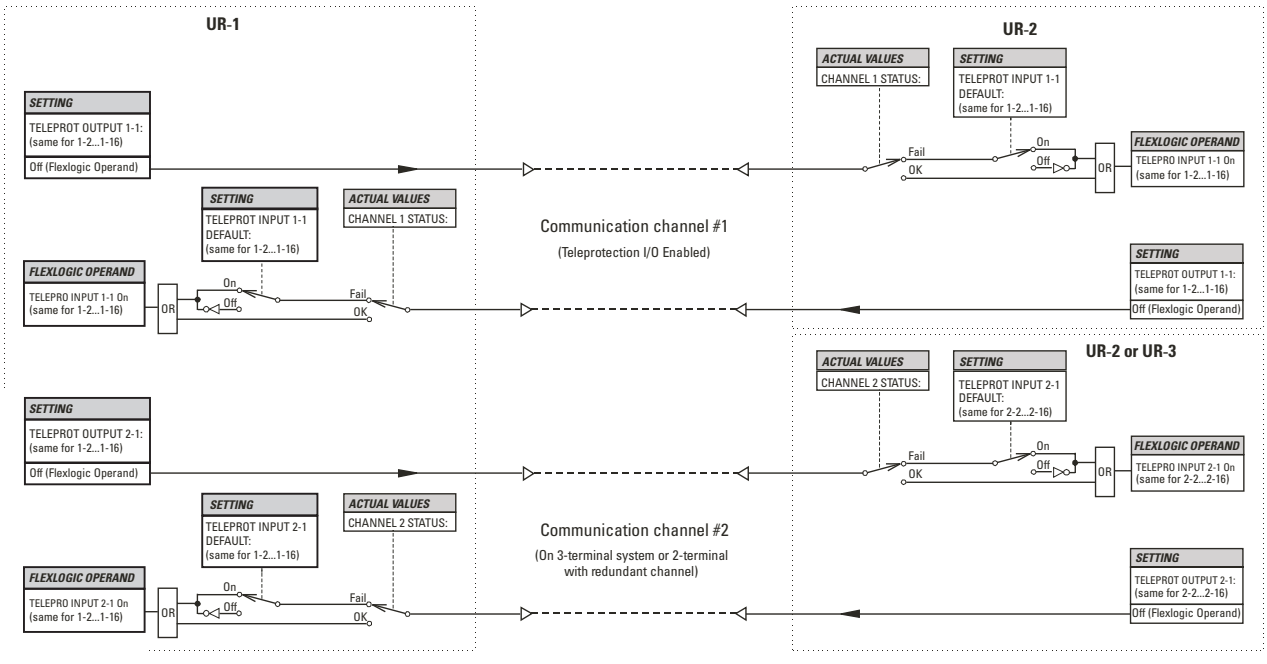
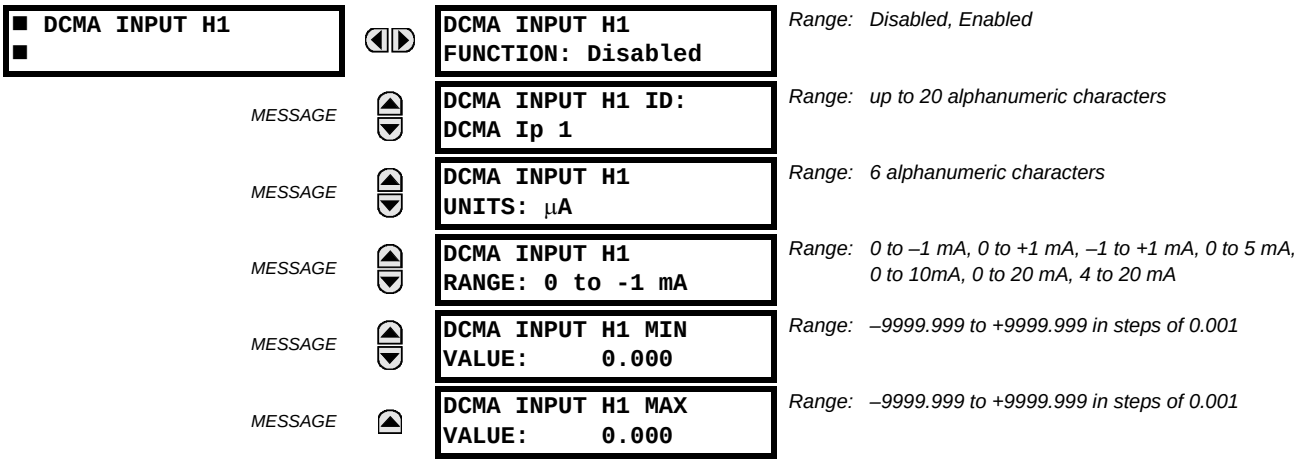


Figure 5–136: TELEPROTECTION INPUT/OUTPUT PROCESSING

5.8.1 DCMA INPUTS

PATH: SETTINGS ⇨⇩ TRANSDUCER I/O ⇨⇩ DCMA INPUTS ⇨ DCMA INPUT H1(W8)



Hardware and software is provided to receive signals from external transducers and convert these signals into a digital format for use as required. The relay will accept inputs in the range of –1 to +20 mA DC, suitable for use with most common transducer output ranges; all inputs are assumed to be linear over the complete range. Specific hardware details are contained in chapter 3.

Before the dcmA input signal can be used, the value of the signal measured by the relay must be converted to the range and quantity of the external transducer primary input parameter, such as DC voltage or temperature. The relay simplifies this process by internally scaling the output from the external transducer and displaying the actual primary parameter.

dcmA input channels are arranged in a manner similar to CT and VT channels. The user configures individual channels with the settings shown here.

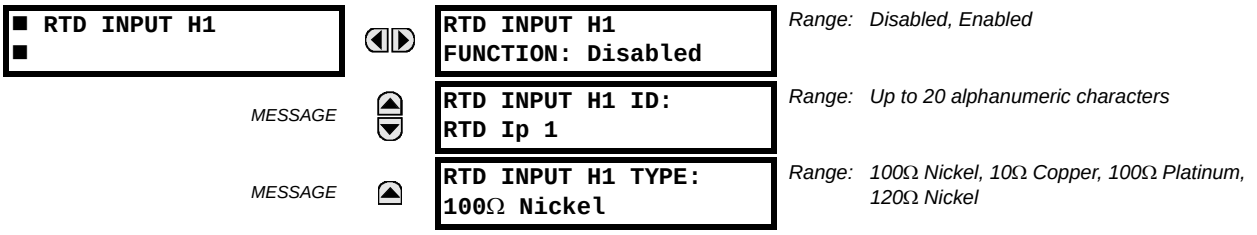
The channels are arranged in sub-modules of two channels, numbered from 1 through 8 from top to bottom. On power-up, the relay will automatically generate configuration settings for every channel, based on the order code, in the same general manner that is used for CTs and VTs. Each channel is assigned a slot letter followed by the row number, 1 through 8 inclusive, which is used as the channel number. The relay generates an actual value for each available input channel.

Settings are automatically generated for every channel available in the specific relay as shown above for the first channel of a type 5F transducer module installed in slot H.

The function of the channel may be either “Enabled” or “Disabled”. If “Disabled”, no actual values are created for the channel. An alphanumeric “ID” is assigned to each channel; this ID will be included in the channel actual value, along with the programmed units associated with the parameter measured by the transducer, such as volts, °C, megawatts, etc. This ID is also used to reference the channel as the input parameter to features designed to measure this type of parameter. The **DCMA INPUT H1 RANGE** setting specifies the mA DC range of the transducer connected to the input channel.

The **DCMA INPUT H1 MIN VALUE** and **DCMA INPUT H1 MAX VALUE** settings are used to program the span of the transducer in primary units. For example, a temperature transducer might have a span from 0 to 250°C; in this case the **DCMA INPUT H1 MIN VALUE** value is “0” and the **DCMA INPUT H1 MAX VALUE** value is “250”. Another example would be a watts transducer with a span from –20 to +180 MW; in this case the **DCMA INPUT H1 MIN VALUE** value would be “–20” and the **DCMA INPUT H1 MAX VALUE** value “180”. Intermediate values between the min and max values are scaled linearly.

PATH: SETTINGS ⇨⇩ TRANSDUCER I/O ⇨⇩ RTD INPUTS ⇨ RTD INPUT H1(W8)



Hardware and software is provided to receive signals from external resistance temperature detectors and convert these signals into a digital format for use as required. These channels are intended to be connected to any of the RTD types in common use. Specific hardware details are contained in chapter 3.

RTD input channels are arranged in a manner similar to CT and VT channels. The user configures individual channels with the settings shown here.

The channels are arranged in sub-modules of two channels, numbered from 1 through 8 from top to bottom. On power-up, the relay will automatically generate configuration settings for every channel, based on the order code, in the same general manner that is used for CTs and VTs. Each channel is assigned a slot letter followed by the row number, 1 through 8 inclusive, which is used as the channel number. The relay generates an actual value for each available input channel.

Settings are automatically generated for every channel available in the specific relay as shown above for the first channel of a type 5C transducer module installed in the first available slot.

The function of the channel may be either “Enabled” or “Disabled”. If “Disabled”, there will not be an actual value created for the channel. An alphanumeric ID is assigned to the channel; this ID will be included in the channel actual values. It is also used to reference the channel as the input parameter to features designed to measure this type of parameter. Selecting the type of RTD connected to the channel configures the channel.

Actions based on RTD overtemperature, such as trips or alarms, are done in conjunction with the FlexElements™ feature. In FlexElements™, the operate level is scaled to a base of 100°C. For example, a trip level of 150°C is achieved by setting the operate level at 1.5 pu. FlexElement™ operands are available to FlexLogic™ for further interlocking or to operate an output contact directly.

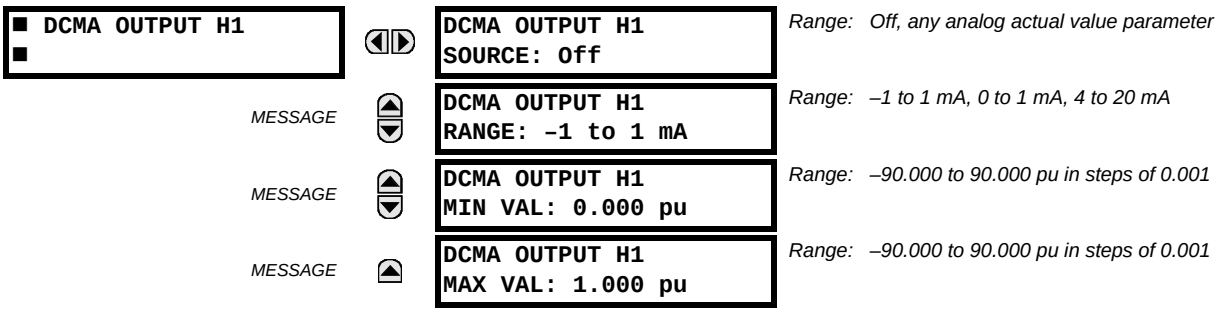
Refer to the following table for reference temperature values for each RTD type.

Table 5–27: RTD TEMPERATURE VS. RESISTANCE

TEMPERATURE		RESISTANCE (IN OHMS)			
°C	°F	100 W PT (DIN 43760)	120 W NI	100 W NI	10 W CU
–50	–58	80.31	86.17	71.81	7.10
–40	–40	84.27	92.76	77.30	7.49
–30	–22	88.22	99.41	82.84	7.88
–20	–4	92.16	106.15	88.45	8.26
–10	14	96.09	113.00	94.17	8.65
0	32	100.00	120.00	100.00	9.04
10	50	103.90	127.17	105.97	9.42
20	68	107.79	134.52	112.10	9.81
30	86	111.67	142.06	118.38	10.19
40	104	115.54	149.79	124.82	10.58
50	122	119.39	157.74	131.45	10.97
60	140	123.24	165.90	138.25	11.35
70	158	127.07	174.25	145.20	11.74
80	176	130.89	182.84	152.37	12.12
90	194	134.70	191.64	159.70	12.51
100	212	138.50	200.64	167.20	12.90
110	230	142.29	209.85	174.87	13.28
120	248	146.06	219.29	182.75	13.67
130	266	149.82	228.96	190.80	14.06
140	284	153.58	238.85	199.04	14.44
150	302	157.32	248.95	207.45	14.83
160	320	161.04	259.30	216.08	15.22
170	338	164.76	269.91	224.92	15.61
180	356	168.47	280.77	233.97	16.00
190	374	172.46	291.96	243.30	16.39
200	392	175.84	303.46	252.88	16.78
210	410	179.51	315.31	262.76	17.17
220	428	183.17	327.54	272.94	17.56
230	446	186.82	340.14	283.45	17.95
240	464	190.45	353.14	294.28	18.34
250	482	194.08	366.53	305.44	18.73

5.8.3 DCMA OUTPUTS

PATH: SETTINGS ⇨⇩ TRANSDUCER I/O ⇨⇩ DCMA OUTPUTS ⇨ DCMA OUTPUT H1(W8)



Hardware and software is provided to generate dcmA signals that allow interfacing with external equipment. Specific hardware details are contained in chapter 3. The dcmA output channels are arranged in a manner similar to transducer input or CT and VT channels. The user configures individual channels with the settings shown below.

The channels are arranged in sub-modules of two channels, numbered 1 through 8 from top to bottom. On power-up, the relay automatically generates configuration settings for every channel, based on the order code, in the same manner used for CTs and VTs. Each channel is assigned a slot letter followed by the row number, 1 through 8 inclusive, which is used as the channel number.

Both the output range and a signal driving a given output are user-programmable via the following settings menu (an example for channel M5 is shown).

The relay checks the driving signal (x in equations below) for the minimum and maximum limits, and subsequently re-scales so the limits defined as **MIN VAL** and **MAX VAL** match the output range of the hardware defined as **RANGE**. The following equation is applied:

$$I_{out} = \begin{cases} I_{min} & \text{if } x < \textbf{MIN VAL} \\ I_{max} & \text{if } x > \textbf{MAX VAL} \\ k(x - \textbf{MIN VAL}) + I_{min} & \text{otherwise} \end{cases} \quad \textbf{(EQ 5.28)}$$

where: x is a driving signal specified by the **SOURCE** setting
I_{min} and I_{max} are defined by the **RANGE** setting
k is a scaling constant calculated as:

$$k = \frac{I_{max} - I_{min}}{\textbf{MAX VAL} - \textbf{MIN VAL}} \quad \textbf{(EQ 5.29)}$$

The feature is intentionally inhibited if the **MAX VAL** and **MIN VAL** settings are entered incorrectly, e.g. when **MAX VAL** – **MIN VAL** < 0.1 pu. The resulting characteristic is illustrated in the following figure.

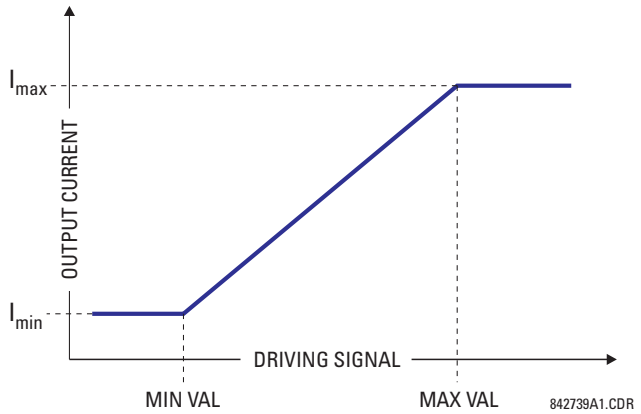


Figure 5–137: DCMA OUTPUT CHARACTERISTIC

The dcmA output settings are described below.

- **DCMA OUTPUT H1 SOURCE**: This setting specifies an internal analog value to drive the analog output. Actual values (FlexAnalog parameters) such as power, current amplitude, voltage amplitude, power factor, etc. can be configured as sources driving dcmA outputs. Refer to Appendix A for a complete list of FlexAnalog parameters.
- **DCMA OUTPUT H1 RANGE**: This setting allows selection of the output range. Each dcmA channel may be set independently to work with different ranges. The three most commonly used output ranges are available.
- **DCMA OUTPUT H1 MIN VAL**: This setting allows setting the minimum limit for the signal that drives the output. This setting is used to control the mapping between an internal analog value and the output current (see the following examples). The setting is entered in per-unit values. The base units are defined in the same manner as the FlexElement™ base units.
- **DCMA OUTPUT H1 MAX VAL**: This setting allows setting the maximum limit for the signal that drives the output. This setting is used to control the mapping between an internal analog value and the output current (see the following

examples). The setting is entered in per-unit values. The base units are defined in the same manner as the FlexElement™ base units.

NOTE

The **DCMA OUTPUT H1 MIN VAL** and **DCMA OUTPUT H1 MAX VAL** settings are ignored for power factor base units (i.e. if the **DCMA OUTPUT H1 SOURCE** is set to FlexAnalog value based on power factor measurement).

Three application examples are described below.

EXAMPLE 1:

A three phase active power on a 13.8 kV system measured via UR-series relay source 1 is to be monitored by the dcmA H1 output of the range of –1 to 1 mA. The following settings are applied on the relay: CT ratio = 1200:5, VT secondary 115, VT connection is delta, and VT ratio = 120. The nominal current is 800 A primary and the nominal power factor is 0.90. The power is to be monitored in both importing and exporting directions and allow for 20% overload compared to the nominal.

The nominal three-phase power is:

$$P = \sqrt{3} \times 13.8 \text{ kV} \times 0.8 \text{ kA} \times 0.9 = 17.21 \text{ MW} \quad \textbf{(EQ 5.30)}$$

The three-phase power with 20% overload margin is:

$$P_{max} = 1.2 \times 17.21 \text{ MW} = 20.65 \text{ MW} \quad \textbf{(EQ 5.31)}$$

The base unit for power (refer to the FlexElements section in this chapter for additional details) is:

$$P_{BASE} = 115 \text{ V} \times 120 \times 1.2 \text{ kA} = 16.56 \text{ MW} \quad \textbf{(EQ 5.32)}$$

The minimum and maximum power values to be monitored (in pu) are:

$$\text{minimum power} = \frac{-20.65 \text{ MW}}{16.56 \text{ MW}} = -1.247 \text{ pu}, \quad \text{maximum power} = \frac{20.65 \text{ MW}}{16.56 \text{ MW}} = 1.247 \text{ pu} \quad \textbf{(EQ 5.33)}$$

The following settings should be entered:

DCMA OUTPUT H1 SOURCE: “SRC 1 P”
DCMA OUTPUT H1 RANGE: “–1 to 1 mA”
DCMA OUTPUT H1 MIN VAL: “–1.247 pu”
DCMA OUTPUT H1 MAX VAL: “1.247 pu”

With the above settings, the output will represent the power with the scale of 1 mA per 20.65 MW. The worst-case error for this application can be calculated by superimposing the following two sources of error:

- ±0.5% of the full scale for the analog output module, or $\pm 0.005 \times (1 - (-1)) \times 20.65 \text{ MW} = \pm 0.207 \text{ MW}$
- ±1% of reading error for the active power at power factor of 0.9

For example at the reading of 20 MW, the worst-case error is 0.01 × 20 MW + 0.207 MW = 0.407 MW.

EXAMPLE 2:

The phase A current (true RMS value) is to be monitored via the H2 current output working with the range from 4 to 20 mA. The CT ratio is 5000:5 and the maximum load current is 4200 A. The current should be monitored from 0 A upwards, allowing for 50% overload.

The phase current with the 50% overload margin is:

$$I_{max} = 1.5 \times 4.2 \text{ kA} = 6.3 \text{ kA} \quad \textbf{(EQ 5.34)}$$

The base unit for current (refer to the FlexElements section in this chapter for additional details) is:

$$I_{BASE} = 5 \text{ kA} \quad \textbf{(EQ 5.35)}$$

The minimum and maximum power values to be monitored (in pu) are:

$$\text{minimum current} = \frac{0 \text{ kA}}{5 \text{ kA}} = 0 \text{ pu}, \quad \text{maximum current} = \frac{6.3 \text{ kA}}{5 \text{ kA}} = 1.26 \text{ pu} \quad \textbf{(EQ 5.36)}$$

The following settings should be entered:

DCMA OUTPUT H2 SOURCE: "SRC 1 Ia RMS"
DCMA OUTPUT H2 RANGE: "4 to 20 mA"
DCMA OUTPUT H2 MIN VAL: "0.000 pu"
DCMA OUTPUT H2 MAX VAL: "1.260 pu"

The worst-case error for this application could be calculated by superimposing the following two sources of error:

- ±0.5% of the full scale for the analog output module, or $\pm 0.005 \times (20 - 4) \times 6.3 \text{ kA} = \pm 0.504 \text{ kA}$
- ±0.25% of reading or ±0.1% of rated (whichever is greater) for currents between 0.1 and 2.0 of nominal

For example, at the reading of 4.2 kA, the worst-case error is max(0.0025 × 4.2 kA, 0.001 × 5 kA) + 0.504 kA = 0.515 kA.

EXAMPLE 3:

A positive-sequence voltage on a 400 kV system measured via Source 2 is to be monitored by the dcmA H3 output with a range of 0 to 1 mA. The VT secondary setting is 66.4 V, the VT ratio setting is 6024, and the VT connection setting is "Delta". The voltage should be monitored in the range from 70% to 110% of nominal.

The minimum and maximum positive-sequence voltages to be monitored are:

$$V_{min} = 0.7 \times \frac{400 \text{ kV}}{\sqrt{3}} = 161.66 \text{ kV}, \quad V_{max} = 1.1 \times \frac{400 \text{ kV}}{\sqrt{3}} = 254.03 \text{ kV} \qquad \textbf{(EQ 5.37)}$$

The base unit for voltage (refer to the FlexElements section in this chapter for additional details) is:

$$V_{BASE} = 0.0664 \text{ kV} \times 6024 = 400 \text{ kV} \qquad \textbf{(EQ 5.38)}$$

The minimum and maximum voltage values to be monitored (in pu) are:

$$\text{minimum voltage} = \frac{161.66 \text{ kV}}{400 \text{ kV}} = 0.404 \text{ pu}, \quad \text{maximum voltage} = \frac{254.03 \text{ kV}}{400 \text{ kV}} = 0.635 \text{ pu} \qquad \textbf{(EQ 5.39)}$$

The following settings should be entered:

DCMA OUTPUT H3 SOURCE: "SRC 2 V_1 mag"
DCMA OUTPUT H3 RANGE: "0 to 1 mA"
DCMA OUTPUT H3 MIN VAL: "0.404 pu"
DCMA OUTPUT H3 MAX VAL: "0.635 pu"

The limit settings differ from the expected 0.7 pu and 1.1 pu because the relay calculates the positive-sequence quantities scaled to the phase-to-ground voltages, even if the VTs are connected in "Delta" (refer to the *Metering Conventions* section in Chapter 6), while at the same time the VT nominal voltage is 1 pu for the settings. Consequently the settings required in this example differ from naturally expected by the factor of $\sqrt{3}$.

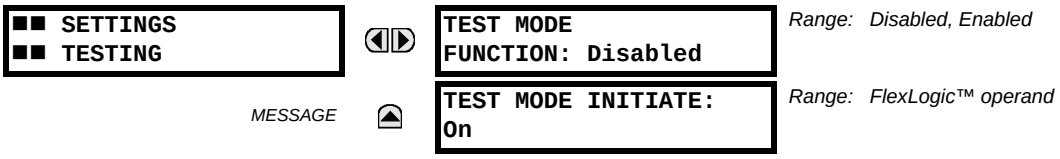
The worst-case error for this application could be calculated by superimposing the following two sources of error:

- ±0.5% of the full scale for the analog output module, or $\pm 0.005 \times (1 - 0) \times 254.03 \text{ kV} = \pm 1.27 \text{ kV}$
- ±0.5% of reading

For example, under nominal conditions, the positive-sequence reads 230.94 kV and the worst-case error is 0.005 x 230.94 kV + 1.27 kV = 2.42 kV.

5.9.1 TEST MODE

PATH: SETTINGS ⇨⇩ TESTING ⇨ TEST MODE



The relay provides test settings to verify that functionality using simulated conditions for contact inputs and outputs. The Test Mode is indicated on the relay faceplate by a flashing Test Mode LED indicator.

To initiate the Test mode, the **TEST MODE FUNCTION** setting must be "Enabled" and the **TEST MODE INITIATE** setting must be set to Logic 1. In particular:

- To initiate Test Mode through relay settings, set **TEST MODE INITIATE** to "On". The Test Mode starts when the **TEST MODE FUNCTION** setting is changed from "Disabled" to "Enabled".
- To initiate Test Mode through a user-programmable condition, such as FlexLogic™ operand (pushbutton, digital input, communication-based input, or a combination of these), set **TEST MODE FUNCTION** to "Enabled" and set **TEST MODE INITIATE** to the desired operand. The Test Mode starts when the selected operand assumes a Logic 1 state.

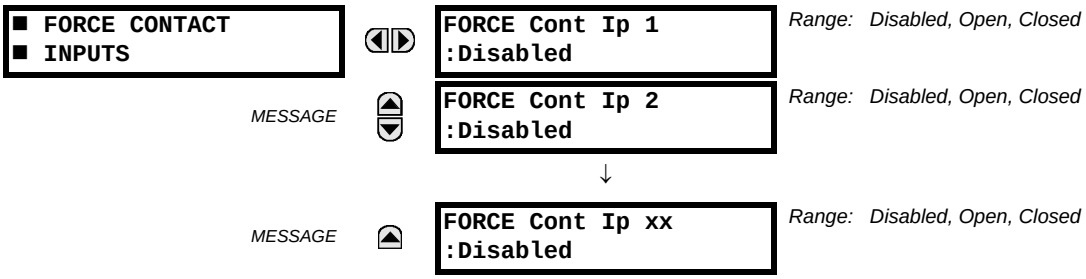
When in Test Mode, the L60 remains fully operational, allowing for various testing procedures. In particular, the protection and control elements, FlexLogic™, and communication-based inputs and outputs function normally.

The only difference between the normal operation and the Test Mode is the behavior of the input and output contacts. The former can be forced to report as open or closed or remain fully operational; the latter can be forced to open, close, freeze, or remain fully operational. The response of the digital input and output contacts to the Test Mode is programmed individually for each input and output using the Force Contact Inputs and Force Contact Outputs test functions described in the following sections.

5

5.9.2 FORCE CONTACT INPUTS

PATH: SETTINGS ⇨⇩ TESTING ⇨⇩ FORCE CONTACT INPUTS

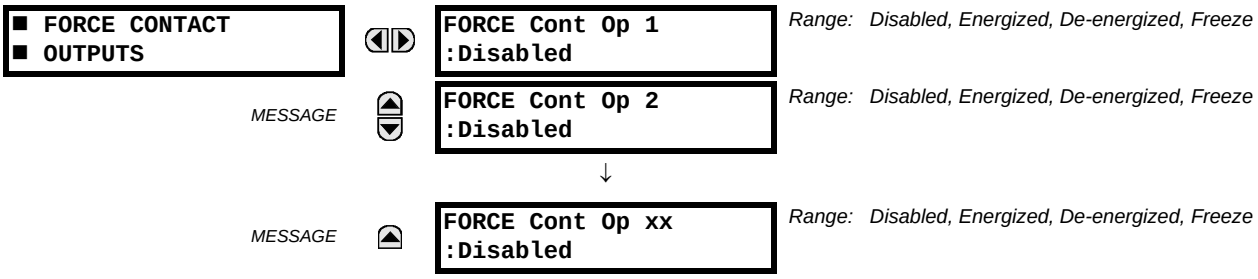


The relay digital inputs (contact inputs) could be pre-programmed to respond to the Test Mode in the following ways:

- If set to "Disabled", the input remains fully operational. It is controlled by the voltage across its input terminals and can be turned on and off by external circuitry. This value should be selected if a given input must be operational during the test. This includes, for example, an input initiating the test, or being a part of a user pre-programmed test sequence.
- If set to "Open", the input is forced to report as opened (Logic 0) for the entire duration of the Test Mode regardless of the voltage across the input terminals.
- If set to "Closed", the input is forced to report as closed (Logic 1) for the entire duration of the Test Mode regardless of the voltage across the input terminals.

The Force Contact Inputs feature provides a method of performing checks on the function of all contact inputs. Once enabled, the relay is placed into Test Mode, allowing this feature to override the normal function of contact inputs. The Test Mode LED will be On, indicating that the relay is in Test Mode. The state of each contact input may be programmed as "Disabled", "Open", or "Closed". All contact input operations return to normal when all settings for this feature are disabled.

PATH: SETTINGS ⇨⇩ TESTING ⇨⇩ FORCE CONTACT OUTPUTS



The relay contact outputs can be pre-programmed to respond to the test mode.

If set to "Disabled", the contact output remains fully operational. If operates when its control operand is logic 1 and will resets when its control operand is logic 0. If set to "Energized", the output will close and remain closed for the entire duration of the test mode, regardless of the status of the operand configured to control the output contact. If set to "De-energized", the output will open and remain opened for the entire duration of the test mode regardless of the status of the operand configured to control the output contact. If set to "Freeze", the output retains its position from before entering the test mode, regardless of the status of the operand configured to control the output contact.

These settings are applied two ways. First, external circuits may be tested by energizing or de-energizing contacts. Second, by controlling the output contact state, relay logic may be tested and undesirable effects on external circuits avoided.

Example 1: Initiating test mode through user-programmable pushbutton 1

For example, the test mode can be initiated from user-programmable pushbutton 1. The pushbutton will be programmed as "Latched" (pushbutton pressed to initiate the test, and pressed again to terminate the test). During the test, digital input 1 should remain operational, digital inputs 2 and 3 should open, and digital input 4 should close. Also, contact output 1 should freeze, contact output 2 should open, contact output 3 should close, and contact output 4 should remain fully operational. The required settings are shown below.

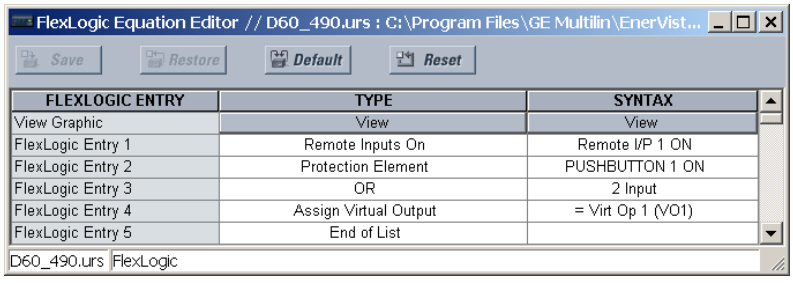
To enable user-programmable pushbutton 1 to initiate the test mode, make the following changes in the SETTINGS ⇨⇩ TESTING ⇨ TEST MODE menu: **TEST MODE FUNCTION:** "Enabled" and **TEST MODE INITIATE:** "PUSHBUTTON 1 ON"

Make the following changes to configure the contact inputs and outputs. In the SETTINGS ⇨⇩ TESTING ⇨⇩ FORCE CONTACT INPUTS and FORCE CONTACT OUTPUTS menus, set:

FORCE Cont Ip 1: "Disabled", **FORCE Cont Ip 2:** "Open", **FORCE Cont Ip 3:** "Open", and **FORCE Cont Ip 4:** "Closed"
FORCE Cont Op 1: "Freeze", **FORCE Cont Op 2:** "De-energized", **FORCE Cont Op 3:** "Energized", and **FORCE Cont Op 4:** "Disabled"

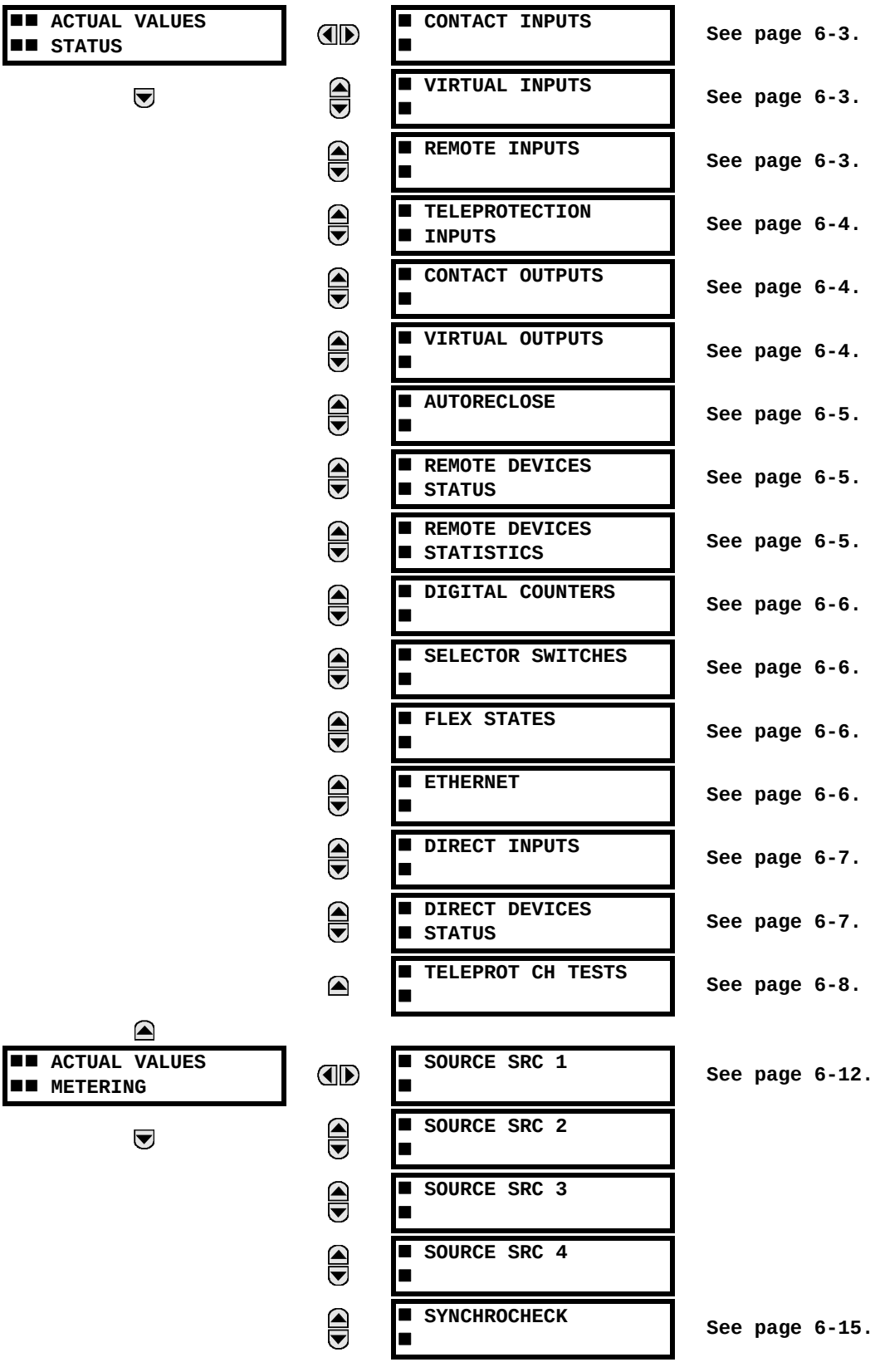
Example 2: Initiating a test from user-programmable pushbutton 1 or through remote input 1

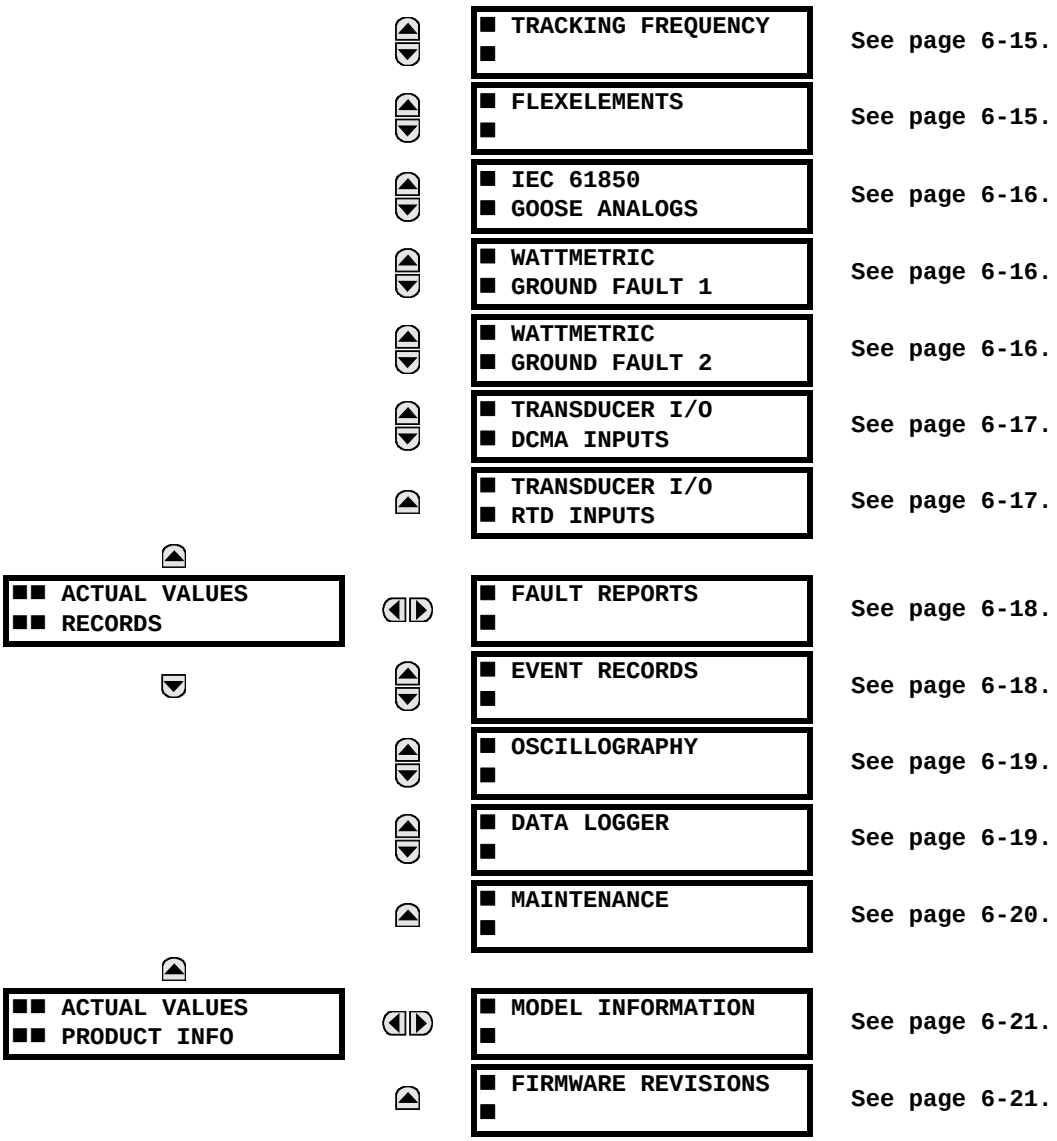
In this example, the test can be initiated locally from user-programmable pushbutton 1 or remotely through remote input 1. Both the pushbutton and the remote input will be programmed as "Latched". Write the following FlexLogic™ equation:



Set the user-programmable pushbutton as latching by changing SETTINGS ⇨ PRODUCT SETUP ⇨⇩ USER-PROGRAMMABLE PUSHBUTTONS ⇨ USER PUSHBUTTON 1 ⇨ PUSHBUTTON 1 FUNCTION to "Latched". To enable either pushbutton 1 or remote input 1 to initiate the Test mode, make the following changes in the SETTINGS ⇨⇩ TESTING ⇨ TEST MODE menu:

TEST MODE FUNCTION: "Enabled" and **TEST MODE INITIATE:** "VO1"


ACTUAL VALUES
STATUS
CONTACT INPUTS
See page 6-3.
VIRTUAL INPUTS
See page 6-3.
REMOTE INPUTS
See page 6-3.
TELEPROTECTION INPUTS
See page 6-4.
CONTACT OUTPUTS
See page 6-4.
VIRTUAL OUTPUTS
See page 6-4.
AUTORECLOSE
See page 6-5.
REMOTE DEVICES STATUS
See page 6-5.
REMOTE DEVICES STATISTICS
See page 6-5.
DIGITAL COUNTERS
See page 6-6.
SELECTOR SWITCHES
See page 6-6.
FLEX STATES
See page 6-6.
ETHERNET
See page 6-6.
DIRECT INPUTS
See page 6-7.
DIRECT DEVICES STATUS
See page 6-7.
TELEPROT CH TESTS
See page 6-8.
ACTUAL VALUES
METERING
SOURCE SRC 1
See page 6-12.
SOURCE SRC 2
SOURCE SRC 3
SOURCE SRC 4
SYNCHROCHECK
See page 6-15.

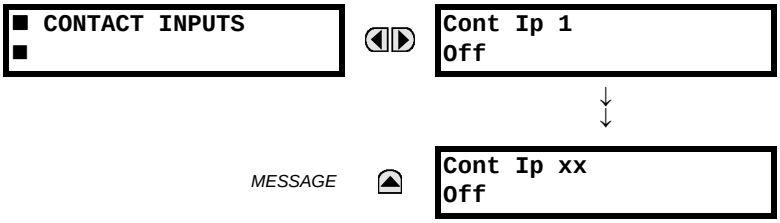

■■ ACTUAL VALUES
■■ RECORDS
■ TRACKING FREQUENCY
■
See page 6-15.
■ FLEXELEMENTS
■
See page 6-15.
■ IEC 61850
■ GOOSE ANALOGS
See page 6-16.
■ WATTMETRIC
■ GROUND FAULT 1
See page 6-16.
■ WATTMETRIC
■ GROUND FAULT 2
See page 6-16.
■ TRANSDUCER I/O
■ DCMA INPUTS
See page 6-17.
■ TRANSDUCER I/O
■ RTD INPUTS
See page 6-17.
■ FAULT REPORTS
■
See page 6-18.
■ EVENT RECORDS
■
See page 6-18.
■ OSCILLOGRAPHY
■
See page 6-19.
■ DATA LOGGER
■
See page 6-19.
■ MAINTENANCE
■
See page 6-20.
■■ ACTUAL VALUES
■■ PRODUCT INFO
■ MODEL INFORMATION
■
See page 6-21.
■ FIRMWARE REVISIONS
■
See page 6-21.

NOTE

For status reporting, 'On' represents Logic 1 and 'Off' represents Logic 0.

6.2.1 CONTACT INPUTS

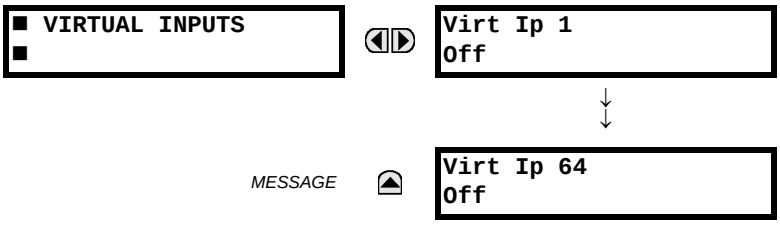
PATH: ACTUAL VALUES ⇨ STATUS ⇨ CONTACT INPUTS



The present status of the contact inputs is shown here. The first line of a message display indicates the ID of the contact input. For example, 'Cont Ip 1' refers to the contact input in terms of the default name-array index. The second line of the display indicates the logic state of the contact input.

6.2.2 VIRTUAL INPUTS

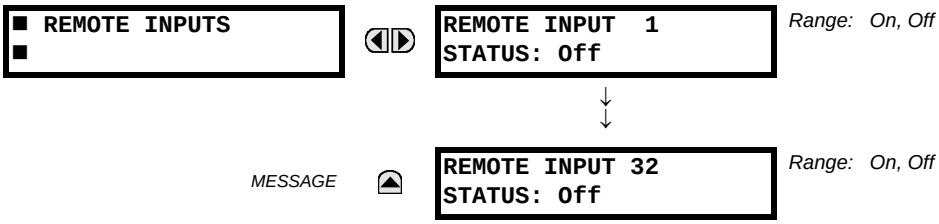
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ VIRTUAL INPUTS



The present status of the 64 virtual inputs is shown here. The first line of a message display indicates the ID of the virtual input. For example, 'Virt Ip 1' refers to the virtual input in terms of the default name. The second line of the display indicates the logic state of the virtual input.

6.2.3 REMOTE INPUTS

PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ REMOTE INPUTS

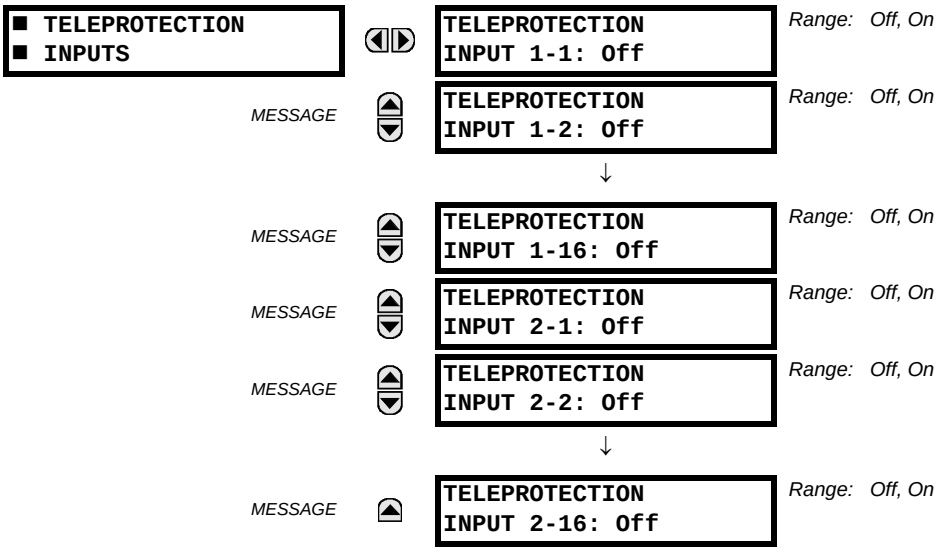


The present state of the 32 remote inputs is shown here.

The state displayed will be that of the remote point unless the remote device has been established to be "Offline" in which case the value shown is the programmed default state for the remote input.

6.2.4 TELEPROTECTION INPUTS

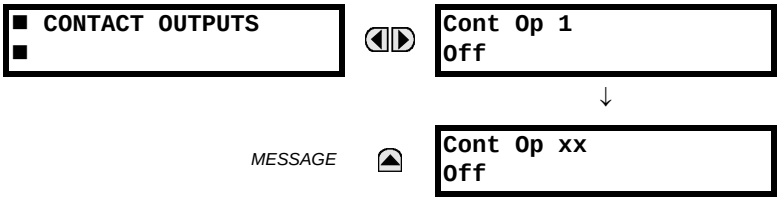
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ TELEPROTECTION INPUTS



The present state of teleprotection inputs from communication channels 1 and 2 are shown here. The state displayed will be that of corresponding remote output unless the channel is declared failed.

6.2.5 CONTACT OUTPUTS

PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ CONTACT OUTPUTS



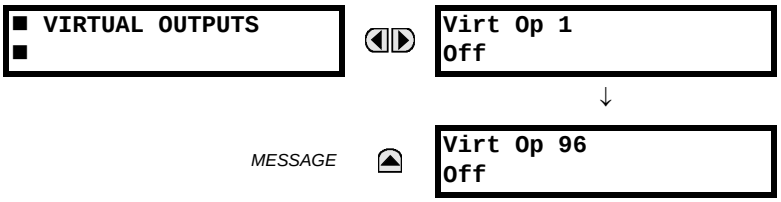
The present state of the contact outputs is shown here. The first line of a message display indicates the ID of the contact output. For example, 'Cont Op 1' refers to the contact output in terms of the default name-array index. The second line of the display indicates the logic state of the contact output.

NOTE

For Form-A outputs, the state of the voltage(V) and/or current(I) detectors will show as: Off, VOff, IOff, On, VOn, and/or IOn. For Form-C outputs, the state will show as Off or On.

6.2.6 VIRTUAL OUTPUTS

PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ VIRTUAL OUTPUTS



The present state of up to 96 virtual outputs is shown here. The first line of a message display indicates the ID of the virtual output. For example, 'Virt Op 1' refers to the virtual output in terms of the default name-array index. The second line of the display indicates the logic state of the virtual output, as calculated by the FlexLogic™ equation for that output.

6.2.7 AUTORECLOSE

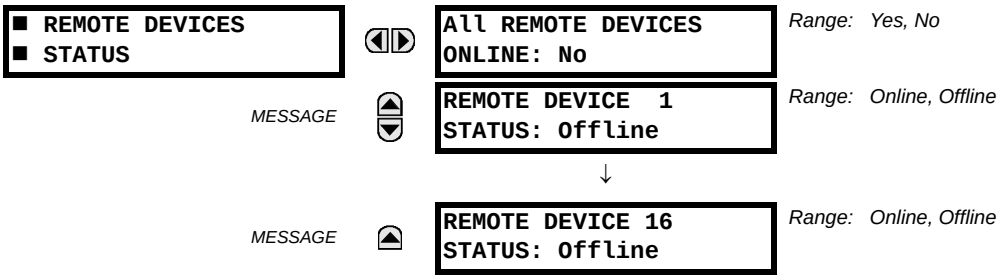
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ AUTORECLOSE ⇨ AUTORECLOSE 1

The automatic reclosure shot count is shown here.

6.2.8 REMOTE DEVICES

a) STATUS

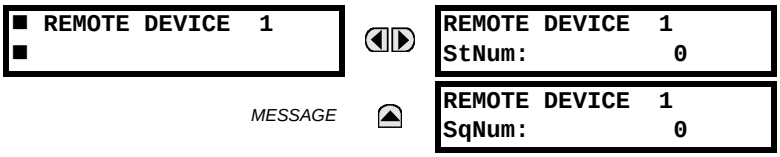
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ REMOTE DEVICES STATUS



The present state of up to 16 programmed remote devices is shown here. The **ALL REMOTE DEVICES ONLINE** message indicates whether or not all programmed remote devices are online. If the corresponding state is "No", then at least one required remote device is not online.

b) STATISTICS

PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ REMOTE DEVICES STATISTICS ⇨ REMOTE DEVICE 1(16)

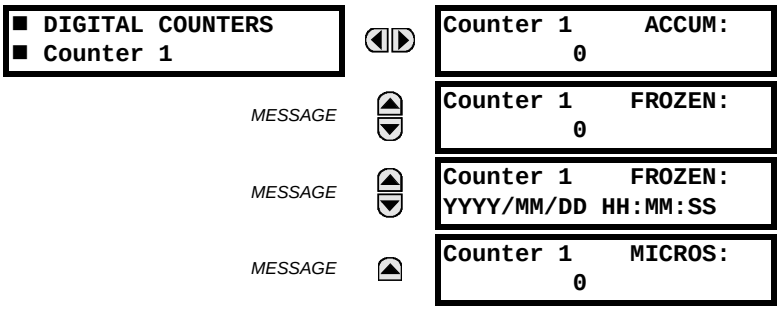


Statistical data (two types) for up to 16 programmed remote devices is shown here.

The **StNum** number is obtained from the indicated remote device and is incremented whenever a change of state of at least one DNA or UserSt bit occurs. The **SqNum** number is obtained from the indicated remote device and is incremented whenever a GSSE message is sent. This number will rollover to zero when a count of 4,294,967,295 is incremented.

6.2.9 DIGITAL COUNTERS

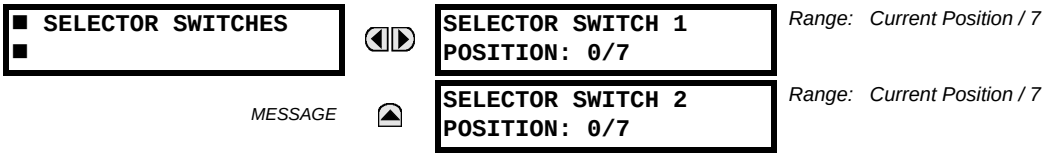
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ DIGITAL COUNTERS ⇨ DIGITAL COUNTERS Counter 1(8)



The present status of the eight digital counters is shown here. The status of each counter, with the user-defined counter name, includes the accumulated and frozen counts (the count units label will also appear). Also included, is the date/time stamp for the frozen count. The **Counter n MICROS** value refers to the microsecond portion of the time stamp.

6.2.10 SELECTOR SWITCHES

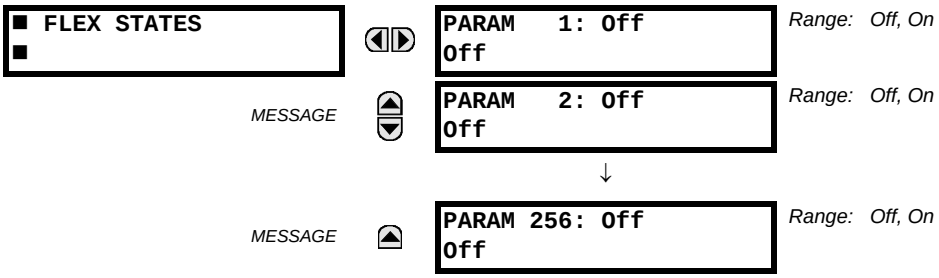
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ SELECTOR SWITCHES



The display shows both the current position and the full range. The current position only (an integer from 0 through 7) is the actual value.

6.2.11 FLEX STATES

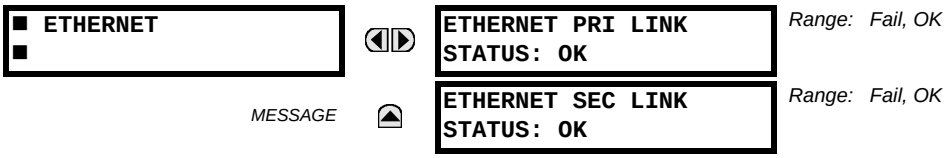
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ FLEX STATES



There are 256 FlexState bits available. The second line value indicates the state of the given FlexState bit.

6.2.12 ETHERNET

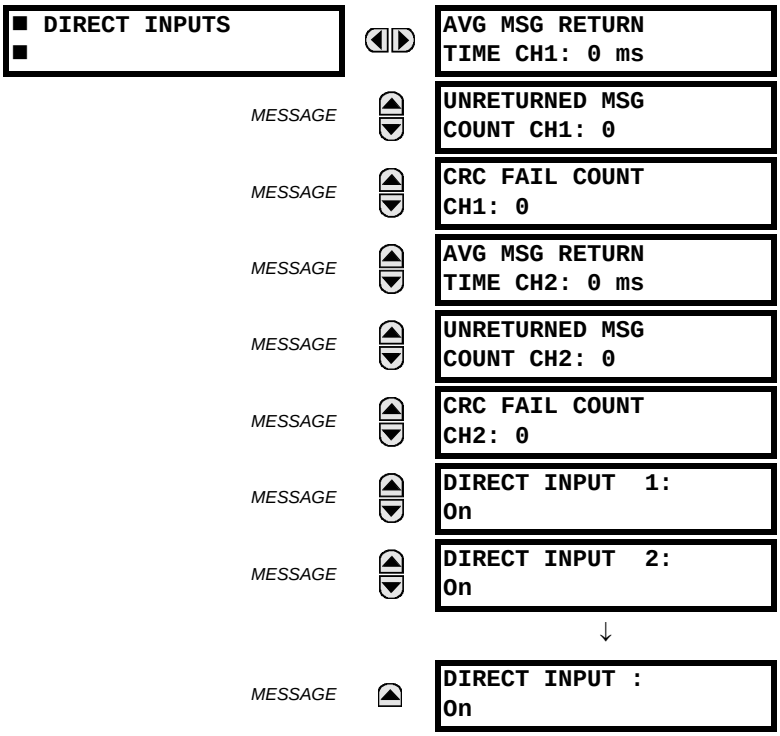
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ ETHERNET



These values indicate the status of the primary and secondary Ethernet links.

6.2.13 DIRECT INPUTS

PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ DIRECT INPUTS



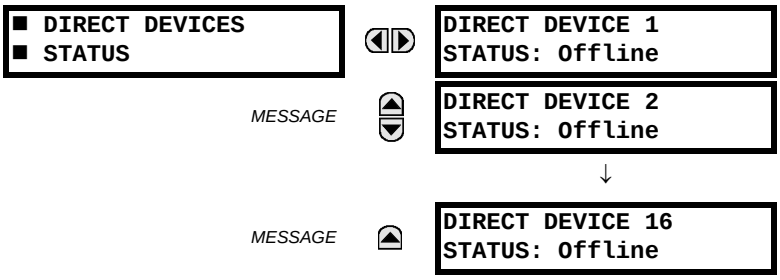
The **AVERAGE MSG RETURN TIME** is the time taken for direct output messages to return to the sender in a direct input/output ring configuration (this value is not applicable for non-ring configurations). This is a rolling average calculated for the last ten messages. There are two return times for dual-channel communications modules.

The **UNRETURNED MSG COUNT** values (one per communications channel) count the direct output messages that do not make the trip around the communications ring. The **CRC FAIL COUNT** values (one per communications channel) count the direct output messages that have been received but fail the CRC check. High values for either of these counts may indicate on a problem with wiring, the communication channel, or the relay(s). The **UNRETURNED MSG COUNT** and **CRC FAIL COUNT** values can be cleared using the **CLEAR DIRECT I/O COUNTERS** command.

The **DIRECT INPUT 1()** values represent the state of each direct input.

6.2.14 DIRECT DEVICES STATUS

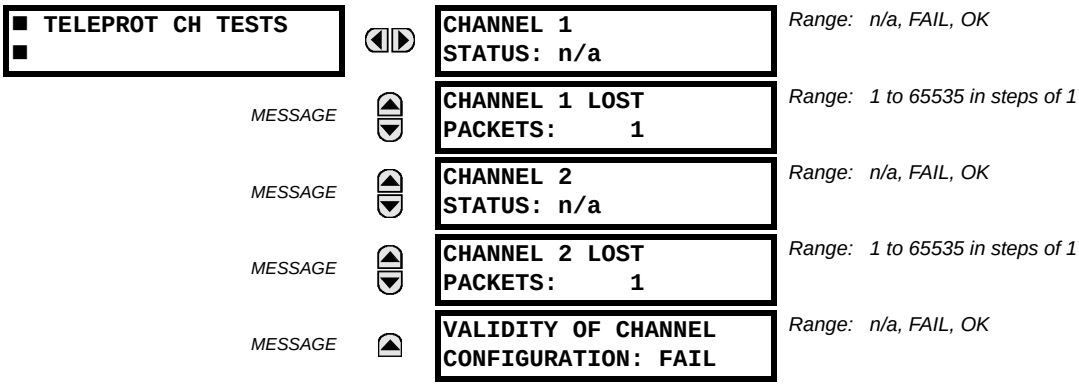
PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ DIRECT DEVICES STATUS



These actual values represent the state of direct devices 1 through 16.

6.2.15 TELEPROTECTION CHANNEL TESTS

PATH: ACTUAL VALUES ⇨ STATUS ⇨⇩ TELEPROT CH TESTS



The status information for two channels is shown here.

- **CHANNEL 1 STATUS**: This represents the receiver status of each channel. If the value is "OK", teleprotection is enabled and data is being received from the remote terminal; If the value is "FAIL", teleprotection enabled and data is not being received from the remote terminal. If "n/a", teleprotection is disabled.
- **CHANNEL 1 LOST PACKETS**: Data is transmitted to the remote terminals in data packets at a rate of two packets per cycle. The number of lost packets represents data packets lost in transmission; this count can be reset to 0 through the **COMMANDS ⇨⇩ CLEAR RECORDS** menu.
- **VALIDITY OF CHANNEL CONFIGURATION**: This value displays the current state of the communications channel identification check, and hence validity. If a remote relay ID does not match the programmed ID at the local relay, the "FAIL" message will be displayed. The "N/A" value appears if the local relay ID is set to a default value of "0", the channel is failed, or if the teleprotection inputs/outputs are not enabled.

a) UR CONVENTION FOR MEASURING POWER AND ENERGY

The following figure illustrates the conventions established for use in UR-series relays.

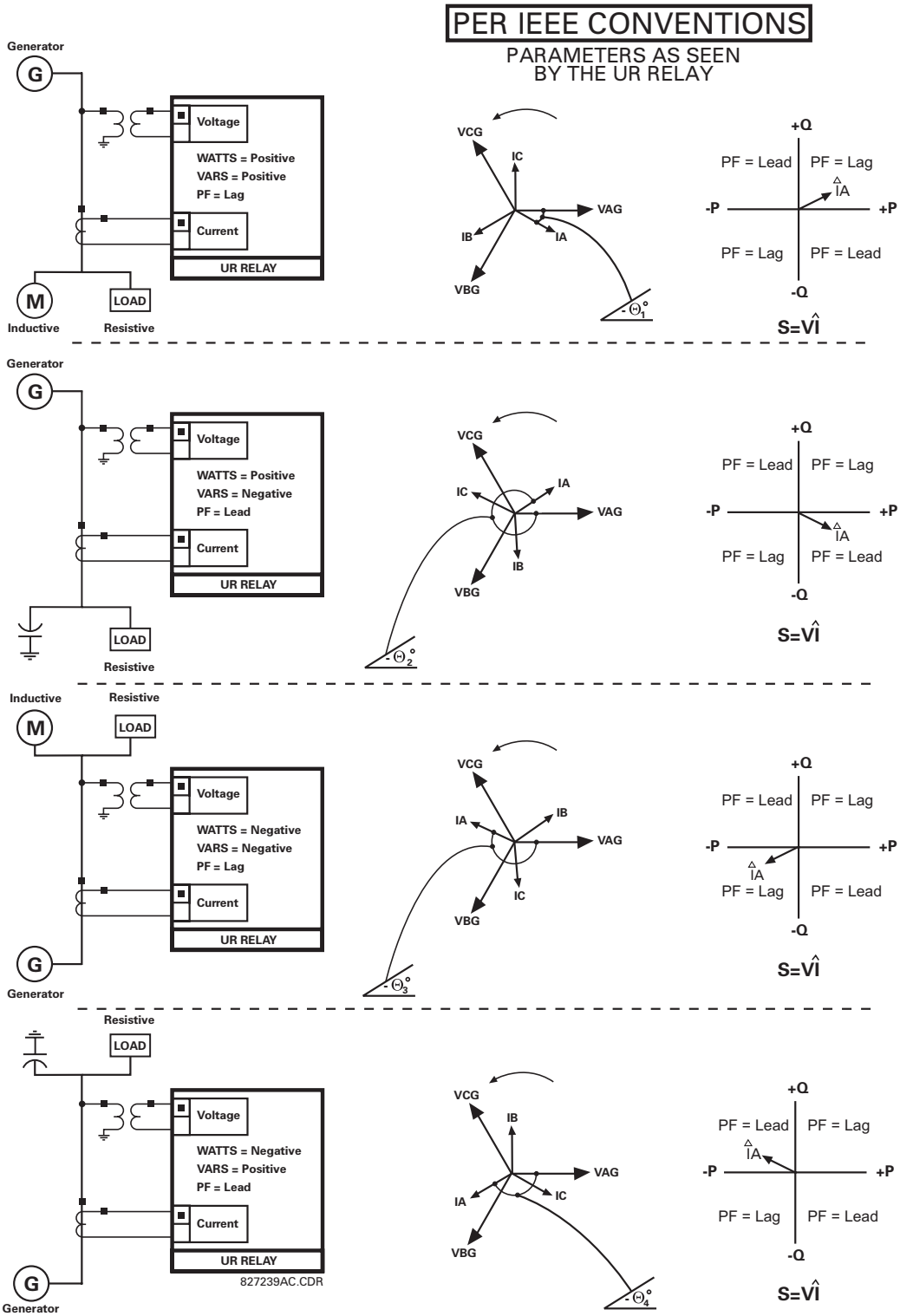


Figure 6–1: FLOW DIRECTION OF SIGNED VALUES FOR WATTS AND VARS

b) UR CONVENTION FOR MEASURING PHASE ANGLES

All phasors calculated by UR-series relays and used for protection, control and metering functions are rotating phasors that maintain the correct phase angle relationships with each other at all times.

For display and oscillography purposes, all phasor angles in a given relay are referred to an AC input channel pre-selected by the **SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ POWER SYSTEM ⇨⇩ FREQUENCY AND PHASE REFERENCE** setting. This setting defines a particular AC signal source to be used as the reference.

The relay will first determine if any “Phase VT” bank is indicated in the source. If it is, voltage channel VA of that bank is used as the angle reference. Otherwise, the relay determines if any “Aux VT” bank is indicated; if it is, the auxiliary voltage channel of that bank is used as the angle reference. If neither of the two conditions is satisfied, then two more steps of this hierarchical procedure to determine the reference signal include “Phase CT” bank and “Ground CT” bank.

If the AC signal pre-selected by the relay upon configuration is not measurable, the phase angles are not referenced. The phase angles are assigned as positive in the leading direction, and are presented as negative in the lagging direction, to more closely align with power system metering conventions. This is illustrated below.

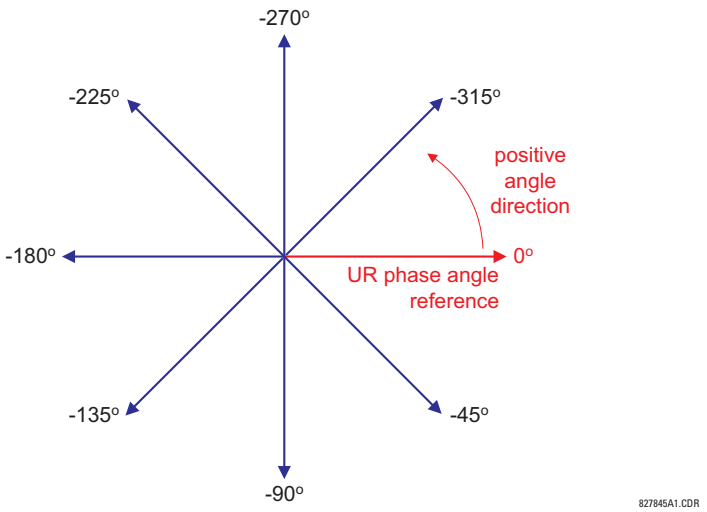


Figure 6–2: UR PHASE ANGLE MEASUREMENT CONVENTION

c) UR CONVENTION FOR MEASURING SYMMETRICAL COMPONENTS

The UR-series of relays calculate voltage symmetrical components for the power system phase A line-to-neutral voltage, and symmetrical components of the currents for the power system phase A current. Owing to the above definition, phase angle relations between the symmetrical currents and voltages stay the same irrespective of the connection of instrument transformers. This is important for setting directional protection elements that use symmetrical voltages.

For display and oscillography purposes the phase angles of symmetrical components are referenced to a common reference as described in the previous sub-section.

WYE-CONNECTED INSTRUMENT TRANSFORMERS:

- ABC phase rotation:

$$V\_0 = \frac{1}{3}(V_{AG} + V_{BG} + V_{CG})$$

$$V\_1 = \frac{1}{3}(V_{AG} + aV_{BG} + a^2V_{CG})$$

$$V\_2 = \frac{1}{3}(V_{AG} + a^2V_{BG} + aV_{CG})$$

- ACB phase rotation:

$$V\_0 = \frac{1}{3}(V_{AG} + V_{BG} + V_{CG})$$

$$V\_1 = \frac{1}{3}(V_{AG} + a^2V_{BG} + aV_{CG})$$

$$V\_2 = \frac{1}{3}(V_{AG} + aV_{BG} + a^2V_{CG})$$

The above equations apply to currents as well.

DELTA-CONNECTED INSTRUMENT TRANSFORMERS:

- ABC phase rotation:

$$V\_0 = \text{N/A}$$

$$V\_1 = \frac{1\angle -30^\circ}{3\sqrt{3}}(V_{AB} + aV_{BC} + a^2V_{CA})$$

$$V\_2 = \frac{1\angle 30^\circ}{3\sqrt{3}}(V_{AB} + a^2V_{BC} + aV_{CA})$$

- ACB phase rotation:

$$V\_0 = \text{N/A}$$

$$V\_1 = \frac{1\angle 30^\circ}{3\sqrt{3}}(V_{AB} + a^2V_{BC} + aV_{CA})$$

$$V\_2 = \frac{1\angle -30^\circ}{3\sqrt{3}}(V_{AB} + aV_{BC} + a^2V_{CA})$$

The zero-sequence voltage is not measurable under the Delta connection of instrument transformers and is defaulted to zero. The table below shows an example of symmetrical components calculations for the ABC phase rotation.

Table 6–1: SYMMETRICAL COMPONENTS CALCULATION EXAMPLE

SYSTEM VOLTAGES, SEC. V *						VT CONN.	RELAY INPUTS, SEC. V			SYMM. COMP, SEC. V		
V_{AG}	V_{BG}	V_{CG}	V_{AB}	V_{BC}	V_{CA}		F5AC	F6AC	F7AC	V_0	V_1	V_2
13.9 ∠0°	76.2 ∠–125°	79.7 ∠–250°	84.9 ∠–313°	138.3 ∠–97°	85.4 ∠–241°	WYE	13.9 ∠0°	76.2 ∠–125°	79.7 ∠–250°	19.5 ∠–192°	56.5 ∠–7°	23.3 ∠–187°
UNKNOWN (only V_1 and V_2 can be determined)			84.9 ∠0°	138.3 ∠–144°	85.4 ∠–288°	DELTA	84.9 ∠0°	138.3 ∠–144°	85.4 ∠–288°	N/A	56.5 ∠–54°	23.3 ∠–234°

* The power system voltages are phase-referenced – for simplicity – to *VAG* and *VAB*, respectively. This, however, is a relative matter. It is important to remember that the L60 displays are always referenced as specified under **SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ POWER SYSTEM ⇨⇩ FREQUENCY AND PHASE REFERENCE**.

The example above is illustrated in the following figure.

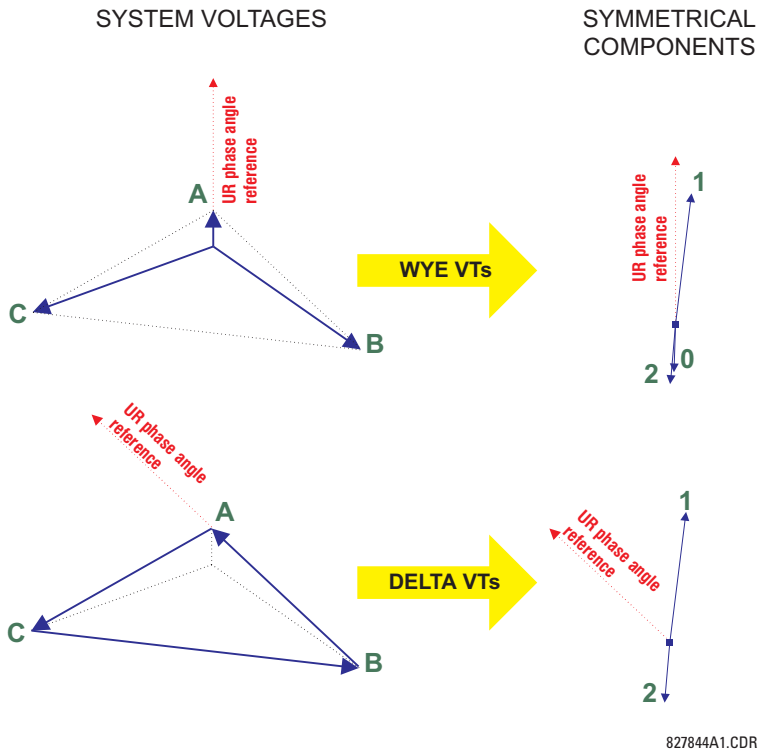
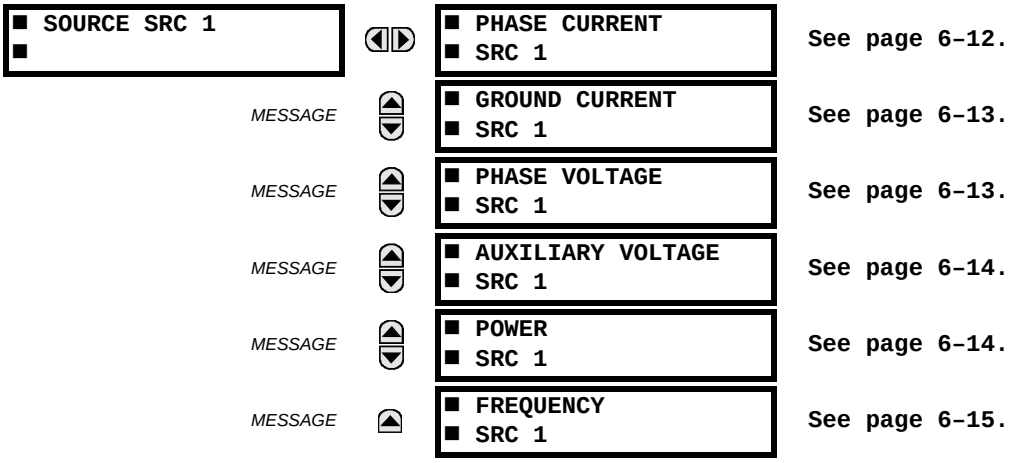


Figure 6–3: MEASUREMENT CONVENTION FOR SYMMETRICAL COMPONENTS

a) MAIN MENU

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ SOURCE SRC1

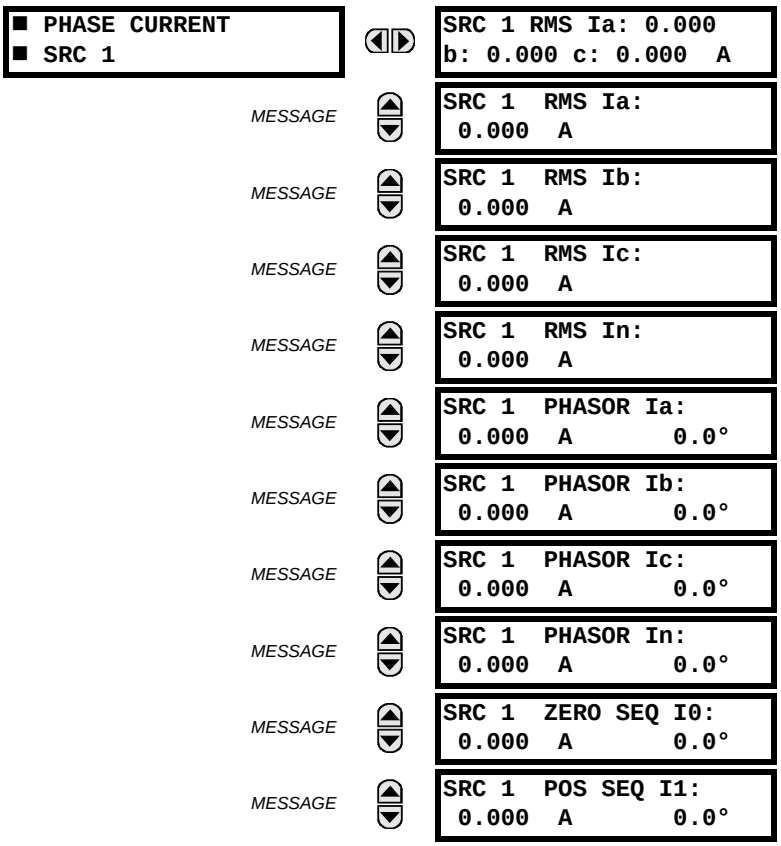


This menu displays the metered values available for each source.

Metered values presented for each source depend on the phase and auxiliary VTs and phase and ground CTs assignments for this particular source. For example, if no phase VT is assigned to this source, then any voltage, energy, and power values will be unavailable.

b) PHASE CURRENT METERING

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨ SOURCE SRC 1 ⇨ PHASE CURRENT



MESSAGE

```
SRC 1  NEG SEQ I2:
 0.000  A       0.0°
```

The metered phase current values are displayed in this menu. The "SRC 1" text will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES).

c) GROUND CURRENT METERING

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨ SOURCE SRC 1 ⇨⇩ GROUND CURRENT

```
■ GROUND CURRENT
■ SRC 1
```

```
SRC 1  RMS Ig:
 0.000  A
```

MESSAGE

```
SRC 1  PHASOR Ig:
 0.000  A       0.0°
```

MESSAGE

```
SRC 1  PHASOR Igd:
 0.000  A       0.0°
```

The metered ground current values are displayed in this menu. The "SRC 1" text will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES).

d) PHASE VOLTAGE METERING

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨ SOURCE SRC 1 ⇨ PHASE VOLTAGE

```
■ PHASE VOLTAGE
■ SRC 1
```

```
SRC 1  RMS Vag:
 0.00  V
```

MESSAGE

```
SRC 1  RMS Vbg:
 0.00  V
```

MESSAGE

```
SRC 1  RMS Vcg:
 0.00  V
```

MESSAGE

```
SRC 1  PHASOR Vag:
 0.000  V       0.0°
```

MESSAGE

```
SRC 1  PHASOR Vbg:
 0.000  V       0.0°
```

MESSAGE

```
SRC 1  PHASOR Vcg:
 0.000  V       0.0°
```

MESSAGE

```
SRC 1  RMS Vab:
 0.00  V
```

MESSAGE

```
SRC 1  RMS Vbc:
 0.00  V
```

MESSAGE

```
SRC 1  RMS Vca:
 0.00  V
```

MESSAGE

```
SRC 1  PHASOR Vab:
 0.000  V       0.0°
```

MESSAGE

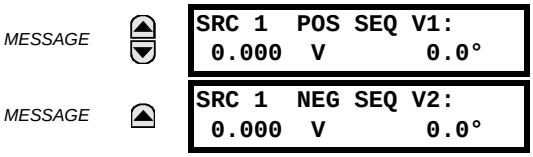
```
SRC 1  PHASOR Vbc:
 0.000  V       0.0°
```

MESSAGE

```
SRC 1  PHASOR Vca:
 0.000  V       0.0°
```

MESSAGE

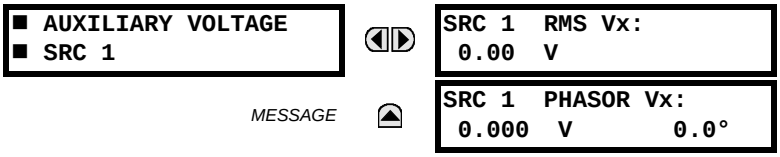
```
SRC 1  ZERO SEQ V0:
 0.000  V       0.0°
```



The metered phase voltage values are displayed in this menu. The "SRC 1" text will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES).

e) AUXILIARY VOLTAGE METERING

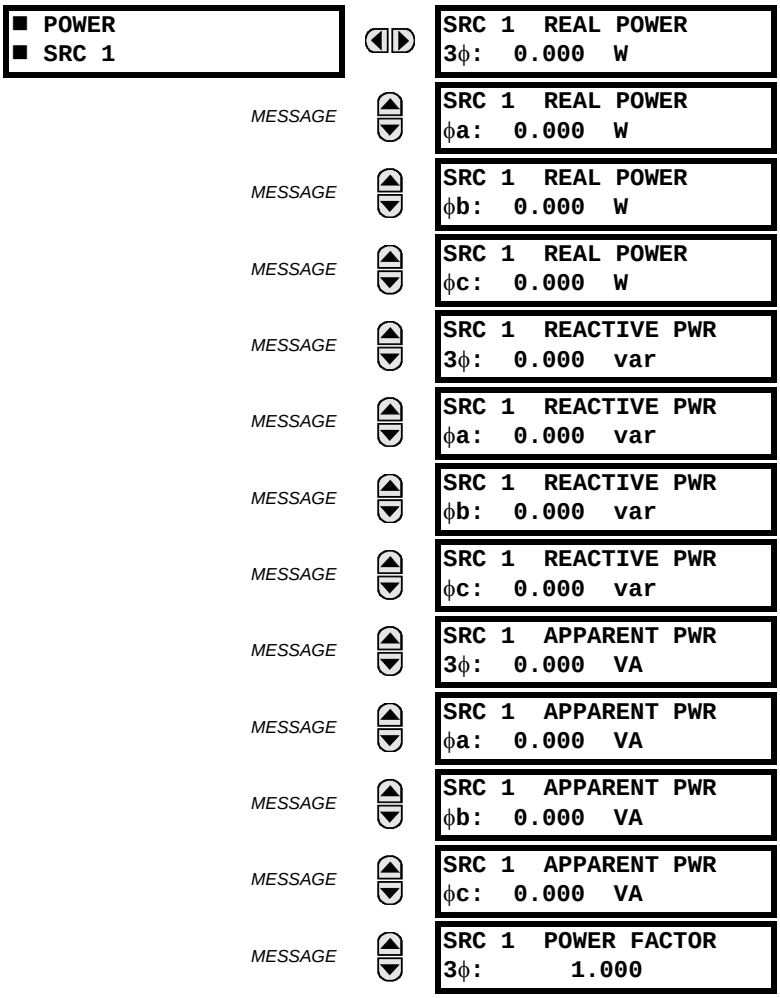
PATH: ACTUAL VALUES ⇨⇩ METERING ⇨ SOURCE SRC 1 ⇨⇩ AUXILIARY VOLTAGE

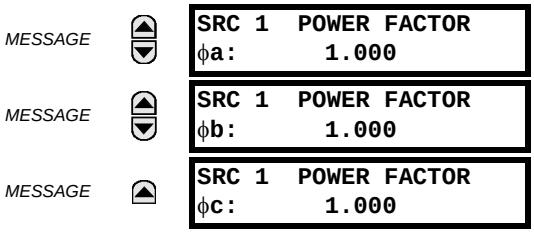


The metered auxiliary voltage values are displayed in this menu. The "SRC 1" text will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES).

f) POWER METERING

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨ SOURCE SRC 1 ⇨⇩ POWER





The metered values for real, reactive, and apparent power, as well as power factor, are displayed in this menu. The "SRC 1" text will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES).

g) FREQUENCY METERING

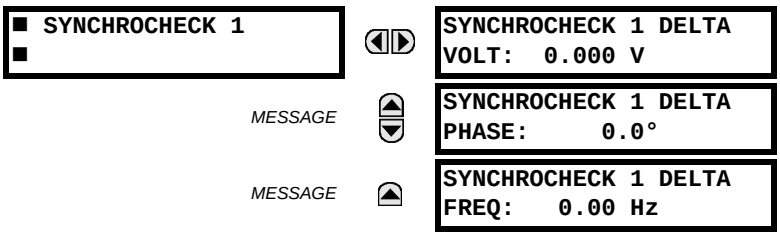
PATH: ACTUAL VALUES ⇨⇩ METERING ⇨ SOURCE SRC 1 ⇨⇩ FREQUENCY

The metered frequency values are displayed in this menu. The "SRC 1" text will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ SIGNAL SOURCES).

SOURCE FREQUENCY is measured via software-implemented zero-crossing detection of an AC signal. The signal is either a Clarke transformation of three-phase voltages or currents, auxiliary voltage, or ground current as per source configuration (see the SYSTEM SETUP ⇨⇩ POWER SYSTEM settings). The signal used for frequency estimation is low-pass filtered. The final frequency measurement is passed through a validation filter that eliminates false readings due to signal distortions and transients.

6.3.3 SYNCHROCHECK

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ SYNCHROCHECK ⇨ SYNCHROCHECK 1(2)



The actual values menu for synchrocheck 2 is identical to that of synchrocheck 1. If a synchrocheck function setting is "Disabled", the corresponding actual values menu item will not be displayed.

6.3.4 TRACKING FREQUENCY

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ TRACKING FREQUENCY

The tracking frequency is displayed here. The frequency is tracked based on the selection of the reference source with the **FREQUENCY AND PHASE REFERENCE** setting in the SETTINGS ⇨⇩ SYSTEM SETUP ⇨⇩ POWER SYSTEM menu. Refer to the *Power System* section of chapter 5 for additional details.

6.3.5 FLEXELEMENTS™

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ FLEXELEMENTS ⇨ FLEXELEMENT 1(8)

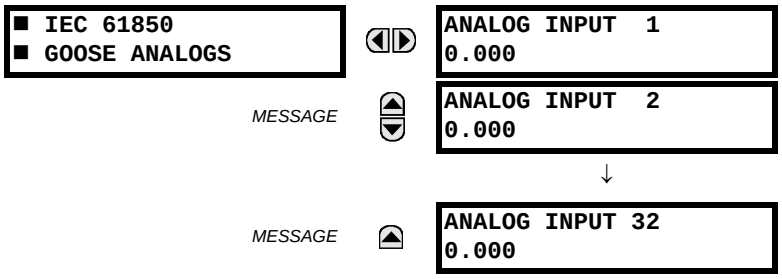
The operating signals for the FlexElements™ are displayed in pu values using the following definitions of the base units.

Table 6–2: FLEXELEMENT™ BASE UNITS

BREAKER ARCING AMPS (Brk X Arc Amp A, B, and C)	BASE = 2000 kA^2 × cycle
dcmA	BASE = maximum value of the **DCMA INPUT MAX** setting for the two transducers configured under the +IN and –IN inputs.
FREQUENCY	f_{BASE} = 1 Hz
PHASE ANGLE	φ_{BASE} = 360 degrees (see the UR angle referencing convention)
POWER FACTOR	PF_{BASE} = 1.00
RTDs	BASE = 100°C
SOURCE CURRENT	I_{BASE} = maximum nominal primary RMS value of the +IN and –IN inputs
SOURCE POWER	P_{BASE} = maximum value of $V_{BASE} \times I_{BASE}$ for the +IN and –IN inputs
SOURCE VOLTAGE	V_{BASE} = maximum nominal primary RMS value of the +IN and –IN inputs
SYNCHROCHECK (Max Delta Volts)	V_{BASE} = maximum primary RMS value of all the sources related to the +IN and –IN inputs

6.3.6 IEC 61580 GOOSE ANALOG VALUES

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ IEC 61850 GOOSE ANALOGS



The L60 Line Phase Comparison System is provided with optional IEC 61850 communications capability. This feature is specified as a software option at the time of ordering. Refer to the *Ordering* section of chapter 2 for additional details. The IEC 61850 protocol features are not available if CPU Type E is ordered.

The IEC 61850 GGIO3 analog input data points are displayed in this menu. The GGIO3 analog data values are received via IEC 61850 GOOSE messages sent from other devices.

6.3.7 WATTMETRIC GROUND FAULT

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ WATTMETRIC GROUND FAULT 1(2)

This menu displays the wattmetric zero-sequence directional element operating power values.

6.3.8 TRANSDUCER INPUTS/OUTPUTS

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ TRANSDUCER I/O DCMA INPUTS ⇨ DCMA INPUT xx

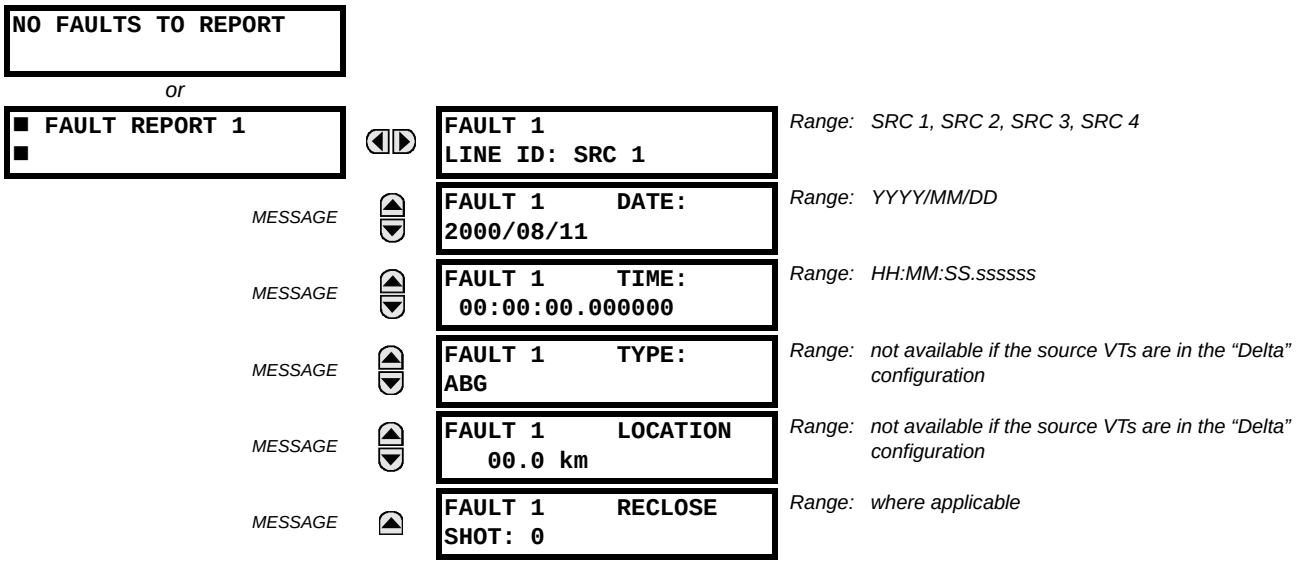
Actual values for each dcmA input channel that is enabled are displayed with the top line as the programmed Channel ID and the bottom line as the value followed by the programmed units.

PATH: ACTUAL VALUES ⇨⇩ METERING ⇨⇩ TRANSDUCER I/O RTD INPUTS ⇨ RTD INPUT xx

Actual values for each RTD input channel that is enabled are displayed with the top line as the programmed Channel ID and the bottom line as the value.

6.4.1 FAULT REPORTS

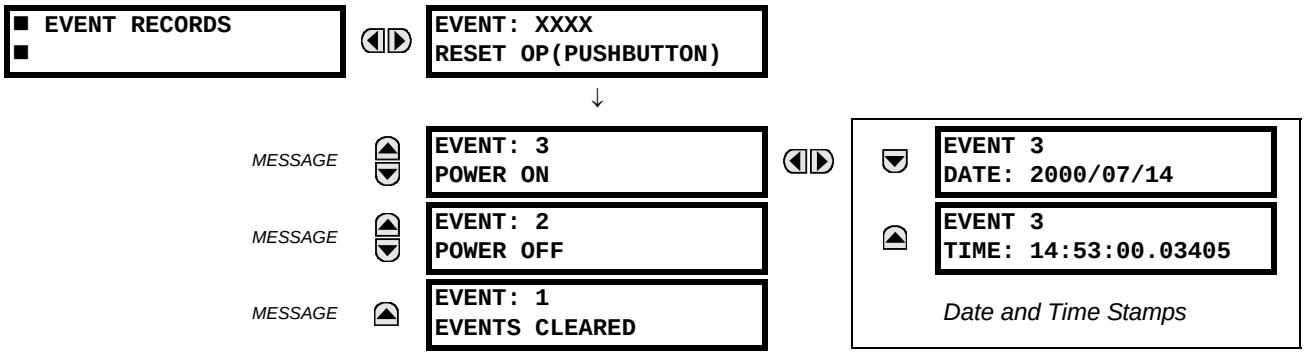
PATH: ACTUAL VALUES ⇨⇩ RECORDS ⇨ FAULT REPORTS ⇨ FAULT REPORT 1(15)



The latest 15 fault reports can be stored. The most recent fault location calculation (when applicable) is displayed in this menu, along with the date and time stamp of the event which triggered the calculation. See the SETTINGS ⇨ PRODUCT SETUP ⇨⇩ FAULT REPORTS menu for assigning the source and trigger for fault calculations. Refer to the COMMANDS ⇨⇩ CLEAR RECORDS menu for manual clearing of the fault reports and to the SETTINGS ⇨ PRODUCT SETUP ⇨⇩ CLEAR RELAY RECORDS menu for automated clearing of the fault reports.

6.4.2 EVENT RECORDS

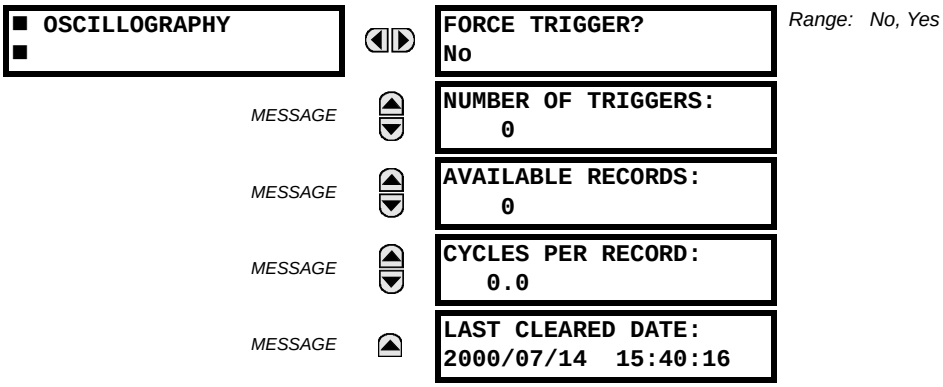
PATH: ACTUAL VALUES ⇨⇩ RECORDS ⇨⇩ EVENT RECORDS



The event records menu shows the contextual data associated with up to the last 1024 events, listed in chronological order from most recent to oldest. If all 1024 event records have been filled, the oldest record will be removed as a new record is added. Each event record shows the event identifier/sequence number, cause, and date/time stamp associated with the event trigger. Refer to the COMMANDS ⇩ CLEAR RECORDS menu for clearing event records.

6.4.3 OSCILLOGRAPHY

PATH: ACTUAL VALUES ⇨⇩ RECORDS ⇨⇩ OSCILLOGRAPHY

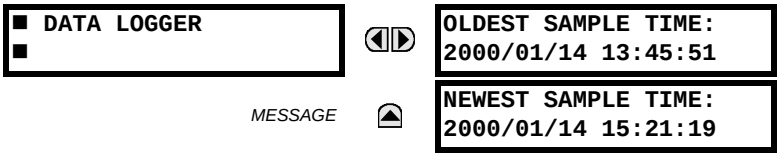


This menu allows the user to view the number of triggers involved and number of oscillography traces available. The 'cycles per record' value is calculated to account for the fixed amount of data storage for oscillography. See the *Oscillography* section of Chapter 5 for further details.

A trigger can be forced here at any time by setting "Yes" to the **FORCE TRIGGER?** command. Refer to the COMMANDS ⇨⇩ CLEAR RECORDS menu for clearing the oscillography records.

6.4.4 DATA LOGGER

PATH: ACTUAL VALUES ⇨⇩ RECORDS ⇨⇩ DATA LOGGER

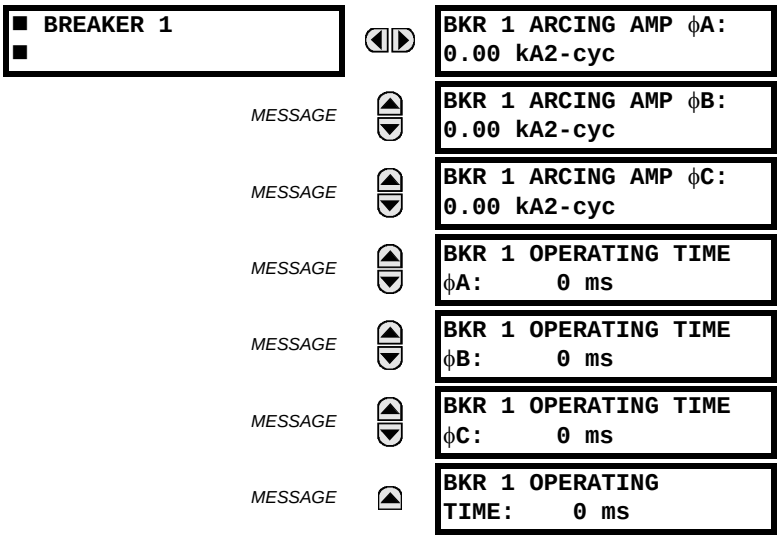


The **OLDEST SAMPLE TIME** represents the time at which the oldest available samples were taken. It will be static until the log gets full, at which time it will start counting at the defined sampling rate. The **NEWEST SAMPLE TIME** represents the time the most recent samples were taken. It counts up at the defined sampling rate. If the data logger channels are defined, then both values are static.

Refer to the COMMANDS ⇨⇩ CLEAR RECORDS menu for clearing data logger records.

6.4.5 BREAKER MAINTENANCE

PATH: ACTUAL VALUES ⇨⇩ RECORDS ⇨⇩ MAINTENANCE ⇨ BREAKER 1(2)



There is an identical menu for each of the breakers. The **BKR 1 ARCING AMP** values are in units of kA^2-cycles. Refer to the **COMMANDS** ⇨⇩ **CLEAR RECORDS** menu for clearing breaker arcing current records. The **BREAKER OPERATING TIME** is defined as the slowest operating time of breaker poles that were initiated to open.

6.5.1 MODEL INFORMATION

PATH: ACTUAL VALUES ⇨⇩ PRODUCT INFO ⇨ MODEL INFORMATION

■ MODEL INFORMATION ■	◀▶	ORDER CODE LINE 1: OC — Range: standard GE multilin order code format; example order code shown
MESSAGE	▲▼	ORDER CODE LINE 2: — Range: standard GE multilin order code format
MESSAGE	▲▼	ORDER CODE LINE 3: — Range: standard GE multilin order code format
MESSAGE	▲▼	ORDER CODE LINE 4: — Range: standard GE multilin order code format
MESSAGE	▲▼	SERIAL NUMBER: — Range: standard GE multilin serial number format
MESSAGE	▲▼	ETHERNET MAC ADDRESS 000000000000 — Range: standard Ethernet MAC address format
MESSAGE	▲▼	MANUFACTURING DATE: 0 — Range: YYYY/MM/DD HH:MM:SS
MESSAGE	▲	OPERATING TIME: 0:00:00 — Range: opearting time in HH:MM:SS

The product order code, serial number, Ethernet MAC address, date/time of manufacture, and operating time are shown here.

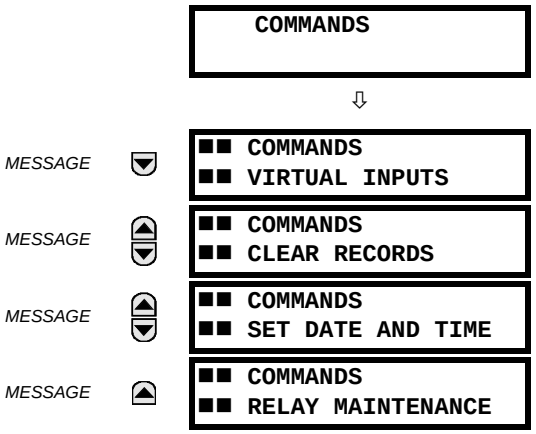
6.5.2 FIRMWARE REVISIONS

PATH: ACTUAL VALUES ⇨⇩ PRODUCT INFO ⇨⇩ FIRMWARE REVISIONS

■ FIRMWARE REVISIONS ■	◀▶	L60 Line Relay REVISION: 4.90 — Range: 0.00 to 655.35 Revision number of the application firmware.
MESSAGE	▲▼	MODIFICATION FILE NUMBER: 0 — Range: 0 to 65535 (ID of the MOD FILE) Value is 0 for each standard firmware release.
MESSAGE	▲▼	BOOT PROGRAM REVISION: 1.13 — Range: 0.00 to 655.35 Revision number of the boot program firmware.
MESSAGE	▲▼	FRONT PANEL PROGRAM REVISION: 0.08 — Range: 0.00 to 655.35 Revision number of faceplate program firmware.
MESSAGE	▲▼	COMPILE DATE: 2004/09/15 04:55:16 — Range: Any valid date and time. Date and time when product firmware was built.
MESSAGE	▲	BOOT DATE: 2004/09/15 16:41:32 — Range: Any valid date and time. Date and time when the boot program was built.

The shown data is illustrative only. A modification file number of 0 indicates that, currently, no modifications have been installed.

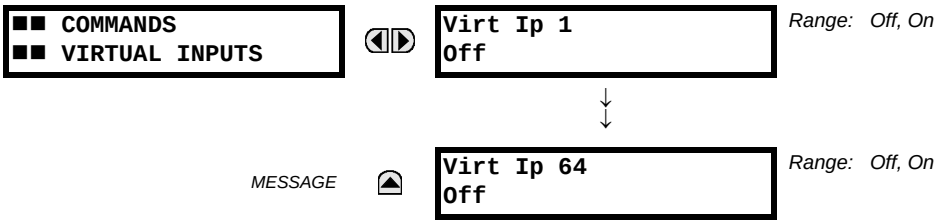
7.1.1 COMMANDS MENU



The commands menu contains relay directives intended for operations personnel. All commands can be protected from unauthorized access via the command password; see the *Password Security* section of chapter 5 for details. The following flash message appears after successfully command entry:

7.1.2 VIRTUAL INPUTS

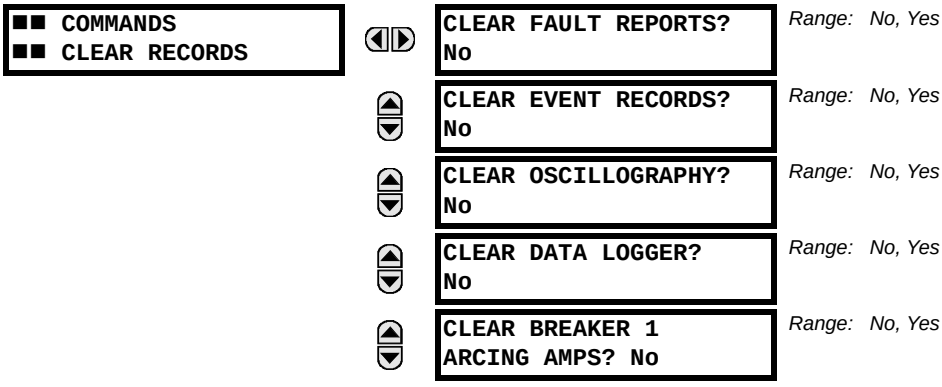
PATH: COMMANDS ⇨ VIRTUAL INPUTS

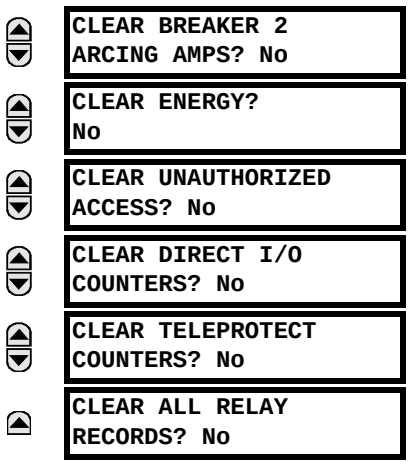


The states of up to 64 virtual inputs are changed here. The first line of the display indicates the ID of the virtual input. The second line indicates the current or selected status of the virtual input. This status will be a state off (logic 0) or on (logic 1).

7.1.3 CLEAR RECORDS

PATH: COMMANDS ⇨⇩ CLEAR RECORDS

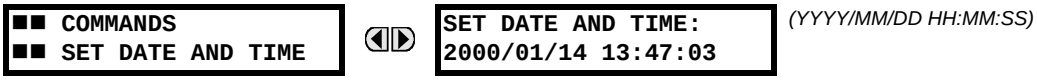




This menu contains commands for clearing historical data such as the event records. Data is cleared by changing a command setting to "Yes" and pressing the ENTER key. After clearing data, the command setting automatically reverts to "No".

7.1.4 SET DATE AND TIME

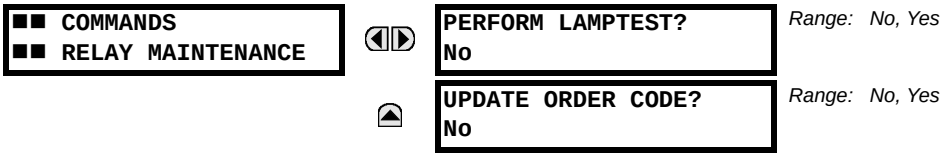
PATH: COMMANDS ⇨⇩ SET DATE AND TIME



The date and time can be entered here via the faceplate keypad only if the IRIG-B or SNTP signal is not in use. The time setting is based on the 24-hour clock. The complete date, as a minimum, must be entered to allow execution of this command. The new time will take effect at the moment the ENTER key is clicked.

7.1.5 RELAY MAINTENANCE

PATH: COMMANDS ⇨⇩ RELAY MAINTENANCE

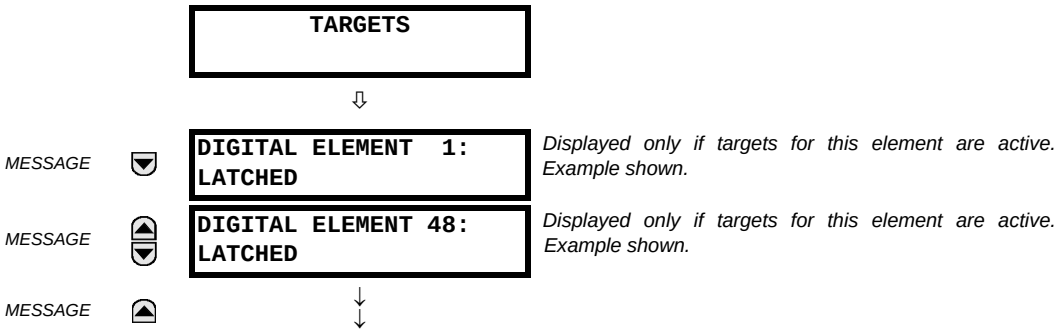


This menu contains commands for relay maintenance purposes. Commands are activated by changing a command setting to "Yes" and pressing the ENTER key. The command setting will then automatically revert to "No".

The **PERFORM LAMPTEST** command turns on all faceplate LEDs and display pixels for a short duration. The **UPDATE ORDER CODE** command causes the relay to scan the backplane for the hardware modules and update the order code to match. If an update occurs, the following message is shown.

There is no impact if there have been no changes to the hardware modules. When an update does not occur, the **ORDER CODE NOT UPDATED** message will be shown.

7.2.1 TARGETS MENU



The status of any active targets will be displayed in the targets menu. If no targets are active, the display will read **No Active Targets**:

7.2.2 TARGET MESSAGES

When there are no active targets, the first target to become active will cause the display to immediately default to that message. If there are active targets and the user is navigating through other messages, and when the default message timer times out (i.e. the keypad has not been used for a determined period of time), the display will again default back to the target message.

The range of variables for the target messages is described below. Phase information will be included if applicable. If a target message status changes, the status with the highest priority will be displayed.

Table 7–1: TARGET MESSAGE PRIORITY STATUS

PRIORITY	ACTIVE STATUS	DESCRIPTION
1	OP	element operated and still picked up
2	PKP	element picked up and timed out
3	LATCHED	element had operated but has dropped out

If a self test error is detected, a message appears indicating the cause of the error. For example **UNIT NOT PROGRAMMED** indicates that the minimal relay settings have not been programmed.

7.2.3 RELAY SELF-TESTS

a) DESCRIPTION

The relay performs a number of self-test diagnostic checks to ensure device integrity. The two types of self-tests (major and minor) are listed in the tables below. When either type of self-test error occurs, the Trouble LED Indicator will turn on and a target message displayed. All errors record an event in the event recorder. Latched errors can be cleared by pressing the RESET key, providing the condition is no longer present.

Major self-test errors also result in the following:

- The critical fail relay on the power supply module is de-energized.
- All other output relays are de-energized and are prevented from further operation.
- The faceplate In Service LED indicator is turned off.
- A RELAY OUT OF SERVICE event is recorded.

b) MAJOR SELF-TEST ERROR MESSAGES

The major self-test errors are listed and described below.

MODULE FAILURE___:
Contact Factory (xxx)

- *Latched target message*: Yes.
- *Description of problem*: Module hardware failure detected.
- *How often the test is performed*: Module dependent.
- *What to do*: Contact the factory and supply the failure code noted in the display. The "xxx" text identifies the failed module (for example, F8L).

INCOMPATIBLE H/W:
Contact Factory (xxx)

- *Latched target message*: Yes.
- *Description of problem*: One or more installed hardware modules is not compatible with the L60 order code.
- *How often the test is performed*: Module dependent.
- *What to do*: Contact the factory and supply the failure code noted in the display. The "xxx" text identifies the failed module (for example, F8L).

EQUIPMENT MISMATCH:
with 2nd line detail

- *Latched target message*: No.
- *Description of problem*: The configuration of modules does not match the order code stored in the L60.
- *How often the test is performed*: On power up. Afterwards, the backplane is checked for missing cards every five seconds.
- *What to do*: Check all modules against the order code, ensure they are inserted properly, and cycle control power. If the problem persists, contact the factory.

FLEXLOGIC ERROR:
with 2nd line detail

- *Latched target message*: No.
- *Description of problem*: A FlexLogic™ equation is incorrect.
- *How often the test is performed*: The test is event driven, performed whenever FlexLogic™ equations are modified.
- *What to do*: Finish all equation editing and use self tests to debug any errors.

UNIT NOT PROGRAMMED:
Check Settings

- *Latched target message*: No.
- *Description of problem*: The **PRODUCT SETUP** ⇨⇩ **INSTALLATION** ⇨ **RELAY SETTINGS** setting indicates the L60 is not programmed.
- *How often the test is performed*: On power up and whenever the **PRODUCT SETUP** ⇨⇩ **INSTALLATION** ⇨ **RELAY SETTINGS** setting is altered.
- *What to do*: Program all settings and then set **PRODUCT SETUP** ⇨⇩ **INSTALLATION** ⇨ **RELAY SETTINGS** to "Programmed".

c) MINOR SELF-TEST ERROR MESSAGES

Most of the minor self-test errors can be disabled. Refer to the settings in the *User-programmable self-tests* section in chapter 5 for additional details.

MAINTENANCE ALERT:
Replace Battery

- *Latched target message*: Yes.
- *Description of problem*: The battery is not functioning.
- *How often the test is performed*: The battery is monitored every five seconds. The error message is displayed after 60 seconds if the problem persists.
- *What to do*: Replace the battery located in the power supply module (1H or 1L).

MAINTENANCE ALERT:
Direct I/O Ring Break

- *Latched target message*: No.
- *Description of problem*: Direct input and output settings are configured for a ring, but the connection is not in a ring.
- *How often the test is performed*: Every second.
- *What to do*: Check direct input and output configuration and wiring.

MAINTENANCE ALERT:
****Bad IRIG-B Signal****

- *Latched target message*: No.
- *Description of problem*: A bad IRIG-B input signal has been detected.
- *How often the test is performed*: Monitored whenever an IRIG-B signal is received.
- *What to do*: Ensure the following:
  - The IRIG-B cable is properly connected.
  - Proper cable functionality (that is, check for physical damage or perform a continuity test).
  - The IRIG-B receiver is functioning.
  - Check the input signal level (it may be less than specification).

  If none of these apply, then contact the factory.

MAINTENANCE ALERT:
Port ## Failure

- *Latched target message*: No.
- *Description of problem*: An Ethernet connection has failed.
- *How often the test is performed*: Monitored every five seconds.
- *What to do*: Check Ethernet connections. Port 1 is the primary port and port 2 is the secondary port.

MAINTENANCE ALERT:
SNTP Failure

- *Latched target message*: No.
- *Description of problem*: The SNTP server is not responding.
- *How often the test is performed*: Every 10 to 60 seconds.
- *What to do*: Check SNTP configuration and network connections.

MAINTENANCE ALERT:
4L Discrepancy

- *Latched target message*: No.
- *Description of problem*: A discrepancy has been detected between the actual and desired state of a latching contact output of an installed type "4L" module.
- *How often the test is performed*: Upon initiation of a contact output state change.
- *What to do*: Verify the state of the output contact and contact the factory if the problem persists.

MAINTENANCE ALERT:
GGIO Ind xxx oscill

- *Latched target message*: No.
- *Description of problem*: A data item in a configurable GOOSE data set is oscillating.
- *How often the test is performed*: Upon scanning of each configurable GOOSE data set.
- *What to do*: The "xxx" text denotes the data item that has been detected as oscillating. Evaluate all logic pertaining to this item.

DIRECT I/O FAILURE:
COMM Path Incomplete

- *Latched target message*: No.
- *Description of problem*: A direct device is configured but not connected.
- *How often the test is performed*: Every second.
- *What to do*: Check direct input and output configuration and wiring.

REMOTE DEVICE FAIL:
COMM Path Incomplete

- *Latched target message*: No.
- *Description of problem*: One or more GOOSE devices are not responding.
- *How often the test is performed*: Event driven. The test is performed when a device programmed to receive GOOSE messages stops receiving. This can be from 1 to 60 seconds, depending on GOOSE packets.
- *What to do*: Check GOOSE setup.

UNEXPECTED RESTART:
Press "RESET" key

- *Latched target message*: Yes.
- *Description of problem*: Abnormal restart from modules being removed or inserted while the L60 is powered-up, when there is an abnormal DC supply, or as a result of internal relay failure.
- *How often the test is performed*: Event driven.
- *What to do*: Contact the factory.

8.1.1 INTRODUCTION

Phase comparison relaying is a kind of differential relaying that compares the phase angles of currents entering one terminal of a transmission line with the phase angles of the currents entering all remote terminals of the same line. For the conditions of a fault within the protected zone (internal fault), the currents entering all the terminals will be in phase. For conditions of a fault outside the zone of protection (external or through fault), or for load flow, the currents entering any one terminal will be 180° out of phase with the currents entering at least one of the remote terminals. The phase comparison relay scheme makes this phase angle comparison and trips the associated breakers for internal faults. Since the terminals of a transmission line are normally many miles apart, some sort of communication channel between the terminals is required to make this comparison.

8.1.2 FUNDAMENTAL PRINCIPLE OF PHASE COMPARISON

The basic operation of a phase comparison scheme requires that the phase angle of two or more currents be compared with each other. In the case of transmission line protection, these currents may originate many miles from each other so, as noted above, some form of communication channel is required as part of the scheme.

If a two-terminal line is considered (see figure below), the relays located at terminal A can measure the current at that terminal directly. The phase angle of the current at the remote terminal (B) must somehow be communicated to terminal A. Since the current sine wave is positive for ½-cycle and then negative for the next ½-cycle, it may be used to key a transmitter first to a MARK signal for a half cycle and then to a SPACE signal for the next half cycle for as long as the current is present. Such a signal transmitted at B and received at A can be compared with the current at A to determine whether the two quantities are in phase or out of phase with each other. Conversely, the current at terminal B may be compared with the signal received from terminal A.

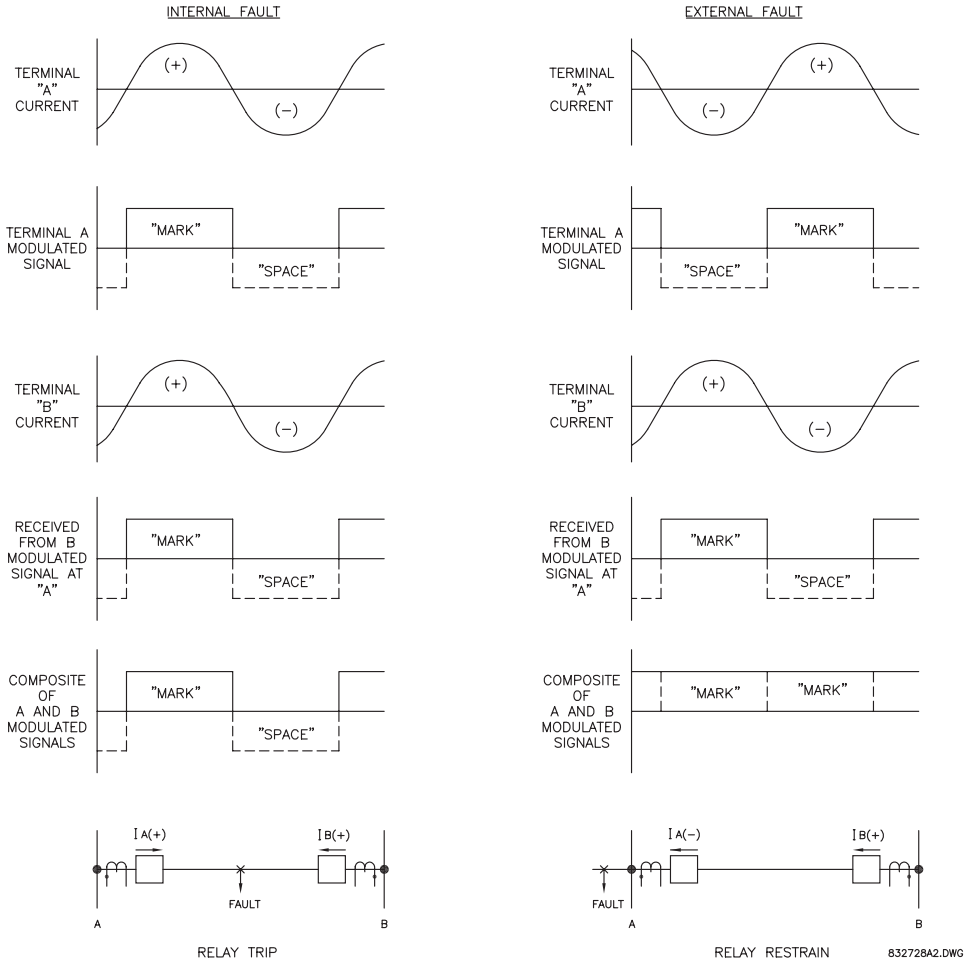


Figure 8–1: PHASE ANGLE COMPARISON

It becomes apparent that a comparison such as that described above must be made on a single phase basis. That is, it would not be possible to compare all three phase currents at terminal A individually with all three at terminal B over one single channel and one single comparing unit. However, to reduce communications channel requirements, all three phase currents are mixed to produce a single phase quantity whose magnitude and phase angle have a definite relation to the magnitude and phase angle of the three original currents. It is this single phase quantity that is phase compared with a similarly obtained quantity at the remote end(s) of the line.

While there are many variations on the basic scheme (these are discussed subsequently), the general method employed to compare the phase angle or phase position of the currents is always the same. The left side of Figure 8–1 illustrates the conditions for a fault internal to the protected zone. The sketches show about 1 cycle of the currents under internal and external faults to represent relay 'A' trip logic.

The MARK-SPACE designations given to the received signal are for identification and have no special significance. If the communication equipment happened to be a simple radio frequency transmitter-receiver, and if the positive half cycle of current keyed the transmitter to ON, then the MARK block corresponds to a received remote signal while the SPACE block corresponds to no signal. Conversely, if the negative portion of the current wave keyed the transmitter to ON, then the SPACE block would represent the received signal.

With a frequency-shift transmitter-receiver as the communication equipment, the MARK block would represent the receipt of the hi-shift frequency and the SPACE block the low-shift frequency if the remote transmitter was keyed to high from a positive current signal. The converse would be true if the transmitter was keyed to high from a negative current signal. In any case the MARK block received at A, whatever it represents, corresponds to positive current at B while the SPACE block corresponds to negative current at B.

If we consider an internal fault (as shown on the left side of Figure 8–1), the relay at A would be comparing modulated quantities illustrated in the sketches. If these two signals at terminal A were to be compared as shown in Figure 8–2A over a frequency-shift equipment, a trip output would occur if positive current and a receiver MARK signal were both concurrently and continuously present for at least one-half cycle (8.33 ms at 60 Hz or 10 ms at 50 Hz). The trip output would be continued for 18 ms to ride over the following half cycle during which the current is negative, and the half cycle after that when the pick-up timing takes place again.

Assuming that the MARK and SPACE signals cannot both be present concurrently then it might be argued that a comparison could be made between the positive half cycle of current and the absence of a receiver SPACE output. Figure 8–2B illustrates this logic.

If the communication equipment happened to be a frequency shift channel so that both the MARK and the SPACE signals were definite outputs, Figure 8–2B would represent a tripping scheme since tripping is predicated on the receipt of a remote MARK or tripping signal. On the other hand, Figure 8–2B would represent a blocking scheme in as much as it will block tripping in the presence of a MARK or blocking signal. It will trip only in the absence of this signal.

The right side of Figure 8–1 illustrates the conditions during an external fault. Referring to Figures 8–2A and 8–2B, neither approach, the blocking or the tripping, will result in a trip output for this condition since the AND circuits will never produce any outputs to the integrator.

The conditions illustrated in Figure 8–1 are ideal. They seldom, if ever, occur in a real power system. Actually, an internal fault would not produce a received signal MARK-SPACE relationship that is exactly in phase with the locally contrived single phase current. This is true for a variety of reasons including the following:

1. Current transformer saturation.
2. Phase angle differences between the currents entering both ends of the line as a result of phase angle differences in the driving system voltages.
3. Load and charging currents of the line.
4. Transit time of the communication signal.
5. Unsymmetrical build-up and tail-off times of the receiver.

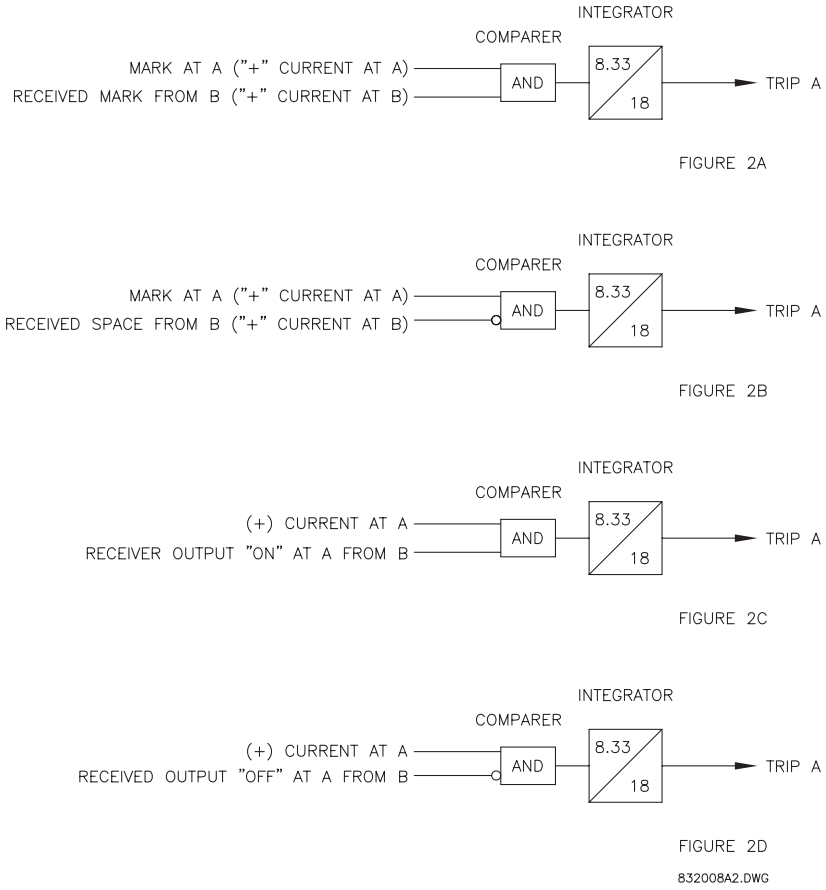


Figure 8–2: TWO-TERMINAL LINE PHASE COMPARISON

Thus, the logic shown in Figures 8–2A and 8–2B would rarely, if ever, produce a trip output on an internal fault because the 8.33 ms (which is the time of a half cycle on a 60 Hz base) requires perfect matching. In actual practice a 3 to 4 ms setting is used rather than the 8.33 setting illustrated. This makes it much easier to trip on internal faults. It also makes it much easier to trip undesirably on external faults. However, experience has indicated that with proper settings and adjustments in the relay such a timer setting offers an excellent compromise. This may be better appreciated if it is recognized that item (a) above is generally minimized and item (b) is nonexistent on external faults.

As shown in Figure 8–3: Stability Angle, a stability angle setting of 3 ms for a 60 Hz system allows for about 65 electrical degrees of blocking zone. This provides sufficient security to prevent tripping in the cases indicated above and provides reliable tripping for all types of internal faults.

In the event that ON-OFF communication equipment were to be employed rather than frequency-shift equipment, the logic would appear as in Figures 8–2C and 8–2D. It will be noted in these two Figures that the reference to MARK and SPACE have been conveniently omitted since the receiver output is either present or not as against the case of the frequency-shift equipment where it could be there in either of two states. Figure 8–2C illustrates a tripping scheme while Figure 8–2D a blocking scheme. Here again, the integrator is, in practice, actually set for 3 to 4 ms.

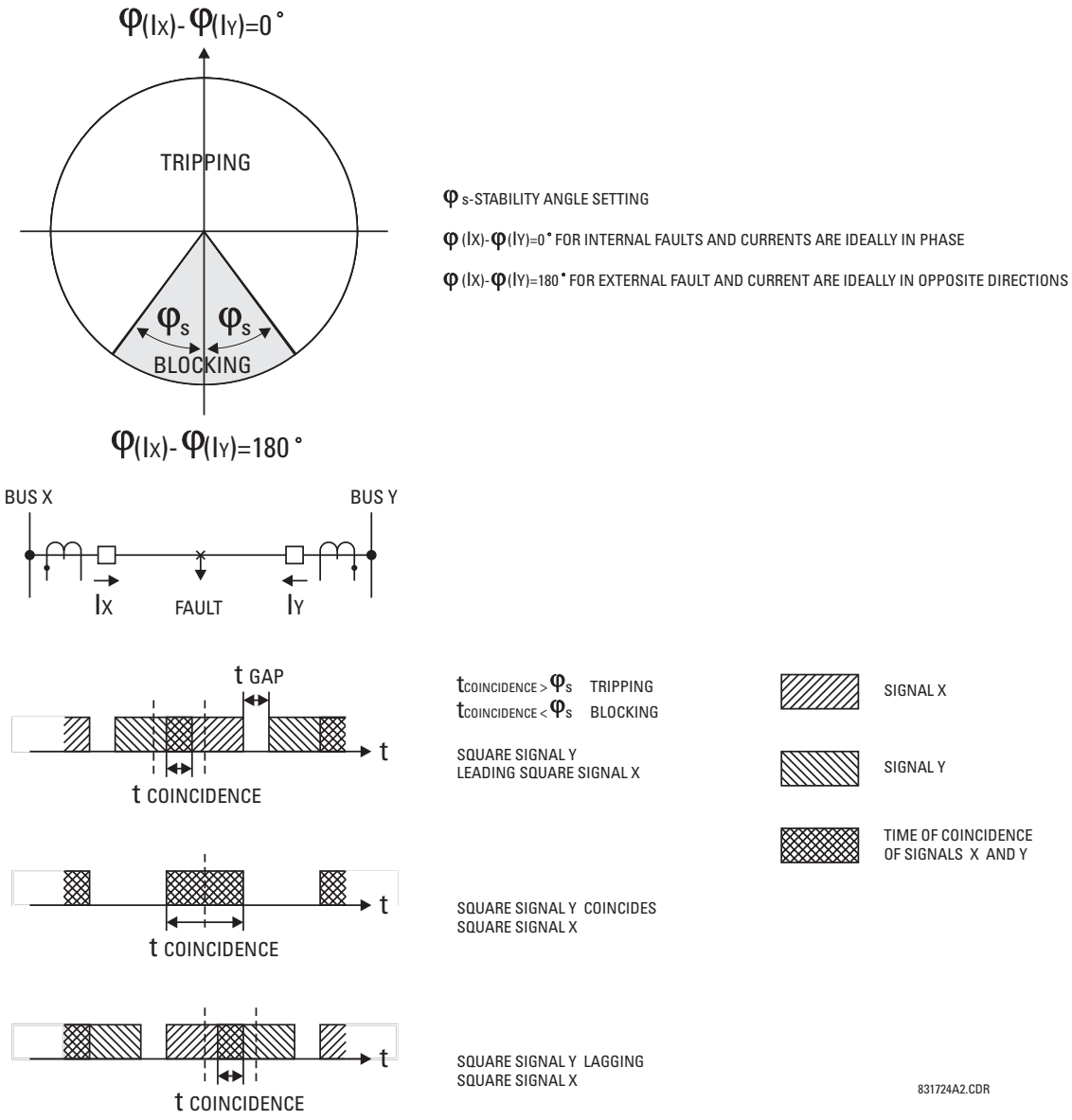


Figure 8–3: STABILITY ANGLE

Figures 8–4A, 8–4B, 8–4C, and 8–4D are for three-terminal lines and they correspond directly to Figures 8–2A, 8–2B, 8–2C, and 8–2D. It will be noted from Figure 8–3 that for a three-terminal line, the relay at A must receive information from both the remote terminals. The same applies to the relays at terminals B and C. As in the case of the two-terminal lines, the integrator illustrated in Figure 8–4 will actually be set for 3 to 4 ms.

While all the sketches in Figures 8–2 and 8–4 compare the positive half cycle of current with a receiver output, the negative half cycle might just as well have been selected. However, if this were done, in Figure 8–2A for example, it would have been necessary to compare the presence of negative current with a received SPACE signal rather than a MARK signal.

It should be recognized that the above discussion, as well as Figures 8–1 and 8–2, are rudimentary. The complete phase comparison scheme is considerably more sophisticated and will be discussed in more detail subsequently. However, at this point it would be well to note that phase comparison on a continuous basis is not permitted mainly because it would tend to reduce the security of the scheme. For this reason, fault detectors are provided. They initiate phase comparison only when a fault occurs on, or in the general vicinity of, the protected line. A simplified sketch of the logic of a phase comparison blocking scheme including fault detectors is illustrated in Figure 8–5. This is a somewhat more fully developed version of Figure 8–2D, and the same logic is present at both ends of a two-terminal line.

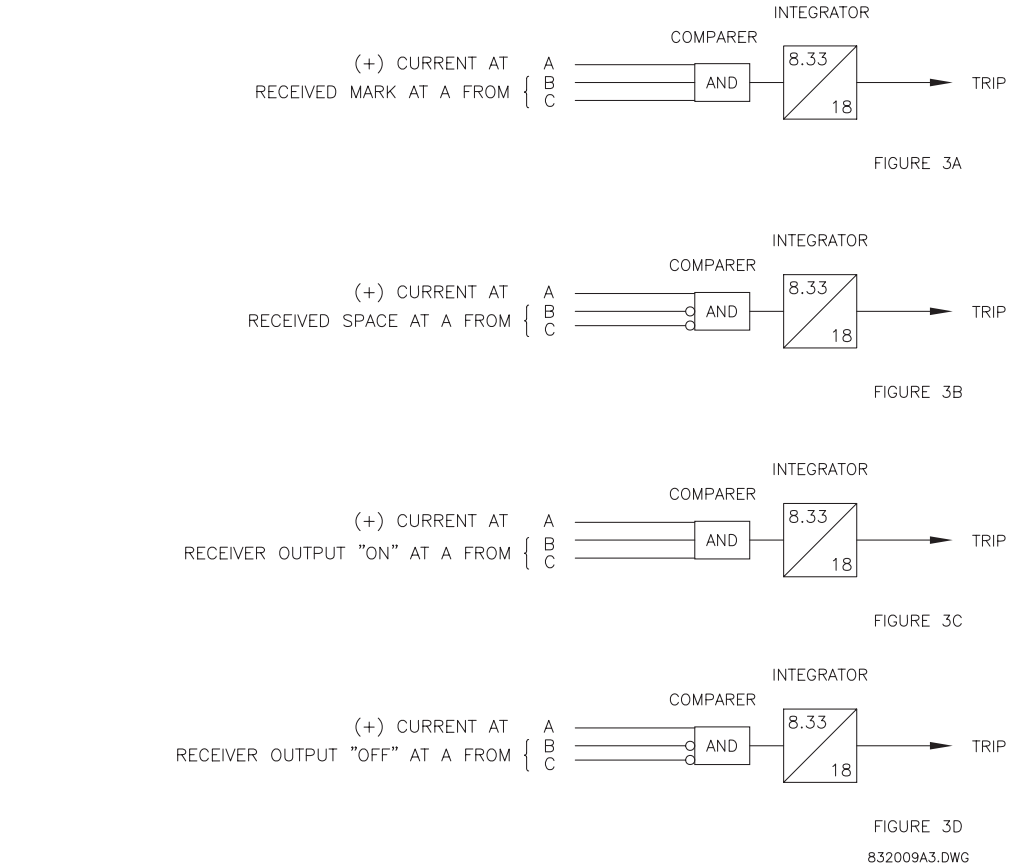


Figure 8–4: THREE-TERMINAL LINE PHASE COMPARISON

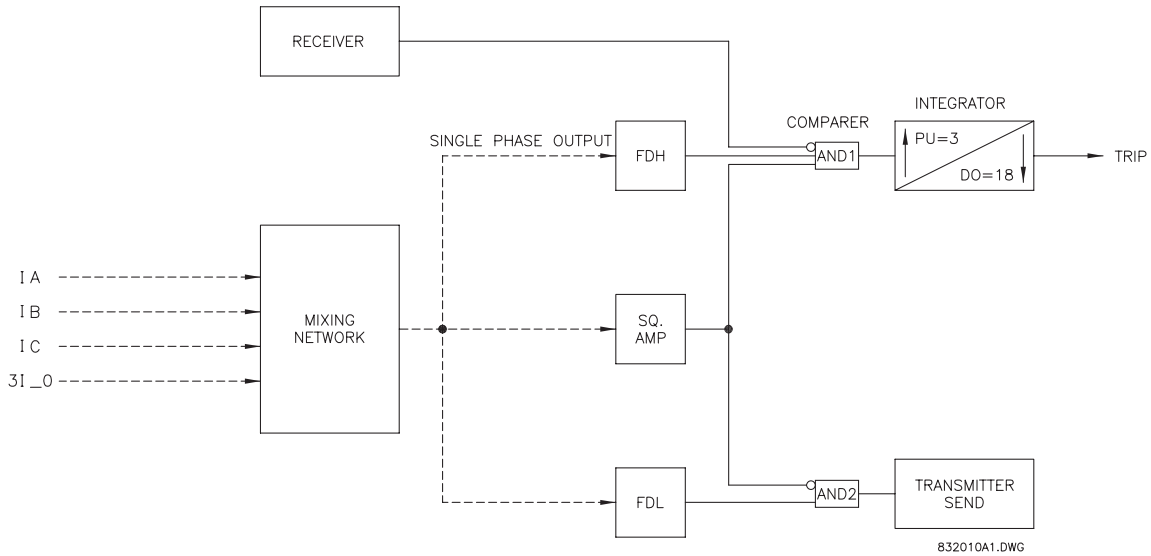


Figure 8–5: SINGLE-PHASE COMPARISON BLOCKING SCHEME PRINCIPLE

It will be noted from Figure 8–5 that AND1 (the comparer) at each end of the line compares the coincidence time of the positive half cycle of current with the absence of receiver output. This is initiated only when a fault is present as indicated by an output from FDH (Fault Detector High-set). FDH is set so that it does not pick up on load current but does pick up for all faults on the protected line section. Thus, when a fault occurs, FDH picks up, and if the receiver output is not present for 3 milliseconds during the positive half cycle of current out of the mixing network, a trip output will be obtained.

Of course, the output from the receiver will depend on the keying of the remote transmitter. The transmitters at all line terminals are keyed in the same manner. They are keyed ON by an output from FDL (Fault Detector Low-set) and keyed OFF by the squaring amplifier via AND2 during the positive half cycles of current. The FDL function is required at all terminals in all phase comparison blocking schemes to initiate a blocking signal from the associated transmitter. This is received at the remote receiver and blocks tripping via the comparer during external faults. FDL has a more sensitive setting and therefore operates faster than the remote FDH function. It is obvious from Figure 8–4 that if an external fault occurred, and FDL did not operate at least as fast as the remote FDH, false tripping could occur because of the lack of receiver output. In general FDL is set so as not to pick up on load current but still with a lower pick up than FDH so that it will operate before FDH. For an internal fault, the currents entering both ends of the line are in phase with each other. Thus, during the half cycle that the SQ AMP is providing an input to AND1, the associated receiver is producing no output, and so tripping will take place at both ends of the line.

For an external fault, the current entering one terminal is 180° out of phase with the current entering the other terminal. Under these conditions, during the half cycles when the SQ AMP is producing outputs, the associated receiver is also providing an output thus preventing an AND1 output. No tripping will take place.

8.1.3 VARIATIONS IN PHASE COMPARISON SCHEMES

There are a number of different phase comparison schemes in general use today and while all of these employ the same basic means of comparison described above, significant differences do exist. These differences relate to the following:

- Phase comparison excitation (component or current to be compared).
- Pure phase comparison vs. combined phase and directional comparison.
- Blocking vs. tripping schemes.
- Single vs. dual phase comparison.

8.1.4 PHASE COMPARISON EXCITATION

a) DESCRIPTION

Before discussing this subject, it is well to consider what takes place in terms of the currents that are available for comparison when a fault occurs on a power system. The table below lists the sequence components of fault current that are present during the various different kinds of faults while Figure 8–6 illustrates the relative phase positions of the sequence components of fault current for the different kinds of faults and the different phases involved.

Table 8–1: FAULT TYPES

TYPE OF FAULT	SEQUENCE COMPONENTS		
	POSITIVE	NEGATIVE	ZERO
Single-Phase-to-Ground	yes	yes	yes
Phase-to-Phase	yes	yes	no
Double-Phase-to-Ground	yes	yes	yes
Three-Phase	yes	no	no

Figure 8–6 shows the relative phase positions of the outputs of a positive sequence network, a negative sequence network, and a zero sequence network all referenced to phase A. The transfer functions of these three networks are given by the following equations.

$$I_1 = \frac{1}{3}(I_a + I_b\angle 120° + I_c\angle -120°)$$

$$I_2 = \frac{1}{3}(I_a + I_b\angle -120° + I_c\angle 120°) \quad \textbf{(EQ 8.1)}$$

$$I_3 = \frac{1}{3}(I_a + I_b + I_c)$$

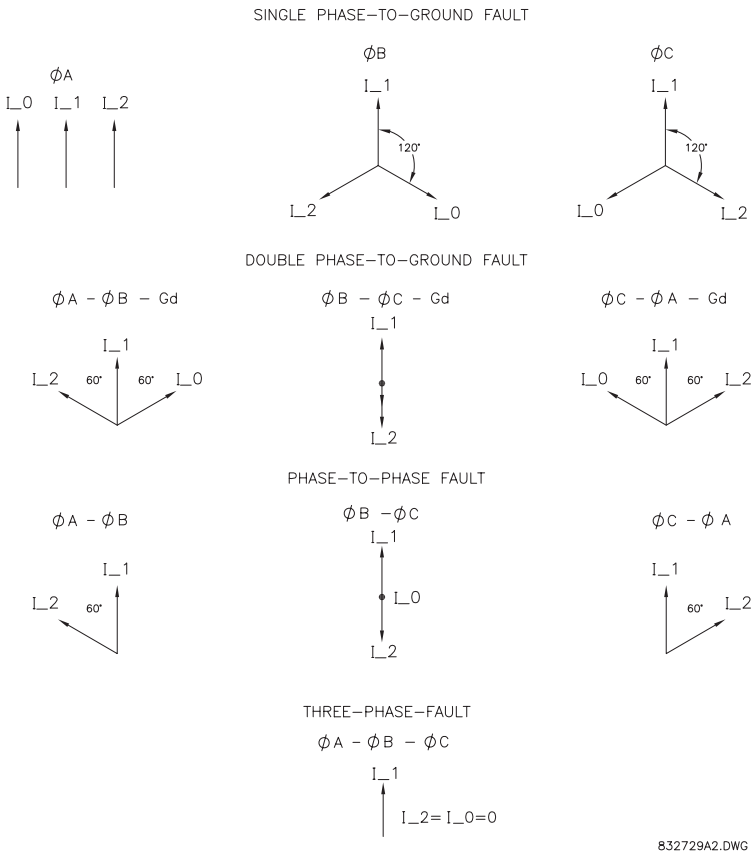


Figure 8–6: SEQUENCE NETWORK OUTPUTS

It is interesting to note that the phase positions of the sequence network outputs differ depending on the phase or phases that are faulted as well as the type of fault. For example, while the positive, negative, and zero sequence components are all in phase for a single-phase-A-to-ground fault, they are 120° out of phase with each other for phase-B-to-ground, and phase-C-to-ground faults.

It will be observed from Table 8–1 that positive sequence currents are available for all kinds of faults, negative sequence currents are available for all but three-phase faults, and zero sequence currents are available only for faults involving ground. Thus, it appears that if one single sequence component of current were to be selected for use to make the phase comparison, the positive sequence component would suffice. Actually, this is not the case in many if not most of the applications because of the presence of through load current during the fault.

For a single-phase-to-ground fault on the protected line, the positive sequence component of fault current entering one end will be in phase with that entering the other end. This is a tripping situation for the phase comparison scheme. However, any load flow across the line during the fault will produce a positive sequence component of load current entering one end of the line that is 180° out of phase with that entering the other end (that is, the positive sequence component of load current entering one end is in phase with that leaving the other end). This is a non-tripping situation for the phase comparison scheme. The phase position of the load component relative to the fault component depends on such factors as the direction of the load flow, power factor of the load flow, and the phase angles of the system impedances. The phase position of the "net" (load plus fault) positive sequence current entering one end of the line relative to that entering the other end will depend on these same factors plus the relative magnitude of the fault and load components of current.

In general, the heavier the fault current and the lighter the load current, the more suitable is the use of pure positive sequence for phase comparison. Heavier line loadings and lower fault currents will tend to make the scheme less apt to function properly for internal faults. Thus, pure positive sequence phase comparison appears practical only in a minority of the cases and so is not suitable for a scheme that is to be generally applicable.

Significant negative sequence currents are present only during faults, they are present in all but balanced three phase faults, and there is no significant negative sequence component of load current. All this combines to make pure negative sequence ideal for phase comparison except that it will not operate for balanced three phase faults. Similar comments may

be made regarding pure zero sequence phase comparison with the additional limitation that it will not operate for phase-to-phase faults. Thus, there does not appear to be one single sequence component or one single phase current that could be used in a phase comparison scheme to protect against all types of faults.

There are a number of different approaches that are possible to provide a complete scheme. Probably, the most obvious would be to make the phase comparison on each phase separately. This is undesirable principally because the cost would be high since three communication channels would be required. Another approach would be to use two separate phase comparison measurements and communication channels, one for pure positive and the other for pure negative sequence currents. The latter would serve to protect against all unbalanced faults while the former would take care of three phase faults and also provide a measure of back-up protection for heavy unbalanced faults. Here again cost is an important factor.

As soon as consideration is given to the use of a separate positive and a separate negative phase sequence comparison, the idea of switching from one to the other presents itself. Such schemes are available. They include detectors separate from the phase comparison function that distinguish between three phase faults and all other types. For three phase faults the negative sequence network is unbalanced so that it produces an output for positive sequence current as well as for negative sequence current. The scheme operates normally to provide negative sequence phase comparison for all unbalanced faults. When a three phase fault occurs, the three-phase detectors at both ends of the line operate to automatically unbalance their respective negative sequence networks and make them sensitive to positive as well as negative sequence currents. Since the fault is three phase, there is no negative sequence current produced so the phase comparison is made on a pure positive sequence basis. This is all accomplished with a common communication channel for both modes.

Another similar approach would be to provide two separate sequence networks, one pure positive sequence and the other pure negative sequence. Then use the three-phase detector to switch the logic so that only for three phase faults the outputs of the positive sequence networks at both ends of the line are compared but for all other faults the negative sequence outputs are compared. Here again all this being accomplished over a common channel. This approach has never been used possibly because of the idea of using “Mixed Excitation.” Mixed Excitation is a term used to describe a phase comparison scheme that mixes the outputs of the different sequence networks in a given proportion and phase angle and then makes a phase comparison for all faults based on this mix. Thus, all such schemes must include positive sequence plus negative sequence and/or zero sequence in order to operate for all faults. The two main questions to be resolved are:

1. Which sequence components should be mixed with the positive sequence?
2. What percentages of the full magnitude of each sequence component of current should be used?

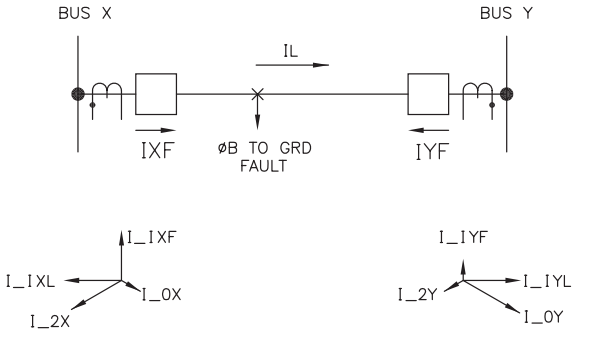
Figure 8-7 illustrates a two-terminal line with an internal phase B-to-ground fault. The phasor diagrams indicate the phase positions of the sequence currents at both ends of the line assuming current flow into the line and also assuming a phase A reference as in equations (1), (2), and (3), previously shown.

At this point it should be recognized that the positive sequence component of current is made up of two parts, the load component (I_1L) and the fault component (I_1F). By an analysis utilizing superposition, the load component (I_1L) may be established as the current flowing just prior to the fault. The three fault components of current (I_1F, I_2F, and I_0F) are then calculated using the voltage that existed at the point of fault just prior to the fault. Since the load component of current is equal to the vector difference between Bus X and Bus Y voltages divided by the impedance of the line, and since the pre-fault voltage (at the point of fault) has a phase position somewhere between that of X and Y voltages, the positive sequence component of fault current will be displaced from the load component by about 90° ± about 30°. The phasor diagrams at the top of Figure 8–7 assume that load current flow is from bus X to bus Y.

The first row of the table in Figure 8–7 indicates that for the conditions assumed, the net positive sequence current entering both ends of the line are about 120° displaced from each other. Heavier fault current and lighter load current would reduce this angle toward zero while the converse would increase the angle toward 180°.

The second and third rows of the table of Figure 8–7 indicate the relative phase positions of the positive plus negative, and positive plus negative plus zero sequence components respectively. These appear to be more unsatisfactory. Rows 4 and 5 combine the components differently and both appear to yield much better results.

It is obvious from Figure 8–6, that a similar fault on a different phase would yield different results. This is illustrated in Figure 8–8 where a phase-A-to-ground fault at the same location is analyzed. As noted earlier, the integrator timers in phase comparison schemes are generally set for about 3 milliseconds. This will permit tripping on internal faults with as much as 115° between the phase angles of the currents entering both ends of the lines. On this basis, only excitation by I_2 – (0.20) × I_1 would prove satisfactory for the two cases studied in Figures 8–7 and 8–8.



SEQUENCE MIXTURE	I X	I Y	ANGLE BETWEEN I X AND I Y
PURE I_1			120°
I_1 + I_2			155°
I_1+I_2+I_0			180°
I_2 – KI_1			35°
I_2–I_0–KI_1			40°

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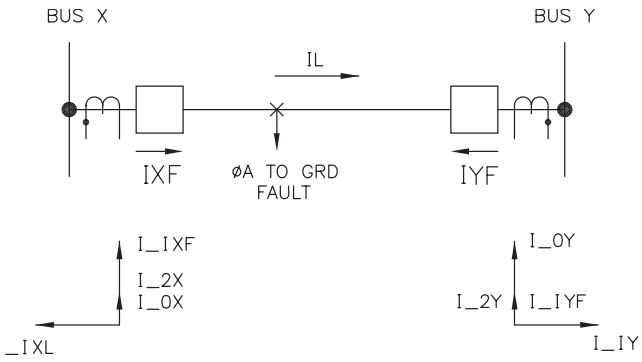
I_IXL=Pos. Sequence Load Component
I_IXF=Pos. Sequence Fault Component
I_IX=I_IXL+I_IXF
K=0.20

Same Applies to IY

Figure 8–7: VECTOR RELATIONSHIPS IN A 2-TERMINAL FAULTED LINE (B-TO-G)



SEQUENCE MIXTURE	I X	I Y	ANGLE BETWEE I X AND I Y
PURE I_1			120° (120°)
I_1 + I_2			85° (155°)
I_1+I_2+I_0			58° (180°)
I_2 – KI_1			70° (35°)
_2–I_0–KI_1			168° (40°)

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Figure 8–8: VECTOR RELATIONSHIPS IN A 2-TERMINAL FAULTED LINE (A-TO-G)

Actually, only two simple faults were investigated. It is obvious that different results would have been obtained for these same kind of faults if the relative magnitudes of load current, positive sequence fault current, and zero sequence fault current had been assumed differently. Also, for the values of currents assumed, different results would obtain for other types of faults. In addition, if different combinations and weighting factors of the sequence components had been investigated still different answers would have resulted. In the proper selection of sequence components and weighting factors for Mixed Excitation phase comparison, the following points must be considered:

- Whatever combination and weighting factors are employed, the application rules should be simple enough to make the application practical.
- As a corollary to the above point, the fewest number of sequence components should be used.
- The effects of load current must be minimized. Thus, negative and/or zero sequence components should be weighted over the positive sequence components.
- The limits of application should be broad enough to render the scheme useful as a protection tool.

In line with the considerations stipulated above, the best overall results using mixed excitation would be attained by using I_2 – KI_1, where K is a constant that is adjustable within limits. While it is likely that the inclusion of zero sequence excitation would be helpful for one case or another, it is not generally employed because the problem of evaluating the overall performance of the scheme would be magnified considerably. This is true mainly because the current distribution in the

zero sequence network is generally quite different from that in the positive and negative sequence networks where the current distributions are approximately the same. For any given fault on a transmission line, the ratio of I_1F / I_2F at any terminal is the same as at any other terminal of that line. This is not true of either I_1F / I_0F or I_2F / I_0F. It is this that makes the use of zero sequence excitation undesirable.

b) MIXED EXCITATION

If the mixing network of Figure 8–5 were designed to produce an output that is proportional to I_2 – KI_1, this logic would then be a simplified representation of a mixed excitation phase comparison scheme. In such schemes, the pick up setting of FDH must be high enough so that the KI_1 output from the mixing network does not result in continuous phase comparison on load current (I_2 is normally zero during normal system conditions). Also, it may be desirable to have FDL set to pick-up at some level above full load so that channel is not keyed on and off continuously during normal load conditions. Since FDH is set higher than FDL, this requirement results in a still higher setting for FDH.

Because FDH controls tripping, this arrangement limits the applicability of the basic scheme to circuits where the minimum three phase fault current is significantly higher than the maximum load current. The requirements for the satisfactory performance of a mixed excitation scheme using overcurrent fault detectors (FDH and FDL) are:

- Both the FDL and FDH fault detectors must be set above full load current.
- All internal faults regardless of type or the particular phases involved must produce enough I_2 - KI_1 to operate FDH at all ends of the line.
- FDL must be set with a lower pick-up than FDH at the remote end(s) of the line for security during external faults.
- The phase angle difference between the I_2 – KI_1 quantities obtained at all terminals of the protected line during all types of internal faults, and for any combination of phases, must be less than 115°.

c) ZERO-SEQUENCE EXCITATION

With zero sequence excitation the phase comparison portion of the overall scheme would not be capable of operating for phase-to-phase and three-phase faults. For this reason the overall protective scheme must include measurement functions that can detect and operate for faults involving any two or more phases. Mho type phase distance functions have typically been employed for this protection.

It should be noted that distance relays designed to operate for faults involving two or more phases will operate for double-phase-to-ground faults and also for certain close-in single-phase-to-ground faults. Thus, it is reasonable to expect that both the phase comparison and distance protection will be activated for many faults.

d) NEGATIVE-SEQUENCE EXCITATION

Since negative-sequence phase comparison protects against all unbalanced faults, the directional comparison functions are required only for three-phase fault protection. However, if these functions are designed to respond to all multi phase faults, then phase-to-phase and double phase-to-ground faults will be protected by both modes while single-phase-to-ground faults will be protected by only the phase comparison mode and three phase faults only by directional comparison.

8.1.5 BLOCKING VS. TRIPPING SCHEMES

a) INTRODUCTION

Earlier discussion in conjunction with Figure 8–2 provides a basis for further consideration of blocking vs. tripping pilot schemes. Figure 8–2C illustrates the comparer integrator logic for a tripping scheme using an ON-OFF type of pilot channel. In order to trip, a receiver output is required to be present during the half cycle that the local current is positive. Figure 8–2D is representative of a blocking pilot scheme where tripping will take place if there is no receiver output during the half cycle that the local current is positive.

If we consider that an input to, or an output from, a logic box is a positive going signal, the logic illustrated in Figures 8–2A and 8–2C assume that a received signal at the input of a receiver will produce a positive going voltage signal at the output of the receiver to the relay logic. This is not always true. Some types of receivers will produce negative (or reference) voltage outputs when a signal is present at the input, and a positive signal output when nothing is received. If this were the situation in Figure 8–2, Figure 8–2B would then represent a blocking scheme. In some applications where receiver outputs are inverted, the interface between the receiver and the relay logic includes an inverter (INV) which in effect inverts the receiver output signal so that a received signal produces a positive going signal at the output of the inverter. The same general statements regarding signal polarities applies to the keying requirements for transmitters. Some transmitters may require a positive signal while others a reference or negative signal to key them off of their quiescent states.

The main point to be gained from the foregoing discussion is that it is not always possible to determine from a logic diagram whether a scheme is of the blocking or tripping type unless an indication is given as to the receiver output voltages. This applies to frequency shift as well as ON-OFF communication equipment.

It will become apparent from subsequent discussion that it is extremely difficult, if not impossible, to provide a concise rigorous definition of the terms Blocking Scheme and Tripping Scheme. Possibly it would be well to proceed with a discussion of the different kinds of channels, their characteristics, and their application before attempting a definition.

b) CHANNEL TYPES

The total channel is composed of the communication equipment itself plus the path or link over which the signal is sent. For relaying purposes there are two basic types of communication equipment.

1. ON-OFF
2. Frequency-shift

The ON-OFF type, as the name implies, operates with the transmitter either being keyed on or off by the relay logic. That is, the transmitter at any given instant is either sending an unmodulated signal or it is sending nothing.

There are two types of frequency-shift equipment. The most prevalent is the two-frequency kind. With this type, the transmitter can send either of two closely spaced frequencies. When no keying signal is applied to the transmitter, it sends one of these two frequencies. When the transmitter is keyed, it shifts to the other frequency. It is always sending one or the other. The frequency-shift receiver has two separate outputs, one for each of the two transmitted signal frequencies. Thus, if the transmitter is sending the MARK frequency, the MARK output is present in the receiver. If the transmitter is sending the SPACE frequency, the receiver SPACE output is present. These types of receivers are basically FM receivers and utilize discriminators. Because of this, the SPACE and MARK outputs from the receiver cannot both be present simultaneously. Also, broad band noise at the input to the receiver tends to provide a balanced signal to the discriminator which forces its output towards zero. If the noise is severe enough to swamp out the real signal, it can cause random receiver output or all output to disappear.

The other kind of frequency-shift equipment is a three-frequency type. When this type of transmitter is in its quiescent state, it sends the center frequency. It has two separate keying inputs so that it can be keyed to shift high or low (MARK or SPACE) from the center frequency. The three-frequency receiver receives all three frequencies but provides only two outputs to the relay logic, the high shift and low shift outputs. When the receiver receives the center frequency neither the high nor low outputs are present. Here again the MARK and SPACE outputs (high and low) cannot both be present simultaneously, and severe broad band noise at the receiver inputs can result in receiver output.

There are several characteristics of communication equipment directly related to phase comparison relaying performance that might well be discussed. Phase comparison types of schemes compare the phase angle of a current derived at one end of a line with a communication signal received from the remote end. The communication signal arrives in a MARK-SPACE arrangement that should represent the positive and negative half cycles of current at the transmitted end of the line. Actually this is not possible for several reasons:

1. There is a time lag from the instant a transmitter is keyed until the output reflects a change. This build up is generally a very short time and is usually insignificant.
2. There is the propagation time from the instant the transmitter sends until this signal arrives at the remote location, approximately 1 millisecond for every 290 km (180 miles) of distance. The same applies from the instant the transmitter stops until the remote signal is gone.
3. There is the build up time in the receiver from the instant the signal appears at its input until the output reflects the change of state. This time plus the build up time in the transmitter is called the channel operating time.
4. There is the tail off time in the transmitter from the instant the keying is removed until the output signal changes or disappears. This is generally very short and is usually insignificant.
5. There is the tail off time in the receiver from the instant the input changes until the output changes accordingly. This time plus the tail off time of the transmitter is called the channel release time.
6. In ON-OFF channels the operating and release times are not generally the same. They can vary with frequency and attenuation.
7. In frequency-shift channels the discriminator employed in the receiver can be balanced so that build up and tail off times are equal, or it can be unbalanced (biased) to the MARK or SPACE side. For example, if it is biased toward MARK and the input signal is symmetrical (half cycle MARK and half cycle SPACE), the output will be more than a half cycle MARK and less than a half cycle SPACE.

8. In general wide band channels tend to operate and release faster than narrow band channels. That is, faster channels use more spectrum than slower channels.

It is obvious from the foregoing that the received signal at any given terminal is not an exact analog of the remote current. There are techniques used in phase comparison schemes to compensate for this and they will be discussed subsequently. Until then it should be assumed that the received signal provides a true representation of the phase position of the remote current.

c) TYPES OF COMMUNICATIONS MEDIA

The communication medium over which the transmitted signal is propagated to the remote receiver can take several forms:

1. Directly over the power line (Power Line Carrier)
2. Multiplexed over the power line (Single Side Band Carrier)
3. Multiplexed over microwave (Microwave)
4. Pair of Wires (Pilot Wire)
5. Leased Facilities: (a) Metallic pilot wire
   (b) Microwave
   (c) Cable

A distinction is made between leased facilities and the other (power company owned) facilities because in many cases the telephone company defines the characteristics of the channel without defining the type of link.

The ON-OFF type of communication equipment is used exclusively over power line carrier links. The transmitted signal is propagated along the power line between the transmitter and the remote receiver. This equipment usually operate in the frequency range of 30 to 200 kHz.

Frequency-shift equipment is available in several frequency ranges. First there are those in the audio range. These are generally employed over single side-band, microwave, pilot wires, and leased facilities. There are also frequency shift channels in the power line carrier frequency range. These are employed directly over the power line as are the ON-OFF types of equipment. Finally there is the frequency shift equipment that operate in and occasionally outside the power line carrier spectrum. These are employed over microwave and leased facilities.

d) POWER LINE CARRIER MEDIA

It is obvious that the performance of any channel that utilizes the protected power line itself as a communications medium will be affected in some way by faults on the power line. A fault on a transmission line can attenuate or completely block a signal, transmitted at one end of the line, from being received at the remote end. Faults external to the protected line have no affect on the signal attenuation since transmission lines that incorporate power line carrier channels are trapped at each end (See Figure 8-9).

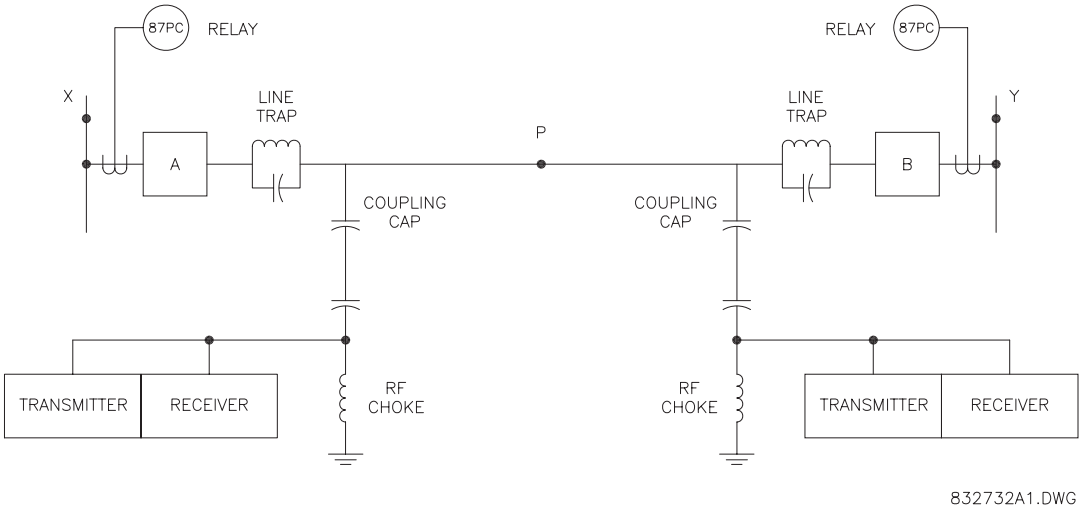


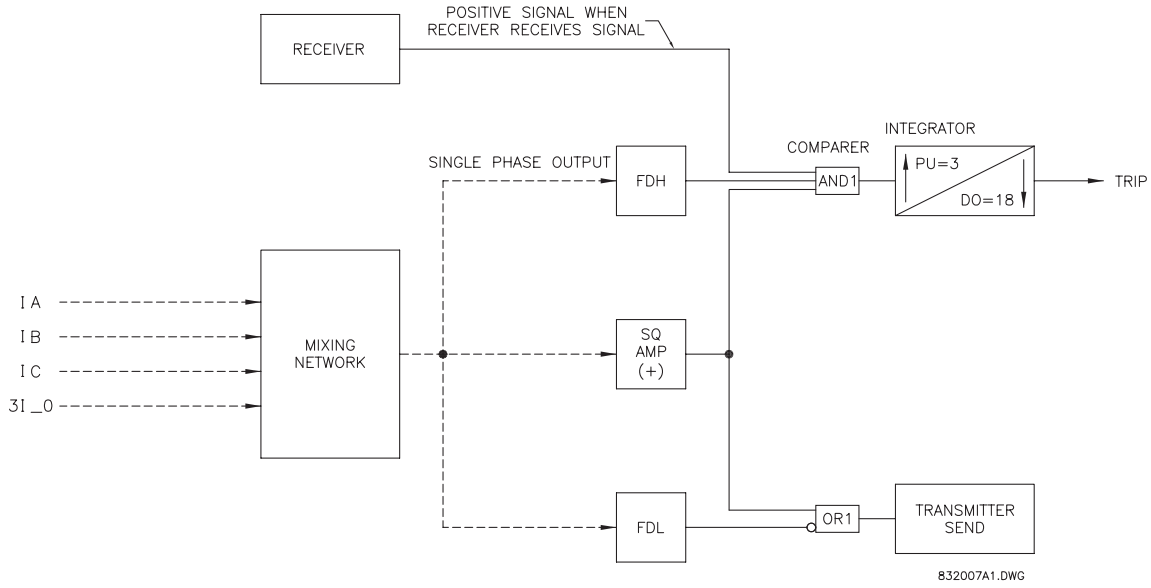
Figure 8–9: TYPICAL POWER LINE CARRIER ARRANGEMENT

In the case of ON-OFF power line carrier channels, the operating frequencies of the equipment at all terminals of the protected line are generally the same. Thus, a signal transmitted from any terminal is received at all terminals. This is not a necessary requirement for using this kind of equipment. Rather it is desirable because the protection schemes that use ON-OFF channels can accommodate a single frequency arrangement and this conserves the carrier spectrum.

When frequency-shift equipment is used over power line carrier, the frequencies of each transmitter on the line must be different from all the others on the same line. For example, if the communication equipment in Figure 8-8 is of the frequency-shift type, the transmitter at the left end must operate at the same frequencies as the receiver at the right end. Also, the right end transmitter and left end receiver must operate at the same frequencies while the frequencies of the two transmitters must be different. This is necessary because with frequency-shift equipment the transmitters associated with a given line protection scheme are not all generally sending the MARK or the SPACE frequencies at the same time. Thus, if a receiver were able to receive more than one transmitter, it could be simultaneously receiving a MARK signal from one and a SPACE signal from another.

This would not result in a workable protection scheme. When power line carrier channels are used, significant losses are present in the coupling equipment and the line itself. Depending on these losses and the ambient noise on the line, the transmitter power required may vary from about 1 to 10 watts and even more in extreme cases.

Consider an ON-OFF tripping type of scheme as defined by Figure 8-10. For a moment assume that FDL and NOT1 do not exist in the logic. During an internal fault, the currents out of the mixing (or sequence) networks at both ends of the line are in phase with each other so that the outputs of the SQ AMP are in phase at both ends of the line. The transmitters at both ends of the line are keyed on during the same half cycles that their associated SQ AMPs are attempting to trip via AND1. Thus, the receivers will be supplying the bottom input to AND1, and tripping will take place when FDH operates to provide the third input.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP(+) – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SINGLE PHASE CURRENT OUTPUT FROM THE MIXING NETWORK EXCEEDS THE PICK–UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SINGLE PHASE CURRENT OUTPUT FROM THE MIXING NETWORK EXCEEDS THE PICK–UP SETTING.

SQ. AMP(+) – PROVIDES AN OUTPUT ONLY ON THE POSITIVE HALF CYCLE.

NOTE: THIS SCHEME REQUIRES TRANSMITTERS OF DIFFERENT FREQUENCIES AT EACH LINE TERMINAL SO THAT A RECEIVER CANNOT RECEIVE.

Figure 8–10: SINGLE-PHASE COMPARISON TRIPPING SCHEME PRINCIPLE

For external faults, the currents out of the mixing networks at the two ends of the line will be 180° out of phase with each other. Therefore, during the half cycle that the SQ AMP at one end of the line is producing an output, the one at the remote end is not, so no tripping will take place. It should be noted that a tripping type of scheme over an ON-OFF channel requires transmitters of different frequency at each end of the line so that no receiver can receive the locally-transmitted signals; otherwise tripping would occur during external faults. For this reason, such schemes are not generally applied.

It appears that the tripping scheme as described above has no need for an FDL function since no blocking coordination is required as is in a blocking scheme. However, this is not the case. The FDL and NOT1 functions provide a means for tripping when one end of the line is open as when picking up a faulted line from one end. For such a condition, the SQ AMP at the open end receives no current and so produces no output to key its transmitter. Without a received signal the closed end of the line cannot trip under any conditions even in the presence of a fault. The FDL function acts as a current detector. It is set with a very low pick up so that any significant output from the mixing network causes it to produce a continuous output. When the mixing network outputs goes to zero, FDL drops out causing an output from NOT1 which in turn keys the transmitter on continuously. This is received at the remote end to provide a continuous signal at the bottom input to AND1. Any fault that picks up FDH will then be tripped at the closed end of the line.

If the mixing network includes a positive sequence output, load current will keep FDL picked up continuously. If the mixing network includes only zero and/or negative sequence outputs, load current will not keep FDL picked up. Thus, with zero or negative sequence phase comparison the receivers at both ends of the line will be producing outputs to AND1 continuously. When a fault occurs, FDL picks-up very fast to restore the keying function to SQ AMP. This operation resembles a blocking scheme, although it is often called a permissive tripping scheme.

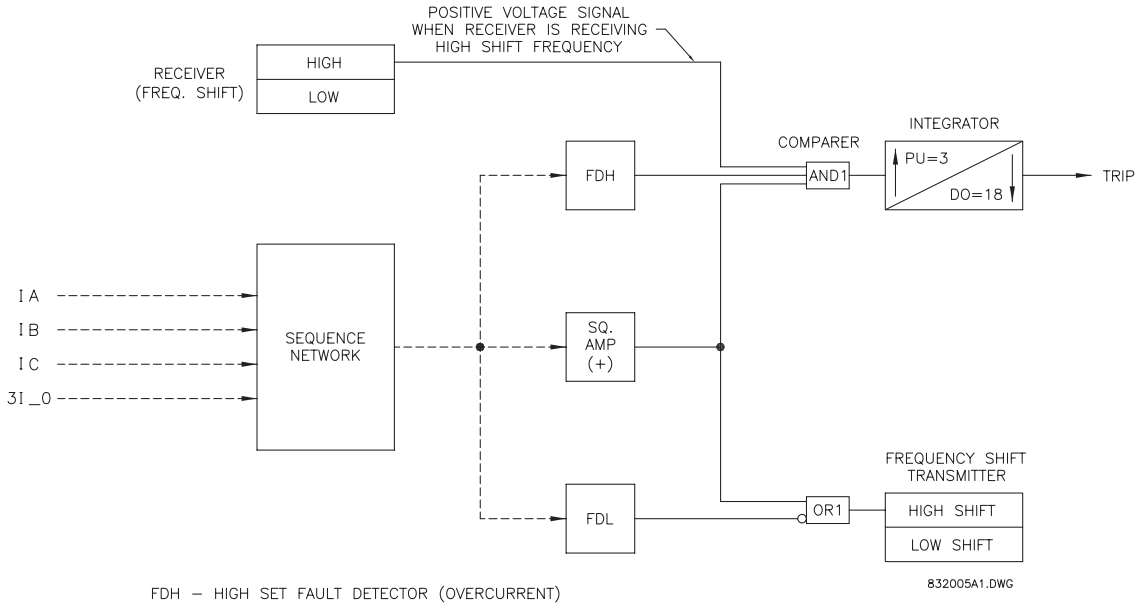
Another scheme to facilitate tripping on single end feed, uses a circuit breaker 52/b switch rather than FDL and NOT1. When the breaker is open, the 52/b switch closes and keys the associated transmitter on continuously. When the breaker is closed, the 52/b switch is open and keying is under control of the SQ AMP. While on the surface the use of 52/b appears simple and direct, the following problems arise that can require more complex logic and station wiring:

1. The 52/b contacts do not generally operate in synchronism with the main poles of the breaker so some timing functions must be included with the logic to compensate for this.
2. In multi-breaker schemes, such as ring buses, two breakers at each terminal are associated with each line so 52/b switches from each breaker are required in series.
3. In multi-breaker schemes one of the two breakers may be out of service but in the closed position. This would require a bypass of its 52/b switch which is open.

Regardless of which tripping scheme is used, it is obvious from Figure 8-9 that in order to trip either circuit breaker A or B for an internal fault at P it is necessary to get a carrier signal through the fault. If the fault attenuates the signal so that this does not happen, no tripping can take place. The amount of attenuation in signal that is produced by the fault will depend on the type of coupling (single phase, interphase, etc.), the type of fault, the phase involved, and the location of the fault on the line. The evaluation of these factors is outside the scope of this discussion.

Figure 8-11 illustrates the same tripping scheme as Figure 8-10 except that it utilizes a frequency shift rather than an ON-OFF communication set. The same comments apply to this scheme as do to that of Figure 8-9. A tripping scheme that operates over a power line carrier channel runs the risk of a failure to trip on internal faults because of signal attenuation. During external faults the line traps isolate the signal on the protected line from the fault. This is of no significance because attenuation or loss of signal on external faults cannot result in any maloperations. Conversely, a blocking scheme is unaffected by loss or attenuation of signal during internal faults because absence of a signal is required in order to trip. During external faults it is important that the blocking signal be isolated from the fault because loss of the signal can result in a false trip. The line traps provide this isolation.

Figures 8-5 and 8-12 illustrate phase comparison blocking schemes with ON-OFF and frequency-shift channels respectively. Figure 8-5 was discussed earlier and Figure 8-12 is exactly the same except for the high frequency shift which is not used in the protection scheme. While only one of the two frequencies of the frequency-shift equipment is used in the protection scheme, the second frequency does perform a useful function. It provides a means for continuous monitoring of the channel. Since one of the two frequencies is always being transmitted, it is possible to monitor the signal at each receiver continuously and incapacitate the protective scheme and/or provide indication at that terminal if the signal is lost.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

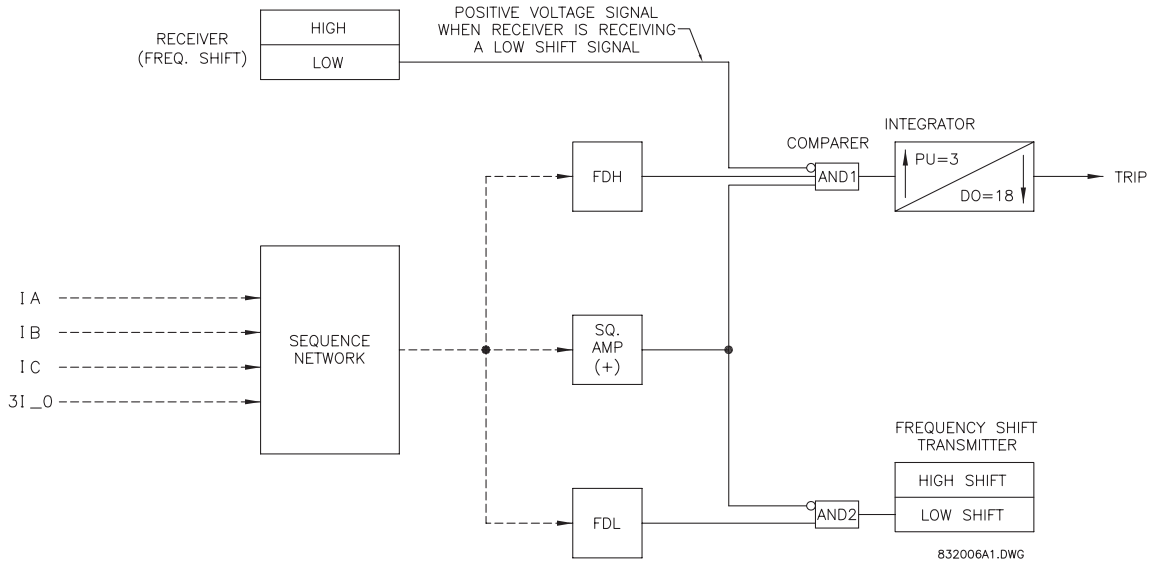
SQ. AMP(+) – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

SQ. AMP(+) – PROVIDES AN OUTPUT ONLY ON THE POSITIVE HALF CYCLE.

Figure 8–11: SINGLE-PHASE COMPARISON TRIPPING SCHEME



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

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SQ. AMP(+) – SQUARING AMPLIFIER

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FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

SQ. AMP(+) – PROVIDES AN OUTPUT ONLY ON THE POSITIVE HALF CYCLE.

Figure 8–12: SINGLE-PHASE COMPARISON BLOCKING SCHEME

Most schemes that use an ON-OFF channel are arranged so that no transmission takes place during normal conditions (no fault). This does not lend itself to continuous monitoring. However, schemes are available that periodically start transmission of a signal at one end of a line which, when received at the remote end, initiates a return transmitted signal. Such schemes can be started manually or automatically on a time schedule. They are called carrier check-back schemes. They can be arranged so as not to affect the normal operation of the scheme even in the event of a fault during a check-back operation.

For the most part, phase comparison blocking carrier schemes use ON-OFF rather than frequency-shift channels, possibly for one or more of the following reasons:

1. The overall speed of the protective scheme is directly related to the speed of the channel. Until recently high speed frequency shift carrier channels were not available. Even today the ON-OFF channel is somewhat faster than the fastest frequency-shift channel.
2. Noise at the input of an ON-OFF channel receiver would tend to produce a blocking signal output. Noise at the input of a frequency-shift channel tends to drive its output to zero which is a tripping condition (in a blocking scheme). This tends to make the frequency-shift blocking scheme less secure against false tripping during external faults. It is possible to build channel condition detectors (signal to noise, loss of channel, etc.) into frequency-shift channels and block tripping when these detectors indicate trouble, but these features increase the complexity and the cost. This approach tends to make the blocking scheme resemble the tripping scheme since the receiver must now indicate an intact channel in order to trip.
3. Aside from the ability to accommodate continuous monitoring, the frequency-shift channel provides little advantage over the ON-OFF carrier channel.

There are very few if any phase comparison tripping schemes in service over carrier channels mainly because of the fear that it will not always be possible to get a trip signal through a fault.

Another scheme that has recently been gaining some favor is the *unblocking scheme*. It is a cross between blocking and tripping, in that it operates in the blocking mode but the blocking signal is sent continuously even in the quiescent state (no fault), and so it must be turned off in order to trip. Thus this scheme, as in the tripping schemes previously described, must include some means to stop the blocking signal from being transmitted at an open terminal in order to permit tripping of the closed remote terminal in the event of a fault. Here again the FDL logic of Figures 8-10 and 8-11 or the circuit breaker auxiliary 52/b switch could be used.

In general, unblocking utilizes frequency-shift channels because this permits monitoring of the continuous blocking signals. As they are usually applied, ON-OFF channels do not lend themselves to monitoring because the single frequency system transmits the same frequency from all transmitters and the loss of any one transmitter could not be detected. If applied in a normal duplex frequency basis (one in each direction) the ON-OFF channel would provide the monitoring features at the cost of carrier spectrum. However, this disadvantage can be overcome by the use of a new application of ON-OFF equipment where the transmitters at the different terminals are operating at frequencies offset from each other yet close enough to be nominally a single frequency system. This application permits monitoring, and at the same time has the advantage of a higher channel speed than the frequency-shift channels, while utilizing less channel spectrum in three terminal line applications.

e) MICROWAVE LINKS

Microwave links are quite commonly used for protective relaying including phase comparison schemes. However, because of the high cost of the microwave equipment, the applications are generally limited to cases where a large number of control and/or monitoring functions are needed between the same terminals as the relaying.

Since microwave links propagate through the atmosphere, rather than over the power line, they are generally unaffected by faults and noise on the power system. Thus, with a microwave link there is no problem of getting a signal through the fault, so tripping type schemes are very acceptable. On the other hand, since there is a possibility of fading of the microwave signal, there is some reluctance to use it in blocking schemes for fear of false tripping in the event of a fade during a nearby external fault. However, blocking schemes are used occasionally mainly because the tripping scheme requires special circuitry (as described earlier) in order to trip on single-end feed to a fault.

The communication equipment multiplexed on to a microwave system for protective relaying is invariably of the frequency-shift type, and usually of the high speed variety. Figures 8-11 and 8-12 are representative of the tripping and blocking schemes respectively. Since, as mentioned above, the microwave signal can fade, some of the frequency-shift receiver equipment includes channel status detectors that operate into the relay logic to incapacitate all tripping when the channel conditions are not normal. The ability to trip is then automatically reinstated when normality returns. With such an arrange-

ment, complete loss of receiver output would incapacitate tripping. If the scheme were a blocking scheme similar to that of Figure 8-12, complete loss of channel during an external fault would permit a false trip unless an incapacitating feature were included in the scheme.

The receiver has only two outputs (high and low). Since the scheme trips on internal faults during the absence of the low-shift output, and since the absence of both the low and high shift outputs incapacitates tripping (where used), the implied requirement for tripping is the presence of the high-shift receiver output. While such a scheme is called a blocking scheme it appears to be, at least by implication, a tripping scheme.

In any case, there is nothing about a microwave channel to alter the previous discussion concerning phase comparison protection. The same basic schemes may be used with the understanding that the microwave signal can fade on occasion. For the most part, phase comparison relaying schemes over microwave channels have been of the tripping types.

f) PILOT WIRE LINKS

There are few, if any, privately owned pilot wires that are used as a link in phase comparison schemes. However, such applications would require a frequency-shift communication equipment used in either a tripping or blocking mode as indicated in Figures 8-11 and 8-12 respectively. Aside from the considerations involved in tripping for a fault with single-end feed, which were discussed previously, the selection between a blocking and a tripping scheme will generally result from a compromise between security and reliability. In order to make such a selection, consideration of the pilot pair, its protection, and its physical location in relation to power conductors must be evaluated.

In general, a high speed channel would require pilot wires that have a frequency response that is somewhat better than the standard telephone voice circuits.

Possibly because of the uncertainties of channel characteristics, plus the availability of pilot wire relays that are much lower in overall cost, phase comparison over privately owned pilot wires is not a common application.

g) LEASED (TELEPHONE COMPANY) FACILITIES

There has been some use of phase comparison relaying over leased facilities including voice grade pilot wire circuits. In general, if a customer requires or specifies the characteristics of a leased channel, the local telephone company could provide this link over microwave, cable, even pilot wires, or a combination of these. In such cases the selection between tripping: and blocking schemes will depend on the performance of the channel as specified. The same basic schemes of Figures 8-11 and 8-12 would apply.

h) FIBER OPTICS

Fiber optic communications links are quite commonly used for protective relaying schemes. Since fiber optic links propagate through the fiber, rather than over the power line, they are generally unaffected by faults and noise on the power system. Thus, with a fiber link there is no problem of getting a signal through the fault, so tripping type schemes are very acceptable. An exception may occur when the fiber optic is embedded in the ground wire used on the line. In this case, the fault may be a result of a break in the ground wire which would prevent transmission of the signals.

In any case, there is nothing about a fiber channel to alter the previous discussion concerning phase comparison protection. The same basic schemes may be used with the understanding that the fiber optic signal can be lost on occasion. For the most part, phase comparison relaying schemes over fiber optic channels are of the tripping types.

i) SUMMATION OF BLOCKING VS. TRIPPING SCHEMES

The foregoing discussion of blocking and tripping schemes was presented without the benefit of a concise definition of these terms. As indicated in the discussion, the difficulty of making such definitions which would always apply is brought about by the channel status feature used in some frequency-shift blocking schemes. Such arrangements tend to be hybrids. Thus, the following simple definitions exclude any considerations of channel status features:

1. A blocking scheme is one that requires a specific output signal from the associated receiver in order to block tripping. Tripping can only take place during the time that this signal is absent.
2. A tripping scheme is one that requires a specific output signal from the associated receiver in order to permit tripping. Tripping can only take place during the time that this signal is present.
3. Where channel status logic is used, these definitions will have to be modified to meet the exact logic of the scheme.

In general, the selection of a blocking or a tripping scheme is one that should be made in conjunction with the chosen channel and with a knowledge of the channel characteristics in the face of system noise. Many different combinations are possible, but of these, only a selected few will meet any given set of requirements.

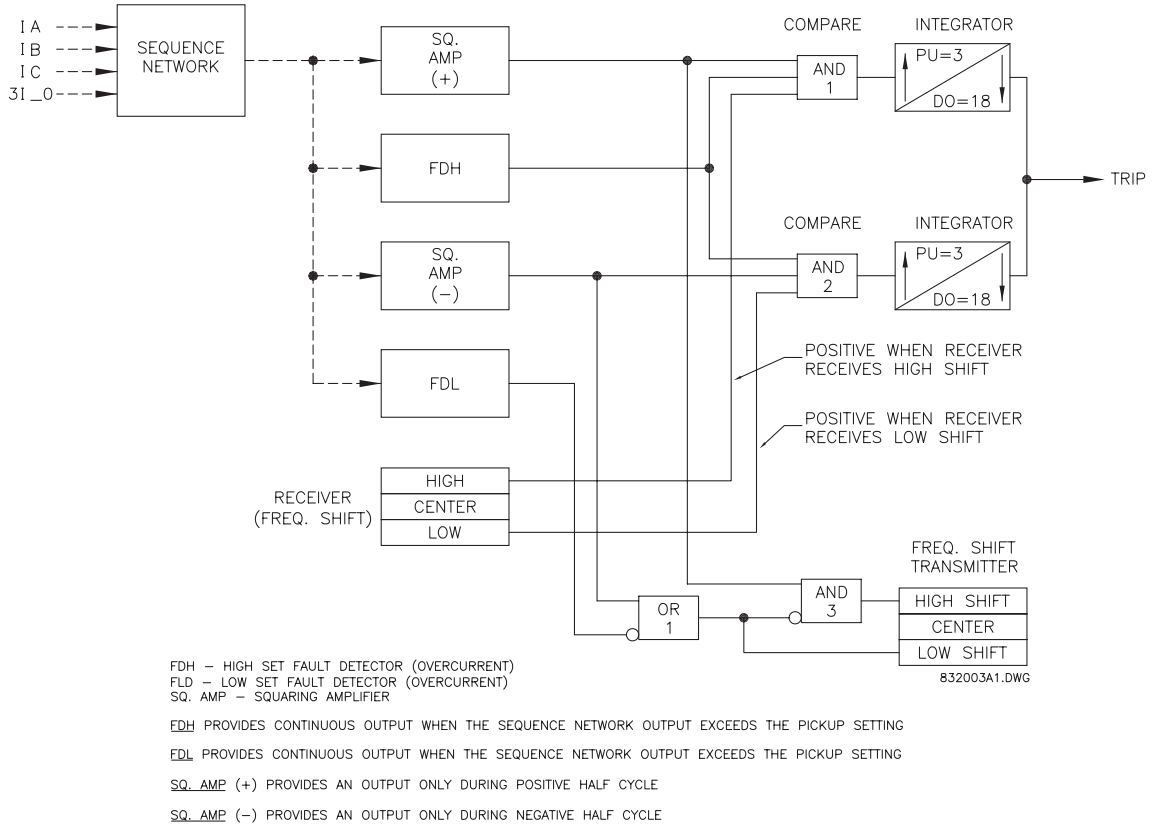
8.1.6 SINGLE VS. DUAL PHASE COMPARISON

In all the phase comparison schemes described so far, a trip attempt is made only every other half cycle. In the examples illustrated, this was every positive half cycle. Such schemes are termed single phase-comparison as against dual phase-comparison where a trip attempt is made every half cycle, positive and negative.

The only advantage of dual-comparison is that its maximum operating time to trip on internal faults will be a half cycle faster than the maximum time for the single phase-comparison. The minimum times for both schemes will be the same. This difference in maximum time results because a fault could occur at such an instant in time when the current is just going negative. Under such conditions, the single phase-comparison would have to wait till the next positive half cycle while the dual phase-comparison could trip on the upcoming negative half cycle.

While, as a general rule, high speed operation and security are on opposite sides of the coin, it is possible to design dual phase-comparison schemes that can provide the added speed with little or no loss in security. However, these schemes are somewhat more complex than equivalent single phase-comparison schemes. Figure 8-13 illustrates the dual phase-comparison tripping scheme that is the counterpart of the single phase-comparison scheme of Figure 8-11. The differences are noted below.

1. The dual scheme uses two separate comparer integrator combinations, one for the positive half cycle and the other for the negative half cycle.
2. A three-frequency, frequency-shift channel is used in dual phase comparison. The high-shift operates in conjunction with the positive half cycle while the low-shift works with the negative half cycle. When the channel is not keyed to either high or low, it operates on the center frequency. There is no center frequency output from the receiver into the relay tripping logic.
3. AND3 is included to make it impossible to key both frequencies simultaneously. It also gives preference to the low-shift which is sent continuously when FDL is dropped out. Thus, on single-end feed tripping can take place only on the negative half cycle.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)
FLD – LOW SET FAULT DETECTOR (OVERCURRENT)
SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICKUP SETTING

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICKUP SETTING

SQ. AMP (+) PROVIDES AN OUTPUT ONLY DURING POSITIVE HALF CYCLE

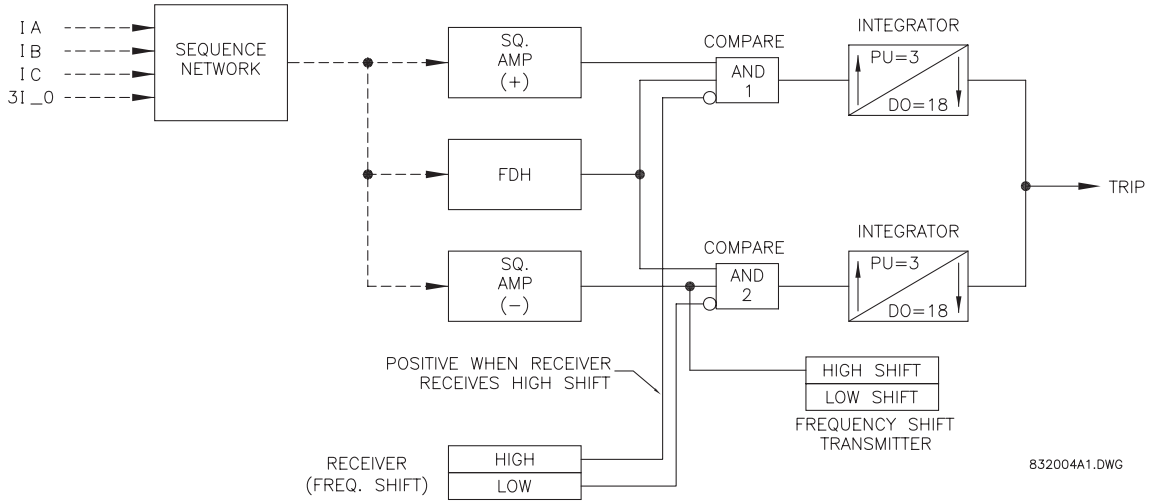
SQ. AMP (−) PROVIDES AN OUTPUT ONLY DURING NEGATIVE HALF CYCLE

Figure 8–13: DUAL PHASE COMPARISON TRIPPING SCHEME

The center frequency, while not actually used in the relay tripping logic, adds security to the scheme during transient conditions.

The dual phase-comparison scheme of Figure 8-13 could be modified to operate over a two-frequency, frequency shift channel by eliminating AND3, FDL, NOT1, and the center frequency. The transmitter could then be arranged to send the low-shift frequency continuously except when keyed by the positive SQ. AMP to the high shift frequency. This arrangement, though simpler than the three frequency scheme, is deemed to be less secure.

Figure 8-14 illustrates a dual phase-comparison blocking scheme using a two-frequency, frequency-shift channel. Since one or the other of the two frequencies must be on at all times, and since both are blocking frequencies, there appears to be little need for an FDL function. Thus, it is not included. When the transmitter is not keyed, it sends low-shift continuously and when it is keyed by the negative squaring amplifier, it shifts to high for the negative half cycle. This scheme is simpler than that of Figure 8-13 but probably is not as secure.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICKUP SETTING

SQ. AMP (+) PROVIDES AN OUTPUT ONLY DURING POSITIVE HALF CYCLE

SQ. AMP (−) PROVIDES AN OUTPUT ONLY DURING NEGATIVE HALF CYCLE

Figure 8–14: DUAL PHASE COMPARISON BLOCKING SCHEME

There does not appear to be any good purpose for a three-frequency channel in dual phase-comparison blocking schemes since the center frequency would not add to the security, or otherwise improve the performance.

It is interesting to note that a dual phase-comparison scheme using an ON-OFF channel would have to be a combined blocking and tripping scheme. During one polarity of half cycle, it would have to trip on absence of any received signal (blocking), and on the other polarity of half cycle, it would have to trip in the presence of the received signal.

In general, it may be concluded that dual phase comparison may be accomplished in the blocking and in the tripping modes. The overall performance of the scheme will be dependent on the characteristics of the channel selected. While dual phase-comparison will reduce the maximum tripping time, it does so at the expense of simplicity and possibly some security depending on how it is accomplished.

There are a number of standard refinements that are required and normally included in all phase comparison schemes. These will be discussed in terms of the basic blocking scheme of Figure 8-4, but will apply generally to all schemes, sometimes in a somewhat different form.

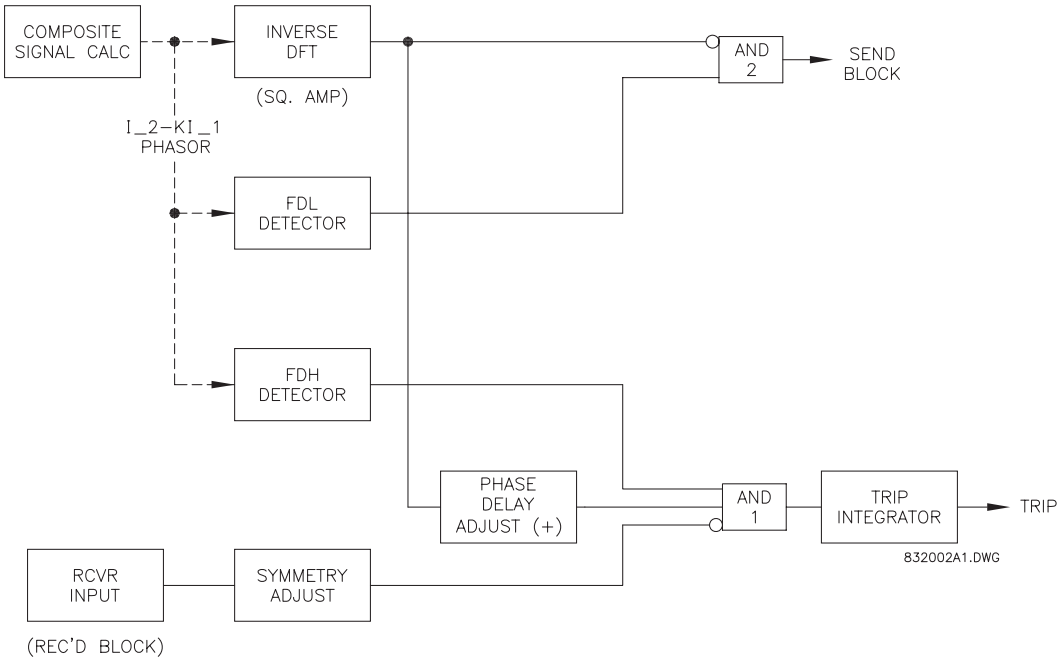
a) SYMMETRY ADJUSTMENT

As was noted in a previous section, receivers are not always symmetrical in their response. That is, if a transmitter is keyed on and off symmetrically every half cycle, the remote receiver output would not necessarily correspond exactly to the keying signal. For example, if an ON-OFF transmitter were keyed on for a half cycle and then off for a half cycle, and so on, the remote receiver output might be on for more than a half cycle and off for less than a half cycle. This affect is primarily due to the filter response in the receiver and is common with ON-OFF type of equipment. It is not a constant value but rather depends on operating frequencies as well as received signal strength. Thus, this asymmetry may vary from equipment to equipment and from time to time (as atmospheric conditions change) in service.

Frequency shift channels are generally symmetrical in their response when the discriminator in the receiver is balanced. If the discriminator is biased to one side or the other the receiver output tends to favor the side to which it is biased.

Because of this, all phase comparison schemes that may operate with asymmetrical channels are equipped with a symmetry adjustment.

The symmetry adjustment is in the receiver input circuit as shown in Figure 8-15. It is set with either a time delay pickup or a time delay drop out depending on whether the receiver elongates or shortens the received signal. The time setting is made in the field after the transmitters, receivers, and coupling equipment have all been tuned and adjusted for proper sensitivity. The proper setting is obtained by keying the transmitter on and off by means of a symmetrical sinusoidal output from the mixing network. Then, while this is taking place, the time delay pickup or dropout of the symmetry logic is adjusted so that the receiver yields a symmetrical output.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

Figure 8–15: BLOCKING SCHEME WITH SYMMETRY AND PHASE DELAY ADJUSTMENTS

The receiver output is now symmetrical, but may be phase shifted in the lagging direction from the actual keying signal at the remote terminal. This latter result is not desirable, but fortunately it may be mitigated. In addition to this there is the propagation delay in getting the communication signal from the remote transmitter to the local receiver (1 millisecond per 186 miles) plus the delay in the receiver itself. All of these add to each other to produce a receiver output that may be significantly phase delayed from the current at the remote end of the line.

This is undesirable because it introduces an error in the phase comparison. There is no way to eliminate this phase delay but there is a way to compensate for it. This compensation is accomplished by the phase delay timer in the comparer input circuit.

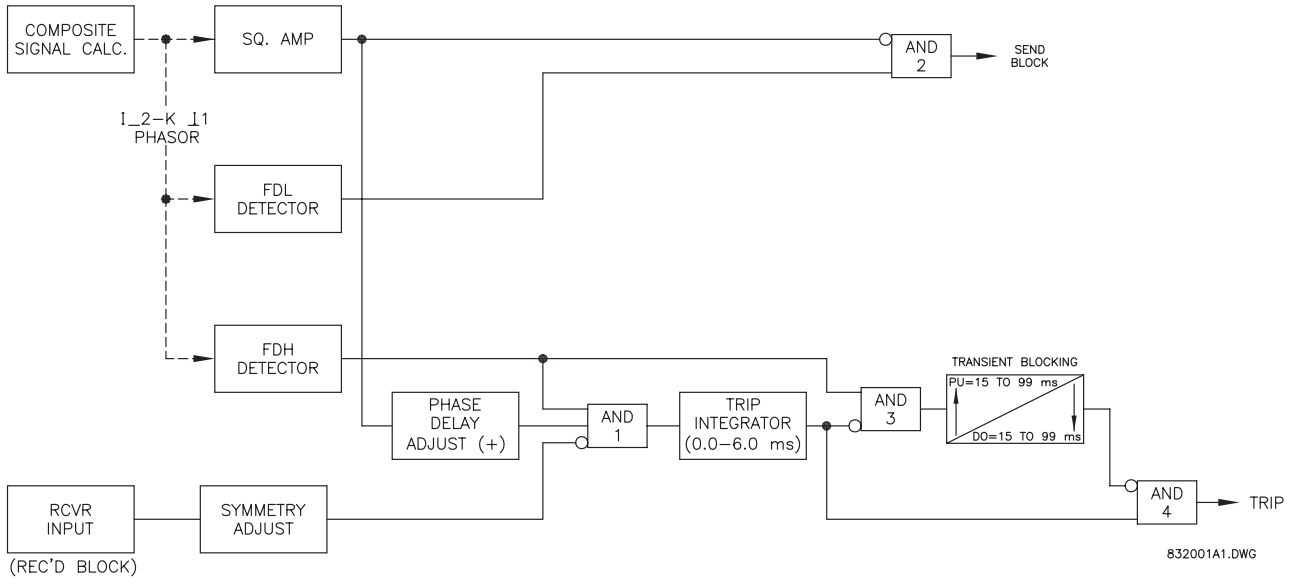
b) PHASE DELAY ADJUSTMENT

The phase delay adjustment is a timer that is set with a pickup and a dropout delay that are equal to each other so that it introduces a phase delay without affecting the symmetry of the input signal. Its output is the same shape as that of the squaring amplifier but delayed in time by the setting. This time delay setting is made in the field to be just equal to the sum of the three delays (symmetry adjustment, propagation, and receiver) discussed above. Thus, with this arrangement in the scheme of Figure 8-15, an external fault would produce a output from the symmetry adjustment logic exactly in phase and symmetrical with the output of the phase delay logic. This is necessary for proper blocking. For internal faults the output from the phase delay timer would be symmetrical with, but 180 degrees out of phase with the receiver output. This is necessary for tripping. It should be recognized that any errors in these adjustments can reduce the tripping margins for internal faults and/or reduce the blocking margins during external faults.

It is interesting to note that the setting of the phase delay timer is dependent on the channel operating time, and that the total tripping time of the scheme is affected by this timer setting. Thus, the tripping speed of the scheme is to that degree dependent on the channel operating time.

c) TRANSIENT BLOCKING

Transient blocking is a feature that is included in all phase comparison schemes. It adds to the security of the scheme during and immediately after the clearing of external faults. Figure 8-16 is a representation of Figure 8-15 except with the transient blocking logic added. This consists of AND3, AND4 and the (15-99)/(15-99) transient blocking timer.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

Figure 8–16: BLOCKING SCHEME WITH TRANSIENT BLOCKING LOGIC

The logic of the transient blocking scheme is such that if a fault is detected (indicated by the operation of FDH) but no trip takes place (as indicated by no output from the trip integrator timer) then AND3 produces an output to the transient blocking timer (15-99)/(15-99). If this condition persists long enough for the transient blocking timer to produce an output, tripping is blocked via the NOT input to AND4. This blocking of a trip output persists for the dropout time setting of the transient blocking timer after the AND3 output disappears as a result of FDH resetting or the trip integrator producing an output.

The pickup time delay setting of the transient blocking timer must be longer than the expected time difference between FDH pickup and a trip integrator output during an internal fault. This insures no delay in tripping in the event of an internal fault, as well as prolonged blocking during the clearing of an external fault during which transient power reversals may tend to cause false tripping.

d) UNBLOCKING DUAL PHASE COMPARISON

The unblocking dual phase comparison scheme is a combination of a blocking scheme with permission to operate. This scheme can be used with the FSK carrier only, as it requires monitoring of the check channel status before the fault using the Guard (Low) frequency and during the fault by detecting/not detecting switching between Guard and Trip (High) frequencies. If both Trip and Guard frequencies disappear prior the fault Guard frequency (i.e. during the fault), then the relay is produces a trip within the programmable trip window time (typically 150 ms) after the FDH detector operates.

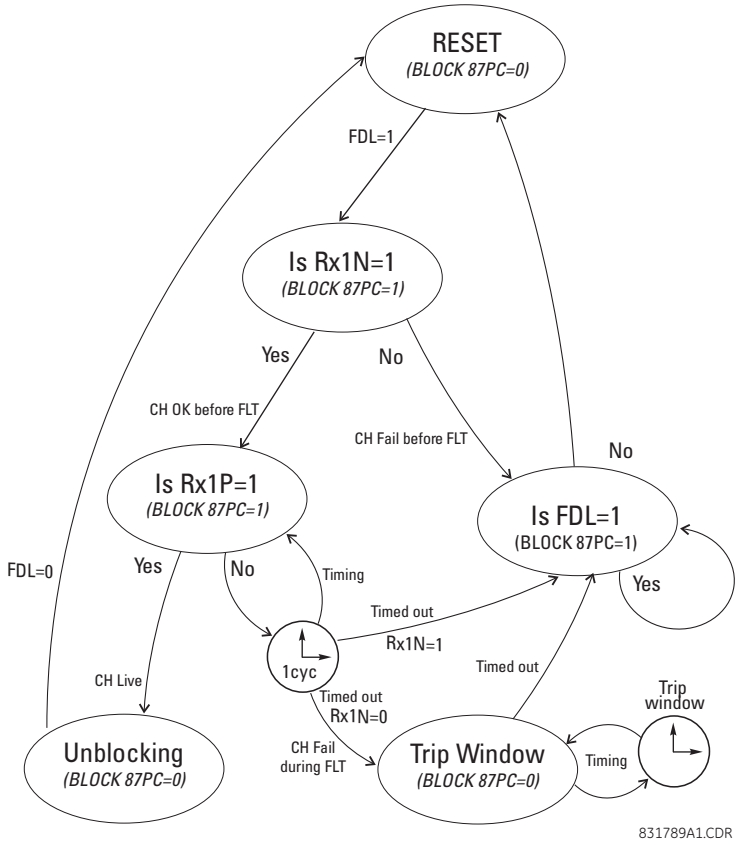


Figure 8–17: UNBLOCKING DUAL FREQUENCY PHASE COMPARISON

The above figure illustrates the state machine used for this scheme. The state machine is started when a fault is detected by FDL. At this moment, the Guard frequency status (Rx1N) is checked. If the Guard frequency is absent, the scheme is locked up, and 87PC is blocked until FDL resets.

If the Guard frequency is present upon fault occurrence, then a switch from Guard to Trip is expected during the next 15 ms. Once this occurs, the scheme is unblocked and regular dual phase comparison (on both positive and negative halves of the sinewave) takes place. If both Guard and Trip frequencies are not present when the 15 ms timer expires, then the phase comparison scheme is allowed to operate during the trip window time after FDH picks up.

Benefits of this scheme are that operating time is faster compared with single phase comparison with enough security built into the scheme.

8.1.8 MULTI-TERMINAL LINES

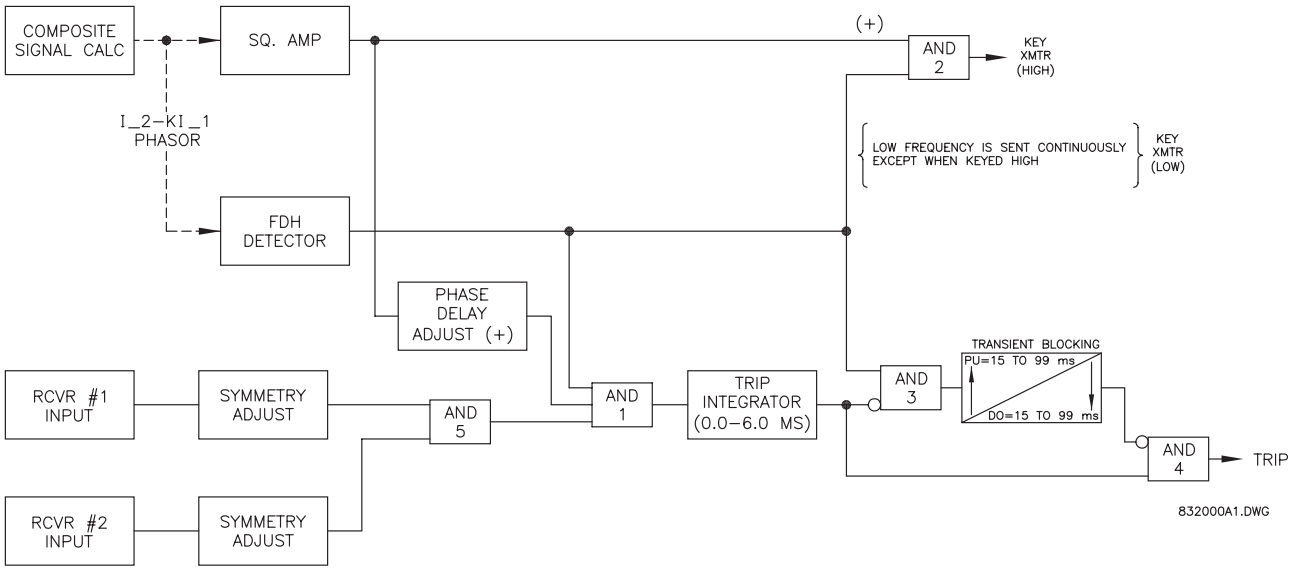
Up to this point these discussions have pertained principally to two-terminal lines. Phase comparison schemes are often applied to lines having more than two terminals and those applications differ somewhat depending on the channel equipment.

a) ON-OFF CHANNEL

The ON-OFF channel equipment is invariably used in blocking type carrier schemes similar to that of Figure 8-16. Since this type of scheme utilizes only one common frequency for all the transmitters and receivers, Figure 8-16 will apply to multi-terminal lines as well as two terminal lines. A blocking signal sent from any terminal will be received at all the other terminals to provide the necessary blocking via the single receiver at that terminal.

b) FREQUENCY SHIFT CHANNEL

Frequency-shift channels are generally used in tripping type schemes. Figure 8-17 illustrates a three-terminal line tripping scheme using a frequency-shift channel. This arrangement requires two receivers at each terminal. One receiver is required for each remote transmitter because each transmitter is operated at a different frequency. In order to trip, a high-shift output is required from both receivers concurrently to AND5. A two-terminal line scheme would require only one receiver which would operate directly into AND1 without the need for AND5. Each channel has its own symmetry adjustment.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH – PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK–UP SETTING.

Figure 8–18: TRIPPING SCHEME FOR 3-TERMINAL LINE

8.1.9 CHARGING CURRENT COMPENSATION

The basic premise for the operation of phase comparison protection schemes in general, and of the L60 phase comparison element in particular, is that the sum of the currents entering the protected zone is zero. In the case of a power system transmission line, this is not entirely true because of the capacitive charging current of the line. For short transmission lines the charging current is a small factor and can therefore be treated as an unknown error. In this application the L60 can be deployed without voltage sensors and the line charging current is included as a constant term in the total variance, increasing the differential restraint current. For long transmission lines the charging current is a significant factor, and should be computed to provide increased sensitivity to fault current.

Compensation for charging current requires the voltage at the terminals be supplied to the relays. The algorithm calculates $C \times dv/dt$ for each phase, which is then subtracted from the measured currents at both ends of the line. This is a simple approach that provides adequate compensation of the capacitive current at the fundamental power system frequency. Travelling waves on the transmission line are not compensated for, and contribute to measurement error accounted for by the stability angle.

Capacitive currents leak from the unit protection zone causing a phase shift for the phase comparison principle. Charging currents are present both in the balanced pre-fault state (positive-sequence charging current) and during internal and external faults (unbalanced charging currents).

The phase shift caused by the capacitive current depends on the *X* / *R* ratio of the line and system equivalents. For large *X* / *R* values, the capacitive current affects mostly magnitudes of the terminal currents. This is a concern for the line current differential, and less of a problem for the phase comparison relays. For smaller *X* / *R* values (highly resistive impedances), the capacitive current has a greater effect on the phase relationship, creating greater problems for phase comparison relays. As long transmission lines are typically EHV (extra high voltage) lines with a high *X* / *R* ratio, the question becomes critical not for a wrong phase due to charge current, but for providing proper coordination between FDL and FDH at opposite line terminals.

The underlying single phase model for compensation for a two and three terminal system are shown below.

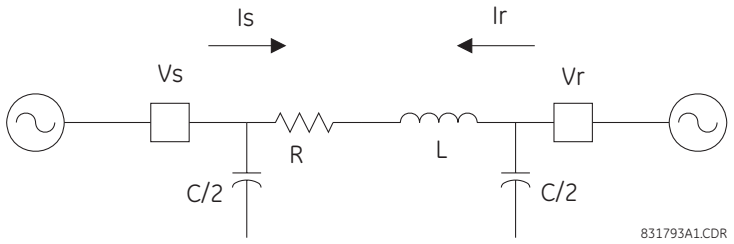


Figure 8–19: TWO-TERMINAL TRANSMISSION LINE SINGLE PHASE MODEL FOR COMPENSATION

If the VTs are connected in wye, the compensation is accurate for both balanced conditions (that is, all positive, negative and zero-sequence components of the charging current are compensated). If the VTs are connected in delta, the compensation is accurate for positive and negative-sequence components of the charging current. Since the zero-sequence voltage is not available, the L60 cannot compensate for the zero sequence current.

The compensation scheme continues to work with the breakers open, provided the voltages are measured on the line side of the breakers.

For very long lines, the distributed nature of the line leads to the classical transmission line equations, which can be solved for voltage and current profiles along the line. What is required for the compensation model is the effective positive and zero-sequence capacitance seen at the line terminals.

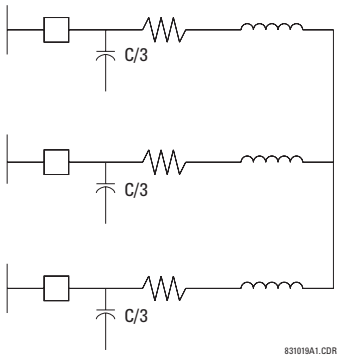


Figure 8–20: THREE-TERMINAL TRANSMISSION LINE SINGLE PHASE MODEL FOR COMPENSATION

In some applications the effect of shunt reactors must be taken into account. Shunt reactors may be installed in very long lines to provide some of the charging current required by the line. This reduces the amount of charging current flowing into the line. In this application, the setting for the line capacitance should be the residual capacitance remaining after subtracting the shunt inductive reactance from the total capacitive reactance at the power system frequency.

With respect to shunt reactors, keep in mind that the inductance (of the reactor) and capacitance (of the line) cancel each other for the fundamental frequency only. When considering transients, an inductor is not a 'negative capacitor'. Therefore, it is prudent to exclude the reactors from the measuring zone by subtracting the reactor current from the line CT current and configuring the charging current compensation for the entire amount of the line capacitive current (not for the net between the line and installed reactors). This approach is not only technically correct, but also simplifies the application by not requiring monitoring of the status (on/off) of the reactors

Charging current is calculated and subtracted from the line current individually per phase. Depending on the number of terminals on the line (two or three as configured by the 87PC function), half or one-third (in case of three-terminal line) of the net line charging current is subtracted at each terminal. For breaker-and-a-half configurations, if the **87PC SIGNAL SOURCE** setting value is "Two Sources Current", the charging current is subtracted per each breaker current individually and proportionally to the current flowing through each breaker.

8.1.10 L60 SIGNAL PROCESSING

As a protection method, phase comparison is a time domain principle. It can be logically analyzed if implemented as a set of operations on instantaneous signals, starting at the local AC currents and received DC voltages encoding the phase information for the remote currents, and culminating at the trip integrators to measure the coincidence time between the operating currents. Early (and still prevailing) implementations of microprocessor-based relays are generally based on frequency domain processing. This means instantaneous currents and voltages are first filtered and represented by phasors, (that is, magnitudes and angles), then trip/no-trip decisions are based upon phasors or similar aggregated values. Successful implementations of the L60 phase comparison principle is based on instantaneous values, not phasors. There are several reasons for using instantaneous value, the main one being the analog nature of the remote information. The transmitted/received analog signal is an on/off binary signal that encodes the information not on signal magnitude, but rather on timing with respect to actual continuous time. In addition, this signal is a subject to impairments that cannot be alleviated by means of filtering, but by manipulations on its shape. Therefore, it is logical to process the communication signals in the phase comparison relay in the time domain, and adjust the reminder of the algorithms to follow the instantaneous approach, not vice versa. The time domain approach follows the methods of the last generation of analog phase comparison relays, giving a chance for equally good performance.

The L60 samples currents and voltage inputs at a rate of 64 samples per cycle. Current samples are pre-filtered using band-pass Finite Response Filters (FIR), with a weighted average of signal samples in a selected data window, to remove the decaying DC component and low-frequency distortions. The L60 implementation uses a data window of 1/3rd of a cycle, resulting in an extra signal (phase) delay of approximately 1 ms.

The pre-filtered instantaneous currents can be used directly in phase-segregated implementations. In mixed-mode applications, they must be converted into a single composite current. This operation uses symmetrical components and may seem at odds with the time-domain approach.

However, the conversion can be done without introducing unnecessary delay by applying a pair of orthogonal filters. Orthogonal filters are two filters that yield phase responses shifted by 90°, and preferably have similar magnitude responses (that is, filtering capabilities). The two filters are often labeled as direct (D) and quadrature (Q). Their outputs are instantaneous values, but can be treated similarly to the real and imaginary parts of a phasor in the frequency domain. The L60 implementation of a phase comparison relay uses a pair of short-window FIR filters to derive the D-Q components while providing for extra transient filtering. Once the D-Q components are obtained, the instantaneous negative-sequence based composite signal (I_2 – K × I_1) is created as follows (ACB phase rotation, phase A as a reference).

$$i_{MIX} = \frac{1}{3}\left(i_{D\_A}(1-K) + \frac{1}{2}(K-1)(i_{D\_B} + i_{D\_C}) + \frac{\sqrt{3}}{2}(K+1)(i_{Q\_B} - i_{Q\_C})\right) \quad \textbf{(EQ 8.2)}$$

Note that the equation above is a linear combinations of current samples, as long as the operations of pre-filtering and deriving the orthogonal components are linear. This guarantees security on external faults regardless of any transients as long as the hardware/algorithms are the same at all line terminals. With both terminals applying the same linear processing, the two mixed currents will always be out-of-phase as waveforms, regardless of their possible distortions and transients.

The quadrature component of the signal is needed to estimate magnitude of the input current for fault detectors:

$$i_{MIX\_Q} = \frac{1}{3}\left(i_{Q\_A}(1-K) + \frac{1}{2}(K-1)(i_{Q\_B} + i_{Q\_C}) + \frac{\sqrt{3}}{2}(K+1)(i_{D\_C} - i_{D\_B})\right) \quad \textbf{(EQ 8.3)}$$

Two levels of fast overcurrent supervision are required: fault detection low (FDL) for keying and fault detection high (FDH) for tripping. These conditions are supervisory; therefore, they do not have to be very accurate. Instead, they shall be fast enough not to slow down the remainder of the 87PC algorithm.

The fast magnitude is calculated as:

$$I_{FAST} = \sqrt{(i_{MIX})^2 + (I_{MIX\_Q})^2} \quad \textbf{(EQ 8.4)}$$

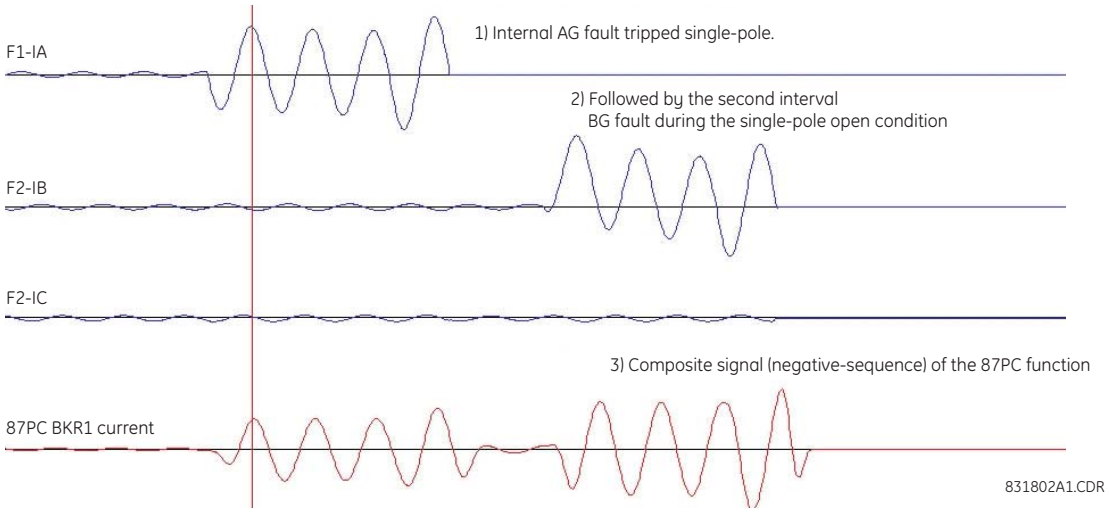


Figure 8–21: EXAMPLE OF MIXING CURRENT OPERATION (RELAY COMTRADE RECORD)

The response of the overcurrent condition to switch off transients, including current reversal on parallel lines and heavily saturated CTs, is important. The key design requirement is keep the FDL and FDH picked up and resetting in a way that ensures both dependability and security in both tripping and blocking arrangements.

From this perspective, to boost the magnitude on heavily saturated CTs, the RMS component is calculated as follows (on a sample-by-sample basis):

$$I_{RMS(k)} = \sqrt{\frac{2}{N_1} \sum_{p=0}^{N_1 - 1} (I_{MIX(k-p)})^2} \quad \textbf{(EQ 8.5)}$$

In the above equation, N_1 represents the number of samples per cycle (64).

The magnitude estimator combines the fast estimator for accuracy, the RMS value for dependability on CT saturation or other severe transients, and the waveform peak for speed:

$$I_{AUX} = \max(I_{RMS}, I_{FAST}, 0.85 \times \text{abs}(i_{MIX})) \quad \textbf{(EQ 8.6)}$$

The local operating current is converted into phase pulses. It is important to realize that the operation is nonlinear, erasing almost all information contained in the magnitude of the signal and presenting exclusively the phase information by encoding the on/off pulses signifying polarity of the operating signal. This polarity is preserved with respect to the universal analog time. This is one of the key advantages of the phase comparison principle, even when implemented digitally: no synchronization is required between the individual relays of the 87PC scheme.

The raw LOC-al pulses (Positive and Negative polarity) are produced disregarding the FDL and FDH flags. The fault detector flags are used in the dual-breaker, key and trip logic. The raw pulses are calculated as follows.

For tripping schemes:

$$\begin{aligned} \text{LOC}_{1P\_RAW} &= i_{1\_MIX} > 0.02 \times \sqrt{2} \times \text{CT}_{1pu} \\ \text{LOC}_{1N\_RAW} &= i_{1\_MIX} < -0.02 \times \sqrt{2} \times \text{CT}_{1pu} \end{aligned} \quad \textbf{(EQ 8.7)}$$

The logical signal that marks the positive polarity (P) is asserted as long as the mixed current is greater than 0.02 pu of the CT nominal. The logical signal that marks the negative polarity (N) is asserted as long as the mixed current is less than –0.02 pu of the CT nominal

To ensure security and dependability for blocking schemes, especially during low current conditions when pulses might be shortened, square pulses are created as follows.

$$\begin{aligned}
\text{PICKUP_LOC}_{1P_RAW} &= i_{1_MIX} > 0.02 \times \sqrt{2} \times \text{CT}_{1pu} \\
\text{DROPOUT_LOC}_{1P_RAW} &= i_{1_MIX} < -0.02 \times \sqrt{2} \times \text{CT}_{1pu} \\
\text{PICKUP_LOC}_{1N_RAW} &= i_{1_MIX} < -0.02 \times \sqrt{2} \times \text{CT}_{1pu} \\
\text{DROPOUT_LOC}_{1N_RAW} &= i_{1_MIX} > 0.02 \times \sqrt{2} \times \text{CT}_{1pu}
\end{aligned} \quad \textbf{(EQ 8.8)}$$

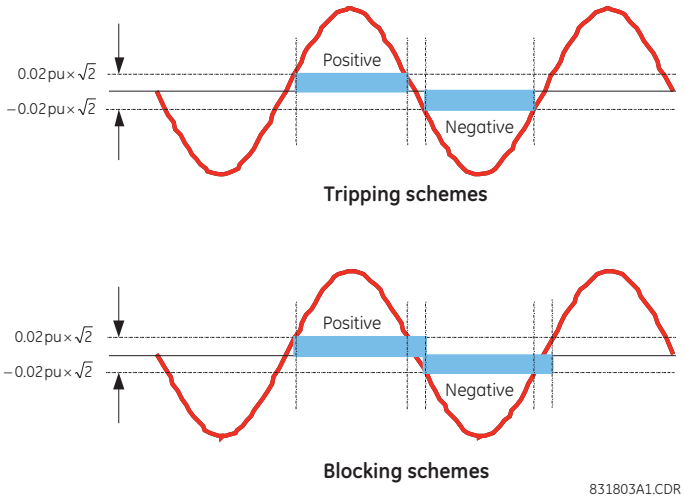


Figure 8–22: FORMATION OF SQUARE PULSES FOR TRIPPING AND BLOCKING SCHEMES

The operation for blocking schemes insures reliable blocking pulses in cases where the operating current is close to the squaring pickup constant (0.02 pu). If the operating signal triggered positive square pulse once it crossed the positive threshold, then it stays within the deadband (between $-0.02 \times \sqrt{2} \times \text{CT}_{1pu}$ and $0.02 \times \sqrt{2} \times \text{CT}_{1pu}$) and the blocking pulse is reset in one cycle.

The phase comparison principle faces security problems when fed from externally summed currents in two-breaker applications. To maintain the excellent immunity to CT saturation of the 'original, single-breaker' phase comparison principle, the two currents must be processed individually and both the phase and magnitude information used to detect the through fault condition.

The dual breaker logic consolidates two pieces of information: fault detector flags signaling the rough current levels and the phase pulses signaling current direction.

The fault detector flags are ORed between the two breakers (breakers 1 and 2) as follows.

FDL = **FDL1** OR **FDL2**

FDH = **FDH1** OR **FDH2**

The rationale behind this logic is that regardless which breaker (or both) carries a current, the elevated current condition (FDL) shall be declared to signal permission or blocking as per the scheme type and fault location. The trip supervision condition (FDH) is processed in a similar manner.

The 'pulse' combination logic ensures security and dependability. With this respect, a distinction must be made between tripping and blocking schemes. The following figure illustrates the dual breaker logic for permissive (section a) and blocking (section b) transmit schemes.

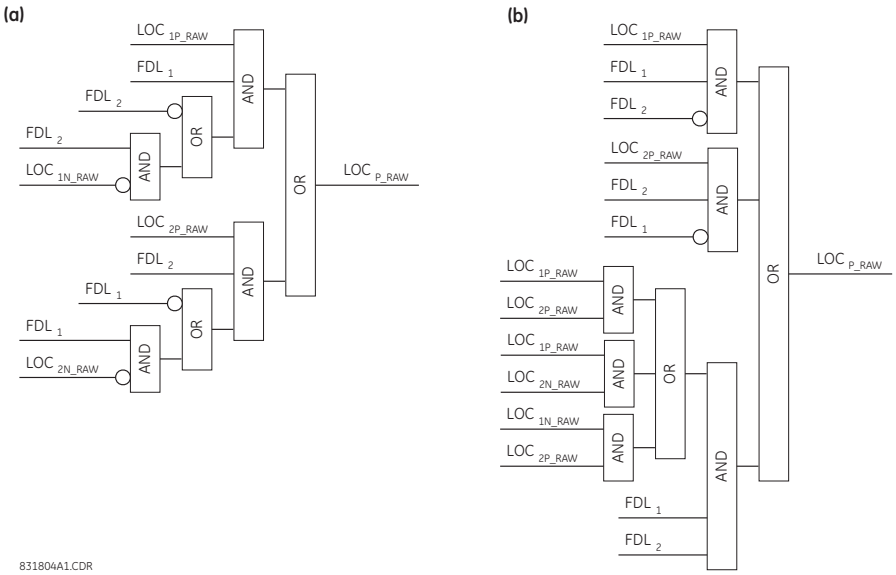


Figure 8–23: DUAL-BREAKER LOGIC FOR PERMISSIVE AND BLOCKING TRANSMIT SCHEMES

For tripping (permissive) schemes, a positive polarity is declared for the terminal if one breaker displays positive polarity when its FDL flag is set, while the other breaker either does not show the negative polarity or its FDL flag is dropped out.

The transmission logic for the blocking follows a different reasoning. Here, a blocking action must be established if any of the two breakers sees a reverse direction. It must be kept in mind that the positive and negative pulses do not necessarily complement each other, and therefore, one must not substitute not(positive polarity) = negative polarity.

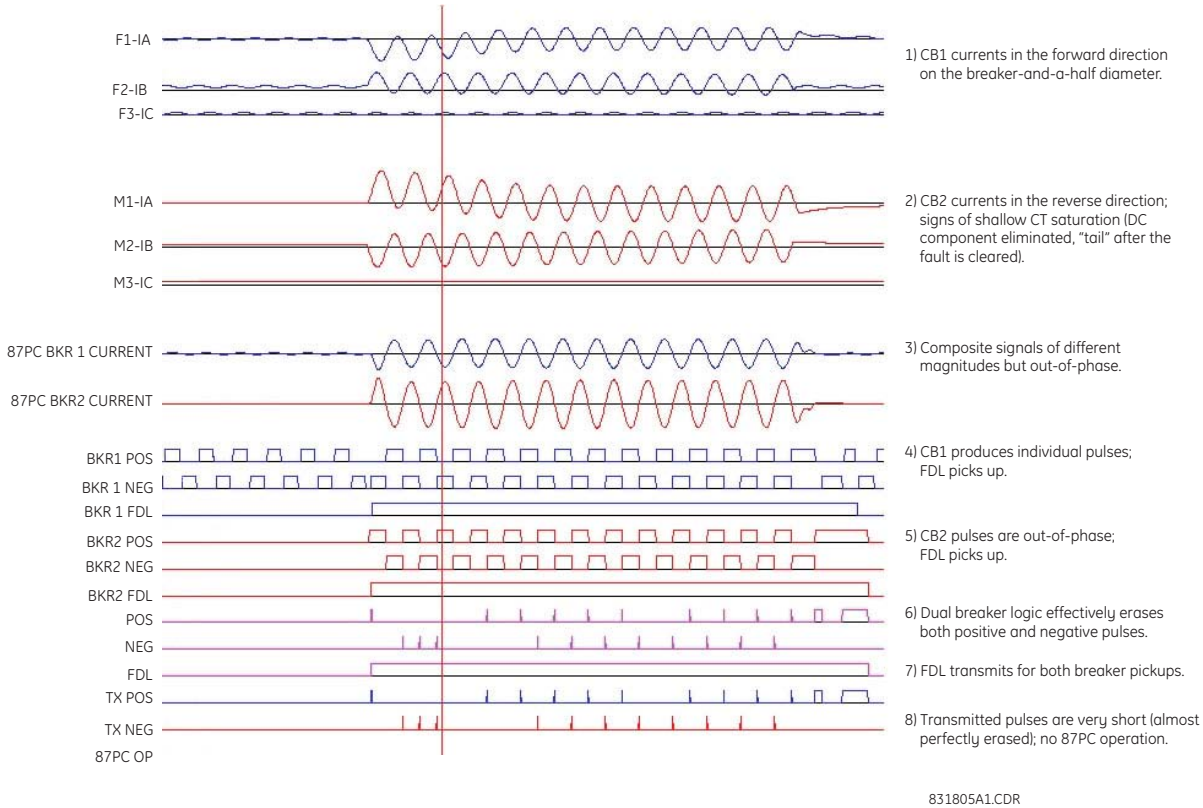


Figure 8–24: PERMISSIVE DUAL-COMPARISON SCHEME LOGIC THROUGH FAULT CONDITION

The external fault behind one relay with a blocking scheme in a dual breaker application results in transmittal of the continuous blocking signal to the remote terminal.

The received pulses may be distorted in a number of ways. Some of those distortions must be filtered out, some of them shall be left as received (their rectification is neither necessary nor safe).

The receive information is delivered from the carrier or other receiver as a DC voltage. In prior generations of relays, the input for this signal was a binary or status circuit that reported only a debounced or filtered true or false indication to the following circuits or microprocessor. In the newest design, this signal is sampled synchronously with the local AC signals through the same A/D converter controlled from the same S&H signal, and at the same high sampling rate. In this way, both the pieces of information (local AC currents, and remote phase signals) are automatically aligned in time, and the analog value of the receiver output status signal can be utilized to achieve the closest approach to the core phase comparison operating principles.

The first and obvious distortion in the received signal is a time delay added by the communication channel. This must be corrected by buffering the pulses to be aligned for time differentials with respect to the slowest remote channel. Digital technology such delays can be used in a precise and straightforward way by buffering the signal sample values in a delay queue. Analog technologies may have difficulties in precisely delaying those signals, particularly if those signals are of variable length and have other impairments.

The second possible distortion is high frequency noise embedded on the mark or space pulses. These should be left unaltered. The receiving relay does not have any reliable information as to the real value of the received information, and therefore shall not alter it based on any assumptions. The phase comparison algorithm has a well-understood security margin due to the averaging action of the trip integrators. The integrators shall deal with this kind of noise, yielding a predictable response that is transparent and easy to grasp by the user.

The third type of distortion is pulse asymmetry. Modern carrier sets claim to be free of this problem, but historically it has been observed that either the mark or the space signals were extended at the receiving end compared with the originally sent signal. Distinction between the delay and asymmetry is relatively straightforward: if the rising edges and the falling edges of the transmit and receive signals are spaced by the same period of time, one deals with a straight delay. If the spacing is different between the rising and falling edges is different, pulse asymmetry takes place on top of the delay. In this case, one of the numbers is labeled as delay, and the difference with respect to the other number is labeled a pulse asymmetry. Both need to be entered as settings in order to deal with this distortion.

The following figure presents two cases of this channel distortion. For the extended mark, the falling edge must be shifted forward in time (accelerated). For extended spaces, the rising edge must be advanced. If not corrected, the pulse asymmetry renders the system unusable for distortions longer than one quarter of a power cycle. This problem shows the advantage of modern DSP technology. Assuming that the signal may be impaired by short lasting noise, it is very difficult to perform this correction accurately in the analog world.

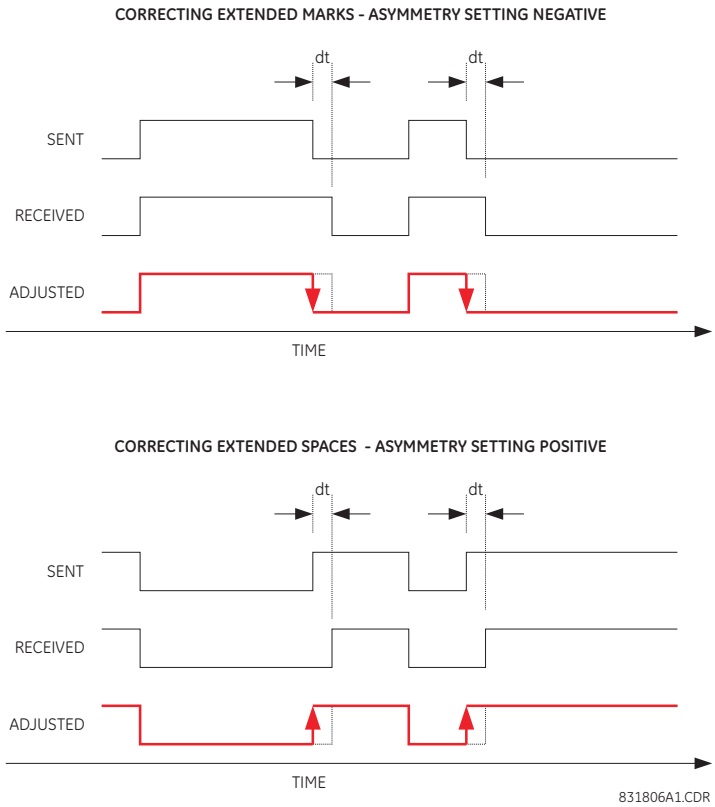


Figure 8–25: PULSE ASYMMETRY, PHENOMENON AND CORRECTION (CHANNEL DELAY NOT SHOWN FOR SIMPLICITY)

The following figure illustrates the alignment algorithm. The figure shows local current, received RX voltage, and the remote pulse aligned with the local pulses accounting for the channel delay setting.

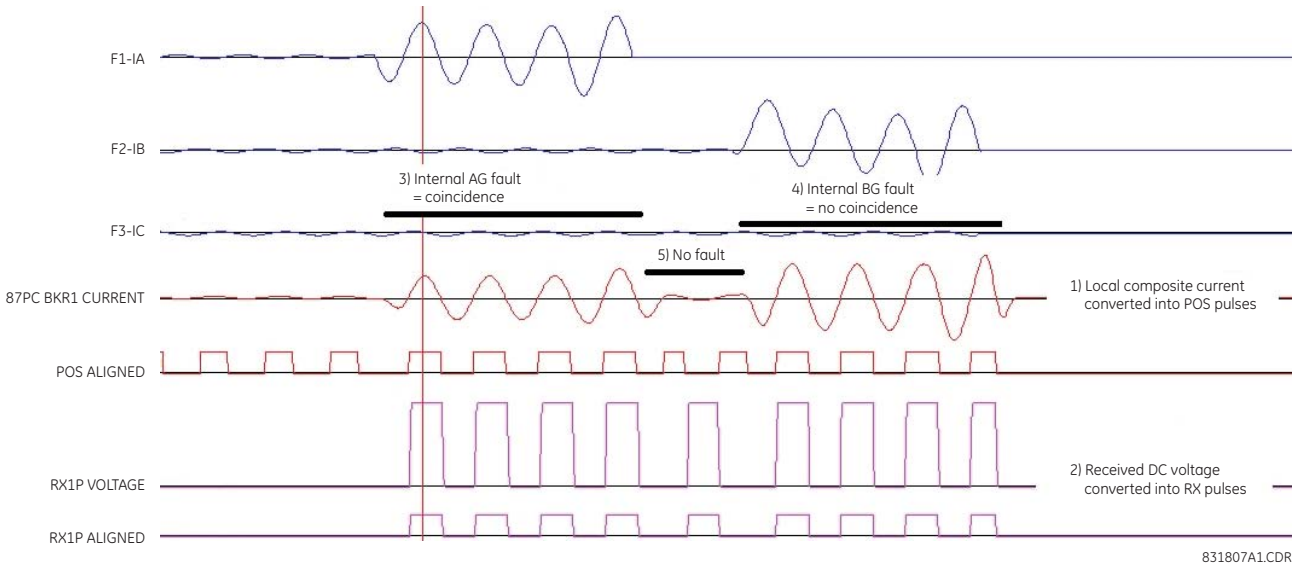


Figure 8–26: ALIGNMENT LOGIC (RELAY COMTRADE RECORD)

Being communication-dependent, a phase comparison relay should treat information delivered from the remote terminals with the same criticality as the local AC currents. This includes monitoring for troubleshooting purposes, accountability, and continuous improvement capability for products and installations. Modern microprocessor-based phase comparison relays

that sample their binary DC input voltages for analog level at the same high sampling rate as they do for analog signal inputs provide great analysis tools: they include all the measured and derived instantaneous signals in their oscillography records (COMTRADE files). This includes flags driving transmission, received DC voltage, local AC currents, and all relevant instantaneous signals leading towards the trip/no-trip condition. Having four receive channels, it is even possible to loop back the transmit voltages to monitor both the signal connected to a local carrier equipment, and received at the remote location.

After all the local and remote pulses are aligned and conditioned, a coincidence condition *X* is established as per the number of terminals and type of the scheme (tripping vs. blocking). For example, for a three-terminal permissive scheme the condition becomes:

X = **FDH** AND **LOC** AND **REM1** AND **REM2**

The above logic is executed for the positive polarity in single-comparison schemes, and independently for positive and negative polarities in dual-comparison schemes.

The coincidence condition is driving an explicitly implemented integrator (summator). In the L60, the integrator counts up by 10 units if the coincidence input is logic 1, counts down by 5 counts if the coincidence input is momentarily logic 0, and counts down by 20 if the input is in logic 0 for extended periods of time. This provides extra security for chattering inputs, allowing for eventual trips in clear situations, and provides for full reset of the integrator before the next coincidence period.

The output of the integrator (or two integrators in dual-comparison schemes) is compared with the coincidence timer setting yielding the final trip/no-trip flag.

The following figure shows an example of the coincidence integration for an internal fault as recorded in a COMTRADE file by the relay under test.

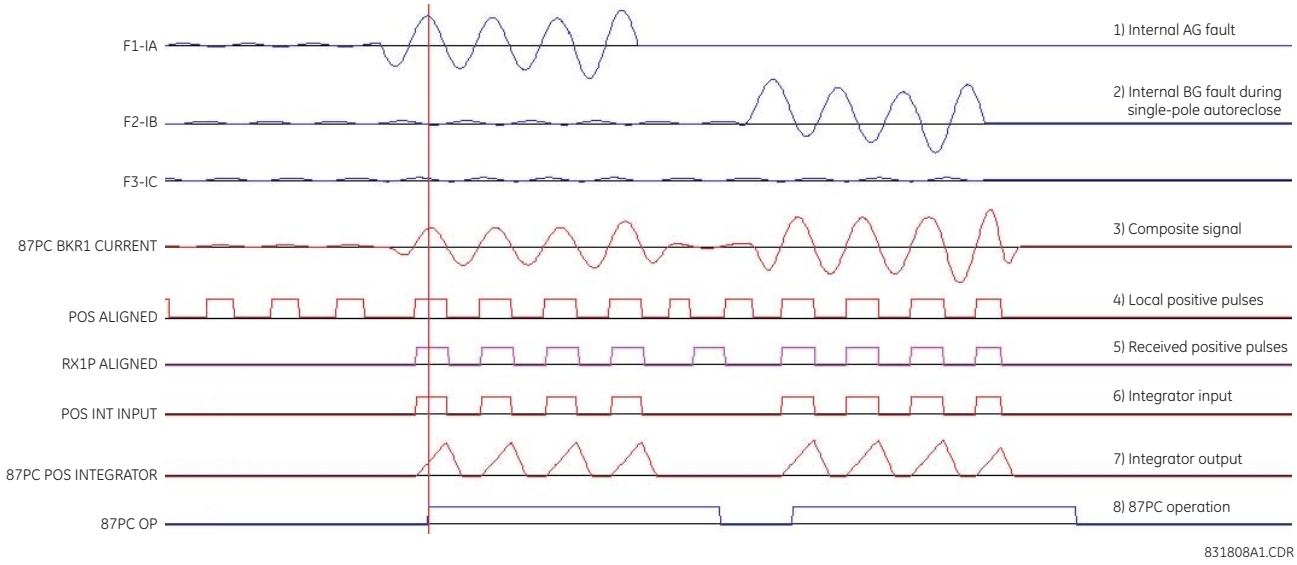


Figure 8–27: TRIP INTEGRATION LOGIC (RELAY COMTRADE RECORD)

The L60 can be programmed to perform an automatic checkback. Under normal system conditions, a relay could initiate transmission and modulate the analog signal to exchange small amounts of information. The ability to abort in cases of system faults is a key to successful deployment. This feature could replace the guard signal when the latter is not available. Furthermore, it provides a more comprehensive communications check from one center of relaying intelligence in the microprocessor at one end to its companion at the other line terminal. This covers all links in the chain of communications, not just the carrier part of the system.

The advantages of the L60 implementation of phase comparison relaying with more pure and secure digital calculations are summarized below. The following methods are critically important to the effectiveness of the new 87PC element.

1. Separated CT inputs from multiple breakers feeding the line enables proper handling of bus through faults at a line terminal as explained above.
2. Developing comparison signals from each breaker separately, and combining with the logic explained above, eliminates security risks caused by combining the breaker currents before calculating the comparison signals.

3. Treating channel receiver inputs as analog signals and sampling the waveform at high speed enables processing of the receiver outputs that overcomes misbehaviors of the channel that fooled earlier phase comparison implementations, as explained above.

8.2.1 OVERVIEW

a) INTRODUCTION

Single pole operations make use of many features of the relay. At the minimum, the Trip Output, Recloser, Breaker Control, Open Pole Detector, and Phase Selector must be fully programmed and in service; and either protection elements or digital inputs representing fault detection must be available for successful operation. When single pole trip-and-reclose is required overall control within the relay is performed by the Trip Output element. This element includes interfaces with pilot aided schemes, the Line Pickup, Breaker Control, and Breaker Failure elements.

Single pole operations are based on use of the Phase Selector to identify the type of the fault, to eliminate incorrect fault identification that can be made by distance elements in some circumstances and to provide trip initiation from elements that are not capable of any fault type identification, such as high-set negative-sequence directional overcurrent element. The scheme is also designed to make use of the advantages provided by communications channels with multiple-bit capacities for fault identification.

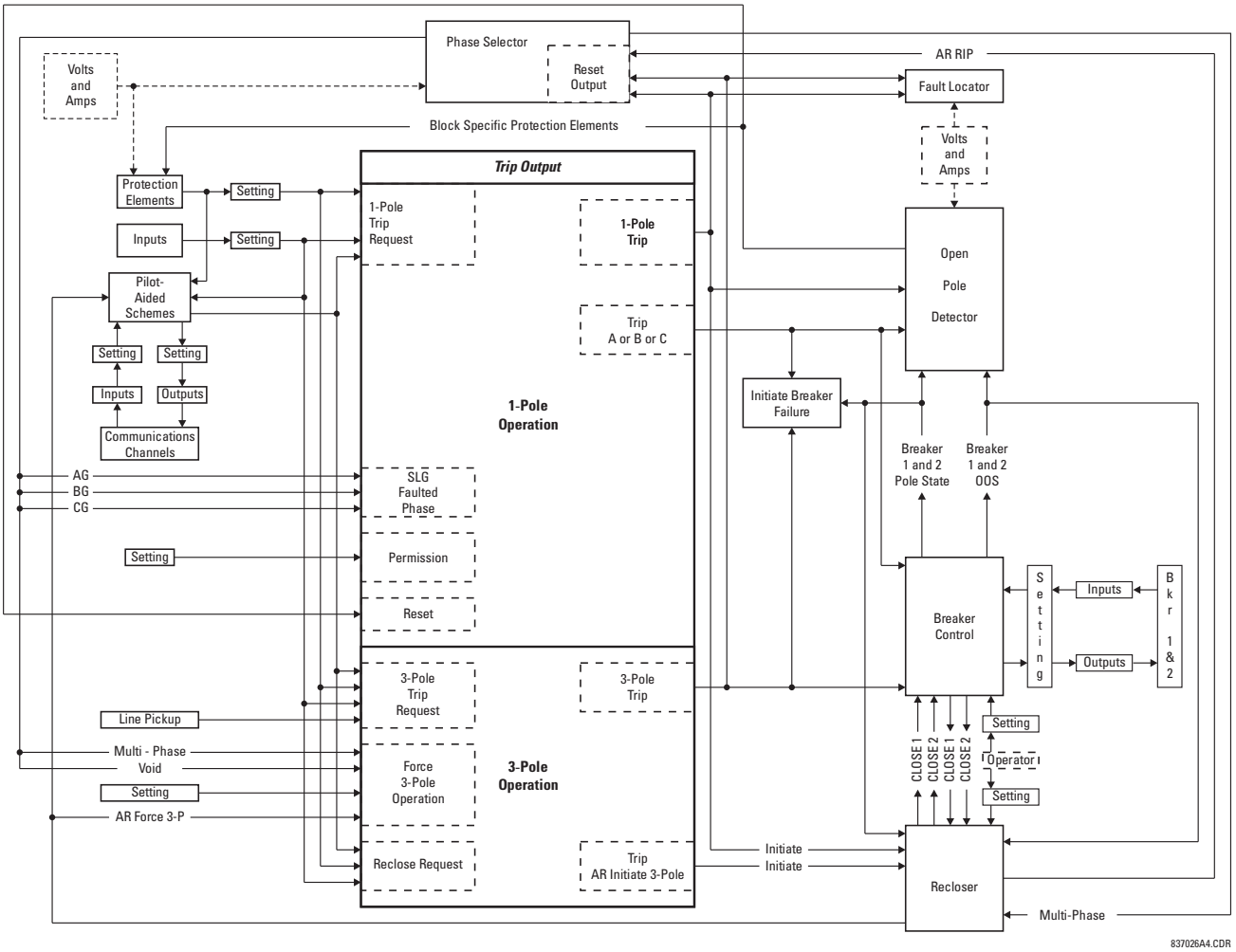


Figure 8–28: SINGLE-POLE OPERATION

The Trip Output element receives requests for single and three pole trips and three pole reclose initiation, which it then processes to generate outputs that are used to:

- determine whether a single or three pole operation should be performed
- initiate tripping of breaker poles A, B and C, either individually or as a group
- initiate Breaker Failure protection for phases A, B and C, either individually or as a group
- notify the Open Pole Detector when a single pole operation is imminent

- initiate either single or three pole reclosing
- notify the Phase Selector when a trip operation is imminent

When notified that a single pole operation has been initiated Open Pole Detector will:

- initiate blocking of protection elements that could potentially maloperate when a breaker pole is open
- instruct the Phase Selector to de-assert all outputs, as an Open Pole invalidates calculations.

The operation of the scheme in a single breaker arrangement will be described. The line is protected by a L60 using the 87PC, Line Pickup, and Zone 1 Phase and Ground Distance elements. 87PC and/or Zone 1 is configured to issue a single-pole trip when appropriate (**TRIP 1-POLE INPUT-1:** "GND DIST Z1 OP", **TRIP 1-POLE INPUT-2:** "PHS DIST Z1 OP"). It is assumed that when tripping three-poles both Zone 1 and 87PC shall initiate three-pole reclosing. This is achieved by setting **TRIP RECLOSE INPUT-1:** "87PC OP", **TRIP RECLOSE INPUT-2:** "GND DIST Z1 OP", and **TRIP RECLOSE INPUT-3:** "PHS DIST Z1 OP".

It is assumed for this discussion that the relay features that are shown on Single Pole Operation diagram above have all been programmed for the application and are in service. The description begins with line breakers open at both the local and remote ends, and the operation of the scheme is described in chronological order.

Because the line is de-energized the Line Pickup element is armed. The Recloser is presently enabled. An operator requests that Breaker Control close the breaker, and it operates output relays to close breaker poles A, B and C. This operator manual close request is also forwarded from Breaker Control to recloser, which becomes disabled, de-asserting its "Enabled" output. This output is transferred to Trip Output, where it converts any input request for a single pole operation into a three-pole operation. At the Recloser, the **AR1 BLK TIME @ MAN CLOSE** timer is started.

The breaker closes and status monitoring contacts on the breaker poles change state; the new breaker pole states are reported to Breaker Control, which in turn transfers these states to the recloser, Trip Output, Breaker Failure and Open Pole Detector. Because a fault is not detected the **AR1 BLK TIME @ MAN CLOSE** times out and the Recloser is enabled, which asserts the "Enabled" output, informing the Trip Output element that single pole trip operations are now permitted. When normal voltage appears on the line the Line Pickup element is disarmed. As the local line breaker has not tripped the operator closes the breaker at the remote end of the line, placing the line in service.

Several scenarios are considered below.

NOTE

The 87PC element must be applied according to the *Single Pole Tripping Applications* section in Chapter 9.

b) SLG FAULT

An AG fault occurs close to the considered relay. Immediately after the fault, the disturbance detector (50DD) picks-up and activates the phase selector. The phase selector recognizes an AG fault by asserting its PHASE SELECT AG operand. The line phase comparison element (ANSI 87PC) and/or ground distance zone 1 (AG element) responds to the fault. As the fault is close to the relay, phase distance zone 1 (AB, CA elements) may respond to this fault as well. In any case, a single-pole operation is requested by zone 1 via the line phase comparison element (ANSI 87PC) and/or the GND DIST Z1 OP and/or PHS DIST Z1 OP operands.

At this moment the request to trip is placed for the trip output. As the fault is recognized as an AG fault, the TRIP PHASE A operand is asserted by the trip output. This signal is passed to the breaker control scheme and results in tripping pole A of the breaker.

Simultaneously with the TRIP PHASE A operand, the TRIP 1-POLE operand is asserted. This operand activates the open pole detector. The latter detector responds to the TRIP PHASE A signal by declaring phase A open by asserting OPEN POLE OP ΦA (even before it is actually opened). The TRIP PHASE A signal resets only after the breaker actually operates as indicated by its auxiliary contact. At this moment the open pole detector responds to the breaker position and continues to indicate phase A opened. This indication results in establishing blocking signals for distance elements (OPEN POLE BLK AB, OPEN POLE BLK CA operands are asserted). If neutral and negative-sequence overcurrent elements are mapped into the trip output to trigger single-pole tripping, they must be blocked with the OPEN POLE BLK N operand, specifically provided for this purpose. The OPEN POLE BLK N operand must be assigned through the block setting of the overcurrent element. The two latter operands block phase distance AB and CA elements, respectively (all zones); the OPEN POLE ΦA OP blocks the ground distance AG elements (all zones). As a result, the Z1 OP and Z2 PKP operands that were picked-up reset immediately. The following distance elements remain operational guarding the line against evolving faults: BG, CG and BC.

Depending on response times, the actual trip is initiated either by zone 1 or by the line phase comparison element (87PC). At the moment TRIP 1-POLE operand is asserted, the phase selector resets and no other trip action could take place. After the trip command is issued all the picked up elements are forced to reset by the open pole detector.

The TRIP 1-POLE operand initiates automatically a single-pole autoreclose. The autoreclose is started and asserts the AR RIP operand. This operand keeps blocking the phase selector so that it does not respond to any subsequent events. At the same time the operand removes zero-sequence directional supervision from ground distance zones 2 and 3 so that they could respond to a single-line-to-ground fault during open pole conditions.

The AR FORCE 3-P TRIP operand is asserted 1.25 cycles following autoreclose initiation. This operand acts as an enabler for any existing trip request. In this case none of the protection elements is picked up at this time, therefore no more trips are initiated.

When the recloser dead time interval is complete it signals the breaker control element to close the breaker. The breaker control element operates output relays to close the breaker.

When pole A of the breaker closes this new status is reported to the breaker control element, which transfers this data to the breaker failure, autorecloser, open pole detector and trip output elements. The response at breaker failure is dependent on the programming of that element. The response at the autorecloser is not relevant to this discussion. At the open pole detector, the blocking signals to protection elements are de-asserted.

If the fault was transient the reset time would expire at the autorecloser and the AR FORCE 3-P TRIP and RIP outputs would be de-asserted, returning all features to the state described at the beginning of this description.

If the fault was permanent appropriate protection elements would detect it and place a trip request for the trip output element. As the AR FORCE 3-P TRIP is still asserted, the request is executed as a three-pole trip.

The response of the system from this point is as described above for the second trip, except the autorecloser will go to lockout upon the next initiation (depending on the number of shots programmed).

c) SLG FAULT EVOLVING INTO LLG

When an AG fault occurs the events unfold initially as in the previous example. If the fault evolves quickly, the phase selector will change its initial assessment from AG to ABG fault and when the trip request is placed either by zone 1 or the line phase comparison element (ANSI 87PC), a three-pole trip will be initiated. If this is the case, all three TRIP PHASE A, TRIP PHASE B and TRIP PHASE C operands will be asserted. The command is passed to the breaker control element and results in a three-pole trip. At the same time the recloser is initiated as per settings of the trip output. As the TRIP 3-POLE operand is asserted (not the TRIP 1-POLE operand) the open pole is not activated. Because the AR RIP in progress is asserted, the phase selector is blocked as well.

If the fault evolves slowly, the sequence is different: The relay trips phase A as in the previous example. The phase selector resets, the open pole detector is activated and forces the zone 1 and zone 2 AG, AB, CA and negative-sequence overcurrent elements to reset. If the zone 1 BG or line phase comparison element (ANSI 87PC) picks up, no trip command will be issued until the AR FORCE 3-P TRIP is asserted. This happens 1.25 cycles after the first trip. If at this time or any time later a request for trip is placed (due to an evolving fault), a three-pole trip is initiated. The TRIP 1-POLE operand is de-asserted by the TRIP 3-POLE operand, resetting the open pole detector. Shortly all three-poles are opened.

When the dead time expires, the recloser signals the breaker control to close the breaker. At this time all the protection elements are operational, as the open pole detector is not blocking any elements. If the line-side VTs are used, the line pickup element is armed as well. If there is a fault on the line, these elements will pickup the fault and issue next request for trip. This request results in three-pole trip as the AR FORCE 3-P TRIP is still asserted.

The response of the system from this point is as described above for the second trip, except the recloser will go to lockout upon the next initiation (depending on the number of shots programmed).

8.2.2 PHASE SELECTION

The L60 uses phase relations between current symmetrical components for phase selection. First, the algorithm validates if there is enough zero, positive, and negative-sequence currents for reliable analysis. The comparison is adaptive; that is, the magnitudes of the three symmetrical components used mutually as restraints confirm if a given component is large enough to be used for phase selection. Once the current magnitudes are validated, the algorithm analyzes phase relations between the negative and positive-sequence currents and negative and zero-sequence currents (when applicable) as illustrated below.

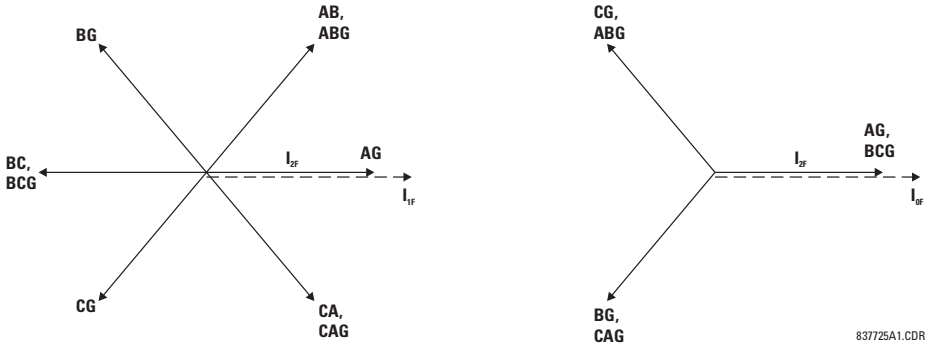


Figure 8–29: PHASE SELECTION PRINCIPLE (ABC PHASE ROTATION)

Due to dual comparisons, the algorithm is very secure. For increased accuracy and to facilitate operation in weak systems, the pre-fault components are removed from the analyzed currents. The algorithm is very fast and ensures proper phase selection before any of the correctly set protection elements operates.

Under unusual circumstances such as weak-infeed conditions with the zero-sequence current dominating during any ground fault, or during cross-country faults, the current-based phase selector may not recognize any of the known fault pattern. If this is the case, voltages are used for phase selection. The voltage algorithm is the same as the current-based algorithm; for example, phase angles between the zero, negative, and positive-sequence voltages are used. The pre-fault values are subtracted prior to any calculations.

The pre-fault quantities are captured and the calculations start when the disturbance detector (50DD) operates.

When the trip command is issued by the trip output logic (TRIP 1-POLE or TRIP 3-POLE) and during open pole conditions (OPEN POLE OP), the phase selector resets all its output operands and ignores any subsequent operations of the disturbance detector.

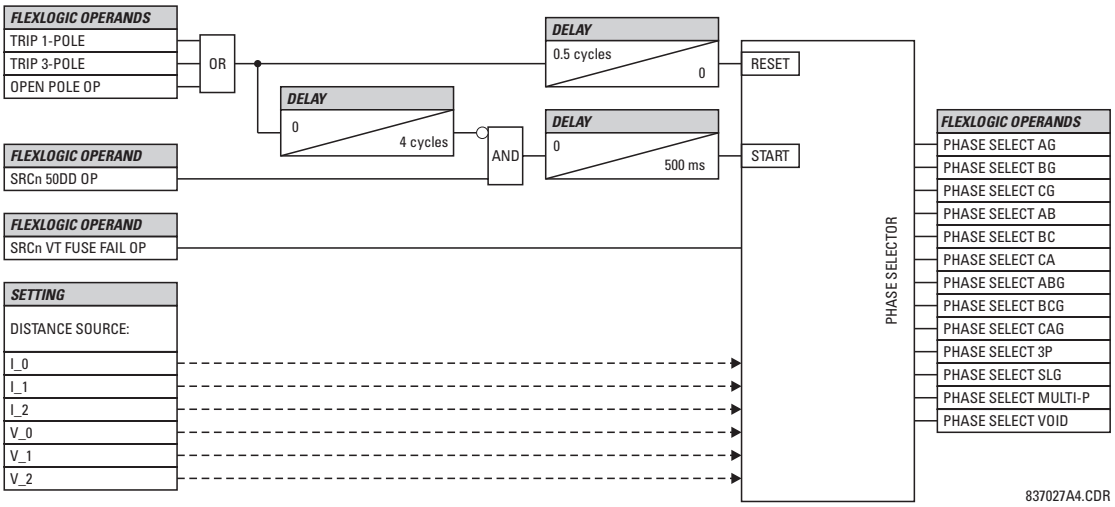


Figure 8–30: PHASE SELECTOR LOGIC

8.3.1 FAULT TYPE DETERMINATION

Fault type determination is required for calculation of fault location – the algorithm uses the angle between the negative and positive sequence components of the relay currents. To improve accuracy and speed of operation, the fault components of the currents are used; that is, the pre-fault phasors are subtracted from the measured current phasors. In addition to the angle relationships, certain extra checks are performed on magnitudes of the negative and zero-sequence currents.

The single-ended fault location method assumes that the fault components of the currents supplied from the local (A) and remote (B) systems are in phase. The figure below shows an equivalent system for fault location.

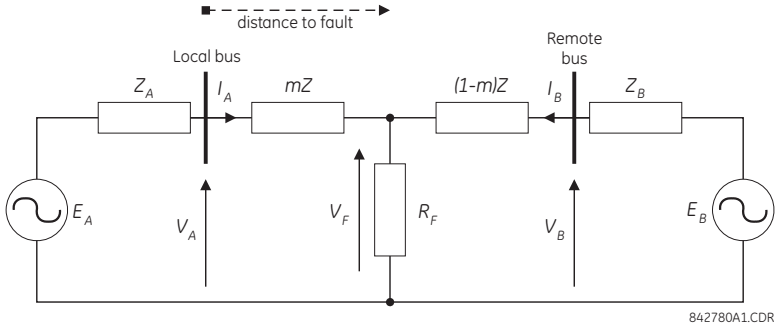


Figure 8–31: EQUIVALENT SYSTEM FOR FAULT LOCATION

The following equations hold true for this equivalent system.

$$V_A = m \cdot Z \cdot I_A + R_F \cdot (I_A + I_B) \quad \textbf{(EQ 8.9)}$$

where: m = sought pu distance to fault, Z = positive sequence impedance of the line.

The currents from the local and remote systems can be parted between their fault (F) and pre-fault load (pre) components:

$$I_A = I_{AF} + I_{Apre} \quad \textbf{(EQ 8.10)}$$

and neglecting shunt parameters of the line:

$$I_B = I_{BF} - I_{Apre} \quad \textbf{(EQ 8.11)}$$

Inserting the I_A and I_B equations into the V_A equation and solving for the fault resistance yields:

$$R_F = \frac{V_A - m \cdot Z \cdot I_A}{I_{AF} \cdot \left(1 + \frac{I_{BF}}{I_{AF}}\right)} \quad \textbf{(EQ 8.12)}$$

Assuming the fault components of the currents, I_{AF} and I_{BF} are in phase, and observing that the fault resistance, as impedance, does not have any imaginary part gives:

$$\mathrm{Im}\left(\frac{V_A - m \cdot Z \cdot I_A}{I_{AF}}\right) = 0 \quad \textbf{(EQ 8.13)}$$

where: Im() represents the imaginary part of a complex number. Solving the above equation for the unknown m creates the following fault location algorithm:

$$m = \frac{\mathrm{Im}(V_A \cdot I_{AF}^*)}{\mathrm{Im}(Z \cdot I_A \cdot I_{AF}^*)} \quad \textbf{(EQ 8.14)}$$

where ***** denotes the complex conjugate and $I_{AF} = I_A - I_{Apre}$.

Depending on the fault type, appropriate voltage and current signals are selected from the phase quantities before applying the two equations above (the superscripts denote phases, the subscripts denote stations).

For AG faults:

$$V_A = V_A^A, \quad I_A = I_A^A + K_0 \cdot I_{0A} \quad \textbf{(EQ 8.15)}$$

For BG faults:

$$V_A = V_A^B, \quad I_A = I_A^B + K_0 \cdot I_{0A} \qquad \textbf{(EQ 8.16)}$$

For CG faults:

$$V_A = V_A^C, \quad I_A = I_A^{BC} + K_0 \cdot I_{0A} \qquad \textbf{(EQ 8.17)}$$

For AB and ABG faults:

$$V_A = V_A^A - V_A^B, \quad I_A = I_A^A - I_A^B \qquad \textbf{(EQ 8.18)}$$

For BC and BCG faults:

$$V_A = V_A^B - V_A^C, \quad I_A = I_A^B - I_A^C \qquad \textbf{(EQ 8.19)}$$

For CA and CAG faults:

$$V_A = V_A^C - V_A^A, \quad I_A = I_A^C - I_A^A \qquad \textbf{(EQ 8.20)}$$

where K_0 is the zero sequence compensation factor (for the first six equations above)

For ABC faults, all three AB, BC, and CA loops are analyzed and the final result is selected based upon consistency of the results

The element calculates the distance to the fault (with *m* in miles or kilometers) and the phases involved in the fault.

The relay allows locating faults from delta-connected VTs. If the **FAULT REPORT 1 VT SUBSTITUTION** setting is set to “None”, and the VTs are connected in wye, the fault location is performed based on the actual phase to ground voltages. If the VTs are connected in delta, fault location is suspended.

If the **FAULT REPORT 1 VT SUBSTITUTION** setting value is “V0” and the VTs are connected in a wye configuration, the fault location is performed based on the actual phase to ground voltages. If the VTs are connected in a delta configuration, fault location is performed based on the delta voltages and externally supplied neutral voltage:

$$\begin{aligned} V_A &= \frac{1}{3}(V_N + V_{AB} - V_{CA}) \\ V_B &= \frac{1}{3}(V_N + V_{BC} - V_{AB}) \\ V_B &= \frac{1}{3}(V_N + V_{CA} - V_{BC}) \end{aligned} \qquad \textbf{(EQ 8.21)}$$

If the **FAULT REPORT 1 VT SUBSTITUTION** setting value is “I0” and the VTs are connected in a wye configuration, the fault location is performed based on the actual phase to ground voltages. If the VTs are connected in a delta configuration, fault location is performed based on the delta voltages and zero-sequence voltage approximated based on the zero-sequence current:

$$\begin{aligned} V_A &= \frac{1}{3}(V_{AB} - V_{CA}) - Z_{SYS0} I_0 \\ V_B &= \frac{1}{3}(V_{BC} - V_{AB}) - Z_{SYS0} I_0 \\ V_B &= \frac{1}{3}(V_{CA} - V_{BC}) - Z_{SYS0} I_0 \end{aligned} \qquad \textbf{(EQ 8.22)}$$

where Z_{SYS0} is the equivalent zero-sequence impedance behind the relay as entered under the fault report setting menu.

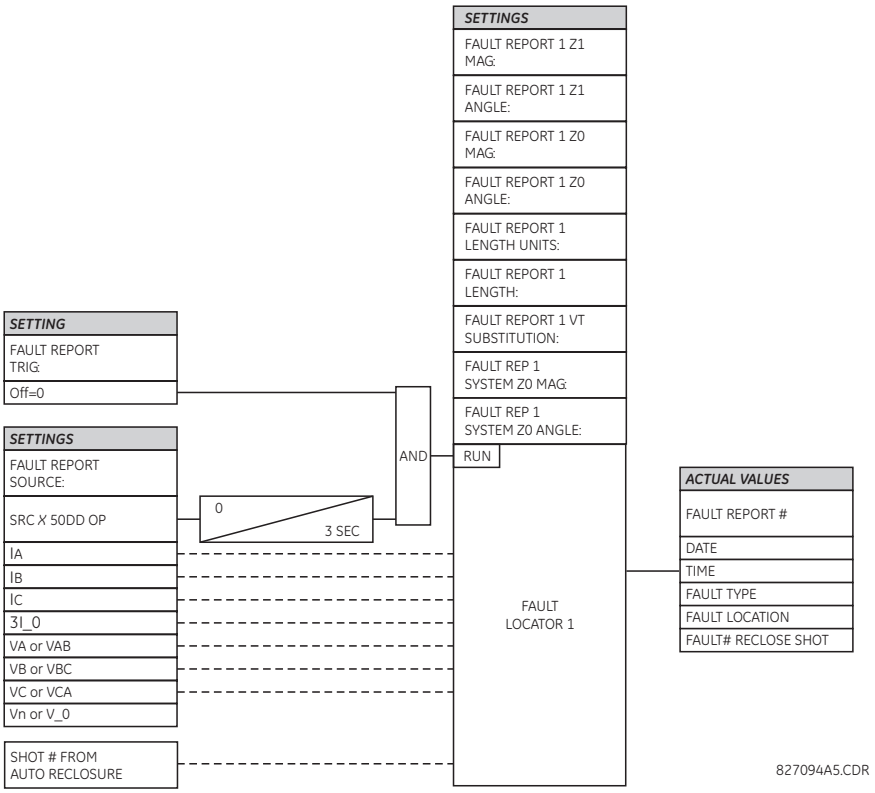


Figure 8–32: FAULT LOCATOR SCHEME

9.1.1 DESCRIPTION

The L60 Phase Comparison relay is designed to provide high-speed protection of transmission lines against all phase and ground faults when operated in the “mixed-excitation” mode. The term “mixed-excitation”, when applied to phase comparison, describes a scheme that first mixes different sequence quantities in a given proportion and phase angle, then performs a phase-comparison based on this mix.

A complete explanation of the Phase Comparison Element operation principles can be found in Chapter 8.

9.1.2 USE OF SETTINGS

87PC SIGNAL:

A mixed I_2–KI_1 signal or 3I_0 can be chosen as the operating signal for FDH and FDL excitation. In “mixed excitation” mode, the relay provides high-speed protection of transmission lines against all phase and ground faults. However, if a user wants the relay to operate only during ground faults, the 3I_0 mode can be chosen.

87PC MIXED SIGNAL K:

The K factor must be chosen for the mixed excitation operating signal. As indicated in Chapter 8: *Theory of Operation*, best results are obtained using a value of 0.2 (the default setting). The selected K value can range from 0.00 to 0.25. Setting K = 0 makes a phase comparison on the basis of negative-sequence excitation only. In such a scheme, the relay protects against all unbalanced faults; a suitable phase-distance relay should be used to protect against three-phase faults.

The user must remember that K is an important tool to set FDL and consequently FDH at the lower setting, especially in the cases when the margin between the maximum load current and the minimum fault current is very small. Reducing K to 0.15 or 0.10 makes phase comparison protection less sensitive to load current which in turn allows the user to provide enough sensitivity to the fault current. From the other hand it makes protection less sensitive to the balanced three-phase fault which in fact occurs very rarely.

87PC FDL PICKUP:

The main function of FDL is keying the transmitter. FDL pickup must be set above the KI_1 output of the mixing network for the maximum expected load. The recommended FDL setting is as follows;

- FDL = 1.1 × K × I1L where I1L is the maximum line load current and K is a mixed signal factor as described above. Higher margin may be required to definitely avoid FDL pickup during normal load condition.
- If the 3I_0 operating signal has been chosen, FDL should be set as FDL=1.1 × I1L where I1L is a maximum line load current.

It must be noted that in some cases a channel may also perform other functions if it is objectionable to key the transmitter constantly. In such cases, FDL could be set well below the KI_1 value of the mixing network resulting from maximum load but not less than 0.05 pu which defines the minimum required current from current transformers.

87PC FDH PICKUP:

The main function of FDH is to permit tripping as it arms the tripping output. FDH pickup must be set high enough so that it will not operate on maximum load. Also FDH must be set high enough to reset itself in the presence of heavy loads following clearing an external fault. The recommended setting for FDH is as follows:

$$FDH = (4/3) \times FDL + 0.375 \times Ic1$$

where Ic1 is total positive-sequence charging current under normal conditions.

A distance relay is recommended as an external fault detector if the minimum internal three-phase fault is less than twice the maximum load current. It allows coincidence detector to start comparing the local and received signals and to make trip decision if FDH is not picked up. Setting FD INPUT described below is to be used for assigning a distance element or some other elements.

If 3I_0 operating signal has been chosen, FDH should be set at most 0.66 times but preferably 0.5 times the minimum internal ground fault current to provide reliable sensitivity of the fault.

87PC FDL AUX:

This setting is provided for cases when sensitivity of the built-in FDL operating on the I_2 – K*I_1 quantity is not sufficient. This can happen on the weak terminal of the heavily loaded line. FDL AUX is connected in parallel with built-in FDL fault detector and is intended to be assigned with elements such as distance, negative-sequence overvoltage and overcurrent,

and ground directional. The user must be aware that auxiliary element assigned with FDL AUX does not provide any tripping function, but only starts the carrier to send pulses to remote terminal and allow the coincidence detector to make trip/block decisions.

87PC FDH AUX:

This setting is provided for cases (similar to FDL AUX) when sensitivity of the built-in FDH operating on the I_2 – K*I_1 quantity is not sufficient. FDH AUX is connected in parallel with the built-in FDH fault detector and is intended to be assigned with elements such as distance, negative-sequence overvoltage and overcurrent, and ground directional. FDH (along with FDH AUX) provides arming action for phase comparison trip decisions, allowing trips only when the coincidence detector detects internal fault conditions and FDL (or FDL AUX) operates.

87PC SYMMETRY CH 1(2):

This setting is used to make the local squared signal and the received signal from the remote terminal symmetrical. To set it properly, keying of the remote transmitter and an oscilloscope are required. If the received signal is ideally symmetrical with respect to the "Mark" and "Space" signals, a value of 0 ms (set as default) should be used. If for example, measured length of the "Mark" is longer than "Space" for 4.0 ms, setting "–2.0 ms" to be entered. If the measured length of the "Mark" is shorter than "Space" for 3.0 ms, setting "+1.5 ms" is to be entered. As sum of "Mark" and "Space" signals equals the length of the power cycle, corresponding scaling of the signals should be made for off nominal system frequencies.

Negative setting time is needed if the receiver elongates the received signal and positive setting time is needed if the receiver shortens the signal.

The L60 allows the customer to check and set channel symmetry without using an oscilloscope, by means of FlexLogic™ operands and applying the corresponding current to the relays which in turn key the PLC and consequently measure "Mark" and "Space" signals on the oscillography. Moving cursors and measuring an average from a few points time, the user can determine and enter setting.

87PC PHASE DELAY CH1(2):

This setting is made in the field to be equal to the sum of three delays; symmetry adjustment, propagation time of the line and receiver. Different methods can be used.

The L60 allows the customer to check and set phase delay without using an oscilloscope and by means of FlexLogic™ operands and applying the corresponding current to both relays. Oscillography shows the time difference (including PLC delay and line propagation time) between local and remote signals. Moving cursors and measuring an average from a few points time, the user can determine and apply the proper setting

87PC STABILITY ANGLE:

Stability angle setting must accommodate the security requirements for the external fault and dependability requirements for the internal fault. Default value 3 ms corresponds to about 65 degrees of blocking zone for a 60 Hz system. It overrides sources angular shift resulting from load, charging current, CT errors, etc.

The stability angle js can be estimated as follows:

$$\phi s = \phi load + \phi capac + \phi ct$$

where: $\phi load$ is a sources angular shift phase between the line terminal at maximum expected load, expressed in electrical degrees.
$\phi capac$ is the capacitive current compensation angle evaluated as $\phi capac = \arctan(Icapac / I_{FDH})$ expressed in electrical degrees, where Icapac is a line capacitive current, I_{FDH}-setting of FDH (fault detector high).
ϕct is the CTs error and saturation compensation angle and can be adopted as equal 10° for most cases unless there is a special consideration or concern. For such cases ϕct can be increased up to 20°.

87PC TRANS BLOCK PICKUP:

This setting is used to increase security during and after clearing of an external fault and to prevent false tripping during current reversals. The setting should be higher than the time difference in operation between FDH and output from the coincidence discriminator. A setting 10-30 ms gives sufficient security for most conditions.

87PC TRANS BLOCK RESET:

This setting is used to reset transient blocking and allow tripping. According to local conditions, setting should be considered as the sum of protection operating time and breaker opening time of the adjacent line and minus the Transient Pickup value to override uncertainty during clearing external faults. The faster the fault clearing at the adjacent line, the lower setting could be applied.

Ttr_rst = Tprot_adj + Tbreak_adj – Ttr_pkp

where: Tprot_adj is the expected time of main protection operation on the adjacent line,
Tbreak_adj is the operation time of the breaker on the adjacent line,
Ttr_pkp is selected Transient Pickup time.

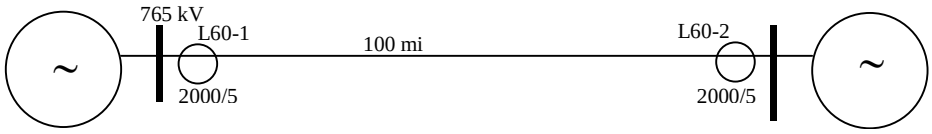
87PC BLOCK:

The user can define some cases when blocking of the phase comparison scheme is required. This setting will block the tripping function. PLC alarm contacts indicating channel failure are usually assigned for this setting,. especially in blocking schemes.

87PC CHNL LOSS TRIP WINDOW:

This setting is applicable to the 2TL-BL-DPC-2FL scheme only. The typical setting is 150 ms.

9.1.3 SETTINGS EXAMPLE



Consider settings for a single-circuit 765 kV line, 100 miles length, 50 Ohms primary impedance, 5520 ohms shunt capacitance of the line, maximum expected load of 2000A, CT ratio 2000/5, minimum expected internal 3-phase fault is 8000A.

1. Mixed signal factor K=0.2
2. FDL pickup: I_{FDL} = 1.1 × 2000 × 0.2 = 440 A or 440 / 400 = 1.1 A secondary.
   The setting is 1.1 / 5 = 0.22 pu.
3. FDH pickup: I_{FDH} = 4/3*I_{FDL}+0.375*Icapac = 1.33*440+0.375*80 = 615.2 A or 615.2/400 = 1.54 A secondary; setting is 1.76/5 = 0.31 pu. Where Icapac=765000/(√3*5520) = 80 A
4. Stability angle:

   $\underline{\phi}$load = 2*arcsin((2000*50*√3)/(2*765000)) = 13.0°

   $\underline{\phi}$capac = arctan(Icapac/I_{FDH}) = arctan(80/615.2) = 7.4°

   $\underline{\phi}$s(deg) = 13.0°+7.4°+10° = 30.4°

   Minimum recommended setting 60° (set as default) should be applied.
5. Check against requirement for trip supervision by distance relay: As minimum internal 3-phase fault is much than twice the maximum line load current, no distance element is required for be assigned to FD INPUT setting.

9.2.1 DESCRIPTION

Many high voltage lines have transformers tapped to the line serving as an economic approach to the supply of customer load. A typical configuration is shown in the figure below.

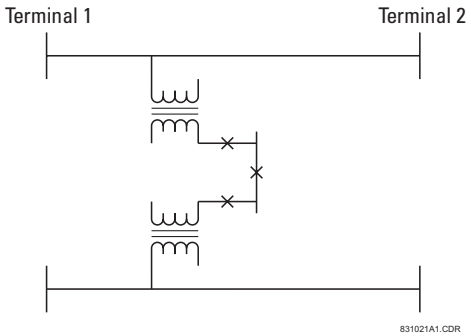


Figure 9–1: TYPICAL HV LINE CONFIGURATION

Two distinctly different approaches are available, Distance Backup and Distance Supervision, depending on which concerns are dominant. In either case, the distance function can provide a definite time backup feature to give a timed clearance for a failure of the L60 communications. Additionally, a POTT (Permissive Over-reaching Transfer Trip) scheme can be selected and activated after detection of an L60 communications failure, if an alternate lower bandwidth communications channel is available.

If **Distance Backup** is employed, dependability concerns usually relate to a failure of the communications. The distance elements can then effectively provide a means of fault identification and clearance. However, for a line with tapped transformers, a number of other issues need to be considered to ensure stability for the L60.

Any differential scheme has a potential problem when a LV fault occurs at the tapped transformer location, and the current at the tap is not measured. Because the transformer size can become quite large, the required increase in the differential setting to avoid operation for the LV bus fault can result in a loss of sensitivity.

If the tapped transformer is a source of zero sequence infeed, then the L60 zero-sequence current removal has to enabled as described in the next section.

The zero sequence infeed creates an apparent impedance setting issue for the backup ground distance and the zero sequence compensation term is also not accurate, so that the positive sequence reach setting must be increased to compensate. The phase distance reach setting may also have to be increased to cope with a transfer across the two transformers, but this is dependent on the termination and configuration of the parallel line.

Three terminal line applications generally will result in larger reach settings for the distance backup and require a calculation of the apparent impedance for a remote fault. This should be carried out for each of the three terminals, as the calculated apparent impedance will be different at each terminal.

Distance Supervision essentially offers a solution for the LV fault condition, but the differential setting must still be increased to avoid operation for an external L-g or L-L-g fault external ground fault. In addition, the distance element reach setting must still see all faults within the protected line and be less than the impedance for a LV bus fault

The effective SIR (source impedance ratio) for the LV fault generally is not high, so that CVT transients do not contribute to measuring errors.

If the distance supervision can be set to avoid operation for a transformer LV fault, then generally the filtering associated with the distance measuring algorithm will ensure no operation under magnetizing inrush conditions. The distance element can be safely set up to $2.5 \times V_{nom} / I_{peak}$, where V_{nom} is the system nominal voltage and I_{peak} is the peak value of the magnetizing inrush current.

For those applications where the tapped station is close to one terminal, then it may be difficult to set the distance supervision to reach the end of the line, and at the same time avoid operation for a LV fault. For this system configuration, a 3-terminal L60 should be utilized; the third terminal is then fed from CT on the high side of the tapped transformer.

9.2.2 LINES WITH TAPPED TRANSFORMERS

If a protected line has a tapped transformer, it is preferable to apply the L60 in a three-terminal configuration. This provides the most secure and reliable solution. However, if current measurements or the channel between the tapped line(s) and the two other terminals are not available, then the measures outlined in the following sections must be taken.

9.2.3 TRANSFORMER LOAD CURRENTS

The L60 can be applied on the line with a tapped transformer. Since the tapped line may be energized from one terminal only, or there may be a low current flowing through the line, the phase-comparison element must set to provide stability. Accordingly, the FDH pickup setting must be high enough to prevent maloperation from the total load current of the tapped transformer(s). However, this does not guarantee correct operation of L60 during transformer energization and LV transformer faults. Increasing the FDL and FDH settings to be immune from transformer inrush current and transformer LV fault decreases sensitivity – as such, calculations should take into account the requirement for the pickup setting resulting from line charging currents as well. Certainly, a security factor must be applied to the above stability conditions. Alternatively, distance supervision can be considered to prevent maloperation due to transformer load currents.

9.2.4 LV-SIDE FAULTS

Distance supervision should be used to prevent maloperation of the L60 protection system during faults on the LV side of the transformer(s). As explained earlier, the distance elements should be set to overreach all line terminals, and at the same time safely underreach the LV busbars of all the tapped transformers. This may present some challenges, particularly for long lines and large transformer tapped close to the substations. If the L60 system retrofits distance relays, there is a good chance that one can set the distance elements to satisfy the imposed. If more than one transformer is tapped, particularly on parallel lines, and the LV sides are interconnected, detailed short circuit studies may be needed to determine the distance settings.

9.2.5 TRANSFORMER INRUSH CURRENT

The L60 has the capability to detect harmonics caused by transformer inrush current or other phenomena like sub-synchronous oscillations caused by active power system components. During transformer energization, current at the line terminal CTs contain the entire spectrum of harmonics, including 2nd, 5th, 11th and 14th. On the HV-side of the transformer, the 2nd harmonic prevails and is used to detect transfer inrush for transformer differential inhibit. However, on the line terminal CT, the shunt reactor harmonic spectrum contains additional harmonics due to line capacitance and inductance. Therefore, it is beneficial to use THD for line protection. The figure below illustrates an HV line with tapped transformer energization, depicting the difference in inrush currents to the transformer location and line terminal CT.

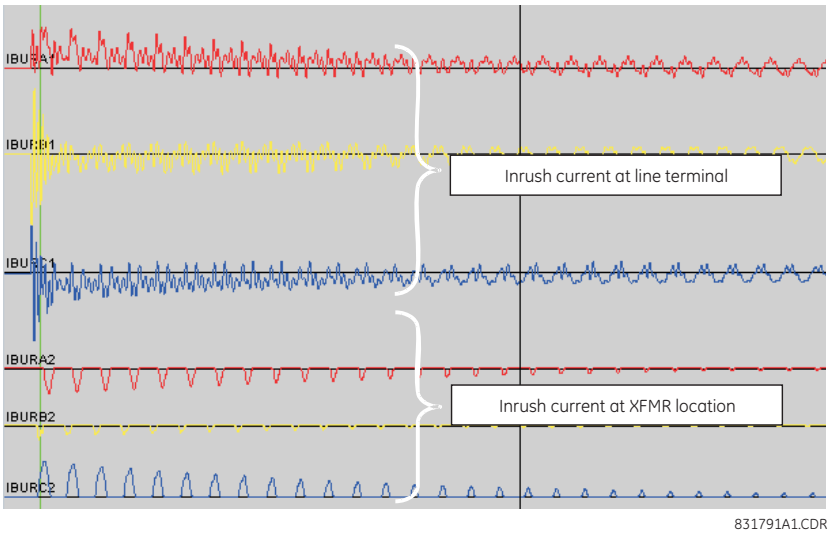
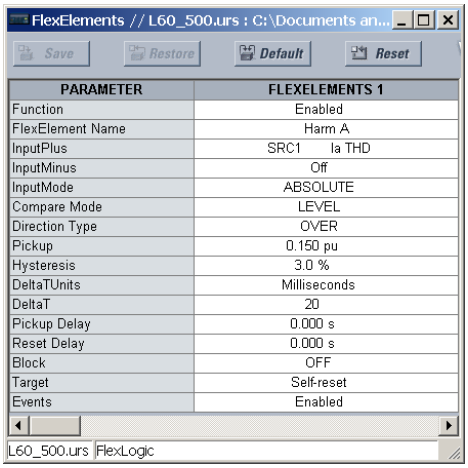


Figure 9–2: SAMPLE INRUSH CURRENT OF THE TAPPED LINE TRANSFORMER ENERGIZATION

The L60 measures total harmonic distortion (THD) in all three phase currents and neutral current. These measurements are available for protection purposes though FlexElements™ (universal comparators). The FlexElement™ output can be used to block sensitive neutral instantaneous overcurrent or phase comparison on transformer energization.



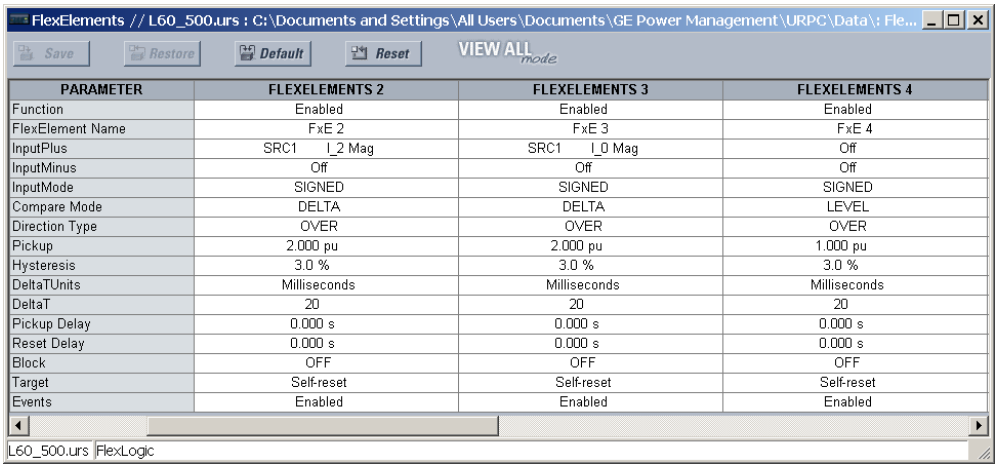
PARAMETER	FLEXELEMENTS 1
Function	Enabled
FlexElement Name	Harm A
InputPlus	SRC1 Ia THD
InputMinus	Off
InputMode	ABSOLUTE
Compare Mode	LEVEL
Direction Type	OVER
Pickup	0.150 pu
Hysteresis	3.0 %
DeltaTUnits	Milliseconds
DeltaT	20
Pickup Delay	0.000 s
Reset Delay	0.000 s
Block	OFF
Target	Self-reset
Events	Enabled

Figure 9–3: USING FLEXELEMENTS™ FOR HARMONICS DETECTION

The typical pickup setting for THD is 10 to 25%. THD measurements are available per source. As such, for breaker-and-a-half applications, the source used to sum the CT currents can be used.

9.2.6 TRACTIONAL LOAD

Where tractional load is tapped form the line protected by L60, significant and variable negative-sequence current may exist on the line, thereby not allowing sensitive FDL and FDH settings. On such lines, it is beneficial to detect faults based on change in the sequence components of the currents. Again, FlexElements™ can be used for such an application.



PARAMETER	FLEXELEMENTS 2	FLEXELEMENTS 3	FLEXELEMENTS 4
Function	Enabled	Enabled	Enabled
FlexElement Name	FxE 2	FxE 3	FxE 4
InputPlus	SRC1 I_2 Mag	SRC1 I_0 Mag	Off
InputMinus	Off	Off	Off
InputMode	SIGNED	SIGNED	SIGNED
Compare Mode	DELTA	DELTA	LEVEL
Direction Type	OVER	OVER	OVER
Pickup	2.000 pu	2.000 pu	1.000 pu
Hysteresis	3.0 %	3.0 %	3.0 %
DeltaTUnits	Milliseconds	Milliseconds	Milliseconds
DeltaT	20	20	20
Pickup Delay	0.000 s	0.000 s	0.000 s
Reset Delay	0.000 s	0.000 s	0.000 s
Block	OFF	OFF	OFF
Target	Self-reset	Self-reset	Self-reset
Events	Enabled	Enabled	Enabled

Figure 9–4: USING FLEXELEMENTS™ TO DETECT CHANGES IN CURRENT SEQUENCE COMPONENTS

The example above depicts FlexElements™ programmed to detect changes in the positive, negative and zero-sequence currents two times per power cycle on a 50 Hz system. The FlexElement™ outputs should be assigned to the **87PC FDL AUX** and **87PC FDH AUX** settings to start phase comparison when a change in the current components is detected. These Flex-Elements™ are immune to slow increases of the current components, but will operate for step changes of the operating quantities.

9.2.7 SENSITIVITY ISSUES

Phase comparison is fundamentally dependent on the coincidence of local and remote squares to ensure a correct tripping decision. However, correct starting by the FDL detector and arming action by the FDH detector should be ensured to allow the coincidence detector operate correctly. Therefore, some precautions are necessary when choosing settings for FDL and FDH or assigning auxiliary elements to compliment those detectors.

Even if direct coordination between FDL and FDH at opposite ends of the line is not required, FDH and FDL must have enough security margin. This is especially critical when the blocking scheme is used. It is not advisable to set the FDH pickup at one end of the line close to or lower than FDL at other end of the line. FDL at the remote terminal should always be more sensitive and reach further to external faults behind remote bus. In the figure below, it is critical to ensure that for any fault F1 beyond terminal B, where FDH of Protection #1 still operates, the FDL at terminal B is sensitive enough and has at least 20% margin for operation. The fault current must also be considered, even for through faults which might be quite different due to line capacitance, reactors on the line, etc. The situation worsens when there is a tapped load off the protected line which can infeed/outfeed fault current. The same checks are required to coordinate Protection #2 FDH with Protection #1 FDL for fault F2.

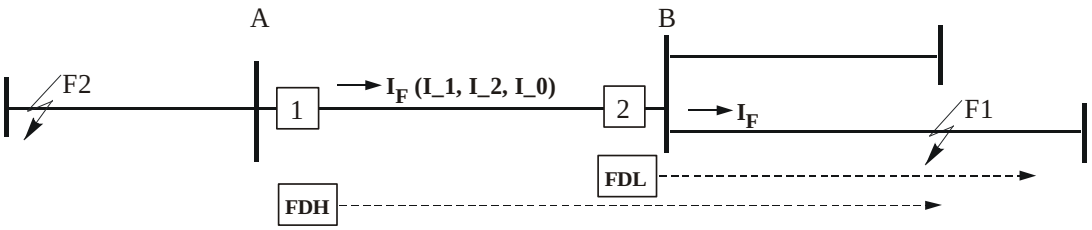


Figure 9–5: COORDINATION BETWEEN FDH AND FDL AT OPPOSITE ENDS OF THE LINE

Taking into consideration the points indicated above, the procedure for choosing FDL/FDH settings and checking sensitivity is as follows:

1. Pickup settings for FDL and FDH are calculated per the recommendations above.
2. For all internal faults on the line, a check is performed to ensure a minimum 20% margin in sensitivity for both FDL and FDH detectors at all terminals, according to the operating quantity formula for all system configurations.
3. If there is not enough margin in sensitivity, then steps must be taken to provide carrier start and trip permission. It is preferable to employ built-in functionality, as it provides reliable and deterministic coordination between FDL and FDH at opposite ends of the line. The following options can be employed:
   - Lowering the *K* factor in the composite signals. As such, detectors are less dependent on load current and can be set to be more sensitive to asymmetrical faults. However, this may affect sensitivity to three-phase faults and must be addressed by using supplementary protection functions (see below).
   - Assigning supplementary protection elements. Protection elements, like forward-looking overreaching phase distance or simple undervoltage protection, can be assigned via the FDL AUX or FDH AUX settings to boost 87PC carrier start and trip supervision.
4. Once the FDL and FDH settings are selected, check for FDL and FDH coordination at opposite line terminals as indicated in the figure above.
   - For an external fault at the adjacent line (fault F1 for protection at terminal A), determine the sensitivity of FDH.
   - For protection at terminal B, ensure FDL sensitivity by a margin that overlaps the Protection A FDH zone by at least 20%.
   - If there is not enough sensitivity, a reverse looking distance zone or neutral/negative-sequence directional overcurrent element might be assigned to the FDL AUX setting to secure FDL operation during external faults.
   - Similar checks must be performed for the F2 fault.

In some applications, for example, radial line terminated with autotransformer or terminal with a weak source, where there might be issues with sensitivity of FDL and FDH, additional elements have to be assigned to 87PC FDL AUX and 87PC FDH AUX settings. These elements include distance, negative-sequence overvoltage, zero-sequence overvoltage, positive-sequence undervoltage.

The phase comparison process of exchanging with HF signals is ready when the operating current (mixed or zero-sequence) is above 2%. If an internal fault is detected, the challenge is to provide starting transmitting signals at both ends and to have enough operating quantity for arming FDH to operate and to allow tripping.

9.2.8 SINGLE-POLE TRIPPING APPLICATIONS

Phase comparison is fundamentally dependent on the coincidence of local and remote squares to ensure a correct tripping decision. However, correct starting by the FDL detector and arming action by the FDH detector should be ensured to allow the coincidence detector operate correctly. Therefore, some precautions are necessary when choosing settings for FDL and FDH or assigning auxiliary elements to compliment those detectors.

Even if direct coordination between FDL and FDH at opposite ends of the line is not required, FDH and FDL must have enough security margin. This is especially critical when the blocking scheme is used. It is not advisable to set the FDH pickup at one end of the line close to or lower than FDL at other end of the line. FDL at the remote terminal should always be more sensitive and reach further to external faults behind remote bus. In the figure below, it is critical to ensure that for any fault F1 beyond terminal B, where FDH of Protection #1 still operates, the FDL at terminal B is sensitive enough and has at least 20% margin for operation. The fault current must also be considered, even for through faults which might be quite different due to line capacitance, reactors on the line, etc. The situation worsens when there is a tapped load off the protected line which can infeed/outfeed fault current. The same checks are required to coordinate Protection #2 FDH with Protection #1 FDL for fault F2.

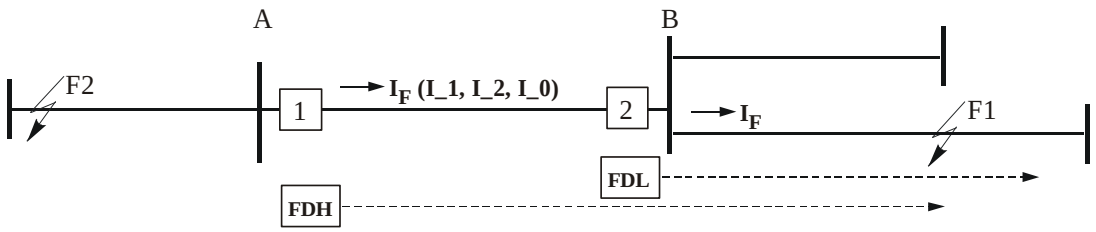


Figure 9–6: COORDINATION BETWEEN FDH AND FDL AT OPPOSITE ENDS OF THE LINE

Taking into consideration the points indicated above, the procedure for choosing FDL/FDH settings and checking sensitivity is as follows:

1. Pickup settings for FDL and FDH are calculated per the recommendations above.
2. For all internal faults on the line, a check is performed to ensure a minimum 20% margin in sensitivity for both FDL and FDH detectors at all terminals, according to the operating quantity formula for all system configurations.
3. If there is not enough margin in sensitivity, then steps must be taken to provide carrier start and trip permission. It is preferable to employ built-in functionality, as it provides reliable and deterministic coordination between FDL and FDH at opposite ends of the line. The following options can be employed:
   - Lowering the *K* factor in the composite signals. As such, detectors are less dependent on load current and can be set to be more sensitive to asymmetrical faults. However, this may affect sensitivity to three-phase faults and must be addressed by using supplementary protection functions (see below).
   - Assigning supplementary protection elements. Protection elements, like forward-looking overreaching phase distance or simple undervoltage protection, can be assigned via the FDL AUX or FDH AUX settings to boost 87PC carrier start and trip supervision.
4. Once the FDL and FDH settings are selected, check for FDL and FDH coordination at opposite line terminals as indicated in the figure above.
   - For an external fault at the adjacent line (fault F1 for protection at terminal A), determine the sensitivity of FDH.
   - For protection at terminal B, ensure FDL sensitivity by a margin that overlaps the Protection A FDH zone by at least 20%.
   - If there is not enough sensitivity, a reverse looking distance zone or neutral/negative-sequence directional overcurrent element might be assigned to the FDL AUX setting to secure FDL operation during external faults.
   - Similar checks must be performed for the F2 fault.

In some applications, for example, radial line terminated with autotransformer or terminal with a weak source, where there might be issues with sensitivity of FDL and FDH, additional elements have to be assigned to 87PC FDL AUX and 87PC FDH AUX settings. These elements include distance, negative-sequence overvoltage, zero-sequence overvoltage, positive-sequence undervoltage.

The phase comparison process of exchanging with HF signals is ready when the operating current (mixed or zero-sequence) is above 2%. If an internal fault is detected, the challenge is to provide starting transmitting signals at both ends and to have enough operating quantity for arming FDH to operate and to allow tripping.

9.2.9 SECURITY ON WEAK OR NOISY PLC CHANNELS

On some 87PC blocking applications, PLC channels can exhibit sudden interruptions in the received blocking signals (“holes” in the carrier) due to communications noise caused by arcing on the line, leading to 87PC nuisance trip. Extra security can be achieved by allowing a trip only after two or more operations of the coincidence detector occurring on consecutive power cycles. This can be implemented by setting **87PC RESET** to “0” and using digital elements to count the number of coincidences.

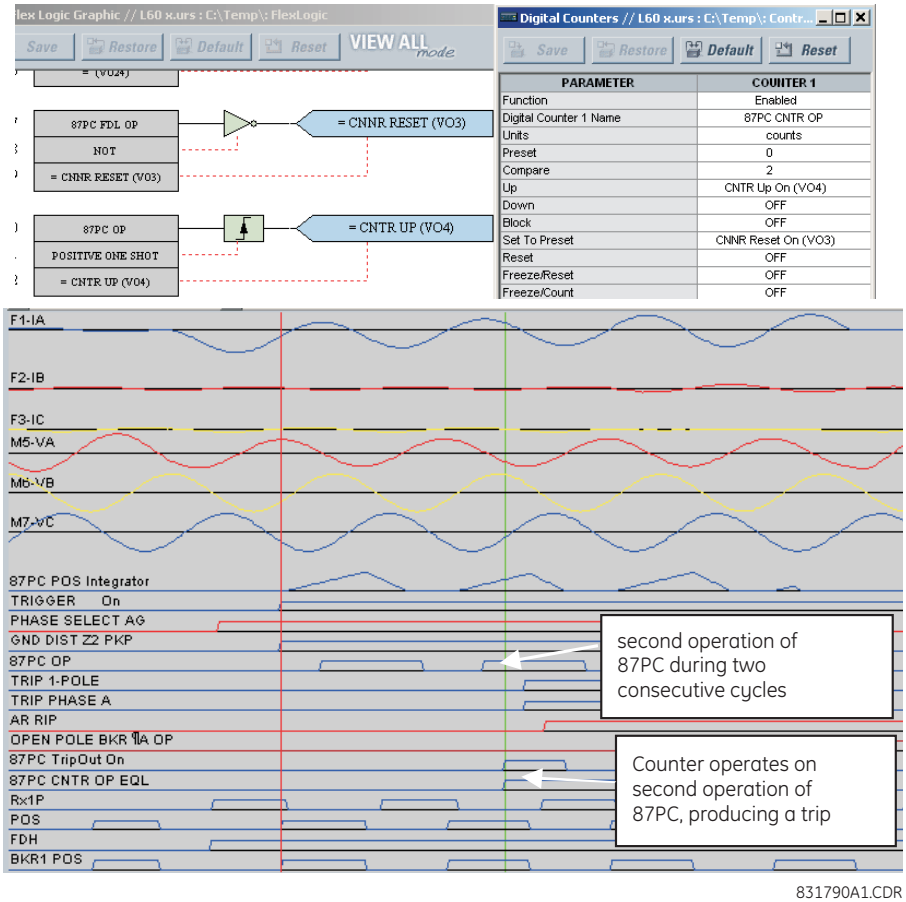


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Figure 9–7: SECURE TRIPPING ON THE 2ND COINCIDENCE OF THE 87PC ELEMENT

a) PHASE CURRENT SUPERVISION AND THE FUSE FAILURE ELEMENT

The phase-to-phase (delta) current is used to supervise the phase distance elements, primarily to ensure that in a de-energized state the distance elements will not be picked up due to noise or induced voltages, on the line.

However, this supervision feature may also be employed to prevent operation under fuse failure conditions. This obviously requires that the setting must be above maximum load current and less than the minimum fault conditions for which operation is expected. This potential problem may be avoided by the use of a separate fuse fail function, which means that the phase current supervision can be set much lower, typically two times the capacitance charging current of the line.

The usage of the fuse fail function is also important during double-contingency events such as an external fault during fuse fail conditions. The current supervision alone would not prevent maloperation in such circumstances.

It must be kept in mind that the fuse failure element provided on the L60 needs some time to detect fuse fail conditions. This may create a race between the instantaneous zone 1 and the fuse failure element. Therefore, for maximum security, it is recommended to both set the current supervision above the maximum load current and use the fuse failure function. The current supervision prevents maloperation immediately after the fuse fail condition giving some time for the fuse failure element to take over and block the distance elements permanently. This is of a secondary importance for time-delayed zones 2 and up as the fuse failure element has some extra time for guaranteed operation. The current supervision may be set below the maximum load current for the time delayed zones.

Blocking distance elements during fuse fail conditions may not be acceptable in some applications and/or under some protection philosophies. Applied solutions may vary from not using the fuse failure element for blocking at all; through using it and modifying – through FlexLogic™ and multiple setting groups mechanisms – other protection functions or other relays to provide some protection after detecting fuse fail conditions and blocking the distance elements; to using it and accepting the fact that the distance protection will not respond to subsequent internal faults until the problem is addressed.

NOTE

To be fully operational, the Fuse Failure element must be enabled, and its output FlexLogic™ operand must be indicated as the blocking signal for the selected protection elements.

For convenience, the current supervision threshold incorporates the $\sqrt{3}$ factor.

b) PHASE DISTANCE ZONE 1

As typically used for direct tripping, the zone 1 reach must be chosen so that it does not extend beyond the far end(s) of the protected line. Zone 1 provides nominally instantaneous protection for any phase fault within a pre-determined distance from the relay location. To ensure that no overreach occurs, typically requires a setting of 80 to 90% of the line length, which covers CT and VT errors, relay inaccuracy and transient overreach as well as uncertainty in the line impedance for each phase, although transposition may minimize this latter concern.

The total relay inaccuracy including both steady state and transient overreach even when supplied from CVTs under the source impedance ratios of up to 30, is below 5%.

c) PHASE DISTANCE ZONE 2

Zone 2 is an overreaching element, which essentially covers the final 10 to 20% whole of the line length with a time delay. The additional function for the zone 2 is as a timed backup for faults on the remote bus. Typically the reach is set to 125% of the positive-sequence impedance of the line, to ensure operation, with an adequate margin, for a fault at 100% of the line length. The necessary time delay must ensure that coordination is achieved with the clearance of a close-in fault on the next line section, including the breaker operating time.

The zone 2 time delay is typically set from 0.2 to 0.6 seconds, although this may have to be reviewed more carefully if a short line terminates on the remote bus, since the two zone 2 elements may overlap and therefore not coordinate in a satisfactory manner.

d) PHASE DISTANCE ZONE 3

If a remote backup philosophy is followed, then the reach of this element must be set to account for any infeed at the remote bus, plus the impedance of the longest line which terminates on this remote bus. The time delay must coordinate with other time-delayed protections on any remote line. Circuit loading limitations created by a long zone reach may be overcome by using lens or quadrilateral characteristics and/or a load encroachment supervising characteristic. Consider-

ation should also be given to a situation where the load impedance may enter into the relay characteristic for a time longer than the chosen time delay, which could occur transiently during a system power swing. For this reason the power swing blocking function should be used.

9.2.11 GROUND DISTANCE

a) NEUTRAL CURRENT SUPERVISION

The current supervision for the ground distance elements responds to an internally calculated neutral current (3 × I_0). The setting for this element should be based on twice the zero-sequence line capacitance current or the maximum zero-sequence unbalance under maximum load conditions. This element should not be used to prevent an output when the load impedance is inside the distance characteristic on a steady state basis.

b) GROUND DISTANCE ZONE 1

The zone 1 reach must be set so that nominally instantaneous operation does not extend beyond the end of the protected line. However this may be somewhat more complicated than for the phase elements, because of zero sequence mutual induction with an adjacent parallel line, possibly carried on the same tower, which can be out of service and grounded at multiple points. A fault beyond 100% of the protected line may cause overreach unless the reach is reduced significantly, sometimes as low as 65% of the line length. If the line being protected does not have a significant interaction with an adjacent circuit, then the typical 80% setting may be used. If there is significant mutual coupling between the parallel lines, then the mutual compensation feature of the ground distance elements can be used instead of a drastic reduction in the reach.

However, even in this case, there is more uncertainty as compared with the phase distance elements because the zero-sequence impedance of the line and thus the zero-sequence-compensating factors may vary significantly due to weather and other conditions.

c) GROUND DISTANCE ZONE 2

To ensure that the zone 2 can see 100% of the line, inter-circuit mutual effects must be considered, as they can contribute to a significant under-reach. Typically this may occur on double circuit lines, when both lines may carry the same current. An analytical study should be carried out to determine the appropriate reach setting.

The main purpose of this element is to operate for faults beyond the reach of the local zone 1 element, and therefore a time delay must be used similar to the phase fault case.

d) GROUND DISTANCE ZONE 3

This remote back up function must have a reach which is set to account for any infeed at the remote bus, plus the impedance of the longest line which terminates on this remote bus. Similar to the phase fault case, a zone 3 element must be time coordinated with timed clearances on the next section.

9.3.1 DESCRIPTION

This scheme is intended for two-terminal line applications only.

This scheme uses an over-reaching Zone 2 distance element to essentially compare the direction to a fault at both the ends of the line.

Ground directional overcurrent functions available in the relay can be used in conjunction with the Zone 2 distance element to key the scheme and initiate its operation. This provides increased coverage for high-resistance faults.

Good directional integrity is the key requirement for an over-reaching forward-looking protection element used to supplement Zone 2. Even though any FlexLogic™ operand could be used for this purpose allowing the user to combine responses of various protection elements, or to apply extra conditions through FlexLogic™ equations, this extra signal is primarily meant to be the output operand from the Neutral Directional IOC. Both of these elements have separate forward (FWD) and reverse (REV) output operands. The forward indication should be used (NEUTRAL DIR OC1 FWD).

An important consideration is when one of the line terminals is open. It is then necessary to identify this condition and arrange for a continuous sending of the permissive signal or use a slower but more secure echo feature to send a signal to the other terminal, which is producing the fault infeed. With any echo scheme however, a means must be provided to avoid a permanent lock up of the transmit/receive loop. The echo co-ordination (ECHO DURATION) and lock-out (ECHO LOCKOUT) timers perform this function by ensuring that the permissive signal is echoed once for a guaranteed duration of time before going to a lockout for a settable period of time.

It should be recognized that in ring bus or breaker and a half situations, it may be the line disconnect or a combination of the disconnect and/or the breaker(s) status that is the indication that the terminal is open.

The **POTT RX PICKUP DELAY** timer is included in the permissive receive path to ride through spurious receive outputs that may be produced during external faults, when power line carrier is utilized as the communications medium.

No current reversal logic is included for the overreaching phase and ground distance elements, because long reaches are not usually required for two terminal lines. A situation can occur however, where the ground distance element will have an extended reach. This situation is encountered when it is desired to account for the zero sequence inter-circuit mutual coupling. This is not a problem for the ground distance elements in the L60 which do have a current reversal logic built into their design as part of the technique used to improve ground fault directionality.

Unlike the distance protection elements the ground directional overcurrent functions do not have their reach well defined, therefore the current reversal logic is incorporated for the extra signal supplementing Zone 2 in the scheme. The transient blocking approach for this POTT scheme is to recognize that a permissive signal has been received and then allow a settable time **TRANS BLOCK PICKUP DELAY** for the local forward looking directional element to pick up.

The scheme generates an output operand (POTT TX) that is used to transmit the signal to the remote end. Choices of communications channel include Remote Inputs/Outputs and telecommunications interfaces. When used with telecommunications facilities the output operand should be assigned to operate an output contact connected to key the transmitter at the interface. Power Line Carrier (PLC) channels are not recommended for this scheme since the PLC signal can be interrupted by a fault.

For proper operation of the scheme the Zone 2 phase and ground distance elements must be enabled, configured and set per rules of distance relaying. The Line Pickup element should be enabled, configured and set properly to detect line-end-open/weak-infeed conditions.

If used by this scheme, the selected ground directional overcurrent function(s) must be enabled, configured and set accordingly The output operand from the scheme (POTT OP) must be configured to interface with other relay functions, output contacts in particular, in order to make the scheme fully operational. Typically, the output operand should be programmed to initiate a trip, breaker fail, and auto-reclose, and drive a user-programmable LED as per user application.

Traditionally, the reach setting of an underreaching distance function shall be set based on the net inductive impedance between the potential source of the relay and the far-end busbar, or location for which the zone must not overreach. Faults behind series capacitors on the protected and adjacent lines need to be considered for this purpose. For further illustration a sample system shown in the figure below is considered.

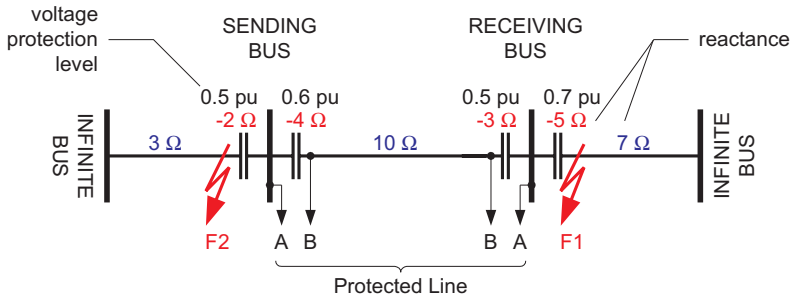

Figure 9–8: SAMPLE SERIES COMPENSATED SYSTEM

Assuming 20% security margin, the underreaching zone shall be set as follows.

At the Sending Bus, one must consider an external fault at F1 as the 5 Ω capacitor would contribute to the overreaching effect. Any fault behind F1 is less severe as extra inductive line impedance increases the apparent impedance:

Reach Setting: 0.8 x (10 – 3 – 5) = 1.6 Ω if the line-side (B) VTs are used
Reach Setting: 0.8 x (10 – 4 – 3 – 5) = –1.6 Ω if the bus-side (A) VTs are used

The negative value means that an underreaching zone cannot be used as the circuit between the potential source of the relay and an external fault for which the relay must not pick-up, is overcompensated, i.e. capacitive.

At the Receiving Bus, one must consider a fault at F2:

Reach Setting: 0.8 x (10 – 4 – 2) = 3.2 Ω if the line-side (B) VTs are used
Reach Setting: 0.8 x (10 – 4 – 3 – 2) = 0.8 Ω if the bus-side (A) VTs are used

Practically, however, to cope with the effect of sub-synchronous oscillations, one may need to reduce the reach even more. As the characteristics of sub-synchronous oscillations are in complex relations with fault and system parameters, no solid setting recommendations are given with respect to extra security margin for sub-synchronous oscillations. It is strongly recommended to use a power system simulator to verify the reach settings or to use an adaptive L60 feature for dynamic reach control.

If the adaptive reach control feature is used, the **PHS DIST Z1 VOLT LEVEL** setting shall be set accordingly.

This setting is a sum of the overvoltage protection levels for all the series capacitors located between the relay potential source and the far-end busbar, or location for which the zone must not overreach. The setting is entered in pu of the phase VT nominal voltage (RMS, not peak value).

If a minimum fault current level (phase current) is causing a voltage drop across a given capacitor that prompts its air gap to flash over or its MOV to carry practically all the current, then the series capacitor shall be excluded from the calculations (the capacitor is immediately by-passed by its overvoltage protection system and does not cause any overreach problems).

If a minimum fault current does not guarantee an immediate capacitor by-pass, then the capacitor must be included in the calculation: its overvoltage protection level, either air gap flash-over voltage or MOV knee-point voltage, shall be used (RMS, not peak value).

Assuming none of the series capacitors in the sample system is guaranteed to get by-passed, the following calculations apply:

For the Sending Bus: 0.5 + 0.7 = 1.2 pu if the line-side (B) VTs are used
0.6 + 0.5 + 0.7 = 1.8 pu if the bus-side (A) VTs are used

For the Receiving Bus: 0.6 + 0.5 = 1.1 pu if the line-side (B) VTs are used
0.6 + 0.5 + 0.5 = 1.6 pu if the bus-side (A) VTs are used

9.5.1 OVERVIEW

The L60 oscillography feature is a powerful tool for tuning, commissioning, and troubleshooting. It also helps to understand the theory of phase-comparison and how the L60 relay incorporates standard analog phase comparison principles. The L60 oscillography allows customer to observe not only AC waveforms and 87PC operate signals, but all details of composite signal forming, fault detector operation, input and output processing, squares forming, coincidence detection, and integration of the signal. All currents are processed per CT breaker on breaker-and-a-half applications (applies to composite signal, fault detectors, etc.).

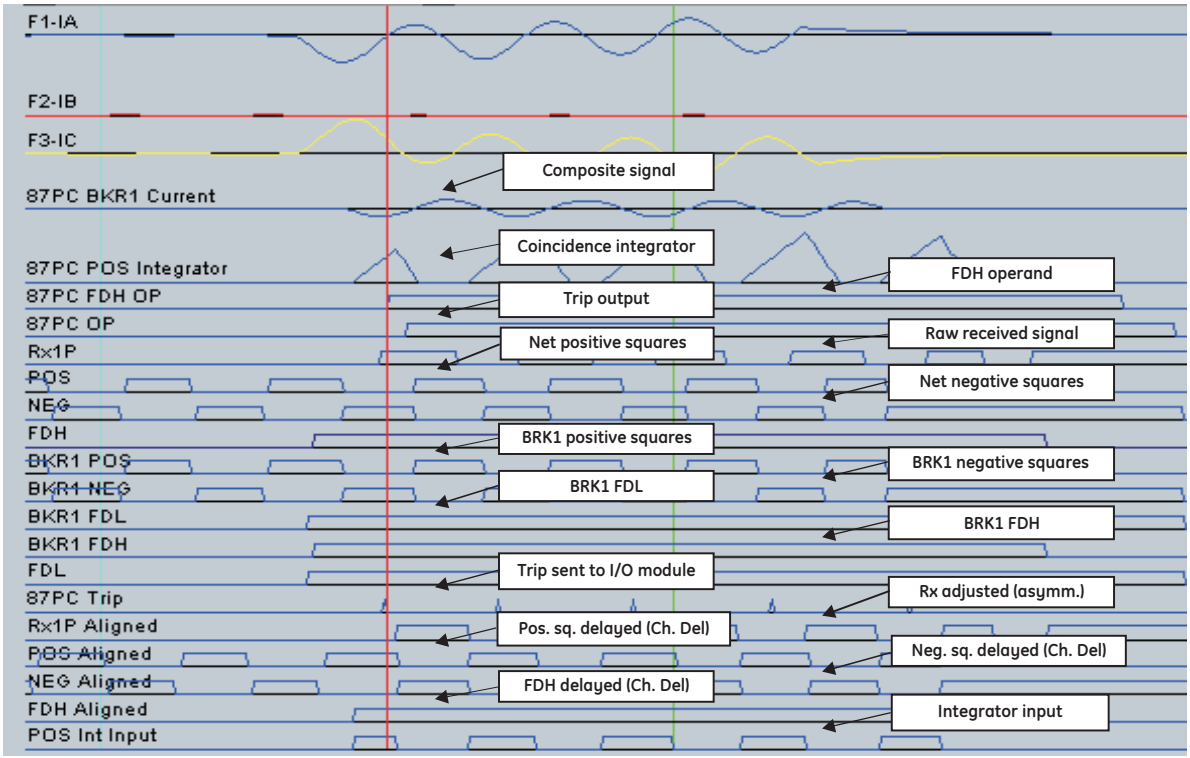

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Figure 9–9: MAIN L60 OSCILLOGRAPHY SIGNALS

As explained in the *Theory of Operation* chapter, the phase comparison operating current is either mixed from all three phase currents into one composite quantity using the I_2 – K × I_1 formula, or it is just 3I_0. In contrast to phase current waveforms, where raw samples are captured and displayed, the operating current is digitally filtered with the DC component and harmonics removed. During no-fault conditions, the operating current is relatively small and dictated mostly by the load positive sequence current (FDL and FDH detectors drop off). However, the **POS** local pulses at the positive half of the power cycle and the **NEG** local pulses at the negative half of the power cycle are present in oscillography once the operating current is greater than 0.02 pu. When the **87PC BRK1** operating current (or **87PC BRK2** current for two-breaker applications) exceeds the FDL pickup setting, the **BRK1 FDL** (and **BRK2 FDL** for two breaker applications) flags are asserted, indicating a fault condition and thus initiating transmitting squares on the positive (**Tx POS**) and negative (**Tx NEG**) halves of the sine-wave. At this moment, the logic is preparing to process the phase comparison algorithms according to the selected schemes and setting values.

The next step is to adjust pulses according to channel asymmetry and channel delay. The received pulse is adjusted in accordance to the **CHANNEL ASYMMETRY** setting. If this setting is quite high, then the adjusted signals (**RX1P ALIGNED**, **RX1N ALIGNED**, etc.) are also delayed to properly align with a local pulse. The local aligned signals (**POS ALIGNED** and **NEG ALIGNED**) are derived from either one CT current or from two CTs current and are delayed as per channel delay setting.

Even when FDL and FDH operate, the scheme will not produce until the **FDH ALIGNED** flag is asserted, which represents the FDH delayed by the channel delay until received signal arrives. The scheme is now ready to produce a trip.

9.5.2 TWO BREAKER CONFIGURATION

The L60 has extra security when 2 CTs are brought into the relay individually and summed internally. Two currents are processed separately to derive the operating signal for each breaker, which is then used for fault detectors and the forming of positive and negative squares. This adds extra security for external faults beyond one of the breakers, with possible CT saturation at the breaker carrying the full fault current from both the local and remote source as illustrated below.

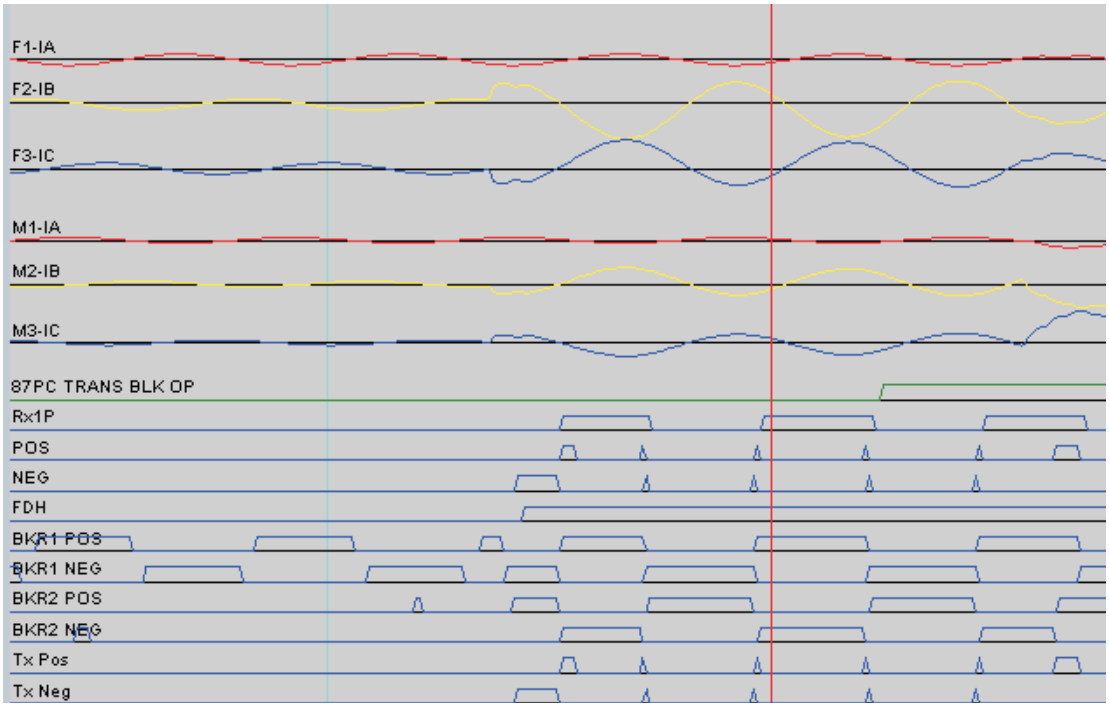

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Figure 9–10: BREAKER-AND-A-HALF SIGNAL PROCESSING

As shown in the oscillography, an external fault occurs on the breaker-and-a half diameter where the “F” CT/VT module is fed from the Breaker 1 CT and the “M” CT/VT module is fed from the Breaker 2 CT. The positive and negative halves of the waveform are opposite at two CTs. Operating in tripping mode, the L60 detects this condition and transmits only when positive samples from both CTs are present. As a result, the transmit signal is very small and does not allow remote operation. In blocking mode, this fault would result in a continuous block signal sent to the remote relay. The separate processing of currents is especially advantageous where fault currents are high and CT saturation is possible. Some times later, transient blocking will recognize an external fault and operate blocking phase comparison until the fault current disappears.

Table A–1: FLEXANALOG DATA ITEMS (Sheet 1 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
6144	SRC 1 Ia RMS	Amps	Source 1 phase A current RMS
6146	SRC 1 Ib RMS	Amps	Source 1 phase B current RMS
6148	SRC 1 Ic RMS	Amps	Source 1 phase C current RMS
6150	SRC 1 In RMS	Amps	Source 1 neutral current RMS
6152	SRC 1 Ia Mag	Amps	Source 1 phase A current magnitude
6154	SRC 1 Ia Angle	Degrees	Source 1 phase A current angle
6155	SRC 1 Ib Mag	Amps	Source 1 phase B current magnitude
6157	SRC 1 Ib Angle	Degrees	Source 1 phase B current angle
6158	SRC 1 Ic Mag	Amps	Source 1 phase C current magnitude
6160	SRC 1 Ic Angle	Degrees	Source 1 phase C current angle
6161	SRC 1 In Mag	Amps	Source 1 neutral current magnitude
6163	SRC 1 In Angle	Degrees	Source 1 neutral current angle
6164	SRC 1 Ig RMS	Amps	Source 1 ground current RMS
6166	SRC 1 Ig Mag	Degrees	Source 1 ground current magnitude
6168	SRC 1 Ig Angle	Amps	Source 1 ground current angle
6169	SRC 1 I_0 Mag	Degrees	Source 1 zero-sequence current magnitude
6171	SRC 1 I_0 Angle	Amps	Source 1 zero-sequence current angle
6172	SRC 1 I_1 Mag	Degrees	Source 1 positive-sequence current magnitude
6174	SRC 1 I_1 Angle	Amps	Source 1 positive-sequence current angle
6175	SRC 1 I_2 Mag	Degrees	Source 1 negative-sequence current magnitude
6177	SRC 1 I_2 Angle	Amps	Source 1 negative-sequence current angle
6178	SRC 1 Igd Mag	Degrees	Source 1 differential ground current magnitude
6180	SRC 1 Igd Angle	Amps	Source 1 differential ground current angle
6208	SRC 2 Ia RMS	Amps	Source 2 phase A current RMS
6210	SRC 2 Ib RMS	Amps	Source 2 phase B current RMS
6212	SRC 2 Ic RMS	Amps	Source 2 phase C current RMS
6214	SRC 2 In RMS	Amps	Source 2 neutral current RMS
6216	SRC 2 Ia Mag	Amps	Source 2 phase A current magnitude
6218	SRC 2 Ia Angle	Degrees	Source 2 phase A current angle
6219	SRC 2 Ib Mag	Amps	Source 2 phase B current magnitude
6221	SRC 2 Ib Angle	Degrees	Source 2 phase B current angle
6222	SRC 2 Ic Mag	Amps	Source 2 phase C current magnitude
6224	SRC 2 Ic Angle	Degrees	Source 2 phase C current angle
6225	SRC 2 In Mag	Amps	Source 2 neutral current magnitude
6227	SRC 2 In Angle	Degrees	Source 2 neutral current angle
6228	SRC 2 Ig RMS	Amps	Source 2 ground current RMS
6230	SRC 2 Ig Mag	Degrees	Source 2 ground current magnitude
6232	SRC 2 Ig Angle	Amps	Source 2 ground current angle
6233	SRC 2 I_0 Mag	Degrees	Source 2 zero-sequence current magnitude
6235	SRC 2 I_0 Angle	Amps	Source 2 zero-sequence current angle
6236	SRC 2 I_1 Mag	Degrees	Source 2 positive-sequence current magnitude
6238	SRC 2 I_1 Angle	Amps	Source 2 positive-sequence current angle
6239	SRC 2 I_2 Mag	Degrees	Source 2 negative-sequence current magnitude
6241	SRC 2 I_2 Angle	Amps	Source 2 negative-sequence current angle
6242	SRC 2 Igd Mag	Degrees	Source 2 differential ground current magnitude

Table A–1: FLEXANALOG DATA ITEMS (Sheet 2 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
6244	SRC 2 Igd Angle	Amps	Source 2 differential ground current angle
6272	SRC 3 Ia RMS	Amps	Source 3 phase A current RMS
6274	SRC 3 Ib RMS	Amps	Source 3 phase B current RMS
6276	SRC 3 Ic RMS	Amps	Source 3 phase C current RMS
6278	SRC 3 In RMS	Amps	Source 3 neutral current RMS
6280	SRC 3 Ia Mag	Amps	Source 3 phase A current magnitude
6282	SRC 3 Ia Angle	Degrees	Source 3 phase A current angle
6283	SRC 3 Ib Mag	Amps	Source 3 phase B current magnitude
6285	SRC 3 Ib Angle	Degrees	Source 3 phase B current angle
6286	SRC 3 Ic Mag	Amps	Source 3 phase C current magnitude
6288	SRC 3 Ic Angle	Degrees	Source 3 phase C current angle
6289	SRC 3 In Mag	Amps	Source 3 neutral current magnitude
6291	SRC 3 In Angle	Degrees	Source 3 neutral current angle
6292	SRC 3 Ig RMS	Amps	Source 3 ground current RMS
6294	SRC 3 Ig Mag	Degrees	Source 3 ground current magnitude
6296	SRC 3 Ig Angle	Amps	Source 3 ground current angle
6297	SRC 3 I_0 Mag	Degrees	Source 3 zero-sequence current magnitude
6299	SRC 3 I_0 Angle	Amps	Source 3 zero-sequence current angle
6300	SRC 3 I_1 Mag	Degrees	Source 3 positive-sequence current magnitude
6302	SRC 3 I_1 Angle	Amps	Source 3 positive-sequence current angle
6303	SRC 3 I_2 Mag	Degrees	Source 3 negative-sequence current magnitude
6305	SRC 3 I_2 Angle	Amps	Source 3 negative-sequence current angle
6306	SRC 3 Igd Mag	Degrees	Source 3 differential ground current magnitude
6308	SRC 3 Igd Angle	Amps	Source 3 differential ground current angle
6336	SRC 4 Ia RMS	Amps	Source 4 phase A current RMS
6338	SRC 4 Ib RMS	Amps	Source 4 phase B current RMS
6340	SRC 4 Ic RMS	Amps	Source 4 phase C current RMS
6342	SRC 4 In RMS	Amps	Source 4 neutral current RMS
6344	SRC 4 Ia Mag	Amps	Source 4 phase A current magnitude
6346	SRC 4 Ia Angle	Degrees	Source 4 phase A current angle
6347	SRC 4 Ib Mag	Amps	Source 4 phase B current magnitude
6349	SRC 4 Ib Angle	Degrees	Source 4 phase B current angle
6350	SRC 4 Ic Mag	Amps	Source 4 phase C current magnitude
6352	SRC 4 Ic Angle	Degrees	Source 4 phase C current angle
6353	SRC 4 In Mag	Amps	Source 4 neutral current magnitude
6355	SRC 4 In Angle	Degrees	Source 4 neutral current angle
6356	SRC 4 Ig RMS	Amps	Source 4 ground current RMS
6358	SRC 4 Ig Mag	Degrees	Source 4 ground current magnitude
6360	SRC 4 Ig Angle	Amps	Source 4 ground current angle
6361	SRC 4 I_0 Mag	Degrees	Source 4 zero-sequence current magnitude
6363	SRC 4 I_0 Angle	Amps	Source 4 zero-sequence current angle
6364	SRC 4 I_1 Mag	Degrees	Source 4 positive-sequence current magnitude
6366	SRC 4 I_1 Angle	Amps	Source 4 positive-sequence current angle
6367	SRC 4 I_2 Mag	Degrees	Source 4 negative-sequence current magnitude
6369	SRC 4 I_2 Angle	Amps	Source 4 negative-sequence current angle
6370	SRC 4 Igd Mag	Degrees	Source 4 differential ground current magnitude
6656	SRC 1 Vag RMS	Volts	Source 1 phase AG voltage RMS

Table A–1: FLEXANALOG DATA ITEMS (Sheet 3 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
6658	SRC 1 Vbg RMS	Volts	Source 1 phase BG voltage RMS
6660	SRC 1 Vcg RMS	Volts	Source 1 phase CG voltage RMS
6662	SRC 1 Vag Mag	Volts	Source 1 phase AG voltage magnitude
6664	SRC 1 Vag Angle	Degrees	Source 1 phase AG voltage angle
6665	SRC 1 Vbg Mag	Volts	Source 1 phase BG voltage magnitude
6667	SRC 1 Vbg Angle	Degrees	Source 1 phase BG voltage angle
6668	SRC 1 Vcg Mag	Volts	Source 1 phase CG voltage magnitude
6670	SRC 1 Vcg Angle	Degrees	Source 1 phase CG voltage angle
6671	SRC 1 Vab RMS	Volts	Source 1 phase AB voltage RMS
6673	SRC 1 Vbc RMS	Volts	Source 1 phase BC voltage RMS
6675	SRC 1 Vca RMS	Volts	Source 1 phase CA voltage RMS
6677	SRC 1 Vab Mag	Volts	Source 1 phase AB voltage magnitude
6679	SRC 1 Vab Angle	Degrees	Source 1 phase AB voltage angle
6680	SRC 1 Vbc Mag	Volts	Source 1 phase BC voltage magnitude
6682	SRC 1 Vbc Angle	Degrees	Source 1 phase BC voltage angle
6683	SRC 1 Vca Mag	Volts	Source 1 phase CA voltage magnitude
6685	SRC 1 Vca Angle	Degrees	Source 1 phase CA voltage angle
6686	SRC 1 Vx RMS	Volts	Source 1 auxiliary voltage RMS
6688	SRC 1 Vx Mag	Volts	Source 1 auxiliary voltage magnitude
6690	SRC 1 Vx Angle	Degrees	Source 1 auxiliary voltage angle
6691	SRC 1 V_0 Mag	Volts	Source 1 zero-sequence voltage magnitude
6693	SRC 1 V_0 Angle	Degrees	Source 1 zero-sequence voltage angle
6694	SRC 1 V_1 Mag	Volts	Source 1 positive-sequence voltage magnitude
6696	SRC 1 V_1 Angle	Degrees	Source 1 positive-sequence voltage angle
6697	SRC 1 V_2 Mag	Volts	Source 1 negative-sequence voltage magnitude
6699	SRC 1 V_2 Angle	Degrees	Source 1 negative-sequence voltage angle
6720	SRC 2 Vag RMS	Volts	Source 2 phase AG voltage RMS
6722	SRC 2 Vbg RMS	Volts	Source 2 phase BG voltage RMS
6724	SRC 2 Vcg RMS	Volts	Source 2 phase CG voltage RMS
6726	SRC 2 Vag Mag	Volts	Source 2 phase AG voltage magnitude
6728	SRC 2 Vag Angle	Degrees	Source 2 phase AG voltage angle
6729	SRC 2 Vbg Mag	Volts	Source 2 phase BG voltage magnitude
6731	SRC 2 Vbg Angle	Degrees	Source 2 phase BG voltage angle
6732	SRC 2 Vcg Mag	Volts	Source 2 phase CG voltage magnitude
6734	SRC 2 Vcg Angle	Degrees	Source 2 phase CG voltage angle
6735	SRC 2 Vab RMS	Volts	Source 2 phase AB voltage RMS
6737	SRC 2 Vbc RMS	Volts	Source 2 phase BC voltage RMS
6739	SRC 2 Vca RMS	Volts	Source 2 phase CA voltage RMS
6741	SRC 2 Vab Mag	Volts	Source 2 phase AB voltage magnitude
6743	SRC 2 Vab Angle	Degrees	Source 2 phase AB voltage angle
6744	SRC 2 Vbc Mag	Volts	Source 2 phase BC voltage magnitude
6746	SRC 2 Vbc Angle	Degrees	Source 2 phase BC voltage angle
6747	SRC 2 Vca Mag	Volts	Source 2 phase CA voltage magnitude
6749	SRC 2 Vca Angle	Degrees	Source 2 phase CA voltage angle
6750	SRC 2 Vx RMS	Volts	Source 2 auxiliary voltage RMS
6752	SRC 2 Vx Mag	Volts	Source 2 auxiliary voltage magnitude
6754	SRC 2 Vx Angle	Degrees	Source 2 auxiliary voltage angle

Table A–1: FLEXANALOG DATA ITEMS (Sheet 4 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
6755	SRC 2 V_0 Mag	Volts	Source 2 zero-sequence voltage magnitude
6757	SRC 2 V_0 Angle	Degrees	Source 2 zero-sequence voltage angle
6758	SRC 2 V_1 Mag	Volts	Source 2 positive-sequence voltage magnitude
6760	SRC 2 V_1 Angle	Degrees	Source 2 positive-sequence voltage angle
6761	SRC 2 V_2 Mag	Volts	Source 2 negative-sequence voltage magnitude
6763	SRC 2 V_2 Angle	Degrees	Source 2 negative-sequence voltage angle
6784	SRC 3 Vag RMS	Volts	Source 3 phase AG voltage RMS
6786	SRC 3 Vbg RMS	Volts	Source 3 phase BG voltage RMS
6788	SRC 3 Vcg RMS	Volts	Source 3 phase CG voltage RMS
6790	SRC 3 Vag Mag	Volts	Source 3 phase AG voltage magnitude
6792	SRC 3 Vag Angle	Degrees	Source 3 phase AG voltage angle
6793	SRC 3 Vbg Mag	Volts	Source 3 phase BG voltage magnitude
6795	SRC 3 Vbg Angle	Degrees	Source 3 phase BG voltage angle
6796	SRC 3 Vcg Mag	Volts	Source 3 phase CG voltage magnitude
6798	SRC 3 Vcg Angle	Degrees	Source 3 phase CG voltage angle
6799	SRC 3 Vab RMS	Volts	Source 3 phase AB voltage RMS
6801	SRC 3 Vbc RMS	Volts	Source 3 phase BC voltage RMS
6803	SRC 3 Vca RMS	Volts	Source 3 phase CA voltage RMS
6805	SRC 3 Vab Mag	Volts	Source 3 phase AB voltage magnitude
6807	SRC 3 Vab Angle	Degrees	Source 3 phase AB voltage angle
6808	SRC 3 Vbc Mag	Volts	Source 3 phase BC voltage magnitude
6810	SRC 3 Vbc Angle	Degrees	Source 3 phase BC voltage angle
6811	SRC 3 Vca Mag	Volts	Source 3 phase CA voltage magnitude
6813	SRC 3 Vca Angle	Degrees	Source 3 phase CA voltage angle
6814	SRC 3 Vx RMS	Volts	Source 3 auxiliary voltage RMS
6816	SRC 3 Vx Mag	Volts	Source 3 auxiliary voltage magnitude
6818	SRC 3 Vx Angle	Degrees	Source 3 auxiliary voltage angle
6819	SRC 3 V_0 Mag	Volts	Source 3 zero-sequence voltage magnitude
6821	SRC 3 V_0 Angle	Degrees	Source 3 zero-sequence voltage angle
6822	SRC 3 V_1 Mag	Volts	Source 3 positive-sequence voltage magnitude
6824	SRC 3 V_1 Angle	Degrees	Source 3 positive-sequence voltage angle
6825	SRC 3 V_2 Mag	Volts	Source 3 negative-sequence voltage magnitude
6827	SRC 3 V_2 Angle	Degrees	Source 3 negative-sequence voltage angle
6848	SRC 4 Vag RMS	Volts	Source 4 phase AG voltage RMS
6850	SRC 4 Vbg RMS	Volts	Source 4 phase BG voltage RMS
6852	SRC 4 Vcg RMS	Volts	Source 4 phase CG voltage RMS
6854	SRC 4 Vag Mag	Volts	Source 4 phase AG voltage magnitude
6856	SRC 4 Vag Angle	Degrees	Source 4 phase AG voltage angle
6857	SRC 4 Vbg Mag	Volts	Source 4 phase BG voltage magnitude
6859	SRC 4 Vbg Angle	Degrees	Source 4 phase BG voltage angle
6860	SRC 4 Vcg Mag	Volts	Source 4 phase CG voltage magnitude
6862	SRC 4 Vcg Angle	Degrees	Source 4 phase CG voltage angle
6863	SRC 4 Vab RMS	Volts	Source 4 phase AB voltage RMS
6865	SRC 4 Vbc RMS	Volts	Source 4 phase BC voltage RMS
6867	SRC 4 Vca RMS	Volts	Source 4 phase CA voltage RMS
6869	SRC 4 Vab Mag	Volts	Source 4 phase AB voltage magnitude
6871	SRC 4 Vab Angle	Degrees	Source 4 phase AB voltage angle

Table A–1: FLEXANALOG DATA ITEMS (Sheet 5 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
6872	SRC 4 Vbc Mag	Volts	Source 4 phase BC voltage magnitude
6874	SRC 4 Vbc Angle	Degrees	Source 4 phase BC voltage angle
6875	SRC 4 Vca Mag	Volts	Source 4 phase CA voltage magnitude
6877	SRC 4 Vca Angle	Degrees	Source 4 phase CA voltage angle
6878	SRC 4 Vx RMS	Volts	Source 4 auxiliary voltage RMS
6880	SRC 4 Vx Mag	Volts	Source 4 auxiliary voltage magnitude
6882	SRC 4 Vx Angle	Degrees	Source 4 auxiliary voltage angle
6883	SRC 4 V_0 Mag	Volts	Source 4 zero-sequence voltage magnitude
6885	SRC 4 V_0 Angle	Degrees	Source 4 zero-sequence voltage angle
6886	SRC 4 V_1 Mag	Volts	Source 4 positive-sequence voltage magnitude
6888	SRC 4 V_1 Angle	Degrees	Source 4 positive-sequence voltage angle
6889	SRC 4 V_2 Mag	Volts	Source 4 negative-sequence voltage magnitude
6891	SRC 4 V_2 Angle	Degrees	Source 4 negative-sequence voltage angle
7168	SRC 1 P	Watts	Source 1 three-phase real power
7170	SRC 1 Pa	Watts	Source 1 phase A real power
7172	SRC 1 Pb	Watts	Source 1 phase B real power
7174	SRC 1 Pc	Watts	Source 1 phase C real power
7176	SRC 1 Q	Vars	Source 1 three-phase reactive power
7178	SRC 1 Qa	Vars	Source 1 phase A reactive power
7180	SRC 1 Qb	Vars	Source 1 phase B reactive power
7182	SRC 1 Qc	Vars	Source 1 phase C reactive power
7184	SRC 1 S	VA	Source 1 three-phase apparent power
7186	SRC 1 Sa	VA	Source 1 phase A apparent power
7188	SRC 1 Sb	VA	Source 1 phase B apparent power
7190	SRC 1 Sc	VA	Source 1 phase C apparent power
7192	SRC 1 PF	---	Source 1 three-phase power factor
7193	SRC 1 Phase A PF	---	Source 1 phase A power factor
7194	SRC 1 Phase B PF	---	Source 1 phase B power factor
7195	SRC 1 Phase C PF	---	Source 1 phase C power factor
7200	SRC 2 P	Watts	Source 2 three-phase real power
7202	SRC 2 Pa	Watts	Source 2 phase A real power
7204	SRC 2 Pb	Watts	Source 2 phase B real power
7206	SRC 2 Pc	Watts	Source 2 phase C real power
7208	SRC 2 Q	Vars	Source 2 three-phase reactive power
7210	SRC 2 Qa	Vars	Source 2 phase A reactive power
7212	SRC 2 Qb	Vars	Source 2 phase B reactive power
7214	SRC 2 Qc	Vars	Source 2 phase C reactive power
7216	SRC 2 S	VA	Source 2 three-phase apparent power
7218	SRC 2 Sa	VA	Source 2 phase A apparent power
7220	SRC 2 Sb	VA	Source 2 phase B apparent power
7222	SRC 2 Sc	VA	Source 2 phase C apparent power
7224	SRC 2 PF	---	Source 2 three-phase power factor
7225	SRC 2 Phase A PF	---	Source 2 phase A power factor
7226	SRC 2 Phase B PF	---	Source 2 phase B power factor
7227	SRC 2 Phase C PF	---	Source 2 phase C power factor
7232	SRC 3 P	Watts	Source 3 three-phase real power
7234	SRC 3 Pa	Watts	Source 3 phase A real power

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Table A–1: FLEXANALOG DATA ITEMS (Sheet 6 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
7236	SRC 3 Pb	Watts	Source 3 phase B real power
7238	SRC 3 Pc	Watts	Source 3 phase C real power
7240	SRC 3 Q	Vars	Source 3 three-phase reactive power
7242	SRC 3 Qa	Vars	Source 3 phase A reactive power
7244	SRC 3 Qb	Vars	Source 3 phase B reactive power
7246	SRC 3 Qc	Vars	Source 3 phase C reactive power
7248	SRC 3 S	VA	Source 3 three-phase apparent power
7250	SRC 3 Sa	VA	Source 3 phase A apparent power
7252	SRC 3 Sb	VA	Source 3 phase B apparent power
7254	SRC 3 Sc	VA	Source 3 phase C apparent power
7256	SRC 3 PF	---	Source 3 three-phase power factor
7257	SRC 3 Phase A PF	---	Source 3 phase A power factor
7258	SRC 3 Phase B PF	---	Source 3 phase B power factor
7259	SRC 3 Phase C PF	---	Source 3 phase C power factor
7264	SRC 4 P	Watts	Source 4 three-phase real power
7266	SRC 4 Pa	Watts	Source 4 phase A real power
7268	SRC 4 Pb	Watts	Source 4 phase B real power
7270	SRC 4 Pc	Watts	Source 4 phase C real power
7272	SRC 4 Q	Vars	Source 4 three-phase reactive power
7274	SRC 4 Qa	Vars	Source 4 phase A reactive power
7276	SRC 4 Qb	Vars	Source 4 phase B reactive power
7278	SRC 4 Qc	Vars	Source 4 phase C reactive power
7280	SRC 4 S	VA	Source 4 three-phase apparent power
7282	SRC 4 Sa	VA	Source 4 phase A apparent power
7284	SRC 4 Sb	VA	Source 4 phase B apparent power
7286	SRC 4 Sc	VA	Source 4 phase C apparent power
7288	SRC 4 PF	---	Source 4 three-phase power factor
7289	SRC 4 Phase A PF	---	Source 4 phase A power factor
7290	SRC 4 Phase B PF	---	Source 4 phase B power factor
7291	SRC 4 Phase C PF	---	Source 4 phase C power factor
7552	SRC 1 Frequency	Hz	Source 1 frequency
7553	SRC 2 Frequency	Hz	Source 2 frequency
7554	SRC 3 Frequency	Hz	Source 3 frequency
7555	SRC 4 Frequency	Hz	Source 4 frequency
8864	SRC 1 Phase A THD	---	Source 1 phase A total harmonic distortion (THD)
8865	SRC 1 Phase B THD	---	Source 1 phase B total harmonic distortion (THD)
8866	SRC 1 Phase C THD	---	Source 1 phase C total harmonic distortion (THD)
8867	SRC 1 Neutral THD	---	Source 1 neutral total harmonic distortion (THD)
8868	SRC 1 Phase A THD	---	Source 2 phase A total harmonic distortion (THD)
8869	SRC 1 Phase B THD	---	Source 2 phase B total harmonic distortion (THD)
8870	SRC 1 Phase C THD	---	Source 2 phase C total harmonic distortion (THD)
8871	SRC 1 Neutral THD	---	Source 2 neutral total harmonic distortion (THD)
8872	SRC 1 Phase A THD	---	Source 3 phase A total harmonic distortion (THD)
8873	SRC 1 Phase B THD	---	Source 3 phase B total harmonic distortion (THD)
8874	SRC 1 Phase C THD	---	Source 3 phase C total harmonic distortion (THD)
8875	SRC 1 Neutral THD	---	Source 3 neutral total harmonic distortion (THD)
8876	SRC 1 Phase A THD	---	Source 4 phase A total harmonic distortion (THD)

Table A–1: FLEXANALOG DATA ITEMS (Sheet 7 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
8877	SRC 1 Phase B THD	---	Source 4 phase B total harmonic distortion (THD)
8878	SRC 1 Phase C THD	---	Source 4 phase C total harmonic distortion (THD)
8879	SRC 1 Neutral THD	---	Source 4 neutral total harmonic distortion (THD)
9216	Synchchk 1 Delta V	Volts	Synchrocheck 1 delta voltage
9218	Synchchk 1 Delta F	Hz	Synchrocheck 1 delta frequency
9219	Synchchk 1 Delta Phs	Degrees	Synchrocheck 1 delta phase
9220	Synchchk 2 Delta V	Volts	Synchrocheck 2 delta voltage
9222	Synchchk 2 Delta F	Hz	Synchrocheck 2 delta frequency
9223	Synchchk 2 Delta Phs	Degrees	Synchrocheck 2 delta phase
13504	DCMA Inputs 1 Value	mA	dcmA input 1 actual value
13506	DCMA Inputs 2 Value	mA	dcmA input 2 actual value
13508	DCMA Inputs 3 Value	mA	dcmA input 3 actual value
13510	DCMA Inputs 4 Value	mA	dcmA input 4 actual value
13512	DCMA Inputs 5 Value	mA	dcmA input 5 actual value
13514	DCMA Inputs 6 Value	mA	dcmA input 6 actual value
13516	DCMA Inputs 7 Value	mA	dcmA input 7 actual value
13518	DCMA Inputs 8 Value	mA	dcmA input 8 actual value
13520	DCMA Inputs 9 Value	mA	dcmA input 9 actual value
13522	DCMA Inputs 10 Value	mA	dcmA input 10 actual value
13524	DCMA Inputs 11 Value	mA	dcmA input 11 actual value
13526	DCMA Inputs 12 Value	mA	dcmA input 12 actual value
13528	DCMA Inputs 13 Value	mA	dcmA input 13 actual value
13530	DCMA Inputs 14 Value	mA	dcmA input 14 actual value
13532	DCMA Inputs 15 Value	mA	dcmA input 15 actual value
13534	DCMA Inputs 16 Value	mA	dcmA input 16 actual value
13536	DCMA Inputs 17 Value	mA	dcmA input 17 actual value
13538	DCMA Inputs 18 Value	mA	dcmA input 18 actual value
13540	DCMA Inputs 19 Value	mA	dcmA input 19 actual value
13542	DCMA Inputs 20 Value	mA	dcmA input 20 actual value
13544	DCMA Inputs 21 Value	mA	dcmA input 21 actual value
13546	DCMA Inputs 22 Value	mA	dcmA input 22 actual value
13548	DCMA Inputs 23 Value	mA	dcmA input 23 actual value
13550	DCMA Inputs 24 Value	mA	dcmA input 24 actual value
13552	RTD Inputs 1 Value	---	RTD input 1 actual value
13553	RTD Inputs 2 Value	---	RTD input 2 actual value
13554	RTD Inputs 3 Value	---	RTD input 3 actual value
13555	RTD Inputs 4 Value	---	RTD input 4 actual value
13556	RTD Inputs 5 Value	---	RTD input 5 actual value
13557	RTD Inputs 6 Value	---	RTD input 6 actual value
13558	RTD Inputs 7 Value	---	RTD input 7 actual value
13559	RTD Inputs 8 Value	---	RTD input 8 actual value
13560	RTD Inputs 9 Value	---	RTD input 9 actual value
13561	RTD Inputs 10 Value	---	RTD input 10 actual value
13562	RTD Inputs 11 Value	---	RTD input 11 actual value
13563	RTD Inputs 12 Value	---	RTD input 12 actual value
13564	RTD Inputs 13 Value	---	RTD input 13 actual value
13565	RTD Inputs 14 Value	---	RTD input 14 actual value

Table A–1: FLEXANALOG DATA ITEMS (Sheet 8 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
13566	RTD Inputs 15 Value	---	RTD input 15 actual value
13567	RTD Inputs 16 Value	---	RTD input 16 actual value
13568	RTD Inputs 17 Value	---	RTD input 17 actual value
13569	RTD Inputs 18 Value	---	RTD input 18 actual value
13570	RTD Inputs 19 Value	---	RTD input 19 actual value
13571	RTD Inputs 20 Value	---	RTD input 20 actual value
13572	RTD Inputs 21 Value	---	RTD input 21 actual value
13573	RTD Inputs 22 Value	---	RTD input 22 actual value
13574	RTD Inputs 23 Value	---	RTD input 23 actual value
13575	RTD Inputs 24 Value	---	RTD input 24 actual value
13576	RTD Inputs 25 Value	---	RTD input 25 actual value
13577	RTD Inputs 26 Value	---	RTD input 26 actual value
13578	RTD Inputs 27 Value	---	RTD input 27 actual value
13579	RTD Inputs 28 Value	---	RTD input 28 actual value
13580	RTD Inputs 29 Value	---	RTD input 29 actual value
13581	RTD Inputs 30 Value	---	RTD input 30 actual value
13582	RTD Inputs 31 Value	---	RTD input 31 actual value
13583	RTD Inputs 32 Value	---	RTD input 32 actual value
13584	RTD Inputs 33 Value	---	RTD input 33 actual value
13585	RTD Inputs 34 Value	---	RTD input 34 actual value
13586	RTD Inputs 35 Value	---	RTD input 35 actual value
13587	RTD Inputs 36 Value	---	RTD input 36 actual value
13588	RTD Inputs 37 Value	---	RTD input 37 actual value
13589	RTD Inputs 38 Value	---	RTD input 38 actual value
13590	RTD Inputs 39 Value	---	RTD input 39 actual value
13591	RTD Inputs 40 Value	---	RTD input 40 actual value
13592	RTD Inputs 41 Value	---	RTD input 41 actual value
13593	RTD Inputs 42 Value	---	RTD input 42 actual value
13594	RTD Inputs 43 Value	---	RTD input 43 actual value
13595	RTD Inputs 44 Value	---	RTD input 44 actual value
13596	RTD Inputs 45 Value	---	RTD input 45 actual value
13597	RTD Inputs 46 Value	---	RTD input 46 actual value
13598	RTD Inputs 47 Value	---	RTD input 47 actual value
13599	RTD Inputs 48 Value	---	RTD input 48 actual value
24459	Active Setting Group	---	Current setting group
32768	Tracking Frequency	Hz	Tracking frequency
39425	FlexElement 1 Value	---	FlexElement™ 1 actual value
39427	FlexElement 2 Value	---	FlexElement™ 2 actual value
39429	FlexElement 3 Value	---	FlexElement™ 3 actual value
39431	FlexElement 4 Value	---	FlexElement™ 4 actual value
39433	FlexElement 5 Value	---	FlexElement™ 5 actual value
39435	FlexElement 6 Value	---	FlexElement™ 6 actual value
39437	FlexElement 7 Value	---	FlexElement™ 7 actual value
39439	FlexElement 8 Value	---	FlexElement™ 8 actual value
45584	GOOSE Analog In 1	---	IEC 61850 GOOSE analog input 1
45586	GOOSE Analog In 2	---	IEC 61850 GOOSE analog input 2
45588	GOOSE Analog In 3	---	IEC 61850 GOOSE analog input 3

Table A–1: FLEXANALOG DATA ITEMS (Sheet 9 of 9)

ADDRESS	FLEXANALOG NAME	UNITS	DESCRIPTION
45590	GOOSE Analog In 4	---	IEC 61850 GOOSE analog input 4
45592	GOOSE Analog In 5	---	IEC 61850 GOOSE analog input 5
45594	GOOSE Analog In 6	---	IEC 61850 GOOSE analog input 6
45596	GOOSE Analog In 7	---	IEC 61850 GOOSE analog input 7
45598	GOOSE Analog In 8	---	IEC 61850 GOOSE analog input 8
45600	GOOSE Analog In 9	---	IEC 61850 GOOSE analog input 9
45602	GOOSE Analog In 10	---	IEC 61850 GOOSE analog input 10
45604	GOOSE Analog In 11	---	IEC 61850 GOOSE analog input 11
45606	GOOSE Analog In 12	---	IEC 61850 GOOSE analog input 12
45608	GOOSE Analog In 13	---	IEC 61850 GOOSE analog input 13
45610	GOOSE Analog In 14	---	IEC 61850 GOOSE analog input 14
45612	GOOSE Analog In 15	---	IEC 61850 GOOSE analog input 15
45614	GOOSE Analog In 16	---	IEC 61850 GOOSE analog input 16

A

B.1.1 INTRODUCTION

The UR-series relays support a number of communications protocols to allow connection to equipment such as personal computers, RTUs, SCADA masters, and programmable logic controllers. The Modicon Modbus RTU protocol is the most basic protocol supported by the UR. Modbus is available via RS232 or RS485 serial links or via ethernet (using the Modbus/TCP specification). The following description is intended primarily for users who wish to develop their own master communication drivers and applies to the serial Modbus RTU protocol. Note that:

- The UR always acts as a slave device, meaning that it never initiates communications; it only listens and responds to requests issued by a master computer.
- For Modbus®, a subset of the Remote Terminal Unit (RTU) protocol format is supported that allows extensive monitoring, programming, and control functions using read and write register commands.

B.1.2 PHYSICAL LAYER

The Modbus® RTU protocol is hardware-independent so that the physical layer can be any of a variety of standard hardware configurations including RS232 and RS485. The relay includes a faceplate (front panel) RS232 port and two rear terminal communications ports that may be configured as RS485, fiber optic, 10Base-T, or 10Base-F. Data flow is half-duplex in all configurations. See chapter 3 for details on communications wiring.

Each data byte is transmitted in an asynchronous format consisting of 1 start bit, 8 data bits, 1 stop bit, and possibly 1 parity bit. This produces a 10 or 11 bit data frame. This can be important for transmission through modems at high bit rates (11 bit data frames are not supported by many modems at baud rates greater than 300).

The baud rate and parity are independently programmable for each communications port. Baud rates of 300, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 57600, or 115200 bps are available. Even, odd, and no parity are available. Refer to the *Communications* section of chapter 5 for further details.

The master device in any system must know the address of the slave device with which it is to communicate. The relay will not act on a request from a master if the address in the request does not match the relay's slave address (unless the address is the broadcast address – see below).

A single setting selects the slave address used for all ports, with the exception that for the faceplate port, the relay will accept any address when the Modbus® RTU protocol is used.

B.1.3 DATA LINK LAYER

Communications takes place in packets which are groups of asynchronously framed byte data. The master transmits a packet to the slave and the slave responds with a packet. The end of a packet is marked by *dead-time* on the communications line. The following describes general format for both transmit and receive packets. For exact details on packet formatting, refer to subsequent sections describing each function code.

Table B–1: MODBUS PACKET FORMAT

DESCRIPTION	SIZE
SLAVE ADDRESS	1 byte
FUNCTION CODE	1 byte
DATA	*N* bytes
CRC	2 bytes
DEAD TIME	3.5 bytes transmission time

- **SLAVE ADDRESS:** This is the address of the slave device that is intended to receive the packet sent by the master and to perform the desired action. Each slave device on a communications bus must have a unique address to prevent bus contention. All of the relay's ports have the same address which is programmable from 1 to 254; see chapter 5 for details. Only the addressed slave will respond to a packet that starts with its address. Note that the faceplate port is an exception to this rule; it will act on a message containing any slave address.

  A master transmit packet with slave address 0 indicates a broadcast command. All slaves on the communication link take action based on the packet, but none respond to the master. Broadcast mode is only recognized when associated with function code 05h. For any other function code, a packet with broadcast mode slave address 0 will be ignored.

- **FUNCTION CODE:** This is one of the supported functions codes of the unit which tells the slave what action to perform. See the *Supported Function Codes* section for complete details. An exception response from the slave is indicated by setting the high order bit of the function code in the response packet. See the *Exception Responses* section for further details.
- **DATA:** This will be a variable number of bytes depending on the function code. This may include actual values, settings, or addresses sent by the master to the slave or by the slave to the master.
- **CRC:** This is a two byte error checking code. The RTU version of Modbus® includes a 16-bit cyclic redundancy check (CRC-16) with every packet which is an industry standard method used for error detection. If a Modbus slave device receives a packet in which an error is indicated by the CRC, the slave device will not act upon or respond to the packet thus preventing any erroneous operations. See the *CRC-16 Algorithm* section for details on calculating the CRC.
- **DEAD TIME:** A packet is terminated when no data is received for a period of 3.5 byte transmission times (about 15 ms at 2400 bps, 2 ms at 19200 bps, and 300 µs at 115200 bps). Consequently, the transmitting device must not allow gaps between bytes longer than this interval. Once the dead time has expired without a new byte transmission, all slaves start listening for a new packet from the master except for the addressed slave.

B.1.4 CRC-16 ALGORITHM

The CRC-16 algorithm essentially treats the entire data stream (data bits only; start, stop and parity ignored) as one continuous binary number. This number is first shifted left 16 bits and then divided by a characteristic polynomial (1100000000000101B). The 16 bit remainder of the division is appended to the end of the packet, MSByte first. The resulting packet including CRC, when divided by the same polynomial at the receiver will give a zero remainder if no transmission errors have occurred. This algorithm requires the characteristic polynomial to be reverse bit ordered. The most significant bit of the characteristic polynomial is dropped, since it does not affect the value of the remainder.

A C programming language implementation of the CRC algorithm will be provided upon request.

Table B–2: CRC-16 ALGORITHM

SYMBOLS:	-->	data transfer
	A	16 bit working register
	Alow	low order byte of A
	Ahigh	high order byte of A
	CRC	16 bit CRC-16 result
	i,j	loop counters
	(+)	logical EXCLUSIVE-OR operator
	N	total number of data bytes
	Di	i-th data byte (i = 0 to N-1)
	G	16 bit characteristic polynomial = 1010000000000001 (binary) with MSbit dropped and bit order reversed
	shr (x)	right shift operator (th LSbit of x is shifted into a carry flag, a '0' is shifted into the MSbit of x, all other bits are shifted right one location)

ALGORITHM:	1.	FFFF (hex) --> A	
	2.	0 --> i	
	3.	0 --> j	
	4.	Di (+) Alow --> Alow	
	5.	j + 1 --> j	
	6.	shr (A)	
	7.	Is there a carry?	No: go to 8; Yes: G (+) A --> A and continue.
	8.	Is j = 8?	No: go to 5; Yes: continue
	9.	i + 1 --> i	
	10.	Is i = N?	No: go to 3; Yes: continue
	11.	A --> CRC	

B.2.1 SUPPORTED FUNCTION CODES

Modbus® officially defines function codes from 1 to 127 though only a small subset is generally needed. The relay supports some of these functions, as summarized in the following table. Subsequent sections describe each function code in detail.

FUNCTION CODE		MODBUS DEFINITION	GE MULTILIN DEFINITION
HEX	DEC		
03	3	Read holding registers	Read actual values or settings
04	4	Read holding registers	Read actual values or settings
05	5	Force single coil	Execute operation
06	6	Preset single register	Store single setting
10	16	Preset multiple registers	Store multiple settings

B.2.2 READ ACTUAL VALUES OR SETTINGS (FUNCTION CODE 03/04H)

This function code allows the master to read one or more consecutive data registers (actual values or settings) from a relay. Data registers are always 16-bit (two-byte) values transmitted with high order byte first. The maximum number of registers that can be read in a single packet is 125. See the *Modbus Memory Map* table for exact details on the data registers.

Since some PLC implementations of Modbus® only support one of function codes 03h and 04h, the relay interpretation allows either function code to be used for reading one or more consecutive data registers. The data starting address will determine the type of data being read. Function codes 03h and 04h are therefore identical.

The following table shows the format of the master and slave packets. The example shows a master device requesting three register values starting at address 4050h from slave device 11h (17 decimal); the slave device responds with the values 40, 300, and 0 from registers 4050h, 4051h, and 4052h, respectively.

Table B–3: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION	
PACKET FORMAT	EXAMPLE (HEX)
SLAVE ADDRESS	11
FUNCTION CODE	04
DATA STARTING ADDRESS - high	40
DATA STARTING ADDRESS - low	50
NUMBER OF REGISTERS - high	00
NUMBER OF REGISTERS - low	03
CRC - low	A7
CRC - high	4A

SLAVE RESPONSE	
PACKET FORMAT	EXAMPLE (HEX)
SLAVE ADDRESS	11
FUNCTION CODE	04
BYTE COUNT	06
DATA #1 - high	00
DATA #1 - low	28
DATA #2 - high	01
DATA #2 - low	2C
DATA #3 - high	00
DATA #3 - low	00
CRC - low	0D
CRC - high	60

B.2.3 EXECUTE OPERATION (FUNCTION CODE 05H)

This function code allows the master to perform various operations in the relay. Available operations are shown in the *Summary of Operation Codes* table below.

The following table shows the format of the master and slave packets. The example shows a master device requesting the slave device 11h (17 decimal) to perform a reset. The high and low code value bytes always have the values "FF" and "00" respectively and are a remnant of the original Modbus® definition of this function code.

Table B–4: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	05
OPERATION CODE - high	00
OPERATION CODE - low	01
CODE VALUE - high	FF
CODE VALUE - low	00
CRC - low	DF
CRC - high	6A

SLAVE RESPONSE	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	05
OPERATION CODE - high	00
OPERATION CODE - low	01
CODE VALUE - high	FF
CODE VALUE - low	00
CRC - low	DF
CRC - high	6A

Table B–5: SUMMARY OF OPERATION CODES FOR FUNCTION 05H

OPERATION CODE (HEX)	DEFINITION	DESCRIPTION
0000	NO OPERATION	Does not do anything.
0001	RESET	Performs the same function as the faceplate RESET key.
0005	CLEAR EVENT RECORDS	Performs the same function as the faceplate **CLEAR EVENT RECORDS** menu command.
0006	CLEAR OSCILLOGRAPHY	Clears all oscillography records.
1000 to 103F	VIRTUAL IN 1 to 64 ON/OFF	Sets the states of Virtual Inputs 1 to 64 either "ON" or "OFF".

B.2.4 STORE SINGLE SETTING (FUNCTION CODE 06H)

This function code allows the master to modify the contents of a single setting register in an relay. Setting registers are always 16 bit (two byte) values transmitted high order byte first. The following table shows the format of the master and slave packets. The example shows a master device storing the value 200 at memory map address 4051h to slave device 11h (17 dec).

Table B–6: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	06
DATA STARTING ADDRESS - high	40
DATA STARTING ADDRESS - low	51
DATA - high	00
DATA - low	C8
CRC - low	CE
CRC - high	DD

SLAVE RESPONSE	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	06
DATA STARTING ADDRESS - high	40
DATA STARTING ADDRESS - low	51
DATA - high	00
DATA - low	C8
CRC - low	CE
CRC - high	DD

B.2.5 STORE MULTIPLE SETTINGS (FUNCTION CODE 10H)

This function code allows the master to modify the contents of a one or more consecutive setting registers in a relay. Setting registers are 16-bit (two byte) values transmitted high order byte first. The maximum number of setting registers that can be stored in a single packet is 60. The following table shows the format of the master and slave packets. The example shows a master device storing the value 200 at memory map address 4051h, and the value 1 at memory map address 4052h to slave device 11h (17 decimal).

Table B–7: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	10
DATA STARTING ADDRESS - hi	40
DATA STARTING ADDRESS - lo	51
NUMBER OF SETTINGS - hi	00
NUMBER OF SETTINGS - lo	02
BYTE COUNT	04
DATA #1 - high order byte	00
DATA #1 - low order byte	C8
DATA #2 - high order byte	00
DATA #2 - low order byte	01
CRC - low order byte	12
CRC - high order byte	62

SLAVE RESPONSE	
PACKET FORMAT	**EXMAPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	10
DATA STARTING ADDRESS - hi	40
DATA STARTING ADDRESS - lo	51
NUMBER OF SETTINGS - hi	00
NUMBER OF SETTINGS - lo	02
CRC - lo	07
CRC - hi	64

B.2.6 EXCEPTION RESPONSES

Programming or operation errors usually happen because of illegal data in a packet. These errors result in an exception response from the slave. The slave detecting one of these errors sends a response packet to the master with the high order bit of the function code set to 1.

The following table shows the format of the master and slave packets. The example shows a master device sending the unsupported function code 39h to slave device 11.

Table B–8: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	39
CRC - low order byte	CD
CRC - high order byte	F2

SLAVE RESPONSE	
PACKET FORMAT	**EXAMPLE (HEX)**
SLAVE ADDRESS	11
FUNCTION CODE	B9
ERROR CODE	01
CRC - low order byte	93
CRC - high order byte	95

B.3.1 OBTAINING RELAY FILES VIA MODBUS

a) DESCRIPTION

The UR relay has a generic file transfer facility, meaning that you use the same method to obtain all of the different types of files from the unit. The Modbus registers that implement file transfer are found in the "Modbus File Transfer (Read/Write)" and "Modbus File Transfer (Read Only)" modules, starting at address 3100 in the Modbus Memory Map. To read a file from the UR relay, use the following steps:

1. Write the filename to the "Name of file to read" register using a write multiple registers command. If the name is shorter than 80 characters, you may write only enough registers to include all the text of the filename. Filenames are not case sensitive.
2. Repeatedly read all the registers in "Modbus File Transfer (Read Only)" using a read multiple registers command. It is not necessary to read the entire data block, since the UR relay will remember which was the last register you read. The "position" register is initially zero and thereafter indicates how many bytes (2 times the number of registers) you have read so far. The "size of..." register indicates the number of bytes of data remaining to read, to a maximum of 244.
3. Keep reading until the "size of..." register is smaller than the number of bytes you are transferring. This condition indicates end of file. Discard any bytes you have read beyond the indicated block size.
4. If you need to re-try a block, read only the "size of.." and "block of data", without reading the position. The file pointer is only incremented when you read the position register, so the same data block will be returned as was read in the previous operation. On the next read, check to see if the position is where you expect it to be, and discard the previous block if it is not (this condition would indicate that the UR relay did not process your original read request).

The UR relay retains connection-specific file transfer information, so files may be read simultaneously on multiple Modbus connections.

b) OTHER PROTOCOLS

All the files available via Modbus may also be retrieved using the standard file transfer mechanisms in other protocols (for example, TFTP or MMS).

c) COMTRADE, OSCILLOGRAPHY, AND DATA LOGGER FILES

Oscillography and data logger files are formatted using the COMTRADE file format per IEEE PC37.111 Draft 7c (02 September 1997). The files may be obtained in either text or binary COMTRADE format.

d) READING OSCILLOGRAPHY FILES

Familiarity with the oscillography feature is required to understand the following description. Refer to the Oscillography section in Chapter 5 for additional details.

The Oscillography Number of Triggers register is incremented by one every time a new oscillography file is triggered (captured) and cleared to zero when oscillography data is cleared. When a new trigger occurs, the associated oscillography file is assigned a file identifier number equal to the incremented value of this register; the newest file number is equal to the Oscillography_Number_of_Triggers register. This register can be used to determine if any new data has been captured by periodically reading it to see if the value has changed; if the number has increased then new data is available.

The Oscillography Number of Records register specifies the maximum number of files (and the number of cycles of data per file) that can be stored in memory of the relay. The Oscillography Available Records register specifies the actual number of files that are stored and still available to be read out of the relay.

Writing “Yes” (i.e. the value 1) to the Oscillography Clear Data register clears oscillography data files, clears both the Oscillography Number of Triggers and Oscillography Available Records registers to zero, and sets the Oscillography Last Cleared Date to the present date and time.

To read binary COMTRADE oscillography files, read the following filenames:

`OSCnnnn.CFG` and `OSCnnn.DAT`

Replace “nnn” with the desired oscillography trigger number. For ASCII format, use the following file names

`OSCAnnnn.CFG` and `OSCAnnn.DAT`

e) READING DATA LOGGER FILES

Familiarity with the data logger feature is required to understand this description. Refer to the Data Logger section of Chapter 5 for details. To read the entire data logger in binary COMTRADE format, read the following files.

`datalog.cfg` and `datalog.dat`

To read the entire data logger in ASCII COMTRADE format, read the following files.

`dataloga.cfg` and `dataloga.dat`

To limit the range of records to be returned in the COMTRADE files, append the following to the filename before writing it:

- To read from a specific time to the end of the log: <space> startTime
- To read a specific range of records: <space> startTime <space> endTime
- Replace <startTime> and <endTime> with Julian dates (seconds since Jan. 1 1970) as numeric text.

f) READING EVENT RECORDER FILES

To read the entire event recorder contents in ASCII format (the only available format), use the following filename:

`EVT.TXT`

To read from a specific record to the end of the log, use the following filename:

`EVTnnn.TXT` (replace `nnn` with the desired starting record number)

To read from a specific record to another specific record, use the following filename:

`EVT.TXT xxxxx yyyyy` (replace `xxxxx` with the starting record number and `yyyyy` with the ending record number)

g) READING FAULT REPORT FILES

Fault report data has been available via the L60 file retrieval mechanism since UR firmware version 2.00. The file name is **`faultReport#####.htm`**. The ##### refers to the fault report record number. The fault report number is a counter that indicates how many fault reports have ever occurred. The counter rolls over at a value of 65535. Only the last ten fault reports are available for retrieval; a request for a non-existent fault report file will yield a null file. The current value fault report counter is available in “Number of Fault Reports” Modbus register at location 0x3020.

For example, if 14 fault reports have occurred then the files `faultReport5.htm`, `faultReport6.htm`, up to `faultReport14.htm` are available to be read. The expected use of this feature has an external master periodically polling the “Number of Fault Reports' register. If the value changes, then the master reads all the new files.

The contents of the file is in standard HTML notation and can be viewed via any commercial browser.

B.3.2 MODBUS PASSWORD OPERATION

The L60 supports password entry from a local or remote connection.

Local access is defined as any access to settings or commands via the faceplate interface. This includes both keypad entry and the faceplate RS232 connection. Remote access is defined as any access to settings or commands via any rear communications port. This includes both Ethernet and RS485 connections. Any changes to the local or remote passwords enables this functionality.

When entering a settings or command password via EnerVista or any serial interface, the user must enter the corresponding connection password. If the connection is to the back of the L60, the remote password must be used. If the connection is to the RS232 port of the faceplate, the local password must be used.

The command password is set up at memory location 4000. Storing a value of "0" removes command password protection. When reading the password setting, the encrypted value (zero if no password is set) is returned. Command security is required to change the command password. Similarly, the setting password is set up at memory location 4002. These are the same settings and encrypted values found in the **SETTINGS ⇨ PRODUCT SETUP ⇨ PASSWORD SECURITY** menu via the keypad. Enabling password security for the faceplate display will also enable it for Modbus, and *vice-versa*.

To gain command level security access, the command password must be entered at memory location 4008. To gain setting level security access, the setting password must be entered at memory location 400A. The entered setting password must match the current setting password setting, or must be zero, to change settings or download firmware.

Command and setting passwords each have a 30-minute timer. Each timer starts when you enter the particular password, and is re-started whenever you "use" it. For example, writing a setting re-starts the setting password timer and writing a command register or forcing a coil re-starts the command password timer. The value read at memory location 4010 can be used to confirm whether a command password is enabled or disabled (a value of 0 represents disabled). The value read at memory location 4011 can be used to confirm whether a setting password is enabled or disabled.

Command or setting password security access is restricted to the particular port or particular TCP/IP connection on which the entry was made. Passwords must be entered when accessing the relay through other ports or connections, and the passwords must be re-entered after disconnecting and re-connecting on TCP/IP.

B

Table B–9: MODBUS MEMORY MAP (Sheet 1 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Product Information (Read Only)						
0000	UR Product Type	0 to 65535	---	1	F001	0
0002	Product Version	0 to 655.35	---	0.01	F001	1
Product Information (Read Only -- Written by Factory)						
0010	Serial Number	---	---	---	F203	“0”
0020	Manufacturing Date	0 to 4294967295	---	1	F050	0
0022	Modification Number	0 to 65535	---	1	F001	0
0040	Order Code	---	---	---	F204	“Order Code x”
0090	Ethernet MAC Address	---	---	---	F072	0
0093	Reserved (13 items)	---	---	---	F001	0
00A0	CPU Module Serial Number	---	---	---	F203	(none)
00B0	CPU Supplier Serial Number	---	---	---	F203	(none)
00C0	Ethernet Sub Module Serial Number (8 items)	---	---	---	F203	(none)
Self Test Targets (Read Only)						
0200	Self Test States (2 items)	0 to 4294967295	0	1	F143	0
Front Panel (Read Only)						
0204	LED Column *n* State, *n* = 1 to 10 (10 items)	0 to 65535	---	1	F501	0
0220	Display Message	---	---	---	F204	(none)
0248	Last Key Pressed	0 to 47	---	1	F530	0 (None)
Keypress Emulation (Read/Write)						
0280	Simulated keypress -- write zero before each keystroke	0 to 42	---	1	F190	0 (No key -- use between real keys)
Virtual Input Commands (Read/Write Command) (64 modules)						
0400	Virtual Input 1 State	0 to 1	---	1	F108	0 (Off)
0401	Virtual Input 2 State	0 to 1	---	1	F108	0 (Off)
0402	Virtual Input 3 State	0 to 1	---	1	F108	0 (Off)
0403	Virtual Input 4 State	0 to 1	---	1	F108	0 (Off)
0404	Virtual Input 5 State	0 to 1	---	1	F108	0 (Off)
0405	Virtual Input 6 State	0 to 1	---	1	F108	0 (Off)
0406	Virtual Input 7 State	0 to 1	---	1	F108	0 (Off)
0407	Virtual Input 8 State	0 to 1	---	1	F108	0 (Off)
0408	Virtual Input 9 State	0 to 1	---	1	F108	0 (Off)
0409	Virtual Input 10 State	0 to 1	---	1	F108	0 (Off)
040A	Virtual Input 11 State	0 to 1	---	1	F108	0 (Off)
040B	Virtual Input 12 State	0 to 1	---	1	F108	0 (Off)
040C	Virtual Input 13 State	0 to 1	---	1	F108	0 (Off)
040D	Virtual Input 14 State	0 to 1	---	1	F108	0 (Off)
040E	Virtual Input 15 State	0 to 1	---	1	F108	0 (Off)
040F	Virtual Input 16 State	0 to 1	---	1	F108	0 (Off)
0410	Virtual Input 17 State	0 to 1	---	1	F108	0 (Off)
0411	Virtual Input 18 State	0 to 1	---	1	F108	0 (Off)
0412	Virtual Input 19 State	0 to 1	---	1	F108	0 (Off)
0413	Virtual Input 20 State	0 to 1	---	1	F108	0 (Off)
0414	Virtual Input 21 State	0 to 1	---	1	F108	0 (Off)
0415	Virtual Input 22 State	0 to 1	---	1	F108	0 (Off)
0416	Virtual Input 23 State	0 to 1	---	1	F108	0 (Off)
0417	Virtual Input 24 State	0 to 1	---	1	F108	0 (Off)
0418	Virtual Input 25 State	0 to 1	---	1	F108	0 (Off)
0419	Virtual Input 26 State	0 to 1	---	1	F108	0 (Off)
041A	Virtual Input 27 State	0 to 1	---	1	F108	0 (Off)
041B	Virtual Input 28 State	0 to 1	---	1	F108	0 (Off)

Table B–9: MODBUS MEMORY MAP (Sheet 2 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
041C	Virtual Input 29 State	0 to 1	---	1	F108	0 (Off)
041D	Virtual Input 30 State	0 to 1	---	1	F108	0 (Off)
041E	Virtual Input 31 State	0 to 1	---	1	F108	0 (Off)
041F	Virtual Input 32 State	0 to 1	---	1	F108	0 (Off)
0420	Virtual Input 33 State	0 to 1	---	1	F108	0 (Off)
0421	Virtual Input 34 State	0 to 1	---	1	F108	0 (Off)
0422	Virtual Input 35 State	0 to 1	---	1	F108	0 (Off)
0423	Virtual Input 36 State	0 to 1	---	1	F108	0 (Off)
0424	Virtual Input 37 State	0 to 1	---	1	F108	0 (Off)
0425	Virtual Input 38 State	0 to 1	---	1	F108	0 (Off)
0426	Virtual Input 39 State	0 to 1	---	1	F108	0 (Off)
0427	Virtual Input 40 State	0 to 1	---	1	F108	0 (Off)
0428	Virtual Input 41 State	0 to 1	---	1	F108	0 (Off)
0429	Virtual Input 42 State	0 to 1	---	1	F108	0 (Off)
042A	Virtual Input 43 State	0 to 1	---	1	F108	0 (Off)
042B	Virtual Input 44 State	0 to 1	---	1	F108	0 (Off)
042C	Virtual Input 45 State	0 to 1	---	1	F108	0 (Off)
042D	Virtual Input 46 State	0 to 1	---	1	F108	0 (Off)
042E	Virtual Input 47 State	0 to 1	---	1	F108	0 (Off)
042F	Virtual Input 48 State	0 to 1	---	1	F108	0 (Off)
0430	Virtual Input 49 State	0 to 1	---	1	F108	0 (Off)
0431	Virtual Input 50 State	0 to 1	---	1	F108	0 (Off)
0432	Virtual Input 51 State	0 to 1	---	1	F108	0 (Off)
0433	Virtual Input 52 State	0 to 1	---	1	F108	0 (Off)
0434	Virtual Input 53 State	0 to 1	---	1	F108	0 (Off)
0435	Virtual Input 54 State	0 to 1	---	1	F108	0 (Off)
0436	Virtual Input 55 State	0 to 1	---	1	F108	0 (Off)
0437	Virtual Input 56 State	0 to 1	---	1	F108	0 (Off)
0438	Virtual Input 57 State	0 to 1	---	1	F108	0 (Off)
0439	Virtual Input 58 State	0 to 1	---	1	F108	0 (Off)
043A	Virtual Input 59 State	0 to 1	---	1	F108	0 (Off)
043B	Virtual Input 60 State	0 to 1	---	1	F108	0 (Off)
043C	Virtual Input 61 State	0 to 1	---	1	F108	0 (Off)
043D	Virtual Input 62 State	0 to 1	---	1	F108	0 (Off)
043E	Virtual Input 63 State	0 to 1	---	1	F108	0 (Off)
043F	Virtual Input 64 State	0 to 1	---	1	F108	0 (Off)
Digital Counter States (Read Only Non-Volatile) (8 modules)						
0800	Digital Counter 1 Value	-2147483647 to 2147483647	---	1	F004	0
0802	Digital Counter 1 Frozen	-2147483647 to 2147483647	---	1	F004	0
0804	Digital Counter 1 Frozen Time Stamp	0 to 4294967295	---	1	F050	0
0806	Digital Counter 1 Frozen Time Stamp us	0 to 4294967295	---	1	F003	0
0808	...Repeated for Digital Counter 2					
0810	...Repeated for Digital Counter 3					
0818	...Repeated for Digital Counter 4					
0820	...Repeated for Digital Counter 5					
0828	...Repeated for Digital Counter 6					
0830	...Repeated for Digital Counter 7					
0838	...Repeated for Digital Counter 8					
FlexStates (Read Only)						
0900	FlexState Bits (16 items)	0 to 65535	---	1	F001	0
Element States (Read Only)						
1000	Element Operate States (64 items)	0 to 65535	---	1	F502	0

Table B–9: MODBUS MEMORY MAP (Sheet 3 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
User Displays Actuals (Read Only)						
1080	Formatted user-definable displays (16 items)	---	---	---	F200	(none)
Modbus User Map Actuals (Read Only)						
1200	User Map Values (256 items)	0 to 65535	---	1	F001	0
Element Targets (Read Only)						
14C0	Target Sequence	0 to 65535	---	1	F001	0
14C1	Number of Targets	0 to 65535	---	1	F001	0
Element Targets (Read/Write)						
14C2	Target to Read	0 to 65535	---	1	F001	0
Element Targets (Read Only)						
14C3	Target Message	---	---	---	F200	"."
Digital Input/Output States (Read Only)						
1500	Contact Input States (6 items)	0 to 65535	---	1	F500	0
1508	Virtual Input States (8 items)	0 to 65535	---	1	F500	0
1510	Contact Output States (4 items)	0 to 65535	---	1	F500	0
1518	Contact Output Current States (4 items)	0 to 65535	---	1	F500	0
1520	Contact Output Voltage States (4 items)	0 to 65535	---	1	F500	0
1528	Virtual Output States (6 items)	0 to 65535	---	1	F500	0
1530	Contact Output Detectors (4 items)	0 to 65535	---	1	F500	0
Remote Input/Output States (Read Only)						
1540	Remote Device 1 States	0 to 65535	---	1	F500	0
1542	Remote Input States (4 items)	0 to 65535	---	1	F500	0
1550	Remote Devices Online	0 to 1	---	1	F126	0 (No)
Platform Direct Input/Output States (Read Only)						
15C0	Direct input states (6 items)	0 to 65535	---	1	F500	0
15C8	Direct outputs average message return time 1	0 to 65535	ms	1	F001	0
15C9	Direct outputs average message return time 2	0 to 65535	ms	1	F001	0
15CA	Direct inputs/outputs unreturned message count - Ch. 1	0 to 65535	---	1	F001	0
15CB	Direct inputs/outputs unreturned message count - Ch. 2	0 to 65535	---	1	F001	0
15D0	Direct device states	0 to 65535	---	1	F500	0
15D1	Reserved	0 to 65535	---	1	F001	0
15D2	Direct inputs/outputs CRC fail count 1	0 to 65535	---	1	F001	0
15D3	Direct inputs/outputs CRC fail count 2	0 to 65535	---	1	F001	0
Ethernet Fibre Channel Status (Read/Write)						
1610	Ethernet primary fibre channel status	0 to 2	---	1	F134	0 (Fail)
1611	Ethernet secondary fibre channel status	0 to 2	---	1	F134	0 (Fail)
Data Logger Actuals (Read Only)						
1618	Data logger channel count	0 to 16	channel	1	F001	0
1619	Time of oldest available samples	0 to 4294967295	seconds	1	F050	0
161B	Time of newest available samples	0 to 4294967295	seconds	1	F050	0
161D	Data logger duration	0 to 999.9	days	0.1	F001	0
L60 Test Mode (Read Only)						
1640	L60 Test Mode	0 to 1	---	1	F102	0 (Disabled)
L60 Test Mode (Read/Write Settings)						
1641	L60 Trip Control Status	0 to 2	---	1	F134	2
1642	L60 Channel Status (4 items)	0 to 2	---	0.001	F134	2
Source Current (Read Only) (6 modules)						
1800	Source 1 Phase A Current RMS	0 to 999999.999	A	0.001	F060	0
1802	Source 1 Phase B Current RMS	0 to 999999.999	A	0.001	F060	0
1804	Source 1 Phase C Current RMS	0 to 999999.999	A	0.001	F060	0
1806	Source 1 Neutral Current RMS	0 to 999999.999	A	0.001	F060	0
1808	Source 1 Phase A Current Magnitude	0 to 999999.999	A	0.001	F060	0
180A	Source 1 Phase A Current Angle	-359.9 to 0	degrees	0.1	F002	0
180B	Source 1 Phase B Current Magnitude	0 to 999999.999	A	0.001	F060	0

Table B–9: MODBUS MEMORY MAP (Sheet 4 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
180D	Source 1 Phase B Current Angle	-359.9 to 0	degrees	0.1	F002	0
180E	Source 1 Phase C Current Magnitude	0 to 999999.999	A	0.001	F060	0
1810	Source 1 Phase C Current Angle	-359.9 to 0	degrees	0.1	F002	0
1811	Source 1 Neutral Current Magnitude	0 to 999999.999	A	0.001	F060	0
1813	Source 1 Neutral Current Angle	-359.9 to 0	degrees	0.1	F002	0
1814	Source 1 Ground Current RMS	0 to 999999.999	A	0.001	F060	0
1816	Source 1 Ground Current Magnitude	0 to 999999.999	A	0.001	F060	0
1818	Source 1 Ground Current Angle	-359.9 to 0	degrees	0.1	F002	0
1819	Source 1 Zero Sequence Current Magnitude	0 to 999999.999	A	0.001	F060	0
181B	Source 1 Zero Sequence Current Angle	-359.9 to 0	degrees	0.1	F002	0
181C	Source 1 Positive Sequence Current Magnitude	0 to 999999.999	A	0.001	F060	0
181E	Source 1 Positive Sequence Current Angle	-359.9 to 0	degrees	0.1	F002	0
181F	Source 1 Negative Sequence Current Magnitude	0 to 999999.999	A	0.001	F060	0
1821	Source 1 Negative Sequence Current Angle	-359.9 to 0	degrees	0.1	F002	0
1822	Source 1 Differential Ground Current Magnitude	0 to 999999.999	A	0.001	F060	0
1824	Source 1 Differential Ground Current Angle	-359.9 to 0	degrees	0.1	F002	0
1825	Reserved (27 items)	---	---	---	F001	0
1840	...Repeated for Source 2					
1880	...Repeated for Source 3					
18C0	...Repeated for Source 4					
1900	...Repeated for Source 5					
1940	...Repeated for Source 6					
Source Voltage (Read Only) (6 modules)						
1A00	Source 1 Phase AG Voltage RMS		V		F060	0
1A02	Source 1 Phase BG Voltage RMS		V		F060	0
1A04	Source 1 Phase CG Voltage RMS		V		F060	0
1A06	Source 1 Phase AG Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A08	Source 1 Phase AG Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A09	Source 1 Phase BG Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A0B	Source 1 Phase BG Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A0C	Source 1 Phase CG Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A0E	Source 1 Phase CG Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A0F	Source 1 Phase AB or AC Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A11	Source 1 Phase BC or BA Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A13	Source 1 Phase CA or CB Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A15	Source 1 Phase AB or AC Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A17	Source 1 Phase AB or AC Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A18	Source 1 Phase BC or BA Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A1A	Source 1 Phase BC or BA Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A1B	Source 1 Phase CA or CB Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A1D	Source 1 Phase CA or CB Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A1E	Source 1 Auxiliary Voltage RMS		V		F060	0
1A20	Source 1 Auxiliary Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A22	Source 1 Auxiliary Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A23	Source 1 Zero Sequence Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A25	Source 1 Zero Sequence Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A26	Source 1 Positive Sequence Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A28	Source 1 Positive Sequence Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A29	Source 1 Negative Sequence Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A2B	Source 1 Negative Sequence Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
1A2C	Reserved (20 items)	---	---	---	F001	0
1A40	...Repeated for Source 2					
1A80	...Repeated for Source 3					
1AC0	...Repeated for Source 4					

Table B–9: MODBUS MEMORY MAP (Sheet 5 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
1B00	...Repeated for Source 5					
1B40	...Repeated for Source 6					
Source Power (Read Only) (6 modules)						
1C00	Source 1 Three Phase Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C02	Source 1 Phase A Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C04	Source 1 Phase B Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C06	Source 1 Phase C Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C08	Source 1 Three Phase Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C0A	Source 1 Phase A Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C0C	Source 1 Phase B Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C0E	Source 1 Phase C Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C10	Source 1 Three Phase Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C12	Source 1 Phase A Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C14	Source 1 Phase B Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C16	Source 1 Phase C Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C18	Source 1 Three Phase Power Factor	-0.999 to 1	---	0.001	F013	0
1C19	Source 1 Phase A Power Factor	-0.999 to 1	---	0.001	F013	0
1C1A	Source 1 Phase B Power Factor	-0.999 to 1	---	0.001	F013	0
1C1B	Source 1 Phase C Power Factor	-0.999 to 1	---	0.001	F013	0
1C1C	Reserved (4 items)	---	---	---	F001	0
1C20	...Repeated for Source 2					
1C40	...Repeated for Source 3					
1C60	...Repeated for Source 4					
1C80	...Repeated for Source 5					
1CA0	...Repeated for Source 6					
Source Energy (Read Only Non-Volatile) (6 modules)						
1D00	Source 1 Positive Watthour	0 to 1000000000000	Wh	0.001	F060	0
1D02	Source 1 Negative Watthour	0 to 1000000000000	Wh	0.001	F060	0
1D04	Source 1 Positive Varhour	0 to 1000000000000	varh	0.001	F060	0
1D06	Source 1 Negative Varhour	0 to 1000000000000	varh	0.001	F060	0
1D08	Reserved (8 items)	---	---	---	F001	0
1D10	...Repeated for Source 2					
1D20	...Repeated for Source 3					
1D30	...Repeated for Source 4					
1D40	...Repeated for Source 5					
1D50	...Repeated for Source 6					
Energy Commands (Read/Write Command)						
1D60	Energy Clear Command	0 to 1	---	1	F126	0 (No)
Source Frequency (Read Only) (6 modules)						
1D80	Frequency for Source 1	---	Hz	---	F003	0
1D82	Frequency for Source 2	---	Hz	---	F003	0
1D84	Frequency for Source 3	---	Hz	---	F003	0
1D86	Frequency for Source 4	---	Hz	---	F003	0
1D88	Frequency for Source 5	---	Hz	---	F003	0
1D8A	Frequency for Source 6	---	Hz	---	F003	0

Table B–9: MODBUS MEMORY MAP (Sheet 6 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Breaker Flashover (Read/Write Setting) (2 modules)						
21A6	Breaker 1 Flashover Function	0 to 1	---	1	F102	0 (Disabled)
21A7	Breaker 1 Flashover Side 1 Source	0 to 5	---	1	F167	0 (SRC 1)
21A8	Breaker 1 Flashover Side 2 Source	0 to 6	---	1	F211	0 (None)
21A9	Breaker 1 Flashover Status Closed A	0 to 65535	---	1	F300	0
21AA	Breaker 1 Flashover Status Closed B	0 to 65535	---	1	F300	0
21AB	Breaker 1 Flashover Status Closed C	0 to 65535	---	1	F300	0
21AC	Breaker 1 Flashover Voltage Pickup Level	0 to 1.5	pu	0.001	F001	850
21AD	Breaker 1 Flashover Voltage Difference Pickup Level	0 to 100000	V	1	F060	1000
21AF	Breaker 1 Flashover Current Pickup Level	0 to 1.5	pu	0.001	F001	600
21B0	Breaker 1 Flashover Pickup Delay	0 to 65.535	s	0.001	F001	100
21B1	Breaker 1 Flashover Supervision Phase A	0 to 65535	---	1	F300	0
21B2	Breaker 1 Flashover Supervision Phase B	0 to 65535	---	1	F300	0
21B3	Breaker 1 Flashover Supervision Phase C	0 to 65535	---	1	F300	0
21B4	Breaker 1 Flashover Block	0 to 65535	---	1	F300	0
21B5	Breaker 1 Flashover Events	0 to 1	---	1	F102	0 (Disabled)
21B6	Breaker 1 Flashover Target	0 to 2	---	1	F109	0 (Self-Reset)
21B7	Reserved (4 items)	---	---	---	F001	0
21BB	...Repeated for Breaker 2 Flashover	0 to 99999999	kA^2-cyc	1	F060	0
Breaker Arcing Current Actuals (Read Only Non-Volatile) (2 modules)						
21E0	Breaker 1 Arcing Current Phase A	0 to 99999999	kA^2-cyc	1	F060	0
21E2	Breaker 1 Arcing Current Phase B	0 to 99999999	kA^2-cyc	1	F060	0
21E4	Breaker 1 Arcing Current Phase C	0 to 99999999	kA^2-cyc	1	F060	0
21E6	Breaker 1 Operating Time Phase A	0 to 65535	ms	1	F001	0
21E7	Breaker 1 Operating Time Phase B	0 to 65535	ms	1	F001	0
21E8	Breaker 1 Operating Time Phase C	0 to 65535	ms	1	F001	0
21E9	Breaker 1 Operating Time	0 to 65535	ms	1	F001	0
21EA	...Repeated for Breaker Arcing Current 2					
Breaker Arcing Current Commands (Read/Write Command) (2 modules)						
2224	Breaker 1 Arcing Current Clear Command	0 to 1	---	1	F126	0 (No)
2225	Breaker 2 Arcing Current Clear Command	0 to 1	---	1	F126	0 (No)
Passwords Unauthorized Access (Read/Write Command)						
2230	Reset Unauthorized Access	0 to 1	---	1	F126	0 (No)
Source Current THD (Read Only) (4 modules)						
22A0	Source 1 Ia THD	0 to 100	%	0.1	F001	0
22A1	Source 1 Ib THD	0 to 100	%	0.1	F001	0
22A2	Source 1 Ic THD	0 to 100	%	0.1	F001	0
22A3	Source 1 In THD	0 to 100	%	0.1	F001	0
22A4	...Repeated for Source 2					
22A8	...Repeated for Source 3					
22AC	...Repeated for Source 4					
Fault Location (Read Only) (5 modules)						
2340	Fault 1 Prefault Phase A Current Magnitude	0 to 999999.999	A	0.001	F060	0
2342	Fault 1 Prefault Phase A Current Angle	-359.9 to 0	degrees	0.1	F002	0
2343	Fault 1 Prefault Phase B Current Magnitude	0 to 999999.999	A	0.001	F060	0
2345	Fault 1 Prefault Phase B Current Angle	-359.9 to 0	degrees	0.1	F002	0
2346	Fault 1 Prefault Phase C Current Magnitude	0 to 999999.999	A	0.001	F060	0
2348	Fault 1 Prefault Phase C Current Angle	-359.9 to 0	degrees	0.1	F002	0
2349	Fault 1 Prefault Phase A Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
234B	Fault 1 Prefault Phase A Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
234C	Fault 1 Prefault Phase B Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
234E	Fault 1 Prefault Phase B Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
234F	Fault 1 Prefault Phase C Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
2351	Fault 1 Prefault Phase C Voltage Angle	-359.9 to 0	degrees	0.1	F002	0

Table B–9: MODBUS MEMORY MAP (Sheet 7 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
2352	Fault 1 Phase A Current Magnitude	0 to 999999.999	A	0.001	F060	0
2354	Fault 1 Phase A Current Angle	-359.9 to 0	degrees	0.1	F002	0
2355	Fault 1 Phase B Current Magnitude	0 to 999999.999	A	0.001	F060	0
2357	Fault 1 Phase B Current Angle	-359.9 to 0	degrees	0.1	F002	0
2358	Fault 1 Phase C Current Magnitude	0 to 999999.999	A	0.001	F060	0
235A	Fault 1 Phase C Current Angle	-359.9 to 0	degrees	0.1	F002	0
235B	Fault 1 Phase A Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
235D	Fault 1 Phase A Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
235E	Fault 1 Phase B Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
2360	Fault 1 Phase B Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
2361	Fault 1 Phase C Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
2363	Fault 1 Phase C Voltage Angle	-359.9 to 0	degrees	0.1	F002	0
2364	Fault 1 Type	0 to 11	---	1	F148	0 (NA)
2365	Fault 1 Location based on Line length units (km or miles)	-3276.7 to 3276.7	---	0.1	F002	0
2366	...Repeated for Fault 2					
238C	...Repeated for Fault 3					
23B2	...Repeated for Fault 4					
23D8	...Repeated for Fault 5					
Synchrocheck Actuals (Read Only) (2 modules)						
2400	Synchrocheck 1 Delta Voltage	-1000000000000 to 1000000000000	V	1	F060	0
2402	Synchrocheck 1 Delta Frequency	0 to 655.35	Hz	0.01	F001	0
2403	Synchrocheck 1 Delta Phase	0 to 179.9	degrees	0.1	F001	0
2404	...Repeated for Synchrocheck 2					
Autoreclose Status (Read Only) (6 modules)						
2410	Autoreclose 1 Count	0 to 65535	---	1	F001	0
2411	Autoreclose 2 Count	0 to 65535	---	1	F001	0
2412	Autoreclose 3 Count	0 to 65535	---	1	F001	0
2413	Autoreclose 4 Count	0 to 65535	---	1	F001	0
2414	Autoreclose 5 Count	0 to 65535	---	1	F001	0
2415	Autoreclose 6 Count	0 to 65535	---	1	F001	0
Expanded FlexStates (Read Only)						
2B00	FlexStates, one per register (256 items)	0 to 1	---	1	F108	0 (Off)
Expanded Digital Input/Output states (Read Only)						
2D00	Contact Input States, one per register (96 items)	0 to 1	---	1	F108	0 (Off)
2D80	Contact Output States, one per register (64 items)	0 to 1	---	1	F108	0 (Off)
2E00	Virtual Output States, one per register (96 items)	0 to 1	---	1	F108	0 (Off)
Expanded Remote Input/Output Status (Read Only)						
2F00	Remote Device States, one per register (16 items)	0 to 1	---	1	F155	0 (Offline)
2F80	Remote Input States, one per register (64 items)	0 to 1	---	1	F108	0 (Off)
Oscillography Values (Read Only)						
3000	Oscillography Number of Triggers	0 to 65535	---	1	F001	0
3001	Oscillography Available Records	0 to 65535	---	1	F001	0
3002	Oscillography Last Cleared Date	0 to 400000000	---	1	F050	0
3004	Oscillography Number Of Cycles Per Record	0 to 65535	---	1	F001	0
Oscillography Commands (Read/Write Command)						
3005	Oscillography Force Trigger	0 to 1	---	1	F126	0 (No)
3011	Oscillography Clear Data	0 to 1	---	1	F126	0 (No)
Fault Report Indexing (Read Only Non-Volatile)						
3020	Number of Fault Reports	0 to 65535	---	1	F001	0
Fault Report Actuals (Read Only Non-Volatile) (15 modules)						
3030	Fault Report 1 Time	0 to 4294967295	---	1	F050	0
3032	Fault Report 2 Time	0 to 4294967295	---	1	F050	0
3034	Fault Report 3 Time	0 to 4294967295	---	1	F050	0

Table B–9: MODBUS MEMORY MAP (Sheet 8 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
3036	Fault Report 4 Time	0 to 4294967295	---	1	F050	0
3038	Fault Report 5 Time	0 to 4294967295	---	1	F050	0
303A	Fault Report 6 Time	0 to 4294967295	---	1	F050	0
303C	Fault Report 7 Time	0 to 4294967295	---	1	F050	0
303E	Fault Report 8 Time	0 to 4294967295	---	1	F050	0
3040	Fault Report 9 Time	0 to 4294967295	---	1	F050	0
3042	Fault Report 10 Time	0 to 4294967295	---	1	F050	0
3044	Fault Report 11 Time	0 to 4294967295	---	1	F050	0
3046	Fault Report 12 Time	0 to 4294967295	---	1	F050	0
3048	Fault Report 13 Time	0 to 4294967295	---	1	F050	0
304A	Fault Report 14 Time	0 to 4294967295	---	1	F050	0
304C	Fault Report 15 Time	0 to 4294967295	---	1	F050	0
Modbus file transfer (read/write)						
3100	Name of file to read	---	---	---	F204	(none)
Modbus file transfer values (read only)						
3200	Character position of current block within file	0 to 4294967295	---	1	F003	0
3202	Size of currently-available data block	0 to 65535	---	1	F001	0
3203	Block of data from requested file (122 items)	0 to 65535	---	1	F001	0
Event recorder actual values (read only)						
3400	Events Since Last Clear	0 to 4294967295	---	1	F003	0
3402	Number of Available Events	0 to 4294967295	---	1	F003	0
3404	Event Recorder Last Cleared Date	0 to 4294967295	---	1	F050	0
Event recorder commands (read/write)						
3406	Event Recorder Clear Command	0 to 1	---	1	F126	0 (No)
DCMA Input Values (Read Only) (24 modules)						
34C0	DCMA Inputs 1 Value	-9999999 to 9999999	---	1	F004	0
34C2	DCMA Inputs 2 Value	-9999999 to 9999999	---	1	F004	0
34C4	DCMA Inputs 3 Value	-9999999 to 9999999	---	1	F004	0
34C6	DCMA Inputs 4 Value	-9999999 to 9999999	---	1	F004	0
34C8	DCMA Inputs 5 Value	-9999999 to 9999999	---	1	F004	0
34CA	DCMA Inputs 6 Value	-9999999 to 9999999	---	1	F004	0
34CC	DCMA Inputs 7 Value	-9999999 to 9999999	---	1	F004	0
34CE	DCMA Inputs 8 Value	-9999999 to 9999999	---	1	F004	0
34D0	DCMA Inputs 9 Value	-9999999 to 9999999	---	1	F004	0
34D2	DCMA Inputs 10 Value	-9999999 to 9999999	---	1	F004	0
34D4	DCMA Inputs 11 Value	-9999999 to 9999999	---	1	F004	0
34D6	DCMA Inputs 12 Value	-9999999 to 9999999	---	1	F004	0
34D8	DCMA Inputs 13 Value	-9999999 to 9999999	---	1	F004	0
34DA	DCMA Inputs 14 Value	-9999999 to 9999999	---	1	F004	0
34DC	DCMA Inputs 15 Value	-9999999 to 9999999	---	1	F004	0
34DE	DCMA Inputs 16 Value	-9999999 to 9999999	---	1	F004	0
34E0	DCMA Inputs 17 Value	-9999999 to 9999999	---	1	F004	0
34E2	DCMA Inputs 18 Value	-9999999 to 9999999	---	1	F004	0
34E4	DCMA Inputs 19 Value	-9999999 to 9999999	---	1	F004	0
34E6	DCMA Inputs 20 Value	-9999999 to 9999999	---	1	F004	0
34E8	DCMA Inputs 21 Value	-9999999 to 9999999	---	1	F004	0
34EA	DCMA Inputs 22 Value	-9999999 to 9999999	---	1	F004	0
34EC	DCMA Inputs 23 Value	-9999999 to 9999999	---	1	F004	0
34EE	DCMA Inputs 24 Value	-9999999 to 9999999	---	1	F004	0
RTD Input Values (Read Only) (48 modules)						
34F0	RTD Input 1 Value	-32768 to 32767	°C	1	F002	0
34F1	RTD Input 2 Value	-32768 to 32767	°C	1	F002	0
34F2	RTD Input 3 Value	-32768 to 32767	°C	1	F002	0
34F3	RTD Input 4 Value	-32768 to 32767	°C	1	F002	0

Table B–9: MODBUS MEMORY MAP (Sheet 9 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
34F4	RTD Input 5 Value	-32768 to 32767	°C	1	F002	0
34F5	RTD Input 6 Value	-32768 to 32767	°C	1	F002	0
34F6	RTD Input 7 Value	-32768 to 32767	°C	1	F002	0
34F7	RTD Input 8 Value	-32768 to 32767	°C	1	F002	0
34F8	RTD Input 9 Value	-32768 to 32767	°C	1	F002	0
34F9	RTD Input 10 Value	-32768 to 32767	°C	1	F002	0
34FA	RTD Input 11 Value	-32768 to 32767	°C	1	F002	0
34FB	RTD Input 12 Value	-32768 to 32767	°C	1	F002	0
34FC	RTD Input 13 Value	-32768 to 32767	°C	1	F002	0
34FD	RTD Input 14 Value	-32768 to 32767	°C	1	F002	0
34FE	RTD Input 15 Value	-32768 to 32767	°C	1	F002	0
34FF	RTD Input 16 Value	-32768 to 32767	°C	1	F002	0
3500	RTD Input 17 Value	-32768 to 32767	°C	1	F002	0
3501	RTD Input 18 Value	-32768 to 32767	°C	1	F002	0
3502	RTD Input 19 Value	-32768 to 32767	°C	1	F002	0
3503	RTD Input 20 Value	-32768 to 32767	°C	1	F002	0
3504	RTD Input 21 Value	-32768 to 32767	°C	1	F002	0
3505	RTD Input 22 Value	-32768 to 32767	°C	1	F002	0
3506	RTD Input 23 Value	-32768 to 32767	°C	1	F002	0
3507	RTD Input 24 Value	-32768 to 32767	°C	1	F002	0
3508	RTD Input 25 Value	-32768 to 32767	°C	1	F002	0
3509	RTD Input 26 Value	-32768 to 32767	°C	1	F002	0
350A	RTD Input 27 Value	-32768 to 32767	°C	1	F002	0
350B	RTD Input 28 Value	-32768 to 32767	°C	1	F002	0
350C	RTD Input 29 Value	-32768 to 32767	°C	1	F002	0
350D	RTD Input 30 Value	-32768 to 32767	°C	1	F002	0
350E	RTD Input 31 Value	-32768 to 32767	°C	1	F002	0
350F	RTD Input 32 Value	-32768 to 32767	°C	1	F002	0
3510	RTD Input 33 Value	-32768 to 32767	°C	1	F002	0
3511	RTD Input 34 Value	-32768 to 32767	°C	1	F002	0
3512	RTD Input 35 Value	-32768 to 32767	°C	1	F002	0
3513	RTD Input 36 Value	-32768 to 32767	°C	1	F002	0
3514	RTD Input 37 Value	-32768 to 32767	°C	1	F002	0
3515	RTD Input 38 Value	-32768 to 32767	°C	1	F002	0
3516	RTD Input 39 Value	-32768 to 32767	°C	1	F002	0
3517	RTD Input 40 Value	-32768 to 32767	°C	1	F002	0
3518	RTD Input 41 Value	-32768 to 32767	°C	1	F002	0
3519	RTD Input 42 Value	-32768 to 32767	°C	1	F002	0
351A	RTD Input 43 Value	-32768 to 32767	°C	1	F002	0
351B	RTD Input 44 Value	-32768 to 32767	°C	1	F002	0
351C	RTD Input 45 Value	-32768 to 32767	°C	1	F002	0
351D	RTD Input 46 Value	-32768 to 32767	°C	1	F002	0
351E	RTD Input 47 Value	-32768 to 32767	°C	1	F002	0
351F	RTD Input 48 Value	-32768 to 32767	°C	1	F002	0
Expanded Direct Input/Output Status (Read Only)						
3560	Direct Device States, one per register (8 items)	0 to 1	---	1	F155	0 (Offline)
3570	Direct Input States, one per register (96 items)	0 to 1	---	1	F108	0 (Off)
Passwords (Read/Write Command)						
4000	Command Password Setting	0 to 4294967295	---	1	F003	0
Passwords (Read/Write Setting)						
4002	Setting Password Setting	0 to 4294967295	---	1	F003	0
Passwords (Read/Write)						
4008	Command Password Entry	0 to 4294967295	---	1	F003	0
400A	Setting Password Entry	0 to 4294967295	---	1	F003	0

Table B–9: MODBUS MEMORY MAP (Sheet 10 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Passwords (Read Only)						
4010	Command Password Status	0 to 1	---	1	F102	0 (Disabled)
4011	Setting Password Status	0 to 1	---	1	F102	0 (Disabled)
User Display Invoke (Read/Write Setting)						
4040	Invoke and Scroll Through User Display Menu Operand	0 to 65535	---	1	F300	0
LED Test (Read/Write Setting)						
4048	LED Test Function	0 to 1	---	1	F102	0 (Disabled)
4049	LED Test Control	0 to 65535	---	1	F300	0
Preferences (Read/Write Setting)						
404F	Language	0 to 3	---	1	F531	0 (English)
4050	Flash Message Time	0.5 to 10	s	0.1	F001	10
4051	Default Message Timeout	10 to 900	s	1	F001	300
4052	Default Message Intensity	0 to 3	---	1	F101	0 (25%)
4053	Screen Saver Feature	0 to 1	---	1	F102	0 (Disabled)
4054	Screen Saver Wait Time	1 to 65535	min	1	F001	30
4055	Current Cutoff Level	0.002 to 0.02	pu	0.001	F001	20
4056	Voltage Cutoff Level	0.1 to 1	V	0.1	F001	10
Communications (Read/Write Setting)						
407E	COM1 minimum response time	0 to 1000	ms	10	F001	0
407F	COM2 minimum response time	0 to 1000	ms	10	F001	0
4080	Modbus Slave Address	1 to 254	---	1	F001	254
4083	RS485 Com1 Baud Rate	0 to 11	---	1	F112	8 (115200)
4084	RS485 Com1 Parity	0 to 2	---	1	F113	0 (None)
4085	RS485 Com2 Baud Rate	0 to 11	---	1	F112	8 (115200)
4086	RS485 Com2 Parity	0 to 2	---	1	F113	0 (None)
4087	IP Address	0 to 4294967295	---	1	F003	56554706
4089	IP Subnet Mask	0 to 4294967295	---	1	F003	4294966272
408B	Gateway IP Address	0 to 4294967295	---	1	F003	56554497
408D	Network Address NSAP	---	---	---	F074	0
409A	DNP Channel 1 Port	0 to 4	---	1	F177	0 (None)
409B	DNP Channel 2 Port	0 to 4	---	1	F177	0 (None)
409C	DNP Address	0 to 65519	---	1	F001	1
409D	Reserved	0 to 1	---	1	F001	0
409E	DNP Client Addresses (2 items)	0 to 4294967295	---	1	F003	0
40A3	TCP Port Number for the Modbus protocol	1 to 65535	---	1	F001	502
40A4	TCP/UDP Port Number for the DNP Protocol	1 to 65535	---	1	F001	20000
40A5	TCP Port Number for the HTTP (Web Server) Protocol	1 to 65535	---	1	F001	80
40A6	Main UDP Port Number for the TFTP Protocol	1 to 65535	---	1	F001	69
40A7	Data Transfer UDP Port Numbers for the TFTP Protocol (zero means “automatic”) (2 items)	0 to 65535	---	1	F001	0
40A9	DNP Unsolicited Responses Function	0 to 1	---	1	F102	0 (Disabled)
40AA	DNP Unsolicited Responses Timeout	0 to 60	s	1	F001	5
40AB	DNP unsolicited responses maximum retries	1 to 255	---	1	F001	10
40AC	DNP unsolicited responses destination address	0 to 65519	---	1	F001	1
40AD	Ethernet operation mode	0 to 1	---	1	F192	0 (Half-Duplex)
40AE	DNP current scale factor	0 to 8	---	1	F194	2 (1)
40AF	DNP voltage scale factor	0 to 8	---	1	F194	2 (1)
40B0	DNP power scale factor	0 to 8	---	1	F194	2 (1)
40B1	DNP energy scale factor	0 to 8	---	1	F194	2 (1)
40B2	DNP power scale factor	0 to 8	---	1	F194	2 (1)
40B3	DNP other scale factor	0 to 8	---	1	F194	2 (1)
40B4	DNP current default deadband	0 to 65535	---	1	F001	30000
40B6	DNP voltage default deadband	0 to 65535	---	1	F001	30000
40B8	DNP power default deadband	0 to 65535	---	1	F001	30000

Table B–9: MODBUS MEMORY MAP (Sheet 11 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
40BA	DNP energy default deadband	0 to 65535	---	1	F001	30000
40BE	DNP other default deadband	0 to 65535	---	1	F001	30000
40C0	DNP IIN time synchronization bit period	1 to 10080	min	1	F001	1440
40C1	DNP message fragment size	30 to 2048	---	1	F001	240
40C2	DNP client address 3	0 to 4294967295	---	1	F003	0
40C4	DNP client address 4	0 to 4294967295	---	1	F003	0
40C6	DNP client address 5	0 to 4294967295	---	1	F003	0
40C8	DNP number of paired binary output control points	0 to 16	---	1	F001	0
40C9	DNP TCP connection timeout	0 to 16	---	1	F001	0
40CA	Reserved (22 items)	0 to 1	---	1	F001	0
40E0	TCP port number for the IEC 60870-5-104 protocol	1 to 65535	---	1	F001	2404
40E1	IEC 60870-5-104 protocol function	0 to 1	---	1	F102	0 (Disabled)
40E2	IEC 60870-5-104 protocol common address of ASDU	0 to 65535	---	1	F001	0
40E3	IEC 60870-5-104 protocol cyclic data transmit period	1 to 65535	s	1	F001	60
40E4	IEC 60870-5-104 current default threshold	0 to 65535	---	1	F001	30000
40E6	IEC 60870-5-104 voltage default threshold	0 to 65535	---	1	F001	30000
40E8	IEC 60870-5-104 power default threshold	0 to 65535	---	1	F001	30000
40EA	IEC 60870-5-104 energy default threshold	0 to 65535	---	1	F001	30000
40EC	IEC 60870-5-104 power default threshold	0 to 65535	---	1	F001	30000
40EE	IEC 60870-5-104 other default threshold	0 to 65535	---	1	F001	30000
40F0	IEC 60870-5-104 client address (5 items)	0 to 4294967295	---	1	F003	0
40FD	Reserved (60 items)	0 to 1	---	1	F001	0
4140	DNP object 1 default variation	1 to 2	---	1	F001	2
4141	DNP object 2 default variation	1 to 3	---	1	F001	2
4142	DNP object 20 default variation	0 to 3	---	1	F523	0 (1)
4143	DNP object 21 default variation	0 to 3	---	1	F524	0 (1)
4144	DNP object 22 default variation	0 to 3	---	1	F523	0 (1)
4145	DNP object 23 default variation	0 to 3	---	1	F523	0 (1)
4146	DNP object 30 default variation	1 to 5	---	1	F001	1
4147	DNP object 32 default variation	0 to 5	---	1	F525	0 (1)
Simple Network Time Protocol (Read/Write Setting)						
4168	Simple Network Time Protocol (SNTP) function	0 to 1	---	1	F102	0 (Disabled)
4169	Simple Network Time Protocol (SNTP) server IP address	0 to 4294967295	---	1	F003	0
416B	Simple Network Time Protocol (SNTP) UDP port number	1 to 65535	---	1	F001	123
Data Logger Commands (Read/Write Command)						
4170	Data Logger Clear	0 to 1	---	1	F126	0 (No)
Data Logger (Read/Write Setting)						
4181	Data Logger Channel Settings (16 items)	---	---	---	F600	0
4191	Data Logger Mode	0 to 1	---	1	F260	0 (continuous)
4192	Data Logger Trigger	0 to 65535	---	1	F300	0
4193	Data Logger Rate	15 to 3600000	ms	1	F003	60000
Clock (Read/Write Command)						
41A0	Real Time Clock Set Time	0 to 235959	---	1	F050	0
Clock (Read/Write Setting)						
41A2	SR Date Format	0 to 4294967295	---	1	F051	0
41A4	SR Time Format	0 to 4294967295	---	1	F052	0
41A6	IRIG-B Signal Type	0 to 2	---	1	F114	0 (None)
41A7	Clock Events Enable / Disable	0 to 1	---	1	F102	0 (Disabled)
41A8	Time Zone Offset from UTC	–24 to 24	hours	0.5	F002	0
41A9	Daylight Savings Time (DST) Function	0 to 1	---	1	F102	0 (Disabled)
41AA	Daylight Savings Time (DST) Start Month	0 to 11	---	1	F237	0 (January)
41AB	Daylight Savings Time (DST) Start Day	0 to 6	---	1	F238	0 (Sunday)
41AC	Daylight Savings Time (DST) Start Day Instance	0 to 4	---	1	F239	0 (First)
41AD	Daylight Savings Time (DST) Start Hour	0 to 23	---	1	F001	2

Table B–9: MODBUS MEMORY MAP (Sheet 12 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
41AE	Daylight Savings Time (DST) Stop Month	0 to 11	---	1	F237	0 (January)
41AF	Daylight Savings Time (DST) Stop Day	0 to 6	---	1	F238	0 (Sunday)
41B0	Daylight Savings Time (DST) Stop Day Instance	0 to 4	---	1	F239	0 (First)
41B1	Daylight Savings Time (DST) Stop Hour	0 to 23	---	1	F001	2
Fault Report Commands (Read/Write Command)						
41B2	Fault Reports Clear Data Command	0 to 1	---	1	F126	0 (No)
Oscillography (Read/Write Setting)						
41C0	Oscillography Number of Records	1 to 64	---	1	F001	15
41C1	Oscillography Trigger Mode	0 to 1	---	1	F118	0 (Auto. Overwrite)
41C2	Oscillography Trigger Position	0 to 100	%	1	F001	50
41C3	Oscillography Trigger Source	0 to 65535	---	1	F300	0
41C4	Oscillography AC Input Waveforms	0 to 4	---	1	F183	2 (16 samples/cycle)
41D0	Oscillography Analog Channel *n* (16 items)	0 to 65535	---	1	F600	0
4200	Oscillography Digital Channel *n* (63 items)	0 to 65535	---	1	F300	0
Trip and Alarm LEDs (Read/Write Setting)						
4260	Trip LED Input FlexLogic Operand	0 to 65535	---	1	F300	0
4261	Alarm LED Input FlexLogic Operand	0 to 65535	---	1	F300	0
User Programmable LEDs (Read/Write Setting) (48 modules)						
4280	FlexLogic™ Operand to Activate LED	0 to 65535	---	1	F300	0
4281	User LED type (latched or self-resetting)	0 to 1	---	1	F127	1 (Self-Reset)
4282	...Repeated for User-Programmable LED 2					
4284	...Repeated for User-Programmable LED 3					
4286	...Repeated for User-Programmable LED 4					
4288	...Repeated for User-Programmable LED 5					
428A	...Repeated for User-Programmable LED 6					
428C	...Repeated for User-Programmable LED 7					
428E	...Repeated for User-Programmable LED 8					
4290	...Repeated for User-Programmable LED 9					
4292	...Repeated for User-Programmable LED 10					
4294	...Repeated for User-Programmable LED 11					
4296	...Repeated for User-Programmable LED 12					
4298	...Repeated for User-Programmable LED 13					
429A	...Repeated for User-Programmable LED 14					
429C	...Repeated for User-Programmable LED 15					
429E	...Repeated for User-Programmable LED 16					
42A0	...Repeated for User-Programmable LED 17					
42A2	...Repeated for User-Programmable LED 18					
42A4	...Repeated for User-Programmable LED 19					
42A6	...Repeated for User-Programmable LED 20					
42A8	...Repeated for User-Programmable LED 21					
42AA	...Repeated for User-Programmable LED 22					
42AC	...Repeated for User-Programmable LED 23					
42AE	...Repeated for User-Programmable LED 24					
42B0	...Repeated for User-Programmable LED 25					
42B2	...Repeated for User-Programmable LED 26					
42B4	...Repeated for User-Programmable LED 27					
42B6	...Repeated for User-Programmable LED 28					
42B8	...Repeated for User-Programmable LED 29					
42BA	...Repeated for User-Programmable LED 30					
42BC	...Repeated for User-Programmable LED 31					
42BE	...Repeated for User-Programmable LED 32					
42C0	...Repeated for User-Programmable LED 33					
42C2	...Repeated for User-Programmable LED 34					
42C4	...Repeated for User-Programmable LED 35					

Table B–9: MODBUS MEMORY MAP (Sheet 13 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
42C6	...Repeated for User-Programmable LED 36					
42C8	...Repeated for User-Programmable LED 37					
42CA	...Repeated for User-Programmable LED 38					
42CC	...Repeated for User-Programmable LED 39					
42CE	...Repeated for User-Programmable LED 40					
42D0	...Repeated for User-Programmable LED 41					
42D2	...Repeated for User-Programmable LED 42					
42D4	...Repeated for User-Programmable LED 43					
42D6	...Repeated for User-Programmable LED 44					
42D8	...Repeated for User-Programmable LED 45					
42DA	...Repeated for User-Programmable LED 46					
42DC	...Repeated for User-Programmable LED 47					
42DE	...Repeated for User-Programmable LED 48					
Installation (Read/Write Setting)						
43E0	Relay Programmed State	0 to 1	---	1	F133	0 (Not Programmed)
43E1	Relay Name	---	---	---	F202	“Relay-1”
User Programmable Self Tests (Read/Write Setting)						
4441	User Programmable Detect Ring Break Function	0 to 1	---	1	F102	1 (Enabled)
4442	User Programmable Direct Device Off Function	0 to 1	---	1	F102	1 (Enabled)
4443	User Programmable Remote Device Off Function	0 to 1	---	1	F102	1 (Enabled)
4444	User Programmable Primary Ethernet Fail Function	0 to 1	---	1	F102	0 (Disabled)
4445	User Programmable Secondary Ethernet Fail Function	0 to 1	---	1	F102	0 (Disabled)
4446	User Programmable Battery Fail Function	0 to 1	---	1	F102	1 (Enabled)
4447	User Programmable SNTP Fail Function	0 to 1	---	1	F102	1 (Enabled)
4448	User Programmable IRIG-B Fail Function	0 to 1	---	1	F102	1 (Enabled)
CT Settings (Read/Write Setting) (6 modules)						
4480	Phase CT 1 Primary	1 to 65000	A	1	F001	1
4481	Phase CT 1 Secondary	0 to 1	---	1	F123	0 (1 A)
4482	Ground CT 1 Primary	1 to 65000	A	1	F001	1
4483	Ground CT 1 Secondary	0 to 1	---	1	F123	0 (1 A)
4484	...Repeated for CT Bank 2					
4488	...Repeated for CT Bank 3					
448C	...Repeated for CT Bank 4					
4490	...Repeated for CT Bank 5					
4494	...Repeated for CT Bank 6					
VT Settings (Read/Write Setting) (3 modules)						
4500	Phase VT 1 Connection	0 to 1	---	1	F100	0 (Wye)
4501	Phase VT 1 Secondary	50 to 240	V	0.1	F001	664
4502	Phase VT 1 Ratio	1 to 24000	:1	1	F060	1
4504	Auxiliary VT 1 Connection	0 to 6	---	1	F166	1 (Vag)
4505	Auxiliary VT 1 Secondary	50 to 240	V	0.1	F001	664
4506	Auxiliary VT 1 Ratio	1 to 24000	:1	1	F060	1
4508	...Repeated for VT Bank 2					
4510	...Repeated for VT Bank 3					
Source Settings (Read/Write Setting) (6 modules)						
4580	Source 1 Name	---	---	---	F206	“SRC 1"
4583	Source 1 Phase CT	0 to 63	---	1	F400	0
4584	Source 1 Ground CT	0 to 63	---	1	F400	0
4585	Source 1 Phase VT	0 to 63	---	1	F400	0
4586	Source 1 Auxiliary VT	0 to 63	---	1	F400	0
4587	...Repeated for Source 2					
458E	...Repeated for Source 3					
4595	...Repeated for Source 4					
459C	...Repeated for Source 5					

Table B–9: MODBUS MEMORY MAP (Sheet 14 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
45A3	...Repeated for Source 6					
Power System (Read/Write Setting)						
4600	Nominal Frequency	25 to 60	Hz	1	F001	60
4601	Phase Rotation	0 to 1	---	1	F106	0 (ABC)
4602	Frequency And Phase Reference	0 to 5	---	1	F167	0 (SRC 1)
4603	Frequency Tracking Function	0 to 1	---	1	F102	1 (Enabled)
Breaker Control (Read/Write Setting) (2 modules)						
4700	Breaker 1 Function	0 to 1	---	1	F102	0 (Disabled)
4701	Breaker 1 Name	---	---	---	F206	“Bkr 1"
4704	Breaker 1 Mode	0 to 1	---	1	F157	0 (3-Pole)
4705	Breaker 1 Open	0 to 65535	---	1	F300	0
4706	Breaker 1 Close	0 to 65535	---	1	F300	0
4707	Breaker 1 Phase A 3 Pole	0 to 65535	---	1	F300	0
4708	Breaker 1 Phase B	0 to 65535	---	1	F300	0
4709	Breaker 1 Phase C	0 to 65535	---	1	F300	0
470A	Breaker 1 External Alarm	0 to 65535	---	1	F300	0
470B	Breaker 1 Alarm Delay	0 to 1000000	s	0.001	F003	0
470D	Breaker 1 Push Button Control	0 to 1	---	1	F102	0 (Disabled)
470E	Breaker 1 Manual Close Recall Time	0 to 1000000	s	0.001	F003	0
4710	Breaker 1 Out Of Service	0 to 65535	---	1	F300	0
4711	Reserved (7 items)	0 to 65535	---	1	F300	0
4718	...Repeated for Breaker 2					
Synchrocheck (Read/Write Setting) (2 modules)						
4780	Synchrocheck 1 Function	0 to 1	---	1	F102	0 (Disabled)
4781	Synchrocheck 1 V1 Source	0 to 5	---	1	F167	0 (SRC 1)
4782	Synchrocheck 1 V2 Source	0 to 5	---	1	F167	1 (SRC 2)
4783	Synchrocheck 1 Maximum Voltage Difference	0 to 400000	V	1	F060	10000
4785	Synchrocheck 1 Maximum Angle Difference	0 to 100	degrees	1	F001	30
4786	Synchrocheck 1 Maximum Frequency Difference	0 to 2	Hz	0.01	F001	100
4787	Synchrocheck 1 Dead Source Select	0 to 5	---	1	F176	1 (LV1 and DV2)
4788	Synchrocheck 1 Dead V1 Maximum Voltage	0 to 1.25	pu	0.01	F001	30
4789	Synchrocheck 1 Dead V2 Maximum Voltage	0 to 1.25	pu	0.01	F001	30
478A	Synchrocheck 1 Live V1 Minimum Voltage	0 to 1.25	pu	0.01	F001	70
478B	Synchrocheck 1 Live V2 Minimum Voltage	0 to 1.25	pu	0.01	F001	70
478C	Synchrocheck 1 Target	0 to 2	---	1	F109	0 (Self-reset)
478D	Synchrocheck 1 Events	0 to 1	---	1	F102	0 (Disabled)
478E	Synchrocheck 1 Block	0 to 65535	---	1	F300	0
478F	Synchrocheck 1 Frequency Hysteresis	0 to 0.1	Hz	0.01	F001	6
4790	...Repeated for Synchrocheck 2					
Flexcurves A and B (Read/Write Settings)						
4800	FlexCurve A (120 items)	0 to 65535	ms	1	F011	0
48F0	FlexCurve B (120 items)	0 to 65535	ms	1	F011	0
Modbus User Map (Read/Write Setting)						
4A00	Modbus Address Settings for User Map (256 items)	0 to 65535	---	1	F001	0
User Displays Settings (Read/Write Setting) (16 modules)						
4C00	User-Definable Display 1 Top Line Text	---	---	---	F202	“ “
4C0A	User-Definable Display 1 Bottom Line Text	---	---	---	F202	““
4C14	Modbus Addresses of Display 1 Items (5 items)	0 to 65535	---	1	F001	0
4C19	Reserved (7 items)	---	---	---	F001	0
4C20	...Repeated for User-Definable Display 2					
4C40	...Repeated for User-Definable Display 3					
4C60	...Repeated for User-Definable Display 4					
4C80	...Repeated for User-Definable Display 5					
4CA0	...Repeated for User-Definable Display 6					

Table B–9: MODBUS MEMORY MAP (Sheet 15 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
4CC0	...Repeated for User-Definable Display 7					
4CE0	...Repeated for User-Definable Display 8					
4D00	...Repeated for User-Definable Display 9					
4D20	...Repeated for User-Definable Display 10					
4D40	...Repeated for User-Definable Display 11					
4D60	...Repeated for User-Definable Display 12					
4D80	...Repeated for User-Definable Display 13					
4DA0	...Repeated for User-Definable Display 14					
4DC0	...Repeated for User-Definable Display 15					
4DE0	...Repeated for User-Definable Display 16					
User Programmable Pushbuttons (Read/Write Setting) (12 modules)						
4E00	User Programmable Pushbutton 1 Function	0 to 2	---	1	F109	2 (Disabled)
4E01	User Programmable Pushbutton 1 Top Line	---	---	---	F202	(none)
4E0B	User Programmable Pushbutton 1 On Text	---	---	---	F202	(none)
4E15	User Programmable Pushbutton 1 Off Text	---	---	---	F202	(none)
4E1F	User Programmable Pushbutton 1 Drop-Out Time	0 to 60	s	0.05	F001	0
4E20	User Programmable Pushbutton 1 Target	0 to 2	---	1	F109	0 (Self-reset)
4E21	User Programmable Pushbutton 1 Events	0 to 1	---	1	F102	0 (Disabled)
4E22	User Programmable Pushbutton 1 LED Operand	0 to 65535	---	1	F300	0
4E23	User Programmable Pushbutton 1 Autoreset Delay	0 to 600	s	0.05	F001	0
4E24	User Programmable Pushbutton 1 Autoreset Function	0 to 1	---	1	F102	0 (Disabled)
4E25	User Programmable Pushbutton 1 Local Lock	0 to 65535	---	1	F300	0
4E26	User Programmable Pushbutton 1 Message Priority	0 to 2	---	1	F220	0 (Disabled)
4E27	User Programmable Pushbutton 1 Remote Lock	0 to 65535	---	1	F300	0
4E28	User Programmable Pushbutton 1 Reset	0 to 65535	---	1	F300	0
4E29	User Programmable Pushbutton 1 Set	0 to 65535	---	1	F300	0
4E2A	...Repeated for User Programmable Pushbutton 2					
4E54	...Repeated for User Programmable Pushbutton 3					
4E7E	...Repeated for User Programmable Pushbutton 4					
4EA8	...Repeated for User Programmable Pushbutton 5					
4ED2	...Repeated for User Programmable Pushbutton 6					
4EFC	...Repeated for User Programmable Pushbutton 7					
4F26	...Repeated for User Programmable Pushbutton 8					
4F50	...Repeated for User Programmable Pushbutton 9					
4F7A	...Repeated for User Programmable Pushbutton 10					
4FA4	...Repeated for User Programmable Pushbutton 11					
4FCE	...Repeated for User Programmable Pushbutton 12					
Flexlogic (Read/Write Setting)						
5000	FlexLogic™ Entry (512 items)	0 to 65535	---	1	F300	16384
RTD Inputs (Read/Write Setting) (48 modules)						
5400	RTD Input 1 Function	0 to 1	---	1	F102	0 (Disabled)
5401	RTD Input 1 ID	---	---	---	F205	“RTD Ip 1“
5407	RTD Input 1 Type	0 to 3	---	1	F174	0 (100 ohm Platinum)
5413	...Repeated for RTD Input 2					
5426	...Repeated for RTD Input 3					
5439	...Repeated for RTD Input 4					
544C	...Repeated for RTD Input 5					
545F	...Repeated for RTD Input 6					
5472	...Repeated for RTD Input 7					
5485	...Repeated for RTD Input 8					
5498	...Repeated for RTD Input 9					
54AB	...Repeated for RTD Input 10					
54BE	...Repeated for RTD Input 11					
54D1	...Repeated for RTD Input 12					

Table B–9: MODBUS MEMORY MAP (Sheet 16 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
54E4	...Repeated for RTD Input 13					
54F7	...Repeated for RTD Input 14					
550A	...Repeated for RTD Input 15					
551D	...Repeated for RTD Input 16					
5530	...Repeated for RTD Input 17					
5543	...Repeated for RTD Input 18					
5556	...Repeated for RTD Input 19					
5569	...Repeated for RTD Input 20					
557C	...Repeated for RTD Input 21					
558F	...Repeated for RTD Input 22					
55A2	...Repeated for RTD Input 23					
55B5	...Repeated for RTD Input 24					
55C8	...Repeated for RTD Input 25					
55DB	...Repeated for RTD Input 26					
55EE	...Repeated for RTD Input 27					
5601	...Repeated for RTD Input 28					
5614	...Repeated for RTD Input 29					
5627	...Repeated for RTD Input 30					
563A	...Repeated for RTD Input 31					
564D	...Repeated for RTD Input 32					
5660	...Repeated for RTD Input 33					
5673	...Repeated for RTD Input 34					
5686	...Repeated for RTD Input 35					
5699	...Repeated for RTD Input 36					
56AC	...Repeated for RTD Input 37					
56BF	...Repeated for RTD Input 38					
56D2	...Repeated for RTD Input 39					
56E5	...Repeated for RTD Input 40					
56F8	...Repeated for RTD Input 41					
570B	...Repeated for RTD Input 42					
571E	...Repeated for RTD Input 43					
5731	...Repeated for RTD Input 44					
5744	...Repeated for RTD Input 45					
5757	...Repeated for RTD Input 46					
576A	...Repeated for RTD Input 47					
577D	...Repeated for RTD Input 48					
Flexlogic Timers (Read/Write Setting) (32 modules)						
5800	FlexLogic™ Timer 1 Type	0 to 2	---	1	F129	0 (millisecond)
5801	FlexLogic™ Timer 1 Pickup Delay	0 to 60000	---	1	F001	0
5802	FlexLogic™ Timer 1 Dropout Delay	0 to 60000	---	1	F001	0
5803	Reserved (5 items)	0 to 65535	---	1	F001	0
5808	...Repeated for FlexLogic™ Timer 2					
5810	...Repeated for FlexLogic™ Timer 3					
5818	...Repeated for FlexLogic™ Timer 4					
5820	...Repeated for FlexLogic™ Timer 5					
5828	...Repeated for FlexLogic™ Timer 6					
5830	...Repeated for FlexLogic™ Timer 7					
5838	...Repeated for FlexLogic™ Timer 8					
5840	...Repeated for FlexLogic™ Timer 9					
5848	...Repeated for FlexLogic™ Timer 10					
5850	...Repeated for FlexLogic™ Timer 11					
5858	...Repeated for FlexLogic™ Timer 12					
5860	...Repeated for FlexLogic™ Timer 13					
5868	...Repeated for FlexLogic™ Timer 14					

Table B–9: MODBUS MEMORY MAP (Sheet 17 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
5870	...Repeated for FlexLogic™ Timer 15					
5878	...Repeated for FlexLogic™ Timer 16					
5880	...Repeated for FlexLogic™ Timer 17					
5888	...Repeated for FlexLogic™ Timer 18					
5890	...Repeated for FlexLogic™ Timer 19					
5898	...Repeated for FlexLogic™ Timer 20					
58A0	...Repeated for FlexLogic™ Timer 21					
58A8	...Repeated for FlexLogic™ Timer 22					
58B0	...Repeated for FlexLogic™ Timer 23					
58B8	...Repeated for FlexLogic™ Timer 24					
58C0	...Repeated for FlexLogic™ Timer 25					
58C8	...Repeated for FlexLogic™ Timer 26					
58D0	...Repeated for FlexLogic™ Timer 27					
58D8	...Repeated for FlexLogic™ Timer 28					
58E0	...Repeated for FlexLogic™ Timer 29					
58E8	...Repeated for FlexLogic™ Timer 30					
58F0	...Repeated for FlexLogic™ Timer 31					
58F8	...Repeated for FlexLogic™ Timer 32					
Phase Time Overcurrent (Read/Write Grouped Setting) (6 modules)						
5900	Phase Time Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
5901	Phase Time Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5902	Phase Time Overcurrent 1 Input	0 to 1	---	1	F122	0 (Phasor)
5903	Phase Time Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
5904	Phase Time Overcurrent 1 Curve	0 to 16	---	1	F103	0 (IEEE Mod Inv)
5905	Phase Time Overcurrent 1 Multiplier	0 to 600	---	0.01	F001	100
5906	Phase Time Overcurrent 1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
5907	Phase Time Overcurrent 1 Voltage Restraint	0 to 1	---	1	F102	0 (Disabled)
5908	Phase TOC 1 Block For Each Phase (3 items)	0 to 65535	---	1	F300	0
590B	Phase Time Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
590C	Phase Time Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
590D	Reserved (3 items)	0 to 1	---	1	F001	0
5910	...Repeated for Phase Time Overcurrent 2					
5920	...Repeated for Phase Time Overcurrent 3					
5930	...Repeated for Phase Time Overcurrent 4					
5940	...Repeated for Phase Time Overcurrent 5					
5950	...Repeated for Phase Time Overcurrent 6					
Phase Instantaneous Overcurrent (Read/Write Grouped Setting) (12 modules)						
5A00	Phase Instantaneous Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
5A01	Phase Instantaneous Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5A02	Phase Instantaneous Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
5A03	Phase Instantaneous Overcurrent 1 Delay	0 to 600	s	0.01	F001	0
5A04	Phase Instantaneous Overcurrent 1 Reset Delay	0 to 600	s	0.01	F001	0
5A05	Phase IOC1 Block For Each Phase (3 items)	0 to 65535	---	1	F300	0
5A08	Phase Instantaneous Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
5A09	Phase Instantaneous Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
5A0A	Reserved (6 items)	0 to 1	---	1	F001	0
5A10	...Repeated for Phase Instantaneous Overcurrent 2					
5A20	...Repeated for Phase Instantaneous Overcurrent 3					
5A30	...Repeated for Phase Instantaneous Overcurrent 4					
5A40	...Repeated for Phase Instantaneous Overcurrent 5					
5A50	...Repeated for Phase Instantaneous Overcurrent 6					
5A60	...Repeated for Phase Instantaneous Overcurrent 7					
5A70	...Repeated for Phase Instantaneous Overcurrent 8					
5A80	...Repeated for Phase Instantaneous Overcurrent 9					

Table B–9: MODBUS MEMORY MAP (Sheet 18 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
5A90	...Repeated for Phase Instantaneous Overcurrent 10					
5AA0	...Repeated for Phase Instantaneous Overcurrent 11					
5AB0	...Repeated for Phase Instantaneous Overcurrent 12					
Neutral Time Overcurrent (Read/Write Grouped Setting) (6 modules)						
5B00	Neutral Time Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
5B01	Neutral Time Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5B02	Neutral Time Overcurrent 1 Input	0 to 1	---	1	F122	0 (Phasor)
5B03	Neutral Time Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
5B04	Neutral Time Overcurrent 1 Curve	0 to 16	---	1	F103	0 (IEEE Mod Inv)
5B05	Neutral Time Overcurrent 1 Multiplier	0 to 600	---	0.01	F001	100
5B06	Neutral Time Overcurrent 1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
5B07	Neutral Time Overcurrent 1 Block	0 to 65535	---	1	F300	0
5B08	Neutral Time Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
5B09	Neutral Time Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
5B0A	Reserved (6 items)	0 to 1	---	1	F001	0
5B10	...Repeated for Neutral Time Overcurrent 2					
5B20	...Repeated for Neutral Time Overcurrent 3					
5B30	...Repeated for Neutral Time Overcurrent 4					
5B40	...Repeated for Neutral Time Overcurrent 5					
5B50	...Repeated for Neutral Time Overcurrent 6					
Neutral Instantaneous Overcurrent (Read/Write Grouped Setting) (12 modules)						
5C00	Neutral Instantaneous Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
5C01	Neutral Instantaneous Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5C02	Neutral Instantaneous Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
5C03	Neutral Instantaneous Overcurrent 1 Delay	0 to 600	s	0.01	F001	0
5C04	Neutral Instantaneous Overcurrent 1 Reset Delay	0 to 600	s	0.01	F001	0
5C05	Neutral Instantaneous Overcurrent 1 Block	0 to 65535	---	1	F300	0
5C06	Neutral Instantaneous Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
5C07	Neutral Instantaneous Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
5C08	Reserved (8 items)	0 to 1	---	1	F001	0
5C10	...Repeated for Neutral Instantaneous Overcurrent 2					
5C20	...Repeated for Neutral Instantaneous Overcurrent 3					
5C30	...Repeated for Neutral Instantaneous Overcurrent 4					
5C40	...Repeated for Neutral Instantaneous Overcurrent 5					
5C50	...Repeated for Neutral Instantaneous Overcurrent 6					
5C60	...Repeated for Neutral Instantaneous Overcurrent 7					
5C70	...Repeated for Neutral Instantaneous Overcurrent 8					
5C80	...Repeated for Neutral Instantaneous Overcurrent 9					
5C90	...Repeated for Neutral Instantaneous Overcurrent 10					
5CA0	...Repeated for Neutral Instantaneous Overcurrent 11					
5CB0	...Repeated for Neutral Instantaneous Overcurrent 12					
Ground Time Overcurrent (Read/Write Grouped Setting) (6 modules)						
5D00	Ground Time Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
5D01	Ground Time Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5D02	Ground Time Overcurrent 1 Input	0 to 1	---	1	F122	0 (Phasor)
5D03	Ground Time Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
5D04	Ground Time Overcurrent 1 Curve	0 to 16	---	1	F103	0 (IEEE Mod Inv)
5D05	Ground Time Overcurrent 1 Multiplier	0 to 600	---	0.01	F001	100
5D06	Ground Time Overcurrent 1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
5D07	Ground Time Overcurrent 1 Block	0 to 65535	---	1	F300	0
5D08	Ground Time Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
5D09	Ground Time Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
5D0A	Reserved (6 items)	0 to 1	---	1	F001	0
5D10	...Repeated for Ground Time Overcurrent 2					

Table B–9: MODBUS MEMORY MAP (Sheet 19 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
5D20	...Repeated for Ground Time Overcurrent 3					
5D30	...Repeated for Ground Time Overcurrent 4					
5D40	...Repeated for Ground Time Overcurrent 5					
5D50	...Repeated for Ground Time Overcurrent 6					
Ground Instantaneous Overcurrent (Read/Write Grouped Setting) (12 modules)						
5E00	Ground Instantaneous Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5E01	Ground Instantaneous Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
5E02	Ground Instantaneous Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
5E03	Ground Instantaneous Overcurrent 1 Delay	0 to 600	s	0.01	F001	0
5E04	Ground Instantaneous Overcurrent 1 Reset Delay	0 to 600	s	0.01	F001	0
5E05	Ground Instantaneous Overcurrent 1 Block	0 to 65535	---	1	F300	0
5E06	Ground Instantaneous Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
5E07	Ground Instantaneous Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
5E08	Reserved (8 items)	0 to 1	---	1	F001	0
5E10	...Repeated for Ground Instantaneous Overcurrent 2					
5E20	...Repeated for Ground Instantaneous Overcurrent 3					
5E30	...Repeated for Ground Instantaneous Overcurrent 4					
5E40	...Repeated for Ground Instantaneous Overcurrent 5					
5E50	...Repeated for Ground Instantaneous Overcurrent 6					
5E60	...Repeated for Ground Instantaneous Overcurrent 7					
5E70	...Repeated for Ground Instantaneous Overcurrent 8					
5E80	...Repeated for Ground Instantaneous Overcurrent 9					
5E90	...Repeated for Ground Instantaneous Overcurrent 10					
5EA0	...Repeated for Ground Instantaneous Overcurrent 11					
5EB0	...Repeated for Ground Instantaneous Overcurrent 12					
Setting Groups (Read/Write Setting)						
5F80	Setting Group for Modbus Comms (0 means group 1)	0 to 5	---	1	F001	0
5F81	Setting Groups Block	0 to 65535	---	1	F300	0
5F82	FlexLogic to Activate Groups 2 through 6 (5 items)	0 to 65535	---	1	F300	0
5F89	Setting Group Function	0 to 1	---	1	F102	0 (Disabled)
5F8A	Setting Group Events	0 to 1	---	1	F102	0 (Disabled)
Setting Groups (Read Only)						
5F8B	Current Setting Group	0 to 5	---	1	F001	0
Setting Group Names (Read/Write Setting)						
5F8C	Setting Group 1 Name	---	---	---	F203	(none)
5494	Setting Group 2 Name	---	---	---	F203	(none)
5F9C	Setting Group 3 Name	---	---	---	F203	(none)
5FA4	Setting Group 4 Name	---	---	---	F203	(none)
5FAC	Setting Group 5 Name	---	---	---	F203	(none)
5FB4	Setting Group 6 Name	---	---	---	F203	(none)
Wattmetric ground fault settings (read/write grouped, 2 modules)						
6050	Wattmetric ground fault 1 function	0 to 1	---	1	F102	0 (Disabled)
6051	Wattmetric ground fault 1 source	0 to 5	---	1	F167	0 (SRC 1)
6052	Wattmetric ground fault 1 voltage	0 to 1	---	1	F234	0 (Calculated VN)
6053	Wattmetric ground fault 1 overvoltage pickup	0.02 to 3.00	pu	0.01	F001	20
6054	Wattmetric ground fault 1 current	0 to 1	---	1	F235	(Calculated IN)
6055	Wattmetric ground fault 1 overcurrent pickup	0.002 to 30.000	pu	0.001	F001	60
6056	Wattmetric ground fault 1 overcurrent pickup delay	0 to 600	s	0.01	F001	20
6057	Wattmetric ground fault 1 power pickup	0.001 to 1.2	pu	0.001	F001	100
6058	Wattmetric ground fault 1 ECA	0 to 360	° Lag	1	F001	0
6059	Wattmetric ground fault 1 power pickup delay	0 to 600	s	0.01	F001	20
605A	Wattmetric ground fault 1 curve	0 to 5	---	1	F236	0 (Definite Time)
605B	Wattmetric ground fault 1 multiplier	0.01 to 2	s	0.01	F001	100
605C	Wattmetric ground fault 1 block	0 to 65535	---	1	F300	0

Table B–9: MODBUS MEMORY MAP (Sheet 20 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
605D	Wattmetric ground fault 1 target	0 to 2	---	1	F109	0 (Self-reset)
605E	Wattmetric ground fault 1 events	0 to 1	---	1	F102	0 (Disabled)
605F	Wattmetric ground fault 1 reference power	0.001 to 1.2	pu	0.001	F001	500
6060	Reserved	---	---	---	---	---
6061	...Repeated for wattmetric ground fault 2					
Wattmetric ground fault actual values (read only)						
6072	Wattmetric ground fault 1 operating power	0.000 to 1000000.000	W	0.001	F060	0
6074	Wattmetric ground fault 2 operating power	0.000 to 1000000.000	W	0.001	F060	0
Phase comparison: negative-sequence voltage fault detection settings (read/write, grouped)						
6080	Negative-sequence voltage fault detector function	0 to 1	---	1	F102	0 (Disabled)
6081	Negative-sequence voltage fault detector impedance	0 to 100	%	.01	F001	100
6082	Negative-sequence voltage fault detector low pickup	0.005 to 3.000	pu	0.001	F001	10
6083	Negative-sequence voltage fault detector high pickup	0.005 to 3.000	pu	0.001	F001	50
6084	Negative-sequence voltage fault detector block	0 to 65535	---	1	F300	0
6085	Negative-sequence voltage fault detector target	0 to 2	---	1	F109	0 (Self-reset)
6086	Negative-sequence voltage fault detector events	0 to 1	---	1	F102	0 (Disabled)
Phase comparison: rate of change of negative-sequence current settings (read/write, grouped)						
6088	Negative-sequence current rate of change function	0 to 1	---	1	F102	0 (Disabled)
6089	Negative-sequence current rate of change low pickup	0.01 to 5.00	pu	0.01	F001	10
608A	Negative-sequence current rate of change low seal-in	0 to 10.000	s	0.001	F001	600
608B	Negative-sequence current rate of change high pickup	0.01 to 5.00	pu	0.01	F001	50
608C	Negative-sequence current rate of change high seal-in	0 to 10.000	s	0.001	F001	200
608D	Negative-sequence current rate of change supervision	0 to 65535	---	1	F300	0
608E	Negative-sequence current rate of change block	0 to 65535	---	1	F300	0
608F	Negative-sequence current rate of change target	0 to 2	---	1	F109	0 (Self-reset)
6090	Negative-sequence current rate of change events	0 to 1	---	1	F102	0 (Disabled)
Phase comparison: rate of change of positive-sequence current settings (read/write, grouped)						
6088	Positive-sequence current rate of change function	0 to 1	---	1	F102	0 (Disabled)
6089	Positive-sequence current rate of change low pickup	0.01 to 5.00	pu	0.01	F001	10
608A	Positive-sequence current rate of change low seal-in	0 to 10.000	s	0.001	F001	600
608B	Positive-sequence current rate of change high pickup	0.01 to 5.00	pu	0.01	F001	50
608C	Positive-sequence current rate of change high seal-in	0 to 10.000	s	0.001	F001	200
608D	Positive-sequence current rate of change supervision	0 to 65535	---	1	F300	0
608E	Positive-sequence current rate of change block	0 to 65535	---	1	F300	0
608F	Positive-sequence current rate of change target	0 to 2	---	1	F109	0 (Self-reset)
6090	Positive-sequence current rate of change events	0 to 1	---	1	F102	0 (Disabled)
Phase Comparison Open Breaker Keying (Read/Write Grouped Setting)						
60E0	Open Breaker Keying	0 to 1	---	1	F102	0 (Disabled)
60E1	Breaker 1 Auxiliary Contact	0 to 65535	---	1	F300	0
60E2	Breaker 1 Supervision Element	0 to 65535	---	1	F300	0
60E3	Breaker 2 Auxiliary Contact	0 to 65535	---	1	F300	0
60E4	Breaker 2 Supervision Element	0 to 65535	---	1	F300	0
60E5	Weak-Infeed Keying	0 to 65535	---	1	F300	0
60E6	Supervision Element	0 to 65535	---	1	F300	0
60E7	Infeed Pickup Delay	0 to 50	s	0.001	F001	0
60E8	Infeed Reset Delay	0 to 50	s	0.001	F001	35
60E9	Open Breaker Keying Pickup Delay	0 to 50	s	0.001	F001	0
60EA	Open Breaker Keying Reset Delay	0 to 50	s	0.001	F001	0
Phase Comparison Trip Scheme (Read/Write Grouped Setting)						
60F0	87PC Function	0 to 1	---	1	F102	0 (Disabled)
60F1	87PC Channel Loss	0 to 500	ms	0.001	F001	0
60F2	87PC Block	0 to 65535	---	1	F300	0
60F3	87PC Target	0 to 2	---	1	F109	0 (Self-reset)
60F4	87PC Events	0 to 1	---	1	F102	0 (Disabled)

Table B–9: MODBUS MEMORY MAP (Sheet 21 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
60F5	87PC Scheme Select	0 to 8	---	1	F149	1 (2TL-BL-DPC-3FC)
60F6	87PC Scheme Signal	0 to 1	---	1	F150	0 (MIXED I_2 - K*I_1)
60F7	87PC Signal Source	0 to 5	---	1	F167	0 (SRC 1)
60F8	87PC FDL Pickup	0.01 to 15	pu	0.01	F001	50
60FA	87PC FDH Pickup	0.01 to 15	pu	0.01	F001	75
60FB	87PC Mixed Signal K	0 to 0.25	---	0.01	F001	20
60FE	87PC Phase Delay Ch1	0 to 65.535	ms	0.001	F003	0
6100	87PC Phase Delay Ch2	0 to 65.535	ms	0.001	F003	0
6106	87PC Transient Pickup	0 to 65.535	s	0.001	F003	30
610A	87PC Asymmetry Channel 1	–20 to 20	ms	0.1	F004	0
610E	87PC Asymmetry Channel 2	–20 to 20	ms	0.1	F004	0
6110	87PC Stability Angle	40 to 140	degrees	10	F003	75
6112	87PC Transient Reset	0 to 65.535	s	0.001	F003	30
6113	87PC Received Volts Channel 1	0 to 125	V	0.1	F001	120
6114	87PC Received Volts Channel 2	0 to 125	V	0.1	F001	120
6115	87PC High-Speed Contact 1	0 to 64	---	1	F490	0
6116	87PC High-Speed Contact 2	0 to 64	---	1	F490	0
6117	87PC FDL AUX	0 to 65535	---	1	F300	0
6118	87PC FDH AUX	0 to 65535	---	1	F300	0
6119	87PC Reset Delay	0 to 200	ms	1	F001	30
611A	87PC Mixed Signal Reference Angle	0 to 359	°	1	F001	0
611B	87PC Trip Security	0 to 1	---	1	F534	0 (First Coincidence)
611C	87PC Second Coincidence Timer	10 to 200	ms	1	F001	40
611D	87PC Enhanced Stability Angle	40 to 180	°	5	F001	110
CT Failure Detector (Read/Write Setting)						
6120	CT Fail Function	0 to 1	---	1	F102	0 (Disabled)
6121	CT Fail Block	0 to 65535	---	1	F300	0
6122	CT Fail Current Source 1	0 to 5	---	1	F167	0 (SRC 1)
6123	CT Fail Current Pickup 1	0 to 2	pu	0.1	F001	2
6124	CT Fail Current Source 2	0 to 5	---	1	F167	1 (SRC 2)
6125	CT Fail Current Pickup 2	0 to 2	pu	0.1	F001	2
6126	CT Fail Voltage Source	0 to 5	---	1	F167	0 (SRC 1)
6127	CT Fail Voltage Pickup	0 to 2	pu	0.01	F001	20
6128	CT Fail Pickup Delay	0 to 65.535	s	0.001	F001	1000
6129	CT Fail Target	0 to 2	---	1	F109	0 (Self-reset)
612A	CT Fail Events	0 to 1	---	1	F102	0 (Disabled)
Continuous Monitor (Read/Write Setting)						
6130	Continuous Monitor Function	0 to 1	---	1	F102	0 (Disabled)
6131	Continuous Monitor I OP	0 to 65535	---	1	F300	0
6132	Continuous Monitor I Supervision	0 to 65535	---	1	F300	0
6133	Continuous Monitor V OP	0 to 65535	---	1	F300	0
6134	Continuous Monitor V Supervision	0 to 65535	---	1	F300	0
6135	Continuous Monitor Target	0 to 2	---	1	F109	0 (Self-reset)
6136	Continuous Monitor Events	0 to 1	---	1	F102	0 (Disabled)
Negative Sequence Time Overcurrent (Read/Write Grouped Setting) (2 modules)						
6300	Negative Sequence Time Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
6301	Negative Sequence Time Overcurrent 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
6302	Negative Sequence Time Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
6303	Negative Sequence Time Overcurrent 1 Curve	0 to 16	---	1	F103	0 (IEEE Mod Inv)
6304	Negative Sequence Time Overcurrent 1 Multiplier	0 to 600	---	0.01	F001	100
6305	Negative Sequence Time Overcurrent 1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
6306	Negative Sequence Time Overcurrent 1 Block	0 to 65535	---	1	F300	0
6307	Negative Sequence Time Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
6308	Negative Sequence Time Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)

Table B–9: MODBUS MEMORY MAP (Sheet 22 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
6309	Reserved (7 items)	0 to 1	---	1	F001	0
6310	...Repeated for Negative Sequence Time Overcurrent 2					
Negative Sequence Instantaneous Overcurrent (Read/Write Grouped Setting) (2 modules)						
6400	Negative Sequence Instantaneous OC 1 Function	0 to 1	---	1	F102	0 (Disabled)
6401	Negative Sequence Instantaneous OC 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
6402	Negative Sequence Instantaneous Overcurrent 1 Pickup	0 to 30	pu	0.001	F001	1000
6403	Negative Sequence Instantaneous Overcurrent 1 Delay	0 to 600	s	0.01	F001	0
6404	Negative Sequence Instantaneous OC 1 Reset Delay	0 to 600	s	0.01	F001	0
6405	Negative Sequence Instantaneous Overcurrent 1 Block	0 to 65535	---	1	F300	0
6406	Negative Sequence Instantaneous Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
6407	Negative Sequence Instantaneous Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
6408	Reserved (8 items)	0 to 1	---	1	F001	0
6410	...Repeated for Negative Sequence Instantaneous OC 2					
Negative Sequence Overvoltage (Read/Write Grouped Setting)						
64A0	Negative Sequence Overvoltage Function	0 to 1	---	1	F102	0 (Disabled)
64A1	Negative Sequence Overvoltage Source	0 to 5	---	1	F167	0 (SRC 1)
64A2	Negative Sequence Overvoltage Pickup	0 to 1.25	pu	0.001	F001	300
64A3	Negative Sequence Overvoltage Pickup Delay	0 to 600	s	0.01	F001	50
64A4	Negative Sequence Overvoltage Reset Delay	0 to 600	s	0.01	F001	50
64A5	Negative Sequence Overvoltage Block	0 to 65535	---	1	F300	0
64A6	Negative Sequence Overvoltage Target	0 to 2	---	1	F109	0 (Self-reset)
64A7	Negative Sequence Overvoltage Events	0 to 1	---	1	F102	0 (Disabled)
Power Swing Detect (Read/Write Grouped Setting)						
65C0	Power Swing Detect Function	0 to 1	---	1	F102	0 (Disabled)
65C1	Power Swing Detect Source	0 to 5	---	1	F167	0 (SRC 1)
65C2	Power Swing Detect Mode	0 to 1	---	1	F513	0 (Two Step)
65C3	Power Swing Detect Supervision	0.05 to 30	pu	0.001	F001	600
65C4	Power Swing Detect Forward Reach	0.1 to 500	ohms	0.01	F001	5000
65C5	Power Swing Detect Forward RCA	40 to 90	degrees	1	F001	75
65C6	Power Swing Detect Reverse Reach	0.1 to 500	ohms	0.01	F001	5000
65C7	Power Swing Detect Reverse RCA	40 to 90	degrees	1	F001	75
65C8	Power Swing Detect Outer Limit Angle	40 to 140	degrees	1	F001	120
65C9	Power Swing Detect Middle Limit Angle	40 to 140	degrees	1	F001	90
65CA	Power Swing Detect Inner Limit Angle	40 to 140	degrees	1	F001	60
65CB	Power Swing Detect Delay 1 Pickup	0 to 65.535	s	0.001	F001	30
65CC	Power Swing Detect Delay 1 Reset	0 to 65.535	s	0.001	F001	50
65CD	Power Swing Detect Delay 2 Pickup	0 to 65.535	s	0.001	F001	17
65CE	Power Swing Detect Delay 3 Pickup	0 to 65.535	s	0.001	F001	9
65CF	Power Swing Detect Delay 4 Pickup	0 to 65.535	s	0.001	F001	17
65D0	Power Swing Detect Seal In Delay	0 to 65.535	s	0.001	F001	400
65D1	Power Swing Detect Trip Mode	0 to 1	---	1	F514	0 (Delayed)
65D2	Power Swing Detect Block	0 to 65535	---	1	F300	0
65D3	Power Swing Detect Target	0 to 2	---	1	F109	0 (Self-reset)
65D4	Power Swing Detect Event	0 to 1	---	1	F102	0 (Disabled)
65D5	Power Swing Detect Shape	0 to 1	---	1	F085	0 (Mho Shape)
65D6	Power Swing Detect Quad Forward Middle	0.1 to 500	ohms	0.01	F001	6000
65D7	Power Swing Detect Quad Forward Outer	0.1 to 500	ohms	0.01	F001	7000
65D8	Power Swing Detect Quad Reverse Middle	0.1 to 500	ohms	0.01	F001	6000
65D9	Power Swing Detect Quad Reverse Outer	0.1 to 500	ohms	0.01	F001	7000
65DA	Power Swing Detect Outer Right Blinder	0.1 to 500	ohms	0.01	F001	10000
65DB	Power Swing Detect Outer Left Blinder	0.1 to 500	ohms	0.01	F001	10000
65DC	Power Swing Detect Middle Right Blinder	0.1 to 500	ohms	0.01	F001	10000
65DD	Power Swing Detect Middle Left Blinder	0.1 to 500	ohms	0.01	F001	10000
65DE	Power Swing Detect Inner Right Blinder	0.1 to 500	ohms	0.01	F001	10000

Table B–9: MODBUS MEMORY MAP (Sheet 23 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
65DF	Power Swing Detect Inner Left Blinder	0.1 to 500	ohms	0.01	F001	10000
Load Encroachment (Read/Write Grouped Setting)						
6700	Load Encroachment Function	0 to 1	---	1	F102	0 (Disabled)
6701	Load Encroachment Source	0 to 5	---	1	F167	0 (SRC 1)
6702	Load Encroachment Minimum Voltage	0 to 3	pu	0.001	F001	250
6703	Load Encroachment Reach	0.02 to 250	ohms	0.01	F001	100
6704	Load Encroachment Angle	5 to 50	degrees	1	F001	30
6705	Load Encroachment Pickup Delay	0 to 65.535	s	0.001	F001	0
6706	Load Encroachment Reset Delay	0 to 65.535	s	0.001	F001	0
6707	Load Encroachment Block	0 to 65535	---	1	F300	0
6708	Load Encroachment Target	0 to 2	---	1	F109	0 (Self-reset)
6709	Load Encroachment Events	0 to 1	---	1	F102	0 (Disabled)
670A	Reserved (6 items)	0 to 65535	---	1	F001	0
Trip Output (Read/Write Setting)						
6800	Trip Mode	0 to 2	---	1	F195	0 (Disabled)
6801	Trip 3-Pole Input1	0 to 65535	---	1	F300	0
6802	Trip 3-Pole Input2	0 to 65535	---	1	F300	0
6803	Trip 3-Pole Input3	0 to 65535	---	1	F300	0
6804	Trip 3-Pole Input4	0 to 65535	---	1	F300	0
6805	Trip 3-Pole Input5	0 to 65535	---	1	F300	0
6806	Trip 3-Pole Input6	0 to 65535	---	1	F300	0
6807	Trip 1-Pole Input1	0 to 65535	---	1	F300	0
6808	Trip 1-Pole Input2	0 to 65535	---	1	F300	0
6809	Trip 1-Pole Input3	0 to 65535	---	1	F300	0
680A	Trip 1-Pole Input4	0 to 65535	---	1	F300	0
680B	Trip 1-Pole Input5	0 to 65535	---	1	F300	0
680C	Trip 1-Pole Input6	0 to 65535	---	1	F300	0
680D	Trip Reclose Input1	0 to 65535	---	1	F300	0
680E	Trip Reclose Input2	0 to 65535	---	1	F300	0
680F	Trip Reclose Input3	0 to 65535	---	1	F300	0
6810	Trip Reclose Input4	0 to 65535	---	1	F300	0
6811	Trip Reclose Input5	0 to 65535	---	1	F300	0
6812	Trip Reclose Input6	0 to 65535	---	1	F300	0
6813	Trip Force 3-Pole	0 to 65535	---	1	F300	0
6814	Trip Pilot Priority	0 to 65.535	s	0.001	F001	0
6815	Breaker Phase A Open	0 to 65535	---	1	F300	0
6816	Breaker Phase B Open	0 to 65535	---	1	F300	0
6817	Breaker Phase C Open	0 to 65535	---	1	F300	0
6818	Trip Events	0 to 1	---	1	F102	0 (Disabled)
6819	Reverse Fault Operand	0 to 65535	---	1	F300	0
681A	Trip Delay On Evolving Faults	0 to 65.535	s	0.001	F001	0
681B	Reserved (5 items)	0 to 1	---	1	F001	0
Open Pole Detect (Read/Write Setting)						
6820	Open Pole Function	0 to 1	---	1	F102	0 (Disabled)
6821	Open Pole Block	0 to 65535	---	1	F300	0
6822	Open Pole Voltage Supervision	0 to 1	---	1	F102	0 (Disabled)
6823	Open Pole Current Pickup	0 to 30	pu	0.001	F001	50
6824	Open Pole Target	0 to 2	---	1	F109	0 (Self-reset)
6825	Open Pole Events	0 to 1	---	1	F102	0 (Disabled)
6826	Open Pole Line XC0	300 to 9999.9	ohms	0.1	F003	99999
6828	Open Pole Line XC1	300 to 9999.9	ohms	0.1	F003	99999
682A	Open Pole Remote Current Pickup	0 to 30	pu	0.001	F001	50
682B	Reserved (5 items)	0 to 1	---	1	F001	0

Table B–9: MODBUS MEMORY MAP (Sheet 24 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Autoreclose 1P 3P (Read/Write Setting)						
6890	Autoreclose Mode	0 to 3	---	1	F080	0 (1 & 3 Pole)
6891	Autoreclose Maximum Number of Shots	1 to 4	---	1	F001	2
6892	Autoreclose Block Breaker 1	0 to 65535	---	1	F300	0
6893	Autoreclose Close Time Breaker 1	0 to 655.35	s	0.01	F001	10
6894	Autoreclose Breaker Manual Close	0 to 65535	---	1	F300	0
6895	Autoreclose Function	0 to 1	---	1	F102	0 (Disabled)
6896	Autoreclose Block Time Manual Close	0 to 655.35	s	0.01	F001	1000
6897	Autoreclose 1P Initiate	0 to 65535	---	1	F300	0
6898	Autoreclose 3P Initiate	0 to 65535	---	1	F300	0
6899	Autoreclose 3P TD Initiate	0 to 65535	---	1	F300	0
689A	Autoreclose Multi-Phase Fault	0 to 65535	---	1	F300	0
689B	Autoreclose Breaker 1 Pole Open	0 to 65535	---	1	F300	0
689C	Autoreclose Breaker 3 Pole Open	0 to 65535	---	1	F300	0
689D	Autoreclose 3-Pole Dead Time 1	0 to 655.35	s	0.01	F001	50
689E	Autoreclose 3-Pole Dead Time 2	0 to 655.35	s	0.01	F001	120
689F	Autoreclose Extend Dead T1	0 to 65535	---	1	F300	0
68A0	Autoreclose Dead T1 Extension	0 to 655.35	s	0.01	F001	50
68A1	Autoreclose Reset	0 to 65535	---	1	F300	0
68A2	Autoreclose Reset Time	0 to 655.35	s	0.01	F001	6000
68A3	Autoreclose Breaker Closed	0 to 65535	---	1	F300	0
68A4	Autoreclose Block	0 to 65535	---	1	F300	0
68A5	Autoreclose Pause	0 to 65535	---	1	F300	0
68A6	Autoreclose Incomplete Sequence Time	0 to 655.35	s	0.01	F001	500
68A7	Autoreclose Block Breaker 2	0 to 65535	---	1	F300	0
68A8	Autoreclose Close Time Breaker 2	0 to 655.35	s	0.01	F001	10
68A9	Autoreclose Transfer 1 to 2	0 to 1	---	1	F126	0 (No)
68AA	Autoreclose Transfer 2 to 1	0 to 1	---	1	F126	0 (No)
68AB	Autoreclose Breaker 1 Fail Option	0 to 1	---	1	F081	0 (Continue)
68AC	Autoreclose Breaker 2 Fail Option	0 to 1	---	1	F081	0 (Continue)
68AD	Autoreclose 1P Dead Time	0 to 655.35	s	0.01	F001	100
68AE	Autoreclose Breaker Sequence	0 to 4	---	1	F082	3 (1 - 2)
68AF	Autoreclose Transfer Time	0 to 655.35	s	0.01	F001	400
68B0	Autoreclose Event	0 to 1	---	1	F102	0 (Disabled)
68B1	Autoreclose 3P Dead Time 3	0 to 655.35	s	0.01	F001	200
68B2	Autoreclose 3P Dead Time 4	0 to 655.35	s	0.01	F001	400
68B3	Autoreclose Bus Fault Initiate	0 to 65535	s	0.01	F300	0
68B3	Reserved (14 items)	---	---	---	F001	0
Phase Undervoltage (Read/Write Grouped Setting) (2 modules)						
7000	Phase Undervoltage 1 Function	0 to 1	---	1	F102	0 (Disabled)
7001	Phase Undervoltage 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7002	Phase Undervoltage 1 Pickup	0 to 3	pu	0.001	F001	1000
7003	Phase Undervoltage 1 Curve	0 to 1	---	1	F111	0 (Definite Time)
7004	Phase Undervoltage 1 Delay	0 to 600	s	0.01	F001	100
7005	Phase Undervoltage 1 Minimum Voltage	0 to 3	pu	0.001	F001	100
7006	Phase Undervoltage 1 Block	0 to 65535	---	1	F300	0
7007	Phase Undervoltage 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7008	Phase Undervoltage 1 Events	0 to 1	---	1	F102	0 (Disabled)
7009	Phase Undervoltage 1 Measurement Mode	0 to 1	---	1	F186	0 (Phase to Ground)
700A	Reserved (6 items)	0 to 1	---	1	F001	0
7013	...Repeated for Phase Undervoltage 2					
Phase Overvoltage (Read/Write Grouped Setting)						
7040	Phase Overvoltage 1 Function	0 to 1	---	1	F102	0 (Disabled)
7041	Phase Overvoltage 1 Source	0 to 5	---	1	F167	0 (SRC 1)

Table B–9: MODBUS MEMORY MAP (Sheet 25 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
7042	Phase Overvoltage 1 Pickup	0 to 3	pu	0.001	F001	1000
7043	Phase Overvoltage 1 Delay	0 to 600	s	0.01	F001	100
7044	Phase Overvoltage 1 Reset Delay	0 to 600	s	0.01	F001	100
7045	Phase Overvoltage 1 Block	0 to 65535	---	1	F300	0
7046	Phase Overvoltage 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7047	Phase Overvoltage 1 Events	0 to 1	---	1	F102	0 (Disabled)
7048	Reserved (8 items)	0 to 1	---	1	F001	0
Distance (Read/Write Grouped Setting)						
7060	Distance Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7061	Memory Duration	5 to 25	cycles	1	F001	10
7062	Force Self-Polarization	0 to 65535	---	1	F300	0
7062	Force Memory Polarization	0 to 65535	---	1	F300	0
Phase Distance (Read/Write Grouped Setting) (5 modules)						
7070	Phase Distance Zone 1 Function	0 to 1	---	1	F102	0 (Disabled)
7071	Phase Distance Zone 1 Current Supervision	0.05 to 30	pu	0.001	F001	200
7072	Phase Distance Zone 1 Reach	0.02 to 500	ohms	0.01	F001	200
7073	Phase Distance Zone 1 Direction	0 to 2	---	1	F154	0 (Forward)
7074	Phase Distance Zone 1 Comparator Limit	30 to 90	degrees	1	F001	90
7075	Phase Distance Zone 1 Delay	0 to 65.535	s	0.001	F001	0
7076	Phase Distance Zone 1 Block	0 to 65535	---	1	F300	0
7077	Phase Distance Zone 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7078	Phase Distance Zone 1 Events	0 to 1	---	1	F102	0 (Disabled)
7079	Phase Distance Zone 1 Shape	0 to 1	---	1	F120	0 (Mho)
707A	Phase Distance Zone 1 RCA	30 to 90	degrees	1	F001	85
707B	Phase Distance Zone 1 DIR RCA	30 to 90	degrees	1	F001	85
707C	Phase Distance Zone 1 DIR Comp Limit	30 to 90	degrees	1	F001	90
707D	Phase Distance Zone 1 Quad Right Blinder	0.02 to 500	ohms	0.01	F001	1000
707E	Phase Distance Zone 1 Quad Right Blinder RCA	60 to 90	degrees	1	F001	85
707F	Phase Distance Zone 1 Quad Left Blinder	0.02 to 500	ohms	0.01	F001	1000
7080	Phase Distance Zone 1 Quad Left Blinder RCA	60 to 90	degrees	1	F001	85
7081	Phase Distance Zone 1 Volt Limit	0 to 5	pu	0.001	F001	0
7082	Phase Distance Zone 1 Transformer Voltage Connection	0 to 12	---	1	F153	0 (None)
7083	Phase Distance Zone 1 Transformer Current Connection	0 to 12	---	1	F153	0 (None)
7084	Phase Distance Zone 1 Rev Reach	0.02 to 500	ohms	0.01	F001	200
7085	Phase Distance Zone 1 Rev Reach RCA	30 to 90	degrees	1	F001	85
7086	Reserved (10 items)	---	---	---	F001	0
7090	...Repeated for Phase Distance Zone 2					
70B0	...Repeated for Phase Distance Zone 3					
Ground Distance (Read/Write Grouped Setting) (5 modules)						
7130	Ground Distance Zone 1 Function	0 to 1	---	1	F102	0 (Disabled)
7131	Ground Distance Zone 1 Current Supervision	0.05 to 30	pu	0.001	F001	200
7132	Ground Distance Zone 1 Reach	0.02 to 500	ohms	0.01	F001	200
7133	Ground Distance Zone 1 Direction	0 to 2	---	1	F154	0 (Forward)
7134	Ground Distance Zone 1 Comparator Limit	30 to 90	degrees	1	F001	90
7135	Ground Distance Zone 1 Delay	0 to 65.535	s	0.001	F001	0
7136	Ground Distance Zone 1 Block	0 to 65535	---	1	F300	0
7137	Ground Distance Zone 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7138	Ground Distance Zone 1 Events	0 to 1	---	1	F102	0 (Disabled)
7139	Ground Distance Zone 1 Shape	0 to 1	---	1	F120	0 (Mho)
713A	Ground Distance Zone 1 Z0 Z1 Magnitude	0 to 10	---	0.01	F001	270
713B	Ground Distance Zone 1 Z0 Z1 Angle	-90 to 90	degrees	1	F002	0
713C	Ground Distance Zone 1 RCA	30 to 90	degrees	1	F001	85
713D	Ground Distance Zone 1 DIR RCA	30 to 90	degrees	1	F001	85
713E	Ground Distance Zone 1 DIR Comp Limit	30 to 90	degrees	1	F001	90

Table B–9: MODBUS MEMORY MAP (Sheet 26 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
713F	Ground Distance Zone 1 Quad Right Blinder	0.02 to 500	ohms	0.01	F001	1000
7140	Ground Distance Zone 1 Quad Right Blinder RCA	60 to 90	degrees	1	F001	85
7141	Ground Distance Zone 1 Quad Left Blinder	0.02 to 500	ohms	0.01	F001	1000
7142	Ground Distance Zone 1 Quad Left Blinder RCA	60 to 90	degrees	1	F001	85
7143	Ground Distance Zone 1 Z0M Z1 Magnitude	0 to 7	---	0.01	F001	0
7144	Ground Distance Zone 1 Z0M Z1 Angle	-90 to 90	degrees	1	F002	0
7145	Ground Distance Zone 1 Voltage Level	0 to 5	pu	0.001	F001	0
7146	Ground Distance Zone 1 Non-Homogeneous Angle	-40 to 40	degrees	0.1	F002	0
7147	Ground Distance Zone 1 POL Current	0 to 1	---	1	F521	0 (Zero-seq)
7148	Ground Distance Zone 1 Reverse Reach	0.02 to 500	ohms	0.01	F001	200
7149	Ground Distance Zone 1 Reverse Reach RCA	30 to 90	degrees	1	F001	85
714A	Reserved (7 items)	0 to 65535	---	1	F001	0
7151	...Repeated for Ground Distance Zone 2					
7172	...Repeated for Ground Distance Zone 3					
Line Pickup (Read/Write Grouped Setting)						
71F0	Line Pickup Function	0 to 1	---	1	F102	0 (Disabled)
71F1	Line Pickup Signal Source	0 to 5	---	1	F167	0 (SRC 1)
71F2	Line Pickup Phase IOC Pickup	0 to 30	pu	0.001	F001	1000
71F3	Line Pickup UV Pickup	0 to 3	pu	0.001	F001	700
71F4	Line End Open Pickup Delay	0 to 65.535	s	0.001	F001	150
71F5	Line End Open Reset Delay	0 to 65.535	s	0.001	F001	90
71F6	Line Pickup OV Pickup Delay	0 to 65.535	s	0.001	F001	40
71F7	Autoreclose Coordination Pickup Delay	0 to 65.535	s	0.001	F001	45
71F8	Autoreclose Coordination Reset Delay	0 to 65.535	s	0.001	F001	5
71F9	Autoreclose Coordination Bypass	0 to 1	---	1	F102	1 (Enabled)
71FA	Line Pickup Block	0 to 65535	---	1	F300	0
71FB	Line Pickup Target	0 to 2	---	1	F109	0 (Self-reset)
71FC	Line Pickup Events	0 to 1	---	1	F102	0 (Disabled)
71FD	Terminal Open	0 to 65535	---	1	F300	0
71FE	Autoreclose Accelerate	0 to 65535	---	1	F300	0
Phase Directional Overcurrent (Read/Write Grouped Setting) (2 modules)						
7260	Phase Directional Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
7261	Phase Directional Overcurrent 1 Source	0 to 5	---	1	F167	0 (SRC 1)
7262	Phase Directional Overcurrent 1 Block	0 to 65535	---	1	F300	0
7263	Phase Directional Overcurrent 1 ECA	0 to 359	---	1	F001	30
7264	Phase Directional Overcurrent 1 Pol V Threshold	0 to 3	pu	0.001	F001	700
7265	Phase Directional Overcurrent 1 Block Overcurrent	0 to 1	---	1	F126	0 (No)
7266	Phase Directional Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7267	Phase Directional Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
7268	Reserved (8 items)	0 to 1	---	1	F001	0
7270	...Repeated for Phase Directional Overcurrent 2					
Neutral Directional Overcurrent (Read/Write Grouped Setting) (2 modules)						
7280	Neutral Directional Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
7281	Neutral Directional Overcurrent 1 Source	0 to 5	---	1	F167	0 (SRC 1)
7282	Neutral Directional Overcurrent 1 Polarizing	0 to 2	---	1	F230	0 (Voltage)
7283	Neutral Directional Overcurrent 1 Forward ECA	-90 to 90	° Lag	1	F002	75
7284	Neutral Directional Overcurrent 1 Forward Limit Angle	40 to 90	degrees	1	F001	90
7285	Neutral Directional Overcurrent 1 Forward Pickup	0.002 to 30	pu	0.001	F001	50
7286	Neutral Directional Overcurrent 1 Reverse Limit Angle	40 to 90	degrees	1	F001	90
7287	Neutral Directional Overcurrent 1 Reverse Pickup	0.002 to 30	pu	0.001	F001	50
7288	Neutral Directional Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7289	Neutral Directional Overcurrent 1 Block	0 to 65535	---	1	F300	0
728A	Neutral Directional Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
728B	Neutral Directional Overcurrent 1 Polarizing Voltage	0 to 1	---	1	F231	0 (Calculated V0)

Table B–9: MODBUS MEMORY MAP (Sheet 27 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
728C	Neutral Directional Overcurrent 1 Op Current	0 to 1	---	1	F196	0 (Calculated 3I0)
728D	Neutral Directional Overcurrent 1 Offset	0 to 250	ohms	0.01	F001	0
728E	Neutral Directional Overcurrent 1 Pos Seq Restraint	0 to 0.5	---	0.001	F001	63
728F	Reserved	0 to 1	---	1	F001	0
7290	...Repeated for Neutral Directional Overcurrent 2					
Negative Sequence Directional Overcurrent (Read/Write Grouped Setting) (2 modules)						
72A0	Negative Sequence Directional Overcurrent 1 Function	0 to 1	---	1	F102	0 (Disabled)
72A1	Negative Sequence Directional Overcurrent 1 Source	0 to 5	---	1	F167	0 (SRC 1)
72A2	Negative Sequence Directional Overcurrent 1 Type	0 to 1	---	1	F179	0 (Neg Sequence)
72A3	Neg Sequence Directional Overcurrent 1 Forward ECA	0 to 90	° Lag	1	F002	75
72A4	Neg Seq Directional Overcurrent 1 Forward Limit Angle	40 to 90	degrees	1	F001	90
72A5	Neg Sequence Directional Overcurrent 1 Forward Pickup	0.05 to 30	pu	0.01	F001	5
72A6	Neg Seq Directional Overcurrent 1 Reverse Limit Angle	40 to 90	degrees	1	F001	90
72A7	Neg Sequence Directional Overcurrent 1 Reverse Pickup	0.05 to 30	pu	0.01	F001	5
72A8	Negative Sequence Directional Overcurrent 1 Target	0 to 2	---	1	F109	0 (Self-reset)
72A9	Negative Sequence Directional Overcurrent 1 Block	0 to 65535	---	1	F300	0
72AA	Negative Sequence Directional Overcurrent 1 Events	0 to 1	---	1	F102	0 (Disabled)
72AB	Negative Sequence Directional Overcurrent 1 Offset	0 to 250	ohms	0.01	F001	0
72AC	Neg Seq Directional Overcurrent 1 Pos Seq Restraint	0 to 0.5	---	0.001	F001	63
72AD	Reserved (3 items)	0 to 1	---	1	F001	0
72B0	...Repeated for Neg Seq Directional Overcurrent 2					
Breaker Arcing Current Settings (Read/Write Setting) (2 modules)						
72C0	Breaker 1 Arcing Current Function	0 to 1	---	1	F102	0 (Disabled)
72C1	Breaker 1 Arcing Current Source	0 to 5	---	1	F167	0 (SRC 1)
72C2	Breaker 1 Arcing Current Initiate A	0 to 65535	---	1	F300	0
72C3	Breaker 1 Arcing Current Initiate B	0 to 65535	---	1	F300	0
72C4	Breaker 1 Arcing Current Initiate C	0 to 65535	---	1	F300	0
72C5	Breaker 1 Arcing Current Delay	0 to 65.535	s	0.001	F001	0
72C6	Breaker 1 Arcing Current Limit	0 to 50000	kA^2-cyc	1	F001	1000
72C7	Breaker 1 Arcing Current Block	0 to 65535	---	1	F300	0
72C8	Breaker 1 Arcing Current Target	0 to 2	---	1	F109	0 (Self-reset)
72C9	Breaker 1 Arcing Current Events	0 to 1	---	1	F102	0 (Disabled)
72CA	...Repeated for Breaker 2 Arcing Current					
dcmA Inputs (Read/Write Setting) (24 modules)						
7300	dcmA Inputs 1 Function	0 to 1	---	1	F102	0 (Disabled)
7301	dcmA Inputs 1 ID	---	---	---	F205	“DCMA I 1"
7307	Reserved 1 (4 items)	0 to 65535	---	1	F001	0
730B	dcmA Inputs 1 Units	---	---	---	F206	“mA”
730E	dcmA Inputs 1 Range	0 to 6	---	1	F173	6 (4 to 20 mA)
730F	dcmA Inputs 1 Minimum Value	-9999.999 to 9999.999	---	0.001	F004	4000
7311	dcmA Inputs 1 Maximum Value	-9999.999 to 9999.999	---	0.001	F004	20000
7313	Reserved (5 items)	0 to 65535	---	1	F001	0
7318	...Repeated for dcmA Inputs 2					
7330	...Repeated for dcmA Inputs 3					
7348	...Repeated for dcmA Inputs 4					
7360	...Repeated for dcmA Inputs 5					
7378	...Repeated for dcmA Inputs 6					
7390	...Repeated for dcmA Inputs 7					
73A8	...Repeated for dcmA Inputs 8					
73C0	...Repeated for dcmA Inputs 9					
73D8	...Repeated for dcmA Inputs 10					
73F0	...Repeated for dcmA Inputs 11					
7408	...Repeated for dcmA Inputs 12					
7420	...Repeated for dcmA Inputs 13					

Table B–9: MODBUS MEMORY MAP (Sheet 28 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
7438	...Repeated for dcmA Inputs 14					
7450	...Repeated for dcmA Inputs 15					
7468	...Repeated for dcmA Inputs 16					
7480	...Repeated for dcmA Inputs 17					
7498	...Repeated for dcmA Inputs 18					
74B0	...Repeated for dcmA Inputs 19					
74C8	...Repeated for dcmA Inputs 20					
74E0	...Repeated for dcmA Inputs 21					
74F8	...Repeated for dcmA Inputs 22					
7510	...Repeated for dcmA Inputs 23					
7528	...Repeated for dcmA Inputs 24					
User Programmable Pushbuttons (Read/Write Setting) (12 modules)						
7B60	User Programmable Pushbutton 1 Function	0 to 2	---	1	F109	2 (Disabled)
7B61	User Programmable Pushbutton 1 Top Line	---	---	---	F202	(none)
7B6B	User Programmable Pushbutton 1 On Text	---	---	---	F202	(none)
7B75	User Programmable Pushbutton 1 Off Text	---	---	---	F202	(none)
7B7F	User Programmable Pushbutton 1 Drop-Out Time	0 to 60	s	0.05	F001	0
7B80	User Programmable Pushbutton 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7B81	User Programmable Pushbutton 1 Events	0 to 1	---	1	F102	0 (Disabled)
7B82	User Programmable Pushbutton 1 LED Operand	0 to 65535	---	1	F300	0
7B83	User Programmable Pushbutton 1 Autoreset Delay	0 to 600	s	0.05	F001	0
7B84	User Programmable Pushbutton 1 Autoreset Function	0 to 1	---	1	F102	0 (Disabled)
7B85	User Programmable Pushbutton 1 Local Lock	0 to 65535	---	1	F300	0
7B86	User Programmable Pushbutton 1 Message Priority	0 to 2	---	1	F220	0 (Disabled)
7B87	User Programmable Pushbutton 1 Remote Lock	0 to 65535	---	1	F300	0
7B88	User Programmable Pushbutton 1 Reset	0 to 65535	---	1	F300	0
7B89	User Programmable Pushbutton 1 Set	0 to 65535	---	1	F300	0
7B8A	...Repeated for User Programmable Pushbutton 2					
7BB4	...Repeated for User Programmable Pushbutton 3					
7BDE	...Repeated for User Programmable Pushbutton 4					
7C08	...Repeated for User Programmable Pushbutton 5					
7C32	...Repeated for User Programmable Pushbutton 6					
7C5C	...Repeated for User Programmable Pushbutton 7					
7C86	...Repeated for User Programmable Pushbutton 8					
7CB0	...Repeated for User Programmable Pushbutton 9					
7CDA	...Repeated for User Programmable Pushbutton 10					
7D04	...Repeated for User Programmable Pushbutton 11					
7D2E	...Repeated for User Programmable Pushbutton 12					
7D58	...Repeated for User Programmable Pushbutton 13					
7D82	...Repeated for User Programmable Pushbutton 14					
7DAC	...Repeated for User Programmable Pushbutton 15					
7DD6	...Repeated for User Programmable Pushbutton 16					
Neutral Overvoltage (Read/Write Grouped Setting) (3 modules)						
7F00	Neutral Overvoltage 1 Function	0 to 1	---	1	F102	0 (Disabled)
7F01	Neutral Overvoltage 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7F02	Neutral Overvoltage 1 Pickup	0 to 3.00	pu	0.001	F001	300
7F03	Neutral Overvoltage 1 Pickup Delay	0 to 600	s	0.01	F001	100
7F04	Neutral Overvoltage 1 Reset Delay	0 to 600	s	0.01	F001	100
7F05	Neutral Overvoltage 1 Block	0 to 65535	---	1	F300	0
7F06	Neutral Overvoltage 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7F07	Neutral Overvoltage 1 Events	0 to 1	---	1	F102	0 (Disabled)
7F08	Neutral Overvoltage 1 Curves	0 to 3	---	1	F116	0 (Definite Time)
7F09	Reserved (8 items)	0 to 65535	---	1	F001	0
7F10	...Repeated for Neutral Overvoltage 2					

Table B–9: MODBUS MEMORY MAP (Sheet 29 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
7F20	...Repeated for Neutral Overvoltage 3					
Auxiliary Overvoltage (Read/Write Grouped Setting) (3 modules)						
7F30	Auxiliary Overvoltage 1 Function	0 to 1	---	1	F102	0 (Disabled)
7F31	Auxiliary Overvoltage 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7F32	Auxiliary Overvoltage 1 Pickup	0 to 3	pu	0.001	F001	300
7F33	Auxiliary Overvoltage 1 Pickup Delay	0 to 600	s	0.01	F001	100
7F34	Auxiliary Overvoltage 1 Reset Delay	0 to 600	s	0.01	F001	100
7F35	Auxiliary Overvoltage 1 Block	0 to 65535	---	1	F300	0
7F36	Auxiliary Overvoltage 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7F37	Auxiliary Overvoltage 1 Events	0 to 1	---	1	F102	0 (Disabled)
7F38	Reserved (8 items)	0 to 65535	---	1	F001	0
7F40	...Repeated for Auxiliary Overvoltage 2					
7F50	...Repeated for Auxiliary Overvoltage 3					
Auxiliary Undervoltage (Read/Write Grouped Setting) (3 modules)						
7F60	Auxiliary Undervoltage 1 Function	0 to 1	---	1	F102	0 (Disabled)
7F61	Auxiliary Undervoltage 1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7F62	Auxiliary Undervoltage 1 Pickup	0 to 3	pu	0.001	F001	700
7F63	Auxiliary Undervoltage 1 Delay	0 to 600	s	0.01	F001	100
7F64	Auxiliary Undervoltage 1 Curve	0 to 1	---	1	F111	0 (Definite Time)
7F65	Auxiliary Undervoltage 1 Minimum Voltage	0 to 3	pu	0.001	F001	100
7F66	Auxiliary Undervoltage 1 Block	0 to 65535	---	1	F300	0
7F67	Auxiliary Undervoltage 1 Target	0 to 2	---	1	F109	0 (Self-reset)
7F68	Auxiliary Undervoltage 1 Events	0 to 1	---	1	F102	0 (Disabled)
7F69	Reserved (7 items)	0 to 65535	---	1	F001	0
7F70	...Repeated for Auxiliary Undervoltage 2					
7F80	...Repeated for Auxiliary Undervoltage 3					
Frequency (Read Only)						
8000	Tracking Frequency	---	Hz	---	F001	0
Breaker Failure (Read/Write Grouped Setting) (2 modules)						
8600	Breaker Failure 1 Function	0 to 1	---	1	F102	0 (Disabled)
8601	Breaker Failure 1 Mode	0 to 1	---	1	F157	0 (3-Pole)
8602	Breaker Failure 1 Source	0 to 5	---	1	F167	0 (SRC 1)
8603	Breaker Failure 1 Amp Supervision	0 to 1	---	1	F126	1 (Yes)
8604	Breaker Failure 1 Use Seal-In	0 to 1	---	1	F126	1 (Yes)
8605	Breaker Failure 1 Three Pole Initiate	0 to 65535	---	1	F300	0
8606	Breaker Failure 1 Block	0 to 65535	---	1	F300	0
8607	Breaker Failure 1 Phase Amp Supv Pickup	0.001 to 30	pu	0.001	F001	1050
8608	Breaker Failure 1 Neutral Amp Supv Pickup	0.001 to 30	pu	0.001	F001	1050
8609	Breaker Failure 1 Use Timer 1	0 to 1	---	1	F126	1 (Yes)
860A	Breaker Failure 1 Timer 1 Pickup	0 to 65.535	s	0.001	F001	0
860B	Breaker Failure 1 Use Timer 2	0 to 1	---	1	F126	1 (Yes)
860C	Breaker Failure 1 Timer 2 Pickup	0 to 65.535	s	0.001	F001	0
860D	Breaker Failure 1 Use Timer 3	0 to 1	---	1	F126	1 (Yes)
860E	Breaker Failure 1 Timer 3 Pickup	0 to 65.535	s	0.001	F001	0
860F	Breaker Failure 1 Breaker Status 1 Phase A/3P	0 to 65535	---	1	F300	0
8610	Breaker Failure 1 Breaker Status 2 Phase A/3P	0 to 65535	---	1	F300	0
8611	Breaker Failure 1 Breaker Test On	0 to 65535	---	1	F300	0
8612	Breaker Failure 1 Phase Amp Hiset Pickup	0.001 to 30	pu	0.001	F001	1050
8613	Breaker Failure 1 Neutral Amp Hiset Pickup	0.001 to 30	pu	0.001	F001	1050
8614	Breaker Failure 1 Phase Amp Loset Pickup	0.001 to 30	pu	0.001	F001	1050
8615	Breaker Failure 1 Neutral Amp Loset Pickup	0.001 to 30	pu	0.001	F001	1050
8616	Breaker Failure 1 Loset Time	0 to 65.535	s	0.001	F001	0
8617	Breaker Failure 1 Trip Dropout Delay	0 to 65.535	s	0.001	F001	0
8618	Breaker Failure 1 Target	0 to 2	---	1	F109	0 (Self-reset)

Table B–9: MODBUS MEMORY MAP (Sheet 30 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
8619	Breaker Failure 1 Events	0 to 1	---	1	F102	0 (Disabled)
861A	Breaker Failure 1 Phase A Initiate	0 to 65535	---	1	F300	0
861B	Breaker Failure 1 Phase B Initiate	0 to 65535	---	1	F300	0
861C	Breaker Failure 1 Phase C Initiate	0 to 65535	---	1	F300	0
861D	Breaker Failure 1 Breaker Status 1 Phase B	0 to 65535	---	1	F300	0
861E	Breaker Failure 1 Breaker Status 1 Phase C	0 to 65535	---	1	F300	0
861F	Breaker Failure 1 Breaker Status 2 Phase B	0 to 65535	---	1	F300	0
8620	Breaker Failure 1 Breaker Status 2 Phase C	0 to 65535	---	1	F300	0
8621	...Repeated for Breaker Failure 2					
8642	...Repeated for Breaker Failure 3					
8663	...Repeated for Breaker Failure 4					
8684	...Repeated for Breaker Failure 5					
86A5	...Repeated for Breaker Failure 6					
FlexState Settings (Read/Write Setting)						
8800	FlexState Parameters (256 items)	---	---	---	F300	0
Digital Elements (Read/Write Setting) (48 modules)						
8A00	Digital Element 1 Function	0 to 1	---	1	F102	0 (Disabled)
8A01	Digital Element 1 Name	---	---	---	F203	“Dig Element 1“
8A09	Digital Element 1 Input	0 to 65535	---	1	F300	0
8A0A	Digital Element 1 Pickup Delay	0 to 999999.999	s	0.001	F003	0
8A0C	Digital Element 1 Reset Delay	0 to 999999.999	s	0.001	F003	0
8A0E	Digital Element 1 Block	0 to 65535	---	1	F300	0
8A0F	Digital Element 1 Target	0 to 2	---	1	F109	0 (Self-reset)
8A10	Digital Element 1 Events	0 to 1	---	1	F102	0 (Disabled)
8A11	Digital Element 1 Pickup LED	0 to 1	---	1	F102	1 (Enabled)
8A12	Reserved (2 items)	---	---	---	F001	0
8A14	...Repeated for Digital Element 2					
8A28	...Repeated for Digital Element 3					
8A3C	...Repeated for Digital Element 4					
8A50	...Repeated for Digital Element 5					
8A64	...Repeated for Digital Element 6					
8A78	...Repeated for Digital Element 7					
8A8C	...Repeated for Digital Element 8					
8AA0	...Repeated for Digital Element 9					
8AB4	...Repeated for Digital Element 10					
8AC8	...Repeated for Digital Element 11					
8ADC	...Repeated for Digital Element 12					
8AF0	...Repeated for Digital Element 13					
8B04	...Repeated for Digital Element 14					
8B18	...Repeated for Digital Element 15					
8B2C	...Repeated for Digital Element 16					
8B40	...Repeated for Digital Element 17					
8B54	...Repeated for Digital Element 18					
8B68	...Repeated for Digital Element 19					
8B7C	...Repeated for Digital Element 20					
8B90	...Repeated for Digital Element 21					
8BA4	...Repeated for Digital Element 22					
8BB8	...Repeated for Digital Element 23					
8BCC	...Repeated for Digital Element 24					
8BE0	...Repeated for Digital Element 25					
8BF4	...Repeated for Digital Element 26					
8C08	...Repeated for Digital Element 27					
8C1C	...Repeated for Digital Element 28					
8C30	...Repeated for Digital Element 29					

Table B–9: MODBUS MEMORY MAP (Sheet 31 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
8C44	...Repeated for Digital Element 30					
8C58	...Repeated for Digital Element 31					
8C6C	...Repeated for Digital Element 32					
8C80	...Repeated for Digital Element 33					
8C94	...Repeated for Digital Element 34					
8CA8	...Repeated for Digital Element 35					
8CBC	...Repeated for Digital Element 36					
8CD0	...Repeated for Digital Element 37					
8CE4	...Repeated for Digital Element 38					
8CF8	...Repeated for Digital Element 39					
8D0C	...Repeated for Digital Element 40					
8D20	...Repeated for Digital Element 41					
8D34	...Repeated for Digital Element 42					
8D48	...Repeated for Digital Element 43					
8D5C	...Repeated for Digital Element 44					
8D70	...Repeated for Digital Element 45					
8D84	...Repeated for Digital Element 46					
8D98	...Repeated for Digital Element 47					
8DAC	...Repeated for Digital Element 48					
Trip Bus (Read/Write Setting)						
8E00	Trip Bus 1 Function	0 to 1	---	1	F102	0 (Disabled)
8E01	Trip Bus 1 Block	---	---	---	F300	0
8E02	Trip Bus 1 Pickup Delay	0 to 600	s	0.01	F001	0
8E03	Trip Bus 1 Reset Delay	0 to 600	s	0.01	F001	0
8E04	Trip Bus 1 Input 1	0 to 65535	---	1	F300	0
8E05	Trip Bus 1 Input 2	0 to 65535	---	1	F300	0
8E06	Trip Bus 1 Input 3	0 to 65535	---	1	F300	0
8E07	Trip Bus 1 Input 4	0 to 65535	---	1	F300	0
8E08	Trip Bus 1 Input 5	0 to 65535	---	1	F300	0
8E09	Trip Bus 1 Input 6	0 to 65535	---	1	F300	0
8E0A	Trip Bus 1 Input 7	0 to 65535	---	1	F300	0
8E0B	Trip Bus 1 Input 8	0 to 65535	---	1	F300	0
8E0C	Trip Bus 1 Input 9	0 to 65535	---	1	F300	0
8E0D	Trip Bus 1 Input 10	0 to 65535	---	1	F300	0
8E0E	Trip Bus 1 Input 11	0 to 65535	---	1	F300	0
8E0F	Trip Bus 1 Input 12	0 to 65535	---	1	F300	0
8E10	Trip Bus 1 Input 13	0 to 65535	---	1	F300	0
8E11	Trip Bus 1 Input 14	0 to 65535	---	1	F300	0
8E12	Trip Bus 1 Input 15	0 to 65535	---	1	F300	0
8E13	Trip Bus 1 Input 16	0 to 65535	---	1	F300	0
8E14	Trip Bus 1 Latching	0 to 1	---	1	F102	0 (Disabled)
8E15	Trip Bus 1 Reset	0 to 65535	---	1	F300	0
8E16	Trip Bus 1 Target	0 to 2	---	1	F109	0 (Self-reset)
8E16	Trip Bus 1 Events	0 to 1	---	1	F102	0 (Disabled)
8E18	Reserved (8 items)	---	---	---	F001	0
8E20	...Repeated for Trip Bus 2					
8E40	...Repeated for Trip Bus 3					
8E60	...Repeated for Trip Bus 4					
8E80	...Repeated for Trip Bus 5					
8EA0	...Repeated for Trip Bus 6					
FlexElement (Read/Write Setting) (16 modules)						
9000	FlexElement™ 1 Function	0 to 1	---	1	F102	0 (Disabled)
9001	FlexElement™ 1 Name	---	---	---	F206	“FxE 1”
9004	FlexElement™ 1 InputP	0 to 65535	---	1	F600	0

Table B–9: MODBUS MEMORY MAP (Sheet 32 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
9005	FlexElement™ 1 InputM	0 to 65535	---	1	F600	0
9006	FlexElement™ 1 Compare	0 to 1	---	1	F516	0 (LEVEL)
9007	FlexElement™ 1 Input	0 to 1	---	1	F515	0 (SIGNED)
9008	FlexElement™ 1 Direction	0 to 1	---	1	F517	0 (OVER)
9009	FlexElement™ 1 Hysteresis	0.1 to 50	%	0.1	F001	30
900A	FlexElement™ 1 Pickup	-90 to 90	pu	0.001	F004	1000
900C	FlexElement™ 1 DeltaT Units	0 to 2	---	1	F518	0 (Milliseconds)
900D	FlexElement™ 1 DeltaT	20 to 86400	---	1	F003	20
900F	FlexElement™ 1 Pickup Delay	0 to 65.535	s	0.001	F001	0
9010	FlexElement™ 1 Reset Delay	0 to 65.535	s	0.001	F001	0
9011	FlexElement™ 1 Block	0 to 65535	---	1	F300	0
9012	FlexElement™ 1 Target	0 to 2	---	1	F109	0 (Self-reset)
9013	FlexElement™ 1 Events	0 to 1	---	1	F102	0 (Disabled)
9014	...Repeated for FlexElement™ 2					
9028	...Repeated for FlexElement™ 3					
903C	...Repeated for FlexElement™ 4					
9050	...Repeated for FlexElement™ 5					
9064	...Repeated for FlexElement™ 6					
9078	...Repeated for FlexElement™ 7					
908C	...Repeated for FlexElement™ 8					
90A0	...Repeated for FlexElement™ 9					
90B4	...Repeated for FlexElement™ 10					
90C8	...Repeated for FlexElement™ 11					
90DC	...Repeated for FlexElement™ 12					
90F0	...Repeated for FlexElement™ 13					
9104	...Repeated for FlexElement™ 14					
9118	...Repeated for FlexElement™ 15					
912C	...Repeated for FlexElement™ 16					
Fault Report Settings (Read/Write Setting) (up to 5 modules)						
9200	Fault Report 1 Source	0 to 5	---	1	F167	0 (SRC 1)
9201	Fault Report 1 Trigger	0 to 65535	---	1	F300	0
9202	Fault Report 1 Z1 Magnitude	0.01 to 250	ohms	0.01	F001	300
9203	Fault Report 1 Z1 Angle	25 to 90	degrees	1	F001	75
9204	Fault Report 1 Z0 Magnitude	0.01 to 650	ohms	0.01	F001	900
9205	Fault Report 1 Z0 Angle	25 to 90	degrees	1	F001	75
9206	Fault Report 1 Line Length Units	0 to 1	---	1	F147	0 (km)
9207	Fault Report 1 Line Length	0 to 2000		0.1	F001	1000
9208	Fault Report 1 VT Substitution	0 to 2	---	1	F270	0 (None)
9208	Fault Report 1 System Z0 Magnitude	0.01 to 650.00	ohms	0.01	F001	900
9208	Fault Report 1 System Z0 Angle	25 to 90	degrees	1	F001	75
920B	...Repeated for Fault Report 2					
9216	...Repeated for Fault Report 3					
9221	...Repeated for Fault Report 4					
922C	...Repeated for Fault Report 5					
dcmA Outputs (Read/Write Setting) (24 modules)						
9300	dcmA Output 1 Source	0 to 65535	---	1	F600	0
9301	dcmA Output 1 Range	0 to 2	---	1	F522	0 (–1 to 1 mA)
9302	dcmA Output 1 Minimum	–90 to 90	pu	0.001	F004	0
9304	dcmA Output 1 Maximum	–90 to 90	pu	0.001	F004	1000
9306	...Repeated for dcmA Output 2					
930C	...Repeated for dcmA Output 3					
9312	...Repeated for dcmA Output 4					
9318	...Repeated for dcmA Output 5					
931E	...Repeated for dcmA Output 6					

Table B–9: MODBUS MEMORY MAP (Sheet 33 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
9324	...Repeated for dcmA Output 7					
932A	...Repeated for dcmA Output 8					
9330	...Repeated for dcmA Output 9					
9336	...Repeated for dcmA Output 10					
933C	...Repeated for dcmA Output 11					
9342	...Repeated for dcmA Output 12					
9348	...Repeated for dcmA Output 13					
934E	...Repeated for dcmA Output 14					
9354	...Repeated for dcmA Output 15					
935A	...Repeated for dcmA Output 16					
9360	...Repeated for dcmA Output 17					
9366	...Repeated for dcmA Output 18					
936C	...Repeated for dcmA Output 19					
9372	...Repeated for dcmA Output 20					
9378	...Repeated for dcmA Output 21					
937E	...Repeated for dcmA Output 22					
9384	...Repeated for dcmA Output 23					
938A	...Repeated for dcmA Output 24					
Direct Input/Output Names (Read/Write Setting) (96 modules)						
9400	Direct Input 1 Name	0 to 96	---	1	F205	“Dir Ip 1”
9406	Direct Output 1 Name	1 to 96	---	1	F205	“Dir Out 1”
940C	...Repeated for Direct Input/Output 2					
9418	...Repeated for Direct Input/Output 3					
9424	...Repeated for Direct Input/Output 4					
9430	...Repeated for Direct Input/Output 5					
943C	...Repeated for Direct Input/Output 6					
9448	...Repeated for Direct Input/Output 7					
9454	...Repeated for Direct Input/Output 8					
9460	...Repeated for Direct Input/Output 9					
946C	...Repeated for Direct Input/Output 10					
9478	...Repeated for Direct Input/Output 11					
9484	...Repeated for Direct Input/Output 12					
9490	...Repeated for Direct Input/Output 13					
949C	...Repeated for Direct Input/Output 14					
94A8	...Repeated for Direct Input/Output 15					
94B4	...Repeated for Direct Input/Output 16					
94C0	...Repeated for Direct Input/Output 17					
94CC	...Repeated for Direct Input/Output 18					
94D8	...Repeated for Direct Input/Output 19					
94E4	...Repeated for Direct Input/Output 20					
94F0	...Repeated for Direct Input/Output 21					
94FC	...Repeated for Direct Input/Output 22					
9508	...Repeated for Direct Input/Output 23					
9514	...Repeated for Direct Input/Output 24					
9520	...Repeated for Direct Input/Output 25					
952C	...Repeated for Direct Input/Output 26					
9538	...Repeated for Direct Input/Output 27					
9544	...Repeated for Direct Input/Output 28					
9550	...Repeated for Direct Input/Output 29					
955C	...Repeated for Direct Input/Output 30					
9568	...Repeated for Direct Input/Output 31					
9574	...Repeated for Direct Input/Output 32					
FlexElement Actuals (Read Only) (16 modules)						
9A01	FlexElement™ 1 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0

Table B–9: MODBUS MEMORY MAP (Sheet 34 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
9A03	FlexElement™ 2 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
9A05	FlexElement™ 3 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
9A07	FlexElement™ 4 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
9A09	FlexElement™ 5 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
9A0B	FlexElement™ 6 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
9A0D	FlexElement™ 7 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
9A0F	FlexElement™ 8 Actual	-2147483.647 to 2147483.647	---	0.001	F004	0
Teleprotection Inputs/Outputs (Read/Write Settings)						
9B00	Teleprotection Function	0 to 1	---	1	F102	0 (Disabled)
9B01	Teleprotection Number of Terminals	2 to 3	---	1	F001	2
9B02	Teleprotection Number of Channels	1 to 2	---	1	F001	1
9B03	Teleprotection Local Relay ID	0 to 255	---	1	F001	0
9B04	Teleprotection Terminal 1 ID	0 to 255	---	1	F001	0
9B05	Teleprotection Terminal 2 ID	0 to 255	---	1	F001	0
9B06	Reserved (10 items)	0 to 1	---	---	F001	0
9B10	Teleprotection Input 1-n Default States (16 items)	0 to 3	---	1	F086	0 (Off)
9B30	Teleprotection Input 2-n Default States (16 items)	0 to 3	---	1	F086	0 (Off)
9B50	Teleprotection Output 1-n Operand (16 items)	0 to 65535	---	1	F300	0
9B70	Teleprotection Output 2-n Operand (16 items)	0 to 65535	---	1	F300	0
Teleprotection Inputs/Outputs Commands (Read/Write Command)						
9B90	Teleprotection Clear Lost Packets	0 to 1	---	1	F126	0 (No)
Teleprotection Channel Tests (Read Only)						
9B91	Teleprotection Channel 1 Status	0 to 2	---	1	F134	1 (OK)
9B92	Teleprotection Channel 1 Number of Lost Packets	0 to 65535	---	1	F001	0
9B93	Teleprotection Channel 2 Status	0 to 2	---	1	F134	1 (OK)
9B94	Teleprotection Channel 2 Number of Lost Packets	0 to 65535	---	1	F001	0
9B95	Teleprotection Network Status	0 to 2	---	1	F134	2 (n/a)
9BA0	Teleprotection Channel 1 Input States	0 to 1	---	1	F500	0
9BA1	Teleprotection Channel 2 Input States	0 to 1	---	1	F500	0
9BB0	Teleprotection Input 1 States, 1 per register (16 items)	0 to 1	---	1	F108	0 (Off)
9BC0	Teleprotection Input 2 States, 1 per register (16 items)	0 to 1	---	1	F108	0 (Off)
Charge current compensation settings (read/write						
9EF0	Charging current compensation factor	0 to 1	---	1	F102	0 (Disabled)
9EF1	Charging current compensation block	0 to 65535	---	1	F300	0
9EF2	Charging current compensation positive-sequence Xc	0.100 to 65.535	kohms	0.001	F001	100
9EF3	Charging current compensation zero-sequence Xc	0.100 to 65.535	kohms	0.001	F001	100
VT Fuse Failure (Read/Write Setting) (6 modules)						
A040	VT Fuse Failure Function	0 to 1	---	1	F102	0 (Disabled)
A041	...Repeated for module number 2					
A042	...Repeated for module number 3					
A043	...Repeated for module number 4					
A044	...Repeated for module number 5					
A045	...Repeated for module number 6					
Permissive overreach transfer trip (POTT) settings (read/write)						
A070	POTT Scheme Function	0 to 1	---	1	F102	0 (Disabled)
A071	POTT Permissive Echo	0 to 1	---	1	F102	0 (Disabled)
A072	POTT Rx Pickup Delay	0 to 65.535	s	0.001	F001	0
A073	POTT Transient Block Pickup Delay	0 to 65.535	s	0.001	F001	20
A074	POTT Transient Block Reset Delay	0 to 65.535	s	0.001	F001	90
A075	POTT Echo Duration	0 to 65.535	s	0.001	F001	100
A076	POTT Line End Open Pickup Delay	0 to 65.535	s	0.001	F001	50
A077	POTT Seal In Delay	0 to 65.535	s	0.001	F001	400
A078	POTT Ground Direction OC Forward	0 to 65535	---	1	F300	0
A079	POTT Rx	0 to 65535	---	1	F300	0

Table B–9: MODBUS MEMORY MAP (Sheet 35 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
A07A	POTT Echo Lockout	0 to 65.535	s	0.001	F001	250
Selector switch actual values (read only)						
A210	Selector switch 1 position	1 to 7	---	1	F001	0
A211	Selector switch 2 position	1 to 7	---	1	F001	1
Selector switch settings (read/write, 2 modules)						
A280	Selector 1 Function	0 to 1	---	1	F102	0 (Disabled)
A281	Selector 1 Range	1 to 7	---	1	F001	7
A282	Selector 1 Timeout	3 to 60	s	0.1	F001	50
A283	Selector 1 Step Up	0 to 65535	---	1	F300	0
A284	Selector 1 Step Mode	0 to 1	---	1	F083	0 (Time-out)
A285	Selector 1 Acknowledge	0 to 65535	---	1	F300	0
A286	Selector 1 Bit0	0 to 65535	---	1	F300	0
A287	Selector 1 Bit1	0 to 65535	---	1	F300	0
A288	Selector 1 Bit2	0 to 65535	---	1	F300	0
A289	Selector 1 Bit Mode	0 to 1	---	1	F083	0 (Time-out)
A28A	Selector 1 Bit Acknowledge	0 to 65535	---	1	F300	0
A28B	Selector 1 Power Up Mode	0 to 2	---	1	F084	0 (Restore)
A28C	Selector 1 Target	0 to 2	---	1	F109	0 (Self-reset)
A28D	Selector 1 Events	0 to 1	---	1	F102	0 (Disabled)
A28E	Reserved (10 items)	---	---	1	F001	0
A298	...Repeated for Selector 2					
DNP/IEC Points (Read/Write Setting)						
A300	DNP/IEC 60870-5-104 Binary Input Points (256 items)	0 to 65535	---	1	F300	0
A400	DNP/IEC 60870-5-104 Analog Input Points (256 items)	0 to 65535	---	1	F300	0
Flexcurves C and D (Read/Write Setting)						
A600	FlexCurve C (120 items)	0 to 65535	ms	1	F011	0
A680	FlexCurve D (120 items)	0 to 65535	ms	1	F011	0
Non Volatile Latches (Read/Write Setting) (16 modules)						
A700	Non-Volatile Latch 1 Function	0 to 1	---	1	F102	0 (Disabled)
A701	Non-Volatile Latch 1 Type	0 to 1	---	1	F519	0 (Reset Dominant)
A702	Non-Volatile Latch 1 Set	0 to 65535	---	1	F300	0
A703	Non-Volatile Latch 1 Reset	0 to 65535	---	1	F300	0
A704	Non-Volatile Latch 1 Target	0 to 2	---	1	F109	0 (Self-reset)
A705	Non-Volatile Latch 1 Events	0 to 1	---	1	F102	0 (Disabled)
A706	Reserved (4 items)	---	---	---	F001	0
A70A	...Repeated for Non-Volatile Latch 2					
A714	...Repeated for Non-Volatile Latch 3					
A71E	...Repeated for Non-Volatile Latch 4					
A728	...Repeated for Non-Volatile Latch 5					
A732	...Repeated for Non-Volatile Latch 6					
A73C	...Repeated for Non-Volatile Latch 7					
A746	...Repeated for Non-Volatile Latch 8					
A750	...Repeated for Non-Volatile Latch 9					
A75A	...Repeated for Non-Volatile Latch 10					
A764	...Repeated for Non-Volatile Latch 11					
A76E	...Repeated for Non-Volatile Latch 12					
A778	...Repeated for Non-Volatile Latch 13					
A782	...Repeated for Non-Volatile Latch 14					
A78C	...Repeated for Non-Volatile Latch 15					
A796	...Repeated for Non-Volatile Latch 16					
Digital Counter (Read/Write Setting) (8 modules)						
A800	Digital Counter 1 Function	0 to 1	---	1	F102	0 (Disabled)
A801	Digital Counter 1 Name	---	---	---	F205	“Counter 1"
A807	Digital Counter 1 Units	---	---	---	F206	(none)

Table B–9: MODBUS MEMORY MAP (Sheet 36 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
A80A	Digital Counter 1 Block	0 to 65535	---	1	F300	0
A80B	Digital Counter 1 Up	0 to 65535	---	1	F300	0
A80C	Digital Counter 1 Down	0 to 65535	---	1	F300	0
A80D	Digital Counter 1 Preset	–2147483647 to 2147483647	---	1	F004	0
A80F	Digital Counter 1 Compare	–2147483647 to 2147483647	---	1	F004	0
A811	Digital Counter 1 Reset	0 to 65535	---	1	F300	0
A812	Digital Counter 1 Freeze/Reset	0 to 65535	---	1	F300	0
A813	Digital Counter 1 Freeze/Count	0 to 65535	---	1	F300	0
A814	Digital Counter 1 Set To Preset	0 to 65535	---	1	F300	0
A815	Reserved (11 items)	---	---	---	F001	0
A820	...Repeated for Digital Counter 2					
A840	...Repeated for Digital Counter 3					
A860	...Repeated for Digital Counter 4					
A880	...Repeated for Digital Counter 5					
A8A0	...Repeated for Digital Counter 6					
A8C0	...Repeated for Digital Counter 7					
A8E0	...Repeated for Digital Counter 8					
IEC 61850 received analog settings (read/write)						
AA00	IEC 61850 GOOSE analog 1 default value	–1000000 to 1000000	---	0.001	F060	1000
AA02	IEC 61850 GOOSE analog input 1 mode	0 to 1	---	1	F491	0 (Default Value)
AA03	IEC 61850 GOOSE analog input 1 units	---	---	---	F207	(none)
AA05	IEC 61850 GOOSE analog input 1 per-unit base	0 to 999999999.999	---	0.001	F060	1
AA07	...Repeated for IEC 61850 GOOSE analog input 2					
AA0E	...Repeated for IEC 61850 GOOSE analog input 3					
AA15	...Repeated for IEC 61850 GOOSE analog input 4					
AA1C	...Repeated for IEC 61850 GOOSE analog input 5					
AA23	...Repeated for IEC 61850 GOOSE analog input 6					
AA2A	...Repeated for IEC 61850 GOOSE analog input 7					
AA31	...Repeated for IEC 61850 GOOSE analog input 8					
AA38	...Repeated for IEC 61850 GOOSE analog input 9					
AA3F	...Repeated for IEC 61850 GOOSE analog input 10					
AA46	...Repeated for IEC 61850 GOOSE analog input 11					
AA4D	...Repeated for IEC 61850 GOOSE analog input 12					
AA54	...Repeated for IEC 61850 GOOSE analog input 13					
AA5B	...Repeated for IEC 61850 GOOSE analog input 14					
AA62	...Repeated for IEC 61850 GOOSE analog input 15					
AA69	...Repeated for IEC 61850 GOOSE analog input 16					
IEC 61850 GOOSE/GSSE Configuration (Read/Write Setting)						
AA80	Default GOOSE/GSSE Update Time	1 to 60	s	1	F001	60
AA81	IEC 61850 GSSE Function (GsEna)	0 to 1	---	1	F102	1 (Enabled)
AA82	IEC 61850 GSSE ID	---	---	---	F209	“GSSEOut”
AAA3	IEC 61850 GOOSE Function (GoEna)	0 to 1	---	1	F102	0 (Disabled)
AAA4	IEC 61850 GSSE Destination MAC Address	---	---	---	F072	0
AAA7	IEC 61850 Standard GOOSE ID	---	---	---	F209	“GOOSEOut”
AAC8	IEC 61850 Standard GOOSE Destination MAC Address	---	---	---	F072	0
AACB	IEC 61850 GOOSE VLAN Transmit Priority	0 to 7	---	1	F001	4
AACC	IEC 61850 GOOSE VLAN ID	0 to 4095	---	1	F001	0
AACD	IEC 61850 GOOSE ETYPE APPID	0 to 16383	---	1	F001	0
AACE	Reserved (2 items)	0 to 1	---	1	F001	0
IEC 61850 Server Configuration (Read/Write Settings/Commands)						
AAD0	TCP Port Number for the IEC 61850 / MMS Protocol	1 to 65535	---	1	F001	102
AAD1	IEC 61850 Logical Device Name	---	---	---	F213	“IECName”
AAE1	IEC 61850 Logical Device Instance	---	---	---	F213	“LDInst”

Table B–9: MODBUS MEMORY MAP (Sheet 37 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
AAF1	IEC 61850 LPHD Location	---	---	---	F204	“Location”
AB19	Include non-IEC 61850 Data	0 to 1	---	1	F102	0 (Disabled)
AB1A	IEC 61850 Server Data Scanning Function	0 to 1	---	1	F102	0 (Disabled)
AB1B	Command to Clear XCBR1 OpCnt (operation counter)	0 to 1	---	1	F126	0 (No)
AB1C	Command to Clear XCBR2 OpCnt (operation counter)	0 to 1	---	1	F126	0 (No)
AB1D	Reserved (15 items)					
IEC 61850 GGIO4 general analog configuration settings (read/write)						
AF00	Number of analog points in GGIO4	4 to 32	---	4	F001	4
IEC 61850 GGIO4 analog input points configuration settings (read/write)						
AF10	IEC 61850 GGIO4 analog input 1 value	---	---	---	F600	0
AF11	IEC 61850 GGIO4 analog input 1 deadband	0.001 to 100	%	0.001	F003	100000
AF13	IEC 61850 GGIO4 analog input 1 minimum	–1000000000000 to 1000000000000	---	0.001	F060	0
AF15	IEC 61850 GGIO4 analog input 1 maximum	–1000000000000 to 1000000000000	---	0.001	F060	1000000
AF17	...Repeated for IEC 61850 GGIO4 analog input 2					
AF1E	...Repeated for IEC 61850 GGIO4 analog input 3					
AF25	...Repeated for IEC 61850 GGIO4 analog input 4					
AF2C	...Repeated for IEC 61850 GGIO4 analog input 5					
AF33	...Repeated for IEC 61850 GGIO4 analog input 6					
AF3A	...Repeated for IEC 61850 GGIO4 analog input 7					
AF41	...Repeated for IEC 61850 GGIO4 analog input 8					
AF48	...Repeated for IEC 61850 GGIO4 analog input 9					
AF4F	...Repeated for IEC 61850 GGIO4 analog input 10					
AF56	...Repeated for IEC 61850 GGIO4 analog input 11					
AF5D	...Repeated for IEC 61850 GGIO4 analog input 12					
AF64	...Repeated for IEC 61850 GGIO4 analog input 13					
AF6B	...Repeated for IEC 61850 GGIO4 analog input 14					
AF72	...Repeated for IEC 61850 GGIO4 analog input 15					
AF79	...Repeated for IEC 61850 GGIO4 analog input 16					
AF80	...Repeated for IEC 61850 GGIO4 analog input 17					
AF87	...Repeated for IEC 61850 GGIO4 analog input 18					
AF8E	...Repeated for IEC 61850 GGIO4 analog input 19					
AF95	...Repeated for IEC 61850 GGIO4 analog input 20					
AF9C	...Repeated for IEC 61850 GGIO4 analog input 21					
AFA3	...Repeated for IEC 61850 GGIO4 analog input 22					
AFAA	...Repeated for IEC 61850 GGIO4 analog input 23					
AFB1	...Repeated for IEC 61850 GGIO4 analog input 24					
AFB8	...Repeated for IEC 61850 GGIO4 analog input 25					
AFBF	...Repeated for IEC 61850 GGIO4 analog input 26					
AFC6	...Repeated for IEC 61850 GGIO4 analog input 27					
AFCD	...Repeated for IEC 61850 GGIO4 analog input 28					
AFD4	...Repeated for IEC 61850 GGIO4 analog input 29					
AFDB	...Repeated for IEC 61850 GGIO4 analog input 30					
AFE2	...Repeated for IEC 61850 GGIO4 analog input 31					
AFE9	...Repeated for IEC 61850 GGIO4 analog input 32					
IEC 61850 Logical Node Name Prefixes (Read/Write Setting)						
AB30	IEC 61850 Logical Node LPHD1 Name Prefix	0 to 65534	---	1	F206	(None)
AB33	IEC 61850 Logical Node PIOCx Name Prefix (72 items)	0 to 65534	---	1	F206	(None)
AC0B	IEC 61850 Logical Node PTOCx Name Prefix (24 items)	0 to 65534	---	1	F206	(None)
AC53	IEC 61850 Logical Node PTUVx Name Prefix (12 items)	0 to 65534	---	1	F206	(None)
AC77	IEC 61850 Logical Node PTOVx Name Prefix (8 items)	0 to 65534	---	1	F206	(None)
AC8F	IEC 61850 Logical Node PDISx Name Prefix (10 items)	0 to 65534	---	1	F206	(None)
ACAD	IEC 61850 Logical Node RRBFx Name Prefix (24 items)	0 to 65534	---	1	F206	(None)
ACF5	IEC 61850 Logical Node RPSBx Name Prefix	0 to 65534	---	1	F206	(None)

Table B–9: MODBUS MEMORY MAP (Sheet 38 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
ACF8	IEC 61850 Logical Node RRECx Name Prefix (6 items)	0 to 65534	---	1	F206	(None)
AD0A	IEC 61850 Logical Node MMXUx Name Prefix (6 items)	0 to 65534	---	1	F206	(None)
AD1C	IEC 61850 Logical Node GGIOx Name Prefix (4 items)	0 to 65534	---	1	F206	(None)
AD28	IEC 61850 Logical Node RFLOx Name Prefix (5 items)	0 to 65534	---	1	F206	(None)
AD37	IEC 61850 Logical Node XCBRx Name Prefix (2 items)	0 to 65534	---	1	F206	(None)
AD3D	IEC 61850 Logical Node PTRCx Name Prefix (2 items)	0 to 65534	---	1	F206	(None)
AD43	IEC 61850 Logical Node PDIFx Name Prefix (4 items)	0 to 65534	---	1	F206	(None)
AD4F	IEC 61850 Logical Node MMXNx Name Prefix (37 items)	0 to 65534	---	1	F206	(None)
IEC 61850 MMXU Deadbands (Read/Write Setting) (6 modules)						
B0C0	IEC 61850 MMXU TotW Deadband 1	0.001 to 100	%	0.001	F003	10000
B0C2	IEC 61850 MMXU TotVAr Deadband 1	0.001 to 100	%	0.001	F003	10000
B0C4	IEC 61850 MMXU TotVA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0C6	IEC 61850 MMXU TotPF Deadband 1	0.001 to 100	%	0.001	F003	10000
B0C8	IEC 61850 MMXU Hz Deadband 1	0.001 to 100	%	0.001	F003	10000
B0CA	IEC 61850 MMXU PPV.phsAB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0CC	IEC 61850 MMXU PPV.phsBC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0CE	IEC 61850 MMXU PPV.phsCA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0D0	IEC 61850 MMXU PhV.phsADeadband 1	0.001 to 100	%	0.001	F003	10000
B0D2	IEC 61850 MMXU PhV.phsB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0D4	IEC 61850 MMXU PhV.phsC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0D6	IEC 61850 MMXU A.phsA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0D8	IEC 61850 MMXU A.phsB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0DA	IEC 61850 MMXU A.phsC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0DC	IEC 61850 MMXU A.neut Deadband 1	0.001 to 100	%	0.001	F003	10000
B0DE	IEC 61850 MMXU W.phsA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0E0	IEC 61850 MMXU W.phsB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0E2	IEC 61850 MMXU W.phsC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0E4	IEC 61850 MMXU VAr.phsA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0E6	IEC 61850 MMXU VAr.phsB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0E8	IEC 61850 MMXU VAr.phsC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0EA	IEC 61850 MMXU VA.phsA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0EC	IEC 61850 MMXU VA.phsB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0EE	IEC 61850 MMXU VA.phsC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0F0	IEC 61850 MMXU PF.phsA Deadband 1	0.001 to 100	%	0.001	F003	10000
B0F2	IEC 61850 MMXU PF.phsB Deadband 1	0.001 to 100	%	0.001	F003	10000
B0F4	IEC 61850 MMXU PF.phsC Deadband 1	0.001 to 100	%	0.001	F003	10000
B0F6	...Repeated for Deadband 2					
B12C	...Repeated for Deadband 3					
B162	...Repeated for Deadband 4					
B198	...Repeated for Deadband 5					
B1CE	...Repeated for Deadband 6					
IEC 61850 GGIO2 Control Configuration (Read/Write Setting) (64 modules)						
B240	IEC 61850 GGIO2.CF.SPCSO1.ctlModel Value	0 to 2	---	1	F001	2
B241	IEC 61850 GGIO2.CF.SPCSO2.ctlModel Value	0 to 2	---	1	F001	2
B242	IEC 61850 GGIO2.CF.SPCSO3.ctlModel Value	0 to 2	---	1	F001	2
B243	IEC 61850 GGIO2.CF.SPCSO4.ctlModel Value	0 to 2	---	1	F001	2
B244	IEC 61850 GGIO2.CF.SPCSO5.ctlModel Value	0 to 2	---	1	F001	2
B245	IEC 61850 GGIO2.CF.SPCSO6.ctlModel Value	0 to 2	---	1	F001	2
B246	IEC 61850 GGIO2.CF.SPCSO7.ctlModel Value	0 to 2	---	1	F001	2
B247	IEC 61850 GGIO2.CF.SPCSO8.ctlModel Value	0 to 2	---	1	F001	2
B248	IEC 61850 GGIO2.CF.SPCSO9.ctlModel Value	0 to 2	---	1	F001	2
B249	IEC 61850 GGIO2.CF.SPCSO10.ctlModel Value	0 to 2	---	1	F001	2
B24A	IEC 61850 GGIO2.CF.SPCSO11.ctlModel Value	0 to 2	---	1	F001	2
B24B	IEC 61850 GGIO2.CF.SPCSO12.ctlModel Value	0 to 2	---	1	F001	2

Table B–9: MODBUS MEMORY MAP (Sheet 39 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
B24C	IEC 61850 GGIO2.CF.SPCSO13.ctlModel Value	0 to 2	---	1	F001	2
B24D	IEC 61850 GGIO2.CF.SPCSO14.ctlModel Value	0 to 2	---	1	F001	2
B24E	IEC 61850 GGIO2.CF.SPCSO15.ctlModel Value	0 to 2	---	1	F001	2
B24F	IEC 61850 GGIO2.CF.SPCSO16.ctlModel Value	0 to 2	---	1	F001	2
B250	IEC 61850 GGIO2.CF.SPCSO17.ctlModel Value	0 to 2	---	1	F001	2
B251	IEC 61850 GGIO2.CF.SPCSO18.ctlModel Value	0 to 2	---	1	F001	2
B252	IEC 61850 GGIO2.CF.SPCSO19.ctlModel Value	0 to 2	---	1	F001	2
B253	IEC 61850 GGIO2.CF.SPCSO20.ctlModel Value	0 to 2	---	1	F001	2
B254	IEC 61850 GGIO2.CF.SPCSO21.ctlModel Value	0 to 2	---	1	F001	2
B255	IEC 61850 GGIO2.CF.SPCSO22.ctlModel Value	0 to 2	---	1	F001	2
B256	IEC 61850 GGIO2.CF.SPCSO23.ctlModel Value	0 to 2	---	1	F001	2
B257	IEC 61850 GGIO2.CF.SPCSO24.ctlModel Value	0 to 2	---	1	F001	2
B258	IEC 61850 GGIO2.CF.SPCSO25.ctlModel Value	0 to 2	---	1	F001	2
B259	IEC 61850 GGIO2.CF.SPCSO26.ctlModel Value	0 to 2	---	1	F001	2
B25A	IEC 61850 GGIO2.CF.SPCSO27.ctlModel Value	0 to 2	---	1	F001	2
B25B	IEC 61850 GGIO2.CF.SPCSO28.ctlModel Value	0 to 2	---	1	F001	2
B25C	IEC 61850 GGIO2.CF.SPCSO29.ctlModel Value	0 to 2	---	1	F001	2
B25D	IEC 61850 GGIO2.CF.SPCSO30.ctlModel Value	0 to 2	---	1	F001	2
B25E	IEC 61850 GGIO2.CF.SPCSO31.ctlModel Value	0 to 2	---	1	F001	2
B25F	IEC 61850 GGIO2.CF.SPCSO32.ctlModel Value	0 to 2	---	1	F001	2
B260	IEC 61850 GGIO2.CF.SPCSO33.ctlModel Value	0 to 2	---	1	F001	2
B261	IEC 61850 GGIO2.CF.SPCSO34.ctlModel Value	0 to 2	---	1	F001	2
B262	IEC 61850 GGIO2.CF.SPCSO35.ctlModel Value	0 to 2	---	1	F001	2
B263	IEC 61850 GGIO2.CF.SPCSO36.ctlModel Value	0 to 2	---	1	F001	2
B264	IEC 61850 GGIO2.CF.SPCSO37.ctlModel Value	0 to 2	---	1	F001	2
B265	IEC 61850 GGIO2.CF.SPCSO38.ctlModel Value	0 to 2	---	1	F001	2
B266	IEC 61850 GGIO2.CF.SPCSO39.ctlModel Value	0 to 2	---	1	F001	2
B267	IEC 61850 GGIO2.CF.SPCSO40.ctlModel Value	0 to 2	---	1	F001	2
B268	IEC 61850 GGIO2.CF.SPCSO41.ctlModel Value	0 to 2	---	1	F001	2
B269	IEC 61850 GGIO2.CF.SPCSO42.ctlModel Value	0 to 2	---	1	F001	2
B26A	IEC 61850 GGIO2.CF.SPCSO43.ctlModel Value	0 to 2	---	1	F001	2
B26B	IEC 61850 GGIO2.CF.SPCSO44.ctlModel Value	0 to 2	---	1	F001	2
B26C	IEC 61850 GGIO2.CF.SPCSO45.ctlModel Value	0 to 2	---	1	F001	2
B26D	IEC 61850 GGIO2.CF.SPCSO46.ctlModel Value	0 to 2	---	1	F001	2
B26E	IEC 61850 GGIO2.CF.SPCSO47.ctlModel Value	0 to 2	---	1	F001	2
B26F	IEC 61850 GGIO2.CF.SPCSO48.ctlModel Value	0 to 2	---	1	F001	2
B270	IEC 61850 GGIO2.CF.SPCSO49.ctlModel Value	0 to 2	---	1	F001	2
B271	IEC 61850 GGIO2.CF.SPCSO50.ctlModel Value	0 to 2	---	1	F001	2
B272	IEC 61850 GGIO2.CF.SPCSO51.ctlModel Value	0 to 2	---	1	F001	2
B273	IEC 61850 GGIO2.CF.SPCSO52.ctlModel Value	0 to 2	---	1	F001	2
B274	IEC 61850 GGIO2.CF.SPCSO53.ctlModel Value	0 to 2	---	1	F001	2
B275	IEC 61850 GGIO2.CF.SPCSO54.ctlModel Value	0 to 2	---	1	F001	2
B276	IEC 61850 GGIO2.CF.SPCSO55.ctlModel Value	0 to 2	---	1	F001	2
B277	IEC 61850 GGIO2.CF.SPCSO56.ctlModel Value	0 to 2	---	1	F001	2
B278	IEC 61850 GGIO2.CF.SPCSO57.ctlModel Value	0 to 2	---	1	F001	2
B279	IEC 61850 GGIO2.CF.SPCSO58.ctlModel Value	0 to 2	---	1	F001	2
B27A	IEC 61850 GGIO2.CF.SPCSO59.ctlModel Value	0 to 2	---	1	F001	2
B27B	IEC 61850 GGIO2.CF.SPCSO60.ctlModel Value	0 to 2	---	1	F001	2
B27C	IEC 61850 GGIO2.CF.SPCSO61.ctlModel Value	0 to 2	---	1	F001	2
B27D	IEC 61850 GGIO2.CF.SPCSO62.ctlModel Value	0 to 2	---	1	F001	2
B27E	IEC 61850 GGIO2.CF.SPCSO63.ctlModel Value	0 to 2	---	1	F001	2
IEC 61850 Report Settings (Read/Write Setting) (14 modules)						
B280	IEC 61850 Report Control 1 RptID	---	---	---	F209	
B2A1	IEC 61850 Report Control 1 OptFlds	0 to 65535	---	1	F001	0

Table B–9: MODBUS MEMORY MAP (Sheet 40 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
B2A2	IEC 61850 Report Control 1 BufTm	0 to 4294967295	---	1	F003	0
B2A4	IEC 61850 Report Control 1 TrgOps	0 to 65535	---	1	F001	0
B2A5	IEC 61850 Report Control 1 IntgPd	0 to 4294967295	---	1	F003	0
B2A7	...Repeated for Report 2					
B2CE	...Repeated for Report 3					
B2F5	...Repeated for Report 4					
B31C	...Repeated for Report 5					
B343	...Repeated for Report 6					
B36A	...Repeated for Report 7					
B391	...Repeated for Report 8					
B3B8	...Repeated for Report 9					
B3DF	...Repeated for Report 10					
B406	...Repeated for Report 11					
B42D	...Repeated for Report 12					
B454	...Repeated for Report 13					
B47B	...Repeated for Report 14					
B4A2	...Repeated for Report 15					
B4C9	...Repeated for Report 16					
IEC 61850 GGIO1 Configuration Settings (Read/Write Setting)						
B500	Number of Status Indications in GGIO1	8 to 128	---	8	F001	8
B501	IEC 61850 GGIO1 Indication operands (128 items)	---	---	1	F300	0
IEC 61850 Configurable GOOSE Transmission (Read/Write Setting) (8 modules)						
B5A0	IEC 61850 Configurable GOOSE Function	0 to 1	---	1	F102	0 (None)
B5A1	IEC 61850 Configurable GOOSE ID	---	---	---	F209	“GOOSEOut_x_”
B5C2	Configurable GOOSE Destination MAC Address	---	---	---	F072	0
B5C5	IEC 61850 Configurable GOOSE VLAN Transmit Priority	0 to 7	---	1	F001	4
B5C6	IEC 61850 Configurable GOOSE VLAN ID	0 to 4095	---	1	F001	0
B5C7	IEC 61850 Configurable GOOSE ETYPE APPID	0 to 16383	---	1	F001	0
B5C8	IEC 61850 Configurable GOOSE ConfRev	1 to 4294967295	---	1	F003	1
B5CA	Configurable GOOSE Dataset Items for Transmission	0 to 256	---	1	F232	0 (None)
B60A	...Repeated for Module 2					
B674	...Repeated for Module 3					
B6DE	...Repeated for Module 4					
B748	...Repeated for Module 5					
B7B2	...Repeated for Module 6					
B81C	...Repeated for Module 7					
B886	...Repeated for Module 8					
IEC 61850 Configurable GOOSE Reception (Read/Write Setting) (8 modules)						
B900	Configurable GOOSE Dataset Items for Transmission	0 to 128	---	1	F233	0 (None)
B940	...Repeated for Module 2					
B980	...Repeated for Module 3					
B9C0	...Repeated for Module 4					
BA00	...Repeated for Module 5					
BA40	...Repeated for Module 6					
BA80	...Repeated for Module 7					
BAC0	...Repeated for Module 8					
Contact Inputs (Read/Write Setting) (96 modules)						
BB00	Contact Input 1 Name	---	---	---	F205	“Cont Ip 1“
BB06	Contact Input 1 Events	0 to 1	---	1	F102	0 (Disabled)
BB07	Contact Input 1 Debounce Time	0 to 16	ms	0.5	F001	20
BB08	...Repeated for Contact Input 2					
BB10	...Repeated for Contact Input 3					
BB18	...Repeated for Contact Input 4					
BB20	...Repeated for Contact Input 5					

Table B–9: MODBUS MEMORY MAP (Sheet 41 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
BB28	...Repeated for Contact Input 6					
BB30	...Repeated for Contact Input 7					
BB38	...Repeated for Contact Input 8					
BB40	...Repeated for Contact Input 9					
BB48	...Repeated for Contact Input 10					
BB50	...Repeated for Contact Input 11					
BB58	...Repeated for Contact Input 12					
BB60	...Repeated for Contact Input 13					
BB68	...Repeated for Contact Input 14					
BB70	...Repeated for Contact Input 15					
BB78	...Repeated for Contact Input 16					
BB80	...Repeated for Contact Input 17					
BB88	...Repeated for Contact Input 18					
BB90	...Repeated for Contact Input 19					
BB98	...Repeated for Contact Input 20					
BBA0	...Repeated for Contact Input 21					
BBA8	...Repeated for Contact Input 22					
BBB0	...Repeated for Contact Input 23					
BBB8	...Repeated for Contact Input 24					
BBC0	...Repeated for Contact Input 25					
BBC8	...Repeated for Contact Input 26					
BBD0	...Repeated for Contact Input 27					
BBD8	...Repeated for Contact Input 28					
BBE0	...Repeated for Contact Input 29					
BBE8	...Repeated for Contact Input 30					
BBF0	...Repeated for Contact Input 31					
BBF8	...Repeated for Contact Input 32					
BC00	...Repeated for Contact Input 33					
BC08	...Repeated for Contact Input 34					
BC10	...Repeated for Contact Input 35					
BC18	...Repeated for Contact Input 36					
BC20	...Repeated for Contact Input 37					
BC28	...Repeated for Contact Input 38					
BC30	...Repeated for Contact Input 39					
BC38	...Repeated for Contact Input 40					
BC40	...Repeated for Contact Input 41					
BC48	...Repeated for Contact Input 42					
BC50	...Repeated for Contact Input 43					
BC58	...Repeated for Contact Input 44					
BC60	...Repeated for Contact Input 45					
BC68	...Repeated for Contact Input 46					
BC70	...Repeated for Contact Input 47					
BC78	...Repeated for Contact Input 48					
BC80	...Repeated for Contact Input 49					
BC88	...Repeated for Contact Input 50					
BC90	...Repeated for Contact Input 51					
BC98	...Repeated for Contact Input 52					
BCA0	...Repeated for Contact Input 53					
BCA8	...Repeated for Contact Input 54					
BCB0	...Repeated for Contact Input 55					
BCB8	...Repeated for Contact Input 56					
BCC0	...Repeated for Contact Input 57					
BCC8	...Repeated for Contact Input 58					
BCD0	...Repeated for Contact Input 59					

Table B–9: MODBUS MEMORY MAP (Sheet 42 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
BCD8	...Repeated for Contact Input 60					
BCE0	...Repeated for Contact Input 61					
BCE8	...Repeated for Contact Input 62					
BCF0	...Repeated for Contact Input 63					
BCF8	...Repeated for Contact Input 64					
BD00	...Repeated for Contact Input 65					
BD08	...Repeated for Contact Input 66					
BD10	...Repeated for Contact Input 67					
BD18	...Repeated for Contact Input 68					
BD20	...Repeated for Contact Input 69					
BD28	...Repeated for Contact Input 70					
BD30	...Repeated for Contact Input 71					
BD38	...Repeated for Contact Input 72					
BD40	...Repeated for Contact Input 73					
BD48	...Repeated for Contact Input 74					
BD50	...Repeated for Contact Input 75					
BD58	...Repeated for Contact Input 76					
BD60	...Repeated for Contact Input 77					
BD68	...Repeated for Contact Input 78					
BD70	...Repeated for Contact Input 79					
BD78	...Repeated for Contact Input 80					
BD80	...Repeated for Contact Input 81					
BD88	...Repeated for Contact Input 82					
BD90	...Repeated for Contact Input 83					
BD98	...Repeated for Contact Input 84					
BDA0	...Repeated for Contact Input 85					
BDA8	...Repeated for Contact Input 86					
BDB0	...Repeated for Contact Input 87					
BDB8	...Repeated for Contact Input 88					
BDC0	...Repeated for Contact Input 89					
BDC8	...Repeated for Contact Input 90					
BDD0	...Repeated for Contact Input 91					
BDD8	...Repeated for Contact Input 92					
BDE0	...Repeated for Contact Input 93					
BDE8	...Repeated for Contact Input 94					
BDF0	...Repeated for Contact Input 95					
BDF8	...Repeated for Contact Input 96					
Contact Input Thresholds (Read/Write Setting)						
BE00	Contact Input *n* Threshold, *n* = 1 to 24 (24 items)	0 to 3	---	1	F128	1 (33 Vdc)
Virtual Inputs (Read/Write Setting) (64 modules)						
BE30	Virtual Input 1 Function	0 to 1	---	1	F102	0 (Disabled)
BE31	Virtual Input 1 Name	---	---	---	F205	"Virt Ip 1"
BE37	Virtual Input 1 Programmed Type	0 to 1	---	1	F127	0 (Latched)
BE38	Virtual Input 1 Events	0 to 1	---	1	F102	0 (Disabled)
BE39	Reserved (3 items)	---	---	---	F001	0
BE3C	...Repeated for Virtual Input 2					
BE48	...Repeated for Virtual Input 3					
BE54	...Repeated for Virtual Input 4					
BE60	...Repeated for Virtual Input 5					
BE6C	...Repeated for Virtual Input 6					
BE78	...Repeated for Virtual Input 7					
BE84	...Repeated for Virtual Input 8					
BE90	...Repeated for Virtual Input 9					
BE9C	...Repeated for Virtual Input 10					

Table B–9: MODBUS MEMORY MAP (Sheet 43 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
BEA8	...Repeated for Virtual Input 11					
BEB4	...Repeated for Virtual Input 12					
BEC0	...Repeated for Virtual Input 13					
BECC	...Repeated for Virtual Input 14					
BED8	...Repeated for Virtual Input 15					
BEE4	...Repeated for Virtual Input 16					
BEF0	...Repeated for Virtual Input 17					
BEFC	...Repeated for Virtual Input 18					
BF08	...Repeated for Virtual Input 19					
BF14	...Repeated for Virtual Input 20					
BF20	...Repeated for Virtual Input 21					
BF2C	...Repeated for Virtual Input 22					
BF38	...Repeated for Virtual Input 23					
BF44	...Repeated for Virtual Input 24					
BF50	...Repeated for Virtual Input 25					
BF5C	...Repeated for Virtual Input 26					
BF68	...Repeated for Virtual Input 27					
BF74	...Repeated for Virtual Input 28					
BF80	...Repeated for Virtual Input 29					
BF8C	...Repeated for Virtual Input 30					
BF98	...Repeated for Virtual Input 31					
BFA4	...Repeated for Virtual Input 32					
BFB0	...Repeated for Virtual Input 33					
BFBC	...Repeated for Virtual Input 34					
BFC8	...Repeated for Virtual Input 35					
BFD4	...Repeated for Virtual Input 36					
BFE0	...Repeated for Virtual Input 37					
BFEC	...Repeated for Virtual Input 38					
BFF8	...Repeated for Virtual Input 39					
C004	...Repeated for Virtual Input 40					
C010	...Repeated for Virtual Input 41					
C01C	...Repeated for Virtual Input 42					
C028	...Repeated for Virtual Input 43					
C034	...Repeated for Virtual Input 44					
C040	...Repeated for Virtual Input 45					
C04C	...Repeated for Virtual Input 46					
C058	...Repeated for Virtual Input 47					
C064	...Repeated for Virtual Input 48					
C070	...Repeated for Virtual Input 49					
C07C	...Repeated for Virtual Input 50					
C088	...Repeated for Virtual Input 51					
C094	...Repeated for Virtual Input 52					
C0A0	...Repeated for Virtual Input 53					
C0AC	...Repeated for Virtual Input 54					
C0B8	...Repeated for Virtual Input 55					
C0C4	...Repeated for Virtual Input 56					
C0D0	...Repeated for Virtual Input 57					
C0DC	...Repeated for Virtual Input 58					
C0E8	...Repeated for Virtual Input 59					
C0F4	...Repeated for Virtual Input 60					
C100	...Repeated for Virtual Input 61					
C10C	...Repeated for Virtual Input 62					
C118	...Repeated for Virtual Input 63					
C124	...Repeated for Virtual Input 64					

Table B–9: MODBUS MEMORY MAP (Sheet 44 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Virtual Outputs (Read/Write Setting) (96 modules)						
C130	Virtual Output 1 Name	---	---	---	F205	"Virt Op 1 "
C136	Virtual Output 1 Events	0 to 1	---	1	F102	0 (Disabled)
C137	Reserved	---	---	---	F001	0
C138	...Repeated for Virtual Output 2					
C140	...Repeated for Virtual Output 3					
C148	...Repeated for Virtual Output 4					
C150	...Repeated for Virtual Output 5					
C158	...Repeated for Virtual Output 6					
C160	...Repeated for Virtual Output 7					
C168	...Repeated for Virtual Output 8					
C170	...Repeated for Virtual Output 9					
C178	...Repeated for Virtual Output 10					
C180	...Repeated for Virtual Output 11					
C188	...Repeated for Virtual Output 12					
C190	...Repeated for Virtual Output 13					
C198	...Repeated for Virtual Output 14					
C1A0	...Repeated for Virtual Output 15					
C1A8	...Repeated for Virtual Output 16					
C1B0	...Repeated for Virtual Output 17					
C1B8	...Repeated for Virtual Output 18					
C1C0	...Repeated for Virtual Output 19					
C1C8	...Repeated for Virtual Output 20					
C1D0	...Repeated for Virtual Output 21					
C1D8	...Repeated for Virtual Output 22					
C1E0	...Repeated for Virtual Output 23					
C1E8	...Repeated for Virtual Output 24					
C1F0	...Repeated for Virtual Output 25					
C1F8	...Repeated for Virtual Output 26					
C200	...Repeated for Virtual Output 27					
C208	...Repeated for Virtual Output 28					
C210	...Repeated for Virtual Output 29					
C218	...Repeated for Virtual Output 30					
C220	...Repeated for Virtual Output 31					
C228	...Repeated for Virtual Output 32					
C230	...Repeated for Virtual Output 33					
C238	...Repeated for Virtual Output 34					
C240	...Repeated for Virtual Output 35					
C248	...Repeated for Virtual Output 36					
C250	...Repeated for Virtual Output 37					
C258	...Repeated for Virtual Output 38					
C260	...Repeated for Virtual Output 39					
C268	...Repeated for Virtual Output 40					
C270	...Repeated for Virtual Output 41					
C278	...Repeated for Virtual Output 42					
C280	...Repeated for Virtual Output 43					
C288	...Repeated for Virtual Output 44					
C290	...Repeated for Virtual Output 45					
C298	...Repeated for Virtual Output 46					
C2A0	...Repeated for Virtual Output 47					
C2A8	...Repeated for Virtual Output 48					
C2B0	...Repeated for Virtual Output 49					
C2B8	...Repeated for Virtual Output 50					
C2C0	...Repeated for Virtual Output 51					

Table B–9: MODBUS MEMORY MAP (Sheet 45 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C2C8	...Repeated for Virtual Output 52					
C2D0	...Repeated for Virtual Output 53					
C2D8	...Repeated for Virtual Output 54					
C2E0	...Repeated for Virtual Output 55					
C2E8	...Repeated for Virtual Output 56					
C2F0	...Repeated for Virtual Output 57					
C2F8	...Repeated for Virtual Output 58					
C300	...Repeated for Virtual Output 59					
C308	...Repeated for Virtual Output 60					
C310	...Repeated for Virtual Output 61					
C318	...Repeated for Virtual Output 62					
C320	...Repeated for Virtual Output 63					
C328	...Repeated for Virtual Output 64					
C330	...Repeated for Virtual Output 65					
C338	...Repeated for Virtual Output 66					
C340	...Repeated for Virtual Output 67					
C348	...Repeated for Virtual Output 68					
C350	...Repeated for Virtual Output 69					
C358	...Repeated for Virtual Output 70					
C360	...Repeated for Virtual Output 71					
C368	...Repeated for Virtual Output 72					
C370	...Repeated for Virtual Output 73					
C378	...Repeated for Virtual Output 74					
C380	...Repeated for Virtual Output 75					
C388	...Repeated for Virtual Output 76					
C390	...Repeated for Virtual Output 77					
C398	...Repeated for Virtual Output 78					
C3A0	...Repeated for Virtual Output 79					
C3A8	...Repeated for Virtual Output 80					
C3B0	...Repeated for Virtual Output 81					
C3B8	...Repeated for Virtual Output 82					
C3C0	...Repeated for Virtual Output 83					
C3C8	...Repeated for Virtual Output 84					
C3D0	...Repeated for Virtual Output 85					
C3D8	...Repeated for Virtual Output 86					
C3E0	...Repeated for Virtual Output 87					
C3E8	...Repeated for Virtual Output 88					
C3F0	...Repeated for Virtual Output 89					
C3F8	...Repeated for Virtual Output 90					
C400	...Repeated for Virtual Output 91					
C408	...Repeated for Virtual Output 92					
C410	...Repeated for Virtual Output 93					
C418	...Repeated for Virtual Output 94					
C420	...Repeated for Virtual Output 95					
C428	...Repeated for Virtual Output 96					
Mandatory (Read/Write Setting)						
C430	Test Mode Function	0 to 1	---	1	F102	0 (Disabled)
C431	Force VFD and LED	0 to 1	---	1	F126	0 (No)
C432	Test Mode Initiate	0 to 65535	---	1	F300	1
Clear commands (read/write)						
C433	Clear All Relay Records Command	0 to 1	---	1	F126	0 (No)
Contact Outputs (Read/Write Setting) (64 modules)						
C440	Contact Output 1 Name	---	---	---	F205	"Cont Op 1"
C446	Contact Output 1 Operation	0 to 65535	---	1	F300	0

Table B–9: MODBUS MEMORY MAP (Sheet 46 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C447	Contact Output 1 Seal In	0 to 65535	---	1	F300	0
C448	Latching Output 1 Reset	0 to 65535	---	1	F300	0
C449	Contact Output 1 Events	0 to 1	---	1	F102	1 (Enabled)
C44A	Latching Output 1 Type	0 to 1	---	1	F090	0 (Operate-dominant)
C44B	Reserved	---	---	---	F001	0
C44C	...Repeated for Contact Output 2					
C458	...Repeated for Contact Output 3					
C464	...Repeated for Contact Output 4					
C470	...Repeated for Contact Output 5					
C47C	...Repeated for Contact Output 6					
C488	...Repeated for Contact Output 7					
C494	...Repeated for Contact Output 8					
C4A0	...Repeated for Contact Output 9					
C4AC	...Repeated for Contact Output 10					
C4B8	...Repeated for Contact Output 11					
C4C4	...Repeated for Contact Output 12					
C4D0	...Repeated for Contact Output 13					
C4DC	...Repeated for Contact Output 14					
C4E8	...Repeated for Contact Output 15					
C4F4	...Repeated for Contact Output 16					
C500	...Repeated for Contact Output 17					
C50C	...Repeated for Contact Output 18					
C518	...Repeated for Contact Output 19					
C524	...Repeated for Contact Output 20					
C530	...Repeated for Contact Output 21					
C53C	...Repeated for Contact Output 22					
C548	...Repeated for Contact Output 23					
C554	...Repeated for Contact Output 24					
C560	...Repeated for Contact Output 25					
C56C	...Repeated for Contact Output 26					
C578	...Repeated for Contact Output 27					
C584	...Repeated for Contact Output 28					
C590	...Repeated for Contact Output 29					
C59C	...Repeated for Contact Output 30					
C5A8	...Repeated for Contact Output 31					
C5B4	...Repeated for Contact Output 32					
C5C0	...Repeated for Contact Output 33					
C5CC	...Repeated for Contact Output 34					
C5D8	...Repeated for Contact Output 35					
C5E4	...Repeated for Contact Output 36					
C5F0	...Repeated for Contact Output 37					
C5FC	...Repeated for Contact Output 38					
C608	...Repeated for Contact Output 39					
C614	...Repeated for Contact Output 40					
C620	...Repeated for Contact Output 41					
C62C	...Repeated for Contact Output 42					
C638	...Repeated for Contact Output 43					
C644	...Repeated for Contact Output 44					
C650	...Repeated for Contact Output 45					
C65C	...Repeated for Contact Output 46					
C668	...Repeated for Contact Output 47					
C674	...Repeated for Contact Output 48					
C680	...Repeated for Contact Output 49					
C68C	...Repeated for Contact Output 50					

Table B–9: MODBUS MEMORY MAP (Sheet 47 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C698	...Repeated for Contact Output 51					
C6A4	...Repeated for Contact Output 52					
C6B0	...Repeated for Contact Output 53					
C6BC	...Repeated for Contact Output 54					
C6C8	...Repeated for Contact Output 55					
C6D4	...Repeated for Contact Output 56					
C6E0	...Repeated for Contact Output 57					
C6EC	...Repeated for Contact Output 58					
C6F8	...Repeated for Contact Output 59					
C704	...Repeated for Contact Output 60					
C710	...Repeated for Contact Output 61					
C71C	...Repeated for Contact Output 62					
C728	...Repeated for Contact Output 63					
C734	...Repeated for Contact Output 64					
Reset (Read/Write Setting)						
C750	FlexLogic™ operand which initiates a reset	0 to 65535	---	1	F300	0
Control Pushbuttons (Read/Write Setting) (7 modules)						
C760	Control Pushbutton 1 Function	0 to 1	---	1	F102	0 (Disabled)
C761	Control Pushbutton 1 Events	0 to 1	---	1	F102	0 (Disabled)
C762	...Repeated for Control Pushbutton 2					
C764	...Repeated for Control Pushbutton 3					
C766	...Repeated for Control Pushbutton 4					
C768	...Repeated for Control Pushbutton 5					
C76A	...Repeated for Control Pushbutton 6					
C76C	...Repeated for Control Pushbutton 7					
Clear Records (Read/Write Setting)						
C770	Clear Fault Reports operand	0 to 65535	---	1	F300	0
C772	Clear Event Records operand	0 to 65535	---	1	F300	0
C773	Clear Oscillography operand	0 to 65535	---	1	F300	0
C774	Clear Data Logger operand	0 to 65535	---	1	F300	0
C775	Clear Breaker 1 Arcing Current operand	0 to 65535	---	1	F300	0
C776	Clear Breaker 2 Arcing Current operand	0 to 65535	---	1	F300	0
C77C	Clear Channel Status operand	0 to 65535	---	1	F300	0
C77D	Clear Energy operand	0 to 65535	---	1	F300	0
C77F	Clear Unauthorized Access operand	0 to 65535	---	1	F300	0
C782	Reserved (13 items)	---	---	---	F001	0
Force Contact Inputs/Outputs (Read/Write Settings)						
C7A0	Force Contact Input *x* State (96 items)	0 to 2	---	1	F144	0 (Disabled)
C800	Force Contact Output *x* State (64 items)	0 to 3	---	1	F131	0 (Disabled)
Direct Inputs/Outputs (Read/Write Setting)						
C880	Direct Device ID	1 to 16	---	1	F001	1
C881	Direct I/O Channel 1 Ring Configuration Function	0 to 1	---	1	F126	0 (No)
C882	Platform Direct I/O Data Rate	64 to 128	kbps	64	F001	64
C883	Direct I/O Channel 2 Ring Configuration Function	0 to 1	---	1	F126	0 (No)
C884	Platform Direct I/O Crossover Function	0 to 1	---	1	F102	0 (Disabled)
Direct input/output commands (Read/Write Command)						
C888	Direct input/output clear counters command	0 to 1	---	1	F126	0 (No)
Direct inputs (Read/Write Setting) (96 modules)						
C890	Direct Input 1 Device Number	0 to 16	---	1	F001	0
C891	Direct Input 1 Number	0 to 96	---	1	F001	0
C892	Direct Input 1 Default State	0 to 3	---	1	F086	0 (Off)
C893	Direct Input 1 Events	0 to 1	---	1	F102	0 (Disabled)
C894	...Repeated for Direct Input 2					
C898	...Repeated for Direct Input 3					

Table B–9: MODBUS MEMORY MAP (Sheet 48 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C89C	...Repeated for Direct Input 4					
C8A0	...Repeated for Direct Input 5					
C8A4	...Repeated for Direct Input 6					
C8A8	...Repeated for Direct Input 7					
C8AC	...Repeated for Direct Input 8					
C8B0	...Repeated for Direct Input 9					
C8B4	...Repeated for Direct Input 10					
C8B8	...Repeated for Direct Input 11					
C8BC	...Repeated for Direct Input 12					
C8C0	...Repeated for Direct Input 13					
C8C4	...Repeated for Direct Input 14					
C8C8	...Repeated for Direct Input 15					
C8CC	...Repeated for Direct Input 16					
C8D0	...Repeated for Direct Input 17					
C8D4	...Repeated for Direct Input 18					
C8D8	...Repeated for Direct Input 19					
C8DC	...Repeated for Direct Input 20					
C8E0	...Repeated for Direct Input 21					
C8E4	...Repeated for Direct Input 22					
C8E8	...Repeated for Direct Input 23					
C8EC	...Repeated for Direct Input 24					
C8F0	...Repeated for Direct Input 25					
C8F4	...Repeated for Direct Input 26					
C8F8	...Repeated for Direct Input 27					
C8FC	...Repeated for Direct Input 28					
C900	...Repeated for Direct Input 29					
C904	...Repeated for Direct Input 30					
C908	...Repeated for Direct Input 31					
C90C	...Repeated for Direct Input 32					
Platform Direct Outputs (Read/Write Setting) (96 modules)						
CA10	Direct Output 1 Operand	0 to 65535	---	1	F300	0
CA11	Direct Output 1 Events	0 to 1	---	1	F102	0 (Disabled)
CA12	...Repeated for Direct Output 2					
CA14	...Repeated for Direct Output 3					
CA16	...Repeated for Direct Output 4					
CA18	...Repeated for Direct Output 5					
CA1A	...Repeated for Direct Output 6					
CA1C	...Repeated for Direct Output 7					
CA1E	...Repeated for Direct Output 8					
CA20	...Repeated for Direct Output 9					
CA22	...Repeated for Direct Output 10					
CA24	...Repeated for Direct Output 11					
CA26	...Repeated for Direct Output 12					
CA28	...Repeated for Direct Output 13					
CA2A	...Repeated for Direct Output 14					
CA2C	...Repeated for Direct Output 15					
CA2E	...Repeated for Direct Output 16					
CA30	...Repeated for Direct Output 17					
CA32	...Repeated for Direct Output 18					
CA34	...Repeated for Direct Output 19					
CA36	...Repeated for Direct Output 20					
CA38	...Repeated for Direct Output 21					
CA3A	...Repeated for Direct Output 22					
CA3C	...Repeated for Direct Output 23					

Table B–9: MODBUS MEMORY MAP (Sheet 49 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
CA3E	...Repeated for Direct Output 24					
CA40	...Repeated for Direct Output 25					
CA42	...Repeated for Direct Output 26					
CA44	...Repeated for Direct Output 27					
CA46	...Repeated for Direct Output 28					
CA48	...Repeated for Direct Output 29					
CA4A	...Repeated for Direct Output 30					
CA4C	...Repeated for Direct Output 31					
CA4E	...Repeated for Direct Output 32					
Direct Input/Output Alarms (Read/Write Setting)						
CAD0	Direct Input/Output Channel 1 CRC Alarm Function	0 to 1	---	1	F102	0 (Disabled)
CAD1	Direct I/O Channel 1 CRC Alarm Message Count	100 to 10000	---	1	F001	600
CAD2	Direct Input/Output Channel 1 CRC Alarm Threshold	1 to 1000	---	1	F001	10
CAD3	Direct Input/Output Channel 1 CRC Alarm Events	0 to 1	---	1	F102	0 (Disabled)
CAD4	Reserved (4 items)	1 to 1000	---	1	F001	10
CAD8	Direct Input/Output Channel 2 CRC Alarm Function	0 to 1	---	1	F102	0 (Disabled)
CAD9	Direct I/O Channel 2 CRC Alarm Message Count	100 to 10000	---	1	F001	600
CADA	Direct Input/Output Channel 2 CRC Alarm Threshold	1 to 1000	---	1	F001	10
CADB	Direct Input/Output Channel 2 CRC Alarm Events	0 to 1	---	1	F102	0 (Disabled)
CADC	Reserved (4 items)	1 to 1000	---	1	F001	10
CAE0	Direct I/O Ch 1 Unreturned Messages Alarm Function	0 to 1	---	1	F102	0 (Disabled)
CAE1	Direct I/O Ch 1 Unreturned Messages Alarm Msg Count	100 to 10000	---	1	F001	600
CAE2	Direct I/O Ch 1 Unreturned Messages Alarm Threshold	1 to 1000	---	1	F001	10
CAE3	Direct I/O Ch 1 Unreturned Messages Alarm Events	0 to 1	---	1	F102	0 (Disabled)
CAE4	Reserved (4 items)	1 to 1000	---	1	F001	10
CAE8	Direct IO Ch 2 Unreturned Messages Alarm Function	0 to 1	---	1	F102	0 (Disabled)
CAE9	Direct I/O Ch 2 Unreturned Messages Alarm Msg Count	100 to 10000	---	1	F001	600
CAEA	Direct I/O Ch 2 Unreturned Messages Alarm Threshold	1 to 1000	---	1	F001	10
CAEB	Direct I/O Channel 2 Unreturned Messages Alarm Events	0 to 1	---	1	F102	0 (Disabled)
CAEC	Reserved (4 items)	---	---	1	F001	10
Remote Devices (Read/Write Setting) (16 modules)						
CB00	Remote Device 1 GSSE/GOOSE Application ID	---	---	---	F209	“Remote Device 1“
CB21	Remote Device 1 GOOSE Ethernet APPID	0 to 16383	---	1	F001	0
CB22	Remote Device 1 GOOSE Dataset	0 to 8	---	1	F184	0 (Fixed)
CB23	...Repeated for Device 2					
CB46	...Repeated for Device 3					
CB69	...Repeated for Device 4					
CB8C	...Repeated for Device 5					
CBAF	...Repeated for Device 6					
CBD2	...Repeated for Device 7					
CBF5	...Repeated for Device 8					
CC18	...Repeated for Device 9					
CC3B	...Repeated for Device 10					
CC5E	...Repeated for Device 11					
CC81	...Repeated for Device 12					
CCA4	...Repeated for Device 13					
CCC7	...Repeated for Device 14					
CCEA	...Repeated for Device 15					
CD0D	...Repeated for Device 16					
Remote Inputs (Read/Write Setting) (64 modules)						
CFA0	Remote Input 1 Device	1 to 16	---	1	F001	1
CFA1	Remote Input 1 Item	0 to 64	---	1	F156	0 (None)
CFA2	Remote Input 1 Default State	0 to 3	---	1	F086	0 (Off)
CFA3	Remote Input 1 Events	0 to 1	---	1	F102	0 (Disabled)

Table B–9: MODBUS MEMORY MAP (Sheet 50 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
CFA4	Remote Input 1 Name	1 to 64	---	1	F205	“Rem Ip 1”
CFAA	...Repeated for Remote Input 2					
CFB4	...Repeated for Remote Input 3					
CFBE	...Repeated for Remote Input 4					
CFC8	...Repeated for Remote Input 5					
CFD2	...Repeated for Remote Input 6					
CFDC	...Repeated for Remote Input 7					
CFE6	...Repeated for Remote Input 8					
CFF0	...Repeated for Remote Input 9					
CFFA	...Repeated for Remote Input 10					
D004	...Repeated for Remote Input 11					
D00E	...Repeated for Remote Input 12					
D018	...Repeated for Remote Input 13					
D022	...Repeated for Remote Input 14					
D02C	...Repeated for Remote Input 15					
D036	...Repeated for Remote Input 16					
D040	...Repeated for Remote Input 17					
D04A	...Repeated for Remote Input 18					
D054	...Repeated for Remote Input 19					
D05E	...Repeated for Remote Input 20					
D068	...Repeated for Remote Input 21					
D072	...Repeated for Remote Input 22					
D07C	...Repeated for Remote Input 23					
D086	...Repeated for Remote Input 24					
D090	...Repeated for Remote Input 25					
D09A	...Repeated for Remote Input 26					
D0A4	...Repeated for Remote Input 27					
D0AE	...Repeated for Remote Input 28					
D0B8	...Repeated for Remote Input 29					
D0C2	...Repeated for Remote Input 30					
D0CC	...Repeated for Remote Input 31					
D0D6	...Repeated for Remote Input 32					
Remote Output DNA Pairs (Read/Write Setting) (32 modules)						
D220	Remote Output DNA 1 Operand	0 to 65535	---	1	F300	0
D221	Remote Output DNA 1 Events	0 to 1	---	1	F102	0 (Disabled)
D222	Reserved (2 items)	0 to 1	---	1	F001	0
D224	...Repeated for Remote Output 2					
D228	...Repeated for Remote Output 3					
D22C	...Repeated for Remote Output 4					
D230	...Repeated for Remote Output 5					
D234	...Repeated for Remote Output 6					
D238	...Repeated for Remote Output 7					
D23C	...Repeated for Remote Output 8					
D240	...Repeated for Remote Output 9					
D244	...Repeated for Remote Output 10					
D248	...Repeated for Remote Output 11					
D24C	...Repeated for Remote Output 12					
D250	...Repeated for Remote Output 13					
D254	...Repeated for Remote Output 14					
D258	...Repeated for Remote Output 15					
D25C	...Repeated for Remote Output 16					
D260	...Repeated for Remote Output 17					
D264	...Repeated for Remote Output 18					
D268	...Repeated for Remote Output 19					

Table B–9: MODBUS MEMORY MAP (Sheet 51 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
D26C	...Repeated for Remote Output 20					
D270	...Repeated for Remote Output 21					
D274	...Repeated for Remote Output 22					
D278	...Repeated for Remote Output 23					
D27C	...Repeated for Remote Output 24					
D280	...Repeated for Remote Output 25					
D284	...Repeated for Remote Output 26					
D288	...Repeated for Remote Output 27					
D28C	...Repeated for Remote Output 28					
D290	...Repeated for Remote Output 29					
D294	...Repeated for Remote Output 30					
D298	...Repeated for Remote Output 31					
D29C	...Repeated for Remote Output 32					
Remote Output UserSt Pairs (Read/Write Setting) (32 modules)						
D2A0	Remote Output UserSt 1 Operand	0 to 65535	---	1	F300	0
D2A1	Remote Output UserSt 1 Events	0 to 1	---	1	F102	0 (Disabled)
D2A2	Reserved (2 items)	0 to 1	---	1	F001	0
D2A4	...Repeated for Remote Output 2					
D2A8	...Repeated for Remote Output 3					
D2AC	...Repeated for Remote Output 4					
D2B0	...Repeated for Remote Output 5					
D2B4	...Repeated for Remote Output 6					
D2B8	...Repeated for Remote Output 7					
D2BC	...Repeated for Remote Output 8					
D2C0	...Repeated for Remote Output 9					
D2C4	...Repeated for Remote Output 10					
D2C8	...Repeated for Remote Output 11					
D2CC	...Repeated for Remote Output 12					
D2D0	...Repeated for Remote Output 13					
D2D4	...Repeated for Remote Output 14					
D2D8	...Repeated for Remote Output 15					
D2DC	...Repeated for Remote Output 16					
D2E0	...Repeated for Remote Output 17					
D2E4	...Repeated for Remote Output 18					
D2E8	...Repeated for Remote Output 19					
D2EC	...Repeated for Remote Output 20					
D2F0	...Repeated for Remote Output 21					
D2F4	...Repeated for Remote Output 22					
D2F8	...Repeated for Remote Output 23					
D2FC	...Repeated for Remote Output 24					
D300	...Repeated for Remote Output 25					
D304	...Repeated for Remote Output 26					
D308	...Repeated for Remote Output 27					
D30C	...Repeated for Remote Output 28					
D310	...Repeated for Remote Output 29					
D314	...Repeated for Remote Output 30					
D318	...Repeated for Remote Output 31					
D31C	...Repeated for Remote Output 32					
Remote Device Status (Read Only) (16 modules)						
D380	Remote Device 1 StNum	0 to 4294967295	---	1	F003	0
D382	Remote Device 1 SqNum	0 to 4294967295	---	1	F003	0
D384	...Repeated for Remote Device 2					
D388	...Repeated for Remote Device 3					
D38C	...Repeated for Remote Device 4					

Table B–9: MODBUS MEMORY MAP (Sheet 52 of 52)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
D390	...Repeated for Remote Device 5					
D394	...Repeated for Remote Device 6					
D398	...Repeated for Remote Device 7					
D39C	...Repeated for Remote Device 8					
D3A0	...Repeated for Remote Device 9					
D3A4	...Repeated for Remote Device 10					
D3A8	...Repeated for Remote Device 11					
D3AC	...Repeated for Remote Device 12					
D3B0	...Repeated for Remote Device 13					
D3B4	...Repeated for Remote Device 14					
D3B8	...Repeated for Remote Device 15					
D3BC	...Repeated for Remote Device 16					
D3C0	...Repeated for Remote Device 17					
D3C4	...Repeated for Remote Device 18					
D3C8	...Repeated for Remote Device 19					
D3CC	...Repeated for Remote Device 20					
D3D0	...Repeated for Remote Device 21					
D3D4	...Repeated for Remote Device 22					
D3D8	...Repeated for Remote Device 23					
D3DC	...Repeated for Remote Device 24					
D3E0	...Repeated for Remote Device 25					
D3E4	...Repeated for Remote Device 26					
D3E8	...Repeated for Remote Device 27					
D3EC	...Repeated for Remote Device 28					
D3F0	...Repeated for Remote Device 29					
D3F4	...Repeated for Remote Device 30					
D3F8	...Repeated for Remote Device 31					
D3FC	...Repeated for Remote Device 32					

B.4.2 DATA FORMATS

F001
UR_UINT16 UNSIGNED 16 BIT INTEGER

F002
UR_SINT16 SIGNED 16 BIT INTEGER

F003
UR_UINT32 UNSIGNED 32 BIT INTEGER (2 registers)

High order word is stored in the first register.
Low order word is stored in the second register.

F004
UR_SINT32 SIGNED 32 BIT INTEGER (2 registers)

High order word is stored in the first register/
Low order word is stored in the second register.

F005
UR_UINT8 UNSIGNED 8 BIT INTEGER

F006
UR_SINT8 SIGNED 8 BIT INTEGER

F011
UR_UINT16 FLEXCURVE DATA (120 points)

A FlexCurve is an array of 120 consecutive data points (x, y) which are interpolated to generate a smooth curve. The y-axis is the user defined trip or operation time setting; the x-axis is the pickup ratio and is pre-defined. Refer to format F119 for a listing of the pickup ratios; the enumeration value for the pickup ratio indicates the offset into the FlexCurve base address where the corresponding time value is stored.

F012
DISPLAY_SCALE DISPLAY SCALING
(unsigned 16-bit integer)

MSB indicates the SI units as a power of ten. LSB indicates the number of decimal points to display.

Example: Current values are stored as 32 bit numbers with three decimal places and base units in Amps. If the retrieved value is 12345.678 A and the display scale equals 0x0302 then the displayed value on the unit is 12.35 kA.

F013
POWER_FACTOR (SIGNED 16 BIT INTEGER)

Positive values indicate lagging power factor; negative values indicate leading.

F040
UR_UINT48 48-BIT UNSIGNED INTEGER

F050
UR_UINT32 TIME and DATE (UNSIGNED 32 BIT INTEGER)

Gives the current time in seconds elapsed since 00:00:00 January 1, 1970.

F051
UR_UINT32 DATE in SR format (alternate format for F050)

First 16 bits are Month/Day (MM/DD/xxxx). Month: 1=January, 2=February,...,12=December; Day: 1 to 31 in steps of 1
Last 16 bits are Year (xx/xx/YYYY): 1970 to 2106 in steps of 1

F052
UR_UINT32 TIME in SR format (alternate format for F050)

First 16 bits are Hours/Minutes (HH:MM:xx.xxx).
Hours: 0=12am, 1=1am,...,12=12pm,...23=11pm;
Minutes: 0 to 59 in steps of 1

Last 16 bits are Seconds (xx:xx:.SS.SSS): 0=00.000s, 1=00.001,...,59999=59.999s)

F060
FLOATING_POINT IEEE FLOATING POINT (32 bits)

F070
HEX2 2 BYTES - 4 ASCII DIGITS

F071
HEX4 4 BYTES - 8 ASCII DIGITS

F072
HEX6 6 BYTES - 12 ASCII DIGITS

F073
HEX8 8 BYTES - 16 ASCII DIGITS

F074
HEX20 20 BYTES - 40 ASCII DIGITS

F081
ENUMERATION: AUTORECLOSE 1P/3P BKR FAIL OPTION

0 = Continue, 1 = Lockout

F082
ENUMERATION: AUTORECLOSE SINGLE-PHASE / THREE-PHASE BREAKER SEQUENCE

0 = 1, 1 = 2, 2 = 1 & 2, 3 = 1 – 2, 4 = 2 – 1

F083
ENUMERATION: SELECTOR MODES

0 = Time-Out, 1 = Acknowledge

F084
ENUMERATION: SELECTOR POWER UP

0 = Restore, 1 = Synchronize, 2 = Sync/Restore

F085
ENUMERATION: POWER SWING SHAPE

0 = Mho Shape, 1 = Quad Shape

F086
ENUMERATION: DIGITAL INPUT DEFAULT STATE

0 = Off, 1 = On, 2= Latest/Off, 3 = Latest/On

F087
ENUMERATION: 87PC OSCILLOGRAPHY

0 = Basic, 1 = Minimum, 2 = Enhanced, 3 = Maximum

F088
ENUMERATION: 87PC PHASE COMPARISON SCHEME SELECTION

value	scheme
0	2TL-TR-SPC-2FC
1	2TL-BL-SPC-2FC
2	2TL-UB-DPC-2FC
3	2TL-TR-DPC-3FC
4	2TL-BL-DPC-3FC
5	3TL-TR-SPC-2FC
6	3TL-BL-SPC-2FC
7	3TL-TR-DPC-3FC
8	3TL-BL-DPC-3FC

F089
ENUMERATION: 87PC SIGNAL SOURCE

1 = One Source Current, 2 = Two Source Currents

F090
ENUMERATION: LATCHING OUTPUT TYPE

0 = Operate-dominant, 1 = Reset-dominant

F100
ENUMERATION: VT CONNECTION TYPE

0 = Wye; 1 = Delta

F101
ENUMERATION: MESSAGE DISPLAY INTENSITY

0 = 25%, 1 = 50%, 2 = 75%, 3 = 100%

F102
ENUMERATION: DISABLED/ENABLED

0 = Disabled; 1 = Enabled

F103
ENUMERATION: CURVE SHAPES

bitmask	curve shape
0	IEEE Mod Inv
1	IEEE Very Inv
2	IEEE Ext Inv
3	IEC Curve A
4	IEC Curve B
5	IEC Curve C
6	IEC Short Inv
7	IAC Ext Inv
8	IAC Very Inv

bitmask	curve shape
9	IAC Inverse
10	IAC Short Inv
11	I2t
12	Definite Time
13	FlexCurve™ A
14	FlexCurve™ B
15	FlexCurve™ C
16	FlexCurve™ D

F104
ENUMERATION: RESET TYPE

0 = Instantaneous, 1 = Timed, 2 = Linear

F105
ENUMERATION: LOGIC INPUT

0 = Disabled, 1 = Input 1, 2 = Input 2

F106
ENUMERATION: PHASE ROTATION

0 = ABC, 1 = ACB

F108
ENUMERATION: OFF/ON

0 = Off, 1 = On

F109
ENUMERATION: CONTACT OUTPUT OPERATION

0 = Self-reset, 1 = Latched, 2 = Disabled

F110
ENUMERATION: CONTACT OUTPUT LED CONTROL

0 = Trip, 1 = Alarm, 2 = None

F111
ENUMERATION: UNDERVOLTAGE CURVE SHAPES

0 = Definite Time, 1 = Inverse Time

F112
ENUMERATION: RS485 BAUD RATES

bitmask	value
0	300
1	1200
2	2400
3	4800

bitmask	value
4	9600
5	19200
6	38400
7	57600

bitmask	value
8	115200
9	14400
10	28800
11	33600

F113
ENUMERATION: PARITY

0 = None, 1 = Odd, 2 = Even

F114
ENUMERATION: IRIG-B SIGNAL TYPE

0 = None, 1 = DC Shift, 2 = Amplitude Modulated

F115
ENUMERATION: BREAKER STATUS

0 = Auxiliary A, 1 = Auxiliary B

F116
ENUMERATION: NEUTRAL OVERVOLTAGE CURVES

0 = Definite Time, 1 = FlexCurve™ A, 2 = FlexCurve™ B, 3 = FlexCurve™ C

F117
ENUMERATION: NUMBER OF OSCILLOGRAPHY RECORDS

0 = 1×72 cycles, 1 = 3×36 cycles, 2 = 7×18 cycles, 3 = 15×9 cycles

F118
ENUMERATION: OSCILLOGRAPHY MODE

0 = Automatic Overwrite, 1 = Protected

F119
ENUMERATION: FLEXCURVE™ PICKUP RATIOS

mask	value	mask	value	mask	value	mask	value
0	0.00	30	0.88	60	2.90	90	5.90
1	0.05	31	0.90	61	3.00	91	6.00
2	0.10	32	0.91	62	3.10	92	6.50
3	0.15	33	0.92	63	3.20	93	7.00
4	0.20	34	0.93	64	3.30	94	7.50
5	0.25	35	0.94	65	3.40	95	8.00
6	0.30	36	0.95	66	3.50	96	8.50
7	0.35	37	0.96	67	3.60	97	9.00
8	0.40	38	0.97	68	3.70	98	9.50
9	0.45	39	0.98	69	3.80	99	10.00
10	0.48	40	1.03	70	3.90	100	10.50
11	0.50	41	1.05	71	4.00	101	11.00
12	0.52	42	1.10	72	4.10	102	11.50
13	0.54	43	1.20	73	4.20	103	12.00
14	0.56	44	1.30	74	4.30	104	12.50
15	0.58	45	1.40	75	4.40	105	13.00
16	0.60	46	1.50	76	4.50	106	13.50
17	0.62	47	1.60	77	4.60	107	14.00
18	0.64	48	1.70	78	4.70	108	14.50
19	0.66	49	1.80	79	4.80	109	15.00
20	0.68	50	1.90	80	4.90	110	15.50
21	0.70	51	2.00	81	5.00	111	16.00
22	0.72	52	2.10	82	5.10	112	16.50
23	0.74	53	2.20	83	5.20	113	17.00
24	0.76	54	2.30	84	5.30	114	17.50
25	0.78	55	2.40	85	5.40	115	18.00
26	0.80	56	2.50	86	5.50	116	18.50
27	0.82	57	2.60	87	5.60	117	19.00
28	0.84	58	2.70	88	5.70	118	19.50
29	0.86	59	2.80	89	5.80	119	20.00

F120
ENUMERATION: DISTANCE SHAPE

0 = Mho, 1 = Quad

F122
ENUMERATION: ELEMENT INPUT SIGNAL TYPE

0 = Phasor, 1 = RMS

F123
ENUMERATION: CT SECONDARY

0 = 1 A, 1 = 5 A

F124
ENUMERATION: LIST OF ELEMENTS

bitmask	element
0	Phase Instantaneous Overcurrent 1
1	Phase Instantaneous Overcurrent 2
2	Phase Instantaneous Overcurrent 3
3	Phase Instantaneous Overcurrent 4
4	Phase Instantaneous Overcurrent 5
5	Phase Instantaneous Overcurrent 6
6	Phase Instantaneous Overcurrent 7
7	Phase Instantaneous Overcurrent 8
8	Phase Instantaneous Overcurrent 9
9	Phase Instantaneous Overcurrent 10
10	Phase Instantaneous Overcurrent 11
11	Phase Instantaneous Overcurrent 12
16	Phase Time Overcurrent 1
17	Phase Time Overcurrent 2
18	Phase Time Overcurrent 3
19	Phase Time Overcurrent 4
20	Phase Time Overcurrent 5
21	Phase Time Overcurrent 6
24	Phase Directional Overcurrent 1
25	Phase Directional Overcurrent 2
32	Neutral Instantaneous Overcurrent 1
33	Neutral Instantaneous Overcurrent 2
34	Neutral Instantaneous Overcurrent 3
35	Neutral Instantaneous Overcurrent 4
36	Neutral Instantaneous Overcurrent 5
37	Neutral Instantaneous Overcurrent 6
38	Neutral Instantaneous Overcurrent 7
39	Neutral Instantaneous Overcurrent 8
40	Neutral Instantaneous Overcurrent 9
41	Neutral Instantaneous Overcurrent 10
42	Neutral Instantaneous Overcurrent 11
43	Neutral Instantaneous Overcurrent 12
48	Neutral Time Overcurrent 1
49	Neutral Time Overcurrent 2
50	Neutral Time Overcurrent 3
51	Neutral Time Overcurrent 4
52	Neutral Time Overcurrent 5
53	Neutral Time Overcurrent 6
56	Neutral Directional Overcurrent 1
57	Neutral Directional Overcurrent 2

bitmask	element
60	Negative Sequence Directional Overcurrent 1
61	Negative Sequence Directional Overcurrent 2
64	Ground Instantaneous Overcurrent 1
65	Ground Instantaneous Overcurrent 2
66	Ground Instantaneous Overcurrent 3
67	Ground Instantaneous Overcurrent 4
68	Ground Instantaneous Overcurrent 5
69	Ground Instantaneous Overcurrent 6
70	Ground Instantaneous Overcurrent 7
71	Ground Instantaneous Overcurrent 8
72	Ground Instantaneous Overcurrent 9
73	Ground Instantaneous Overcurrent 10
74	Ground Instantaneous Overcurrent 11
75	Ground Instantaneous Overcurrent 12
80	Ground Time Overcurrent 1
81	Ground Time Overcurrent 2
82	Ground Time Overcurrent 3
83	Ground Time Overcurrent 4
84	Ground Time Overcurrent 5
85	Ground Time Overcurrent 6
96	Negative Sequence Instantaneous Overcurrent 1
97	Negative Sequence Instantaneous Overcurrent 2
101	Opposite Phase Rotation
112	Negative Sequence Time Overcurrent 1
113	Negative Sequence Time Overcurrent 2
120	Negative Sequence Overvoltage
121	Wattmetric Zero-Sequence Directional 1
122	Wattmetric Zero-Sequence Directional 2
140	Auxiliary Undervoltage 1
144	Phase Undervoltage 1
145	Phase Undervoltage 2
148	Auxiliary Overvoltage 1
152	Phase Overvoltage 1
156	Neutral Overvoltage 1
161	Phase Distance Zone 2
168	Line Pickup
180	Load Enchroachment
185	PUTT Pilot Scheme
190	Power Swing Detect
224	SRC1 VT Fuse Failure
225	SRC2 VT Fuse Failure
226	SRC3 VT Fuse Failure
227	SRC4 VT Fuse Failure
228	SRC5 VT Fuse Failure
229	SRC6 VT Fuse Failure
232	SRC1 50DD (Disturbance Detection)
233	SRC2 50DD (Disturbance Detection)
234	SRC3 50DD (Disturbance Detection)
235	SRC4 50DD (Disturbance Detection)
245	Continuous Monitor
246	CT Failure
272	Breaker 1
273	Breaker 2

bitmask	element
280	Breaker Failure 1
281	Breaker Failure 2
288	Breaker Arcing Current 1
289	Breaker Arcing Current 2
290	Breaker Arcing Current 3
291	Breaker Arcing Current 4
292	Breaker Arcing Current 5
293	Breaker Arcing Current 6
294	Breaker 1 Flashover
295	Breaker 2 Flashover
304	Autoreclose 1
305	Autoreclose 2
306	Autoreclose 3
307	Autoreclose 4
308	Autoreclose 5
309	Autoreclose 6
312	Synchrocheck 1
313	Synchrocheck 2
336	Setting Group
337	Reset
360	Trip Output
362	Phase Selector
364	Open Pole Detector
376	Autoreclose (single-pole / three-pole)
382	87PC channel test
383	87PC phase comparison trip
384	87PC negative-sequence voltage fault detector
385	87PC negative-sequence current rate of change
386	87PC positive-sequence current rate of change
388	Selector 1
389	Selector 2
390	Control pushbutton 1
391	Control pushbutton 2
392	Control pushbutton 3
393	Control pushbutton 4
394	Control pushbutton 5
395	Control pushbutton 6
396	Control pushbutton 7
400	FlexElement™ 1
401	FlexElement™ 2
402	FlexElement™ 3
403	FlexElement™ 4
404	FlexElement™ 5
405	FlexElement™ 6
406	FlexElement™ 7
407	FlexElement™ 8
420	Non-volatile Latch 1
421	Non-volatile Latch 2
422	Non-volatile Latch 3
423	Non-volatile Latch 4
424	Non-volatile Latch 5
425	Non-volatile Latch 6
426	Non-volatile Latch 7

bitmask	element
427	Non-volatile Latch 8
428	Non-volatile Latch 9
429	Non-volatile Latch 10
430	Non-volatile Latch 11
431	Non-volatile Latch 12
432	Non-volatile Latch 13
433	Non-volatile Latch 14
434	Non-volatile Latch 15
435	Non-volatile Latch 16
544	Digital Counter 1
545	Digital Counter 2
546	Digital Counter 3
547	Digital Counter 4
548	Digital Counter 5
549	Digital Counter 6
550	Digital Counter 7
551	Digital Counter 8
692	Digital Element 1
693	Digital Element 2
694	Digital Element 3
695	Digital Element 4
696	Digital Element 5
697	Digital Element 6
698	Digital Element 7
699	Digital Element 8
700	Digital Element 9
701	Digital Element 10
702	Digital Element 11
703	Digital Element 12
704	Digital Element 13
705	Digital Element 14
706	Digital Element 15
707	Digital Element 16
708	Digital Element 17
709	Digital Element 18
710	Digital Element 19
711	Digital Element 20
712	Digital Element 21
713	Digital Element 22
714	Digital Element 23
715	Digital Element 24
716	Digital Element 25
717	Digital Element 26
718	Digital Element 27
719	Digital Element 28
720	Digital Element 29
721	Digital Element 30
722	Digital Element 31
723	Digital Element 32
724	Digital Element 33
725	Digital Element 34
726	Digital Element 35
727	Digital Element 36

bitmask	element
728	Digital Element 37
729	Digital Element 38
730	Digital Element 39
731	Digital Element 40
732	Digital Element 41
733	Digital Element 42
734	Digital Element 43
735	Digital Element 44
736	Digital Element 45
737	Digital Element 46
738	Digital Element 47
739	Digital Element 48
842	Trip Bus 1
843	Trip Bus 2
844	Trip Bus 3
845	Trip Bus 4
846	Trip Bus 5
847	Trip Bus 6
849	RTD Input 1
849	RTD Input 1
850	RTD Input 2
851	RTD Input 3
852	RTD Input 4
853	RTD Input 5
854	RTD Input 6
855	RTD Input 7
856	RTD Input 8
857	RTD Input 9
858	RTD Input 10
859	RTD Input 11
860	RTD Input 12
861	RTD Input 13
862	RTD Input 14
863	RTD Input 15
864	RTD Input 16
865	RTD Input 17
866	RTD Input 18
867	RTD Input 19
868	RTD Input 20
869	RTD Input 21
870	RTD Input 22
871	RTD Input 23
872	RTD Input 24
873	RTD Input 25
874	RTD Input 26
875	RTD Input 27
876	RTD Input 28
877	RTD Input 29
878	RTD Input 30
879	RTD Input 31
880	RTD Input 32
881	RTD Input 33
882	RTD Input 34

bitmask	element
883	RTD Input 35
884	RTD Input 36
885	RTD Input 37
886	RTD Input 38
887	RTD Input 39
888	RTD Input 40
889	RTD Input 41
890	RTD Input 42
891	RTD Input 43
892	RTD Input 44
893	RTD Input 45
894	RTD Input 46
895	RTD Input 47
896	RTD Input 48
900	User-Programmable Pushbutton 1
901	User-Programmable Pushbutton 2
902	User-Programmable Pushbutton 3
903	User-Programmable Pushbutton 4
904	User-Programmable Pushbutton 5
905	User-Programmable Pushbutton 6
906	User-Programmable Pushbutton 7
907	User-Programmable Pushbutton 8
908	User-Programmable Pushbutton 9
909	User-Programmable Pushbutton 10
910	User-Programmable Pushbutton 11
911	User-Programmable Pushbutton 12
912	User-Programmable Pushbutton 13
913	User-Programmable Pushbutton 14
914	User-Programmable Pushbutton 15
915	User-Programmable Pushbutton 16

F125
ENUMERATION: ACCESS LEVEL

0 = Restricted; 1 = Command, 2 = Setting, 3 = Factory Service

F126
ENUMERATION: NO/YES CHOICE

0 = No, 1 = Yes

F127
ENUMERATION: LATCHED OR SELF-RESETTING

0 = Latched, 1 = Self-Reset

F128
ENUMERATION: CONTACT INPUT THRESHOLD

0 = 17 V DC, 1 = 33 V DC, 2 = 84 V DC, 3 = 166 V DC

F129
ENUMERATION: FLEXLOGIC TIMER TYPE

0 = millisecond, 1 = second, 2 = minute

F130
ENUMERATION: SIMULATION MODE

0 = Off. 1 = Pre-Fault, 2 = Fault, 3 = Post-Fault

F131
ENUMERATION: FORCED CONTACT OUTPUT STATE

0 = Disabled, 1 = Energized, 2 = De-energized, 3 = Freeze

F133
ENUMERATION: PROGRAM STATE

0 = Not Programmed, 1 = Programmed

F134
ENUMERATION: PASS/FAIL

0 = Fail, 1 = OK, 2 = n/a

F135
ENUMERATION: GAIN CALIBRATION

0 = 0x1, 1 = 1x16

F136
ENUMERATION: NUMBER OF OSCILLOGRAPHY RECORDS

0 = 31 x 8 cycles, 1 = 15 x 16 cycles, 2 = 7 x 32 cycles
3 = 3 x 64 cycles, 4 = 1 x 128 cycles

F137
ENUMERATION: USER-PROGRAMMABLE PUSHBUTTON FUNCTION

0 = Disabled, 1 = Self-Reset, 2 = Latched

F138
ENUMERATION: OSCILLOGRAPHY FILE TYPE

0 = Data File, 1 = Configuration File, 2 = Header File

F140
ENUMERATION: CURRENT, SENS CURRENT, VOLTAGE, DISABLED

0 = Disabled, 1 = Current 46 A, 2 = Voltage 280 V,
3 = Current 4.6 A, 4 = Current 2 A, 5 = Notched 4.6 A,
6 = Notched 2 A

F141
ENUMERATION: SELF TEST ERRORS

bitmask	error
0	Any Self Tests
1	Maintenance Alert
10	FlexLogic Error Token
11	Equipment Mismatch
13	Unit Not Programmed
14	System Exception
15	Maintenance Alert
16	Maintenance Alert
17	Maintenance Alert
18	Maintenance Alert
19	Maintenance Alert
20	Maintenance Alert
21	Maintenance Alert
27	Remote Device Off
28	Direct Device Off
29	Maintenance Alert
30	Any Minor Error
31	Any Major Error
32	DSP Error
33	No DSP Interrupts
34	Unit Not Calibrated
35	EEPROM Data Error
36	SRAM Data Error
37	Program Memory
38	Watchdog Error
39	Low On Memory
40	Prototype Firmware
41	Module Failure 01
42	Module Failure 02
43	Module Failure 03
44	Module Failure 04
45	Module Failure 05
46	Module Failure 06
47	Module Failure 07
48	Module Failure 08
49	Module Failure 09
50	Incompatible H/W
51	Maintenance Alert
52	Maintenance Alert
53	Maintenance Alert
54	Maintenance Alert
55	Maintenance Alert
56	Maintenance Alert

F142
ENUMERATION: EVENT RECORDER ACCESS FILE TYPE

0 = All Record Data, 1 = Headers Only, 2 = Numeric Event Cause

F143
UR_UINT32: 32 BIT ERROR CODE (F141 specifies bit number)

A bit value of 0 = no error, 1 = error

F144
ENUMERATION: FORCED CONTACT INPUT STATE

0 = Disabled, 1 = Open, 2 = Closed

F145
ENUMERATION: ALPHABET LETTER

bitmask	type	bitmask	type	bitmask	type	bitmask	type
0	null	7	G	14	N	21	U
1	A	8	H	15	O	22	V
2	B	9	I	16	P	23	W
3	C	10	J	17	Q	24	X
4	D	11	K	18	R	25	Y
5	E	12	L	19	S	26	Z
6	F	13	M	20	T		

F146
ENUMERATION: MISCELLANEOUS EVENT CAUSES

bitmask	definition
0	Events Cleared
1	Oscillography Triggered
2	Date/time Changed
3	Default Settings Loaded
4	Test Mode On
5	Test Mode Off
6	Power On
7	Power Off
8	Relay In Service
9	Relay Out Of Service
10	Watchdog Reset
11	Oscillography Clear
12	Reboot Command
13	Led Test Initiated
14	Flash Programming
15	Fault Report Trigger
16	User Programmable Fault Report Trigger
17	Corrupt DSP Program
18	Reload DSP Settings
19	DSP Hardware Error
20	Ethernet Port 1 Offline
21	Ethernet Port 2 Offline
22	Ethernet Port 3 Offline
23	Ethernet Port 4 Offline
24	Ethernet Port 5 Offline
25	Ethernet Port 6 Offline

F147
ENUMERATION: LINE LENGTH UNITS

0 = km, 1 = miles

F148
ENUMERATION: FAULT TYPE

bitmask	fault type
0	NA
1	AG
2	BG
3	CG
4	AB
5	BC

bitmask	fault type
6	AC
7	ABG
8	BCG
9	ACG
10	ABC
11	ABCG

F149
ENUMERATION: 87PC PHASE COMPARISON SCHEME SELECTION

bitmask	phase comp scheme
0	2TL-PT-DPC-3FC
1	2TL-BL-DPC-3FC
2	2TL-PT-SPC-2FC
3	2TL-BL-SPC-2FC
4	2TL-BL-DPC-2FC
5	3TL-PT-SPC-3FC

F150
ENUMERATION: 87PC PHASE COMPARISON SCHEME SIGNAL SELECTION

0 = MIXED I_2 - K*I_1, 1 = 3I_0

F151
ENUMERATION: RTD SELECTION

bitmask	RTD#
0	NONE
1	RTD 1
2	RTD 2
3	RTD 3
4	RTD 4
5	RTD 5
6	RTD 6
7	RTD 7
8	RTD 8
9	RTD 9
10	RTD 10
11	RTD 11
12	RTD 12
13	RTD 13
14	RTD 14
15	RTD 15
16	RTD 16

bitmask	RTD#
17	RTD 17
18	RTD 18
19	RTD 19
20	RTD 20
21	RTD 21
22	RTD 22
23	RTD 23
24	RTD 24
25	RTD 25
26	RTD 26
27	RTD 27
28	RTD 28
29	RTD 29
30	RTD 30
31	RTD 31
32	RTD 32

bitmask	RTD#
33	RTD 33
34	RTD 34
35	RTD 35
36	RTD 36
37	RTD 37
38	RTD 38
39	RTD 39
40	RTD 40
41	RTD 41
42	RTD 42
43	RTD 43
44	RTD 44
45	RTD 45
46	RTD 46
47	RTD 47
48	RTD 48

F152
ENUMERATION: SETTING GROUP

0 = Active Group, 1 = Group 1, 2 = Group 2, 3 = Group 3
4 = Group 4, 5 = Group 5, 6 = Group 6

F153
ENUMERATION: DISTANCE TRANSFORMER CONNECTION

bitmask	type
0	None
1	Dy1
2	Dy3
3	Dy5
4	Dy7

bitmask	type
5	Dy9
6	Dy11
7	Yd1
8	Yd3
9	Yd5

bitmask	type
10	Yd7
11	Yd9
12	Yd11

F154
ENUMERATION: DISTANCE DIRECTION

0 = Forward, 1 = Reverse, 2 = Non-Directional

F155
ENUMERATION: REMOTE DEVICE STATE

0 = Offline, 1 = Online

F156
ENUMERATION: REMOTE INPUT BIT PAIRS

bitmask	value	bitmask	value
0	NONE	35	UserSt-3
1	DNA-1	36	UserSt-4
2	DNA-2	37	UserSt-5
3	DNA-3	38	UserSt-6
4	DNA-4	39	UserSt-7
5	DNA-5	40	UserSt-8
6	DNA-6	41	UserSt-9
7	DNA-7	42	UserSt-10
8	DNA-8	43	UserSt-11
9	DNA-9	44	UserSt-12
10	DNA-10	45	UserSt-13
11	DNA-11	46	UserSt-14
12	DNA-12	47	UserSt-15
13	DNA-13	48	UserSt-16
14	DNA-14	49	UserSt-17
15	DNA-15	50	UserSt-18
16	DNA-16	51	UserSt-19
17	DNA-17	52	UserSt-20
18	DNA-18	53	UserSt-21
19	DNA-19	54	UserSt-22
20	DNA-20	55	UserSt-23
21	DNA-21	56	UserSt-24
22	DNA-22	57	UserSt-25
23	DNA-23	58	UserSt-26
24	DNA-24	59	UserSt-27
25	DNA-25	60	UserSt-28
26	DNA-26	61	UserSt-29
27	DNA-27	62	UserSt-30
28	DNA-28	63	UserSt-31
29	DNA-29	64	UserSt-32
30	DNA-30	65	Dataset Item 1
31	DNA-31	66	Dataset Item 2
32	DNA-32	67	Dataset Item 3
33	UserSt-1	↓	↓
34	UserSt-2	128	Dataset Item 64

F157
ENUMERATION: BREAKER MODE

0 = 3-Pole, 1 = 1-Pole

F158
ENUMERATION: SCHEME CALIBRATION TEST

0 = Normal, 1 = Symmetry 1, 2 = Symmetry 2, 3 = Delay 1
4 = Delay 2

F159
ENUMERATION: BREAKER AUX CONTACT KEYING

0 = 52a, 1 = 52b, 2 = None

F166
ENUMERATION: AUXILIARY VT CONNECTION TYPE

0 = Vn, 1 = Vag, 2 = Vbg, 3 = Vcg, 4 = Vab, 5 = Vbc, 6 = Vca

F167
ENUMERATION: SIGNAL SOURCE

0 = SRC 1, 1 = SRC 2, 2 = SRC 3, 3 = SRC 4,
4 = SRC 5, 5 = SRC 6

F168
ENUMERATION: INRUSH INHIBIT FUNCTION

0 = Disabled, 1 = Adapt. 2nd, 2 = Trad. 2nd

F170
ENUMERATION: LOW/HIGH OFFSET and GAIN TRANSDUCER INPUT/OUTPUT SELECTION

0 = LOW, 1 = HIGH

F171
ENUMERATION: TRANSDUCER CHANNEL INPUT TYPE

0 = dcmA IN, 1 = Ohms IN, 2 = RTD IN, 3 = dcmA OUT

F172
ENUMERATION: SLOT LETTERS

bitmask	slot	bitmask	slot	bitmask	slot	bitmask	slot
0	F	4	K	8	P	12	U
1	G	5	L	9	R	13	V
2	H	6	M	10	S	14	W
3	J	7	N	11	T	15	X

F173
ENUMERATION: DCMA INPUT/OUTPUT RANGE

bitmask	dcmA input/output range
0	0 to –1 mA
1	0 to 1 mA
2	–1 to 1 mA
3	0 to 5 mA
4	0 to 10 mA
5	0 to 20 mA
6	4 to 20 mA

F174
ENUMERATION: TRANSDUCER RTD INPUT TYPE

0 = 100 Ohm Platinum, 1 = 120 Ohm Nickel,
2 = 100 Ohm Nickel, 3 = 10 Ohm Copper

F175
ENUMERATION: PHASE LETTERS

0 = A, 1 = B, 2 = C

F176
ENUMERATION: SYNCHROCHECK DEAD SOURCE SELECT

bitmask	synchrocheck dead source
0	None
1	LV1 and DV2
2	DV1 and LV2
3	DV1 or DV2
4	DV1 Xor DV2
5	DV1 and DV2

F177
ENUMERATION: COMMUNICATION PORT

0 = None, 1 = COM1-RS485, 2 = COM2-RS485,
3 = Front Panel-RS232, 4 = Network - TCP, 5 = Network - UDP

F178
ENUMERATION: DATA LOGGER RATES

0 = 1 sec, 1 = 1 min, 2 = 5 min, 3 = 10 min, 4 = 15 min,
5 = 20 min, 6 = 30 min, 7 = 60 min, 8 = 15 ms, 9 = 30 ms,
10 = 100 ms, 11 = 500 ms

F179
ENUMERATION: NEGATIVE SEQUENCE DIRECTIONAL OVERCURRENT TYPE

0 = Neg Sequence, 1 = Zero Sequence

F180
ENUMERATION: PHASE/GROUND

0 = PHASE, 1 = GROUND

F181
ENUMERATION: ODD/EVEN/NONE

0 = ODD, 1 = EVEN, 2 = NONE

F183
ENUMERATION: AC INPUT WAVEFORMS

bitmask	definition
0	Off
1	8 samples/cycle
2	16 samples/cycle
3	32 samples/cycle
4	64 samples/cycle

F184
ENUMERATION: REMOTE DEVICE GOOSE DATASET

value	GOOSE dataset
0	Off
1	GooseIn 1
2	GooseIn 2
3	GooseIn 3
4	GooseIn 4
5	GooseIn 5
6	GooseIn 6
7	GooseIn 7
8	GooseIn 8

F185
ENUMERATION: PHASE A,B,C, GROUND SELECTOR

0 = A, 1 = B, 2 = C, 3 = G

F186
ENUMERATION: MEASUREMENT MODE

0 = Phase to Ground, 1 = Phase to Phase

F190
ENUMERATION: SIMULATED KEYPRESS

bitmsk	keypress
0	--- use between real keys
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	0
11	Decimal Pt
12	Plus/Minus
13	Value Up
14	Value Down
15	Message Up
16	Message Down
17	Message Left
18	Message Right
19	Menu
20	Help
21	Escape
22	Enter

bitmsk	keypress
23	Reset
24	User 1
25	User 2
26	User 3
27	User-programmable key 1
28	User-programmable key 2
29	User-programmable key 3
30	User-programmable key 4
31	User-programmable key 5
32	User-programmable key 6
33	User-programmable key 7
34	User-programmable key 8
35	User-programmable key 9
36	User-programmable key 10
37	User-programmable key 11
38	User-programmable key 12
43	User-programmable key 13
44	User-programmable key 14
45	User-programmable key 15
46	User-programmable key 16
47	User 4 (control pushbutton)
48	User 5 (control pushbutton)
49	User 6 (control pushbutton)
50	User 7 (control pushbutton)

F192
ENUMERATION: ETHERNET OPERATION MODE

0 = Half-Duplex, 1 = Full-Duplex

F194
ENUMERATION: DNP SCALE

0 = 0.01, 1 = 0.1, 2 = 1, 3 = 10, 4 = 100, 5 = 1000, 6 = 10000, 7 = 100000, 8 = 0.001

F195
ENUMERATION: SINGLE POLE TRIP MODE

0 = Disabled, 1 = 3 Pole Only, 2 = 3 Pole & 1 Pole

F196
ENUMERATION: NEUTRAL DIRECTIONAL OVERCURRENT OPERATING CURRENT

0 = Calculated 3I0, 1 = Measured IG

F199
ENUMERATION: DISABLED/ENABLED/CUSTOM

0 = Disabled, 1 = Enabled, 2 = Custom

F200
TEXT40: 40-CHARACTER ASCII TEXT

20 registers, 16 Bits: 1st Char MSB, 2nd Char. LSB

F201
TEXT8: 8-CHARACTER ASCII PASSCODE

4 registers, 16 Bits: 1st Char MSB, 2nd Char. LSB

F202
TEXT20: 20-CHARACTER ASCII TEXT

10 registers, 16 Bits: 1st Char MSB, 2nd Char. LSB

F203
TEXT16: 16-CHARACTER ASCII TEXT

F204
TEXT80: 80-CHARACTER ASCII TEXT

F205
TEXT12: 12-CHARACTER ASCII TEXT

F206
TEXT6: 6-CHARACTER ASCII TEXT

F207
TEXT4: 4-CHARACTER ASCII TEXT

F208
TEXT2: 2-CHARACTER ASCII TEXT

F211
ENUMERATION: SOURCE SELECTION

0 = None, 1 = SRC 1, 2 = SRC 2, 3 = SRC 3, 4 = SRC 4, 5 = SRC 5, 6 = SRC 6

F212
ENUMERATION: 87PC SOURCE SELECTION

0 = 1 Source Current; 1 = Two Source Currents

F220
ENUMERATION: PUSHBUTTON MESSAGE PRIORITY

value	priority
0	Disabled
1	Normal
2	High Priority

F222
ENUMERATION: TEST ENUMERATION

0 = Test Enumeration 0, 1 = Test Enumeration 1

F226
ENUMERATION: REMOTE INPUT/OUTPUT TRANSFER METHOD

0 = None, 1 = GSSE, 2 = GOOSE

F227
ENUMERATION: RELAY SERVICE STATUS

0 = Unknown, 1 = Relay In Service, 2 = Relay Out Of Service

F230
ENUMERATION: DIRECTIONAL POLARIZING

0 = Voltage, 1 = Current, 2 = Dual

F231
ENUMERATION: POLARIZING VOLTAGE

0 = Calculated V0, 1 = Measured VX

F232
ENUMERATION: CONFIGURABLE GOOSE DATASET ITEMS FOR TRANSMISSION

value	GOOSE dataset item
0	None
1	GGIO1.ST.Ind1.q
2	GGIO1.ST.Ind1.stVal

value	GOOSE dataset item
3	GGIO1.ST.Ind2.q
4	GGIO1.ST.Ind2.stVal
↓	↓
255	GGIO1.ST.Ind128.q
256	GGIO1.ST.Ind128.stVal
257	MMXU1.MX.TotW.mag.f
258	MMXU1.MX.TotVAr.mag.f
259	MMXU1.MX.TotVA.mag.f
260	MMXU1.MX.TotPF.mag.f
261	MMXU1.MX.Hz.mag.f
262	MMXU1.MX.PPV.phsAB.cVal.mag.f
263	MMXU1.MX.PPV.phsAB.cVal.ang.f
264	MMXU1.MX.PPV.phsBC.cVal.mag.f
265	MMXU1.MX.PPV.phsBC.cVal.ang.f
266	MMXU1.MX.PPV.phsCA.cVal.mag.f
267	MMXU1.MX.PPV.phsCA.cVal.ang.f
268	MMXU1.MX.PhV.phsA.cVal.mag.f
269	MMXU1.MX.PhV.phsA.cVal.ang.f
270	MMXU1.MX.PhV.phsB.cVal.mag.f
271	MMXU1.MX.PhV.phsB.cVal.ang.f
272	MMXU1.MX.PhV.phsC.cVal.mag.f
273	MMXU1.MX.PhV.phsC.cVal.ang.f
274	MMXU1.MX.A.phsA.cVal.mag.f
275	MMXU1.MX.A.phsA.cVal.ang.f
276	MMXU1.MX.A.phsB.cVal.mag.f
277	MMXU1.MX.A.phsB.cVal.ang.f
278	MMXU1.MX.A.phsC.cVal.mag.f
279	MMXU1.MX.A.phsC.cVal.ang.f
280	MMXU1.MX.A.neut.cVal.mag.f
281	MMXU1.MX.A.neut.cVal.ang.f
282	MMXU1.MX.W.phsA.cVal.mag.f
283	MMXU1.MX.W.phsB.cVal.mag.f
284	MMXU1.MX.W.phsC.cVal.mag.f
285	MMXU1.MX.VAr.phsA.cVal.mag.f
286	MMXU1.MX.VAr.phsB.cVal.mag.f
287	MMXU1.MX.VAr.phsC.cVal.mag.f
288	MMXU1.MX.VA.phsA.cVal.mag.f
289	MMXU1.MX.VA.phsB.cVal.mag.f
290	MMXU1.MX.VA.phsC.cVal.mag.f
291	MMXU1.MX.PF.phsA.cVal.mag.f
292	MMXU1.MX.PF.phsB.cVal.mag.f
293	MMXU1.MX.PF.phsC.cVal.mag.f
294	MMXU2.MX.TotW.mag.f
295	MMXU2.MX.TotVAr.mag.f
296	MMXU2.MX.TotVA.mag.f
297	MMXU2.MX.TotPF.mag.f
298	MMXU2.MX.Hz.mag.f
299	MMXU2.MX.PPV.phsAB.cVal.mag.f
300	MMXU2.MX.PPV.phsAB.cVal.ang.f
301	MMXU2.MX.PPV.phsBC.cVal.mag.f
302	MMXU2.MX.PPV.phsBC.cVal.ang.f
303	MMXU2.MX.PPV.phsCA.cVal.mag.f
304	MMXU2.MX.PPV.phsCA.cVal.ang.f

value	GOOSE dataset item
305	MMXU2.MX.PhV.phsA.cVal.mag.f
306	MMXU2.MX.PhV.phsA.cVal.ang.f
307	MMXU2.MX.PhV.phsB.cVal.mag.f
308	MMXU2.MX.PhV.phsB.cVal.ang.f
309	MMXU2.MX.PhV.phsC.cVal.mag.f
310	MMXU2.MX.PhV.phsC.cVal.ang.f
311	MMXU2.MX.A.phsA.cVal.mag.f
312	MMXU2.MX.A.phsA.cVal.ang.f
313	MMXU2.MX.A.phsB.cVal.mag.f
314	MMXU2.MX.A.phsB.cVal.ang.f
315	MMXU2.MX.A.phsC.cVal.mag.f
316	MMXU2.MX.A.phsC.cVal.ang.f
317	MMXU2.MX.A.neut.cVal.mag.f
318	MMXU2.MX.A.neut.cVal.ang.f
319	MMXU2.MX.W.phsA.cVal.mag.f
320	MMXU2.MX.W.phsB.cVal.mag.f
321	MMXU2.MX.W.phsC.cVal.mag.f
322	MMXU2.MX.VAr.phsA.cVal.mag.f
323	MMXU2.MX.VAr.phsB.cVal.mag.f
324	MMXU2.MX.VAr.phsC.cVal.mag.f
325	MMXU2.MX.VA.phsA.cVal.mag.f
326	MMXU2.MX.VA.phsB.cVal.mag.f
327	MMXU2.MX.VA.phsC.cVal.mag.f
328	MMXU2.MX.PF.phsA.cVal.mag.f
329	MMXU2.MX.PF.phsB.cVal.mag.f
330	MMXU2.MX.PF.phsC.cVal.mag.f
331	MMXU3.MX.TotW.mag.f
332	MMXU3.MX.TotVAr.mag.f
333	MMXU3.MX.TotVA.mag.f
334	MMXU3.MX.TotPF.mag.f
335	MMXU3.MX.Hz.mag.f
336	MMXU3.MX.PPV.phsAB.cVal.mag.f
337	MMXU3.MX.PPV.phsAB.cVal.ang.f
338	MMXU3.MX.PPV.phsBC.cVal.mag.f
339	MMXU3.MX.PPV.phsBC.cVal.ang.f
340	MMXU3.MX.PPV.phsCA.cVal.mag.f
341	MMXU3.MX.PPV.phsCA.cVal.ang.f
342	MMXU3.MX.PhV.phsA.cVal.mag.f
343	MMXU3.MX.PhV.phsA.cVal.ang.f
344	MMXU3.MX.PhV.phsB.cVal.mag.f
345	MMXU3.MX.PhV.phsB.cVal.ang.f
346	MMXU3.MX.PhV.phsC.cVal.mag.f
347	MMXU3.MX.PhV.phsC.cVal.ang.f
348	MMXU3.MX.A.phsA.cVal.mag.f
349	MMXU3.MX.A.phsA.cVal.ang.f
350	MMXU3.MX.A.phsB.cVal.mag.f
351	MMXU3.MX.A.phsB.cVal.ang.f
352	MMXU3.MX.A.phsC.cVal.mag.f
353	MMXU3.MX.A.phsC.cVal.ang.f
354	MMXU3.MX.A.neut.cVal.mag.f
355	MMXU3.MX.A.neut.cVal.ang.f
356	MMXU3.MX.W.phsA.cVal.mag.f
357	MMXU3.MX.W.phsB.cVal.mag.f

value	GOOSE dataset item
358	MMXU3.MX.W.phsC.cVal.mag.f
359	MMXU3.MX.VAr.phsA.cVal.mag.f
360	MMXU3.MX.VAr.phsB.cVal.mag.f
361	MMXU3.MX.VAr.phsC.cVal.mag.f
362	MMXU3.MX.VA.phsA.cVal.mag.f
363	MMXU3.MX.VA.phsB.cVal.mag.f
364	MMXU3.MX.VA.phsC.cVal.mag.f
365	MMXU3.MX.PF.phsA.cVal.mag.f
366	MMXU3.MX.PF.phsB.cVal.mag.f
367	MMXU3.MX.PF.phsC.cVal.mag.f
368	MMXU4.MX.TotW.mag.f
369	MMXU4.MX.TotVAr.mag.f
370	MMXU4.MX.TotVA.mag.f
371	MMXU4.MX.TotPF.mag.f
372	MMXU4.MX.Hz.mag.f
373	MMXU4.MX.PPV.phsAB.cVal.mag.f
374	MMXU4.MX.PPV.phsAB.cVal.ang.f
375	MMXU4.MX.PPV.phsBC.cVal.mag.f
376	MMXU4.MX.PPV.phsBC.cVal.ang.f
377	MMXU4.MX.PPV.phsCA.cVal.mag.f
378	MMXU4.MX.PPV.phsCA.cVal.ang.f
379	MMXU4.MX.PhV.phsA.cVal.mag.f
380	MMXU4.MX.PhV.phsA.cVal.ang.f
381	MMXU4.MX.PhV.phsB.cVal.mag.f
382	MMXU4.MX.PhV.phsB.cVal.ang.f
383	MMXU4.MX.PhV.phsC.cVal.mag.f
384	MMXU4.MX.PhV.phsC.cVal.ang.f
385	MMXU4.MX.A.phsA.cVal.mag.f
386	MMXU4.MX.A.phsA.cVal.ang.f
387	MMXU4.MX.A.phsB.cVal.mag.f
388	MMXU4.MX.A.phsB.cVal.ang.f
389	MMXU4.MX.A.phsC.cVal.mag.f
390	MMXU4.MX.A.phsC.cVal.ang.f
391	MMXU4.MX.A.neut.cVal.mag.f
392	MMXU4.MX.A.neut.cVal.ang.f
393	MMXU4.MX.W.phsA.cVal.mag.f
394	MMXU4.MX.W.phsB.cVal.mag.f
395	MMXU4.MX.W.phsC.cVal.mag.f
396	MMXU4.MX.VAr.phsA.cVal.mag.f
397	MMXU4.MX.VAr.phsB.cVal.mag.f
398	MMXU4.MX.VAr.phsC.cVal.mag.f
399	MMXU4.MX.VA.phsA.cVal.mag.f
400	MMXU4.MX.VA.phsB.cVal.mag.f
401	MMXU4.MX.VA.phsC.cVal.mag.f
402	MMXU4.MX.PF.phsA.cVal.mag.f
403	MMXU4.MX.PF.phsB.cVal.mag.f
404	MMXU4.MX.PF.phsC.cVal.mag.f
405	MMXU5.MX.TotW.mag.f
406	MMXU5.MX.TotVAr.mag.f
407	MMXU5.MX.TotVA.mag.f
408	MMXU5.MX.TotPF.mag.f
409	MMXU5.MX.Hz.mag.f
410	MMXU5.MX.PPV.phsAB.cVal.mag.f

value	GOOSE dataset item
411	MMXU5.MX.PPV.phsAB.cVal.ang.f
412	MMXU5.MX.PPV.phsBC.cVal.mag.f
413	MMXU5.MX.PPV.phsBC.cVal.ang.f
414	MMXU5.MX.PPV.phsCA.cVal.mag.f
415	MMXU5.MX.PPV.phsCA.cVal.ang.f
416	MMXU5.MX.PhV.phsA.cVal.mag.f
417	MMXU5.MX.PhV.phsA.cVal.ang.f
418	MMXU5.MX.PhV.phsB.cVal.mag.f
419	MMXU5.MX.PhV.phsB.cVal.ang.f
420	MMXU5.MX.PhV.phsC.cVal.mag.f
421	MMXU5.MX.PhV.phsC.cVal.ang.f
422	MMXU5.MX.A.phsA.cVal.mag.f
423	MMXU5.MX.A.phsA.cVal.ang.f
424	MMXU5.MX.A.phsB.cVal.mag.f
425	MMXU5.MX.A.phsB.cVal.ang.f
426	MMXU5.MX.A.phsC.cVal.mag.f
427	MMXU5.MX.A.phsC.cVal.ang.f
428	MMXU5.MX.A.neut.cVal.mag.f
429	MMXU5.MX.A.neut.cVal.ang.f
430	MMXU5.MX.W.phsA.cVal.mag.f
431	MMXU5.MX.W.phsB.cVal.mag.f
432	MMXU5.MX.W.phsC.cVal.mag.f
433	MMXU5.MX.VAr.phsA.cVal.mag.f
434	MMXU5.MX.VAr.phsB.cVal.mag.f
435	MMXU5.MX.VAr.phsC.cVal.mag.f
436	MMXU5.MX.VA.phsA.cVal.mag.f
437	MMXU5.MX.VA.phsB.cVal.mag.f
438	MMXU5.MX.VA.phsC.cVal.mag.f
439	MMXU5.MX.PF.phsA.cVal.mag.f
440	MMXU5.MX.PF.phsB.cVal.mag.f
441	MMXU5.MX.PF.phsC.cVal.mag.f
442	MMXU6.MX.TotW.mag.f
443	MMXU6.MX.TotVAr.mag.f
444	MMXU6.MX.TotVA.mag.f
445	MMXU6.MX.TotPF.mag.f
446	MMXU6.MX.Hz.mag.f
447	MMXU6.MX.PPV.phsAB.cVal.mag.f
448	MMXU6.MX.PPV.phsAB.cVal.ang.f
449	MMXU6.MX.PPV.phsBC.cVal.mag.f
450	MMXU6.MX.PPV.phsBC.cVal.ang.f
451	MMXU6.MX.PPV.phsCA.cVal.mag.f
452	MMXU6.MX.PPV.phsCA.cVal.ang.f
453	MMXU6.MX.PhV.phsA.cVal.mag.f
454	MMXU6.MX.PhV.phsA.cVal.ang.f
455	MMXU6.MX.PhV.phsB.cVal.mag.f
456	MMXU6.MX.PhV.phsB.cVal.ang.f
457	MMXU6.MX.PhV.phsC.cVal.mag.f
458	MMXU6.MX.PhV.phsC.cVal.ang.f
459	MMXU6.MX.A.phsA.cVal.mag.f
460	MMXU6.MX.A.phsA.cVal.ang.f
461	MMXU6.MX.A.phsB.cVal.mag.f
462	MMXU6.MX.A.phsB.cVal.ang.f
463	MMXU6.MX.A.phsC.cVal.mag.f

value	GOOSE dataset item
464	MMXU6.MX.A.phsC.cVal.ang.f
465	MMXU6.MX.A.neut.cVal.mag.f
466	MMXU6.MX.A.neut.cVal.ang.f
467	MMXU6.MX.W.phsA.cVal.mag.f
468	MMXU6.MX.W.phsB.cVal.mag.f
469	MMXU6.MX.W.phsC.cVal.mag.f
470	MMXU6.MX.VAr.phsA.cVal.mag.f
471	MMXU6.MX.VAr.phsB.cVal.mag.f
472	MMXU6.MX.VAr.phsC.cVal.mag.f
473	MMXU6.MX.VA.phsA.cVal.mag.f
474	MMXU6.MX.VA.phsB.cVal.mag.f
475	MMXU6.MX.VA.phsC.cVal.mag.f
476	MMXU6.MX.PF.phsA.cVal.mag.f
477	MMXU6.MX.PF.phsB.cVal.mag.f
478	MMXU6.MX.PF.phsC.cVal.mag.f
479	GGIO4.MX.AnIn1.mag.f
480	GGIO4.MX.AnIn2.mag.f
481	GGIO4.MX.AnIn3.mag.f
482	GGIO4.MX.AnIn4.mag.f
483	GGIO4.MX.AnIn5.mag.f
484	GGIO4.MX.AnIn6.mag.f
485	GGIO4.MX.AnIn7.mag.f
486	GGIO4.MX.AnIn8.mag.f
487	GGIO4.MX.AnIn9.mag.f
488	GGIO4.MX.AnIn10.mag.f
489	GGIO4.MX.AnIn11.mag.f
490	GGIO4.MX.AnIn12.mag.f
491	GGIO4.MX.AnIn13.mag.f
492	GGIO4.MX.AnIn14.mag.f
493	GGIO4.MX.AnIn15.mag.f
494	GGIO4.MX.AnIn16.mag.f
495	GGIO4.MX.AnIn17.mag.f
496	GGIO4.MX.AnIn18.mag.f
497	GGIO4.MX.AnIn19.mag.f
498	GGIO4.MX.AnIn20.mag.f
499	GGIO4.MX.AnIn21.mag.f
500	GGIO4.MX.AnIn22.mag.f
501	GGIO4.MX.AnIn23.mag.f
502	GGIO4.MX.AnIn24.mag.f
503	GGIO4.MX.AnIn25.mag.f
504	GGIO4.MX.AnIn26.mag.f
505	GGIO4.MX.AnIn27.mag.f
506	GGIO4.MX.AnIn28.mag.f
507	GGIO4.MX.AnIn29.mag.f
508	GGIO4.MX.AnIn30.mag.f
509	GGIO4.MX.AnIn31.mag.f
510	GGIO4.MX.AnIn32.mag.f

F233
ENUMERATION: CONFIGURABLE GOOSE DATASET ITEMS FOR RECEPTION

value	GOOSE dataset item
0	None
1	GGIO3.ST.Ind1.q
2	GGIO3.ST.Ind1.stVal
3	GGIO3.ST.Ind2.q
4	GGIO3.ST.Ind2.stVal
↓	↓
127	GGIO1.ST.Ind64q
128	GGIO1.ST.Ind64.stVal
129	GGIO3.MX.AnIn1.mag.f
130	GGIO3.MX.AnIn2.mag.f
131	GGIO3.MX.AnIn3.mag.f
132	GGIO3.MX.AnIn4.mag.f
133	GGIO3.MX.AnIn5.mag.f
134	GGIO3.MX.AnIn6.mag.f
135	GGIO3.MX.AnIn7.mag.f
136	GGIO3.MX.AnIn8.mag.f
137	GGIO3.MX.AnIn9.mag.f
138	GGIO3.MX.AnIn10.mag.f
139	GGIO3.MX.AnIn11.mag.f
140	GGIO3.MX.AnIn12.mag.f
141	GGIO3.MX.AnIn13.mag.f
142	GGIO3.MX.AnIn14.mag.f
143	GGIO3.MX.AnIn15.mag.f
144	GGIO3.MX.AnIn16.mag.f

F234
ENUMERATION: WATTMETRIC GROUND FAULT VOLTAGE

value	voltage
0	Calculated VN
1	Measured VX

F235
ENUMERATION: WATTMETRIC GROUND FAULT CURRENT

value	current
0	Calculated IN
1	Measured IG

F237
ENUMERATION: REAL TIME CLOCK MONTH

value	month
0	January
1	February
2	March
3	April
4	May

value	month
5	June
6	July
7	August
8	September
9	October
10	November
11	December

F238
ENUMERATION: REAL TIME CLOCK DAY

value	day
0	Sunday
1	Monday
2	Tuesday
3	Wednesday
4	Thursday
5	Friday
6	Saturday

F239
ENUMERATION: REAL TIME CLOCK DAYLIGHT SAVINGS TIME START DAY INSTANCE

value	instance
0	First
1	Second
2	Third
3	Fourth
4	Last

F260
ENUMERATION: DATA LOGGER MODE

0 = Continuous, 1 = Trigger

F239
ENUMERATION: FAULT REPORT SYSTEM Z0 MAGNITUDE

value	magnitude
0	None
1	I0
2	V0

F300
UR_UINT16: FLEXLOGIC™ BASE TYPE (6-bit type)

The FlexLogic™ BASE type is 6 bits and is combined with a 9 bit descriptor and 1 bit for protection element to form a 16 bit value. The combined bits are of the form: PTTTTTTDDDDDDDDD, where P bit if set, indicates that the FlexLogic™ type is associated with a protection element state and T represents bits for the BASE type, and D represents bits for the descriptor.

The values in square brackets indicate the base type with P prefix [PTTTTTT] and the values in round brackets indicate the descriptor range.

[0] Off(0) – this is boolean FALSE value
[0] On (1) – this is boolean TRUE value
[2] CONTACT INPUTS (1 to 96)
[3] CONTACT INPUTS OFF (1 to 96)
[4] VIRTUAL INPUTS (1 to 64)
[6] VIRTUAL OUTPUTS (1 to 96)
[10] CONTACT OUTPUTS VOLTAGE DETECTED (1 to 64)
[11] CONTACT OUTPUTS VOLTAGE OFF DETECTED (1 to 64)
[12] CONTACT OUTPUTS CURRENT DETECTED (1 to 64)
[13] CONTACT OUTPUTS CURRENT OFF DETECTED (1 to 64)
[14] REMOTE INPUTS (1 to 32)
[28] INSERT (via keypad only)
[32] END
[34] NOT (1 INPUT)
[36] 2 INPUT XOR (0)
[38] LATCH SET/RESET (2 inputs)
[40] OR (2 to 16 inputs)
[42] AND (2 to 16 inputs)
[44] NOR (2 to 16 inputs)
[46] NAND (2 to 16 inputs)
[48] TIMER (1 to 32)
[50] ASSIGN VIRTUAL OUTPUT (1 to 96)
[52] SELF-TEST ERROR (see F141 for range)
[56] ACTIVE SETTING GROUP (1 to 6)
[62] MISCELLANEOUS EVENTS (see F146 for range)
[64 to 127] ELEMENT STATES

F400
UR_UINT16: CT/VT BANK SELECTION

bitmask	bank selection
0	Card 1 Contact 1 to 4
1	Card 1 Contact 5 to 8
2	Card 2 Contact 1 to 4
3	Card 2 Contact 5 to 8
4	Card 3 Contact 1 to 4
5	Card 3 Contact 5 to 8

F491
ENUMERATION: ANALOG INPUT MODE

0 = Default Value, 1 = Last Known

F500
UR_UINT16: PACKED BITFIELD

First register indicates input/output state with bits 0 (MSB) to 15 (LSB) corresponding to input/output state 1 to 16. The second register indicates input/output state with bits 0 to 15 corresponding to input/output state 17 to 32 (if required) The third register indicates input/output state with bits 0 to 15 corresponding to input/output state 33 to 48 (if required). The fourth register indicates input/output state with bits 0 to 15 corresponding to input/output state 49 to 64 (if required).

The number of registers required is determined by the specific data item. A bit value of 0 = Off and 1 = On.

F501
UR_UINT16: LED STATUS

Low byte of register indicates LED status with bit 0 representing the top LED and bit 7 the bottom LED. A bit value of 1 indicates the LED is on, 0 indicates the LED is off.

F502
BITFIELD: ELEMENT OPERATE STATES

Each bit contains the operate state for an element. See the F124 format code for a list of element IDs. The operate bit for element ID X is bit [X mod 16] in register [X/16].

F504
BITFIELD: 3-PHASE ELEMENT STATE

bitmask	element state
0	Pickup
1	Operate
2	Pickup Phase A
3	Pickup Phase B
4	Pickup Phase C
5	Operate Phase A
6	Operate Phase B
7	Operate Phase C

F505
BITFIELD: CONTACT OUTPUT STATE

0 = Contact State, 1 = Voltage Detected, 2 = Current Detected

F506|
BITFIELD: 1 PHASE ELEMENT STATE

0 = Pickup, 1 = Operate

F507
BITFIELD: COUNTER ELEMENT STATE

0 = Count Greater Than, 1 = Count Equal To, 2 = Count Less Than

F508
BITFIELD: DISTANCE ELEMENT STATE

bitmask	distance element state
0	Pickup
1	Operate
2	Pickup AB
3	Pickup BC
4	Pickup CA
5	Operate AB
6	Operate BC
7	Operate CA
8	Timed
9	Operate IAB
10	Operate IBC
11	Operate ICA

F509
BITFIELD: SIMPLE ELEMENT STATE

0 = Operate

F511
BITFIELD: 3-PHASE SIMPLE ELEMENT STATE

0 = Operate, 1 = Operate A, 2 = Operate B, 3 = Operate C

F513
ENUMERATION: POWER SWING MODE

0 = Two Step, 1 = Three Step

F514
ENUMERATION: POWER SWING TRIP MODE

0 = Delayed, 1 = Early

F515
ENUMERATION ELEMENT INPUT MODE

0 = Signed, 1 = Absolute

F516
ENUMERATION ELEMENT COMPARE MODE

0 = Level, 1 = Delta

F517
ENUMERATION: ELEMENT DIRECTION OPERATION

0 = Over, 1 = Under

F518
ENUMERATION: FLEXELEMENT™ UNITS

0 = Milliseconds, 1 = Seconds, 2 = Minutes

F519
ENUMERATION: NON-VOLATILE LATCH

0 = Reset-Dominant, 1 = Set-Dominant

F522
ENUMERATION: TRANSDUCER DCMA OUTPUT RANGE

0 = –1 to 1 mA; 1 = 0 to 1 mA; 2 = 4 to 20 mA

F523
ENUMERATION: DNP OBJECTS 20, 22, AND 23 DEFAULT VARIATION

bitmask	default variation
0	1
1	2
2	5
3	6

F524
ENUMERATION: DNP OBJECT 21 DEFAULT VARIATION

bitmask	Default Variation
0	1
1	2
2	9
3	10

F525
ENUMERATION: DNP OBJECT 32 DEFAULT VARIATION

bitmask	default variation
0	1
1	2
2	3
3	4
4	5
5	7

F530
ENUMERATION: FRONT PANEL INTERFACE KEYPRESS

bitmask	keypress
0	None
1	Menu
2	Message Up
3	7
4	8
5	9
6	Help
7	Message Left
8	4
9	5
10	6
11	Escape
12	Message Right
13	1
14	2
15	3
16	Enter
17	Message Down
18	0
19	Decimal
20	+/–
21	Value Up

bitmask	keypress
22	Value Down
23	Reset
24	User 1
25	User 2
26	User 3
31	User PB 1
32	User PB 2
33	User PB 3
34	User PB 4
35	User PB 5
36	User PB 6
37	User PB 7
38	User PB 8
39	User PB 9
40	User PB 10
41	User PB 11
42	User PB 12
44	User 4
45	User 5
46	User 6
47	User 7

F531
ENUMERATION: LANGUAGE

0 = English, 1 = French, 2 = Chinese, 3 = Russian

F534
ENUMERATION: 87PC TRIP SECURITY

0 = First Coincidence, 1 = Enhanced

F600
UR_UINT16: FLEXANALOG PARAMETER

Corresponds to the modbus address of the value used when this parameter is selected. Only certain values may be used as FlexAnalogs (basically all metering quantities used in protection).

C.1.1 INTRODUCTION

The IEC 61850 standard is the result of electric utilities and vendors of electronic equipment to produce standardized communications systems. IEC 61850 is a series of standards describing client/server and peer-to-peer communications, substation design and configuration, testing, environmental and project standards. The complete set includes:

- IEC 61850-1: Introduction and overview
- IEC 61850-2: Glossary
- IEC 61850-3: General requirements
- IEC 61850-4: System and project management
- IEC 61850-5: Communications and requirements for functions and device models
- IEC 61850-6: Configuration description language for communication in electrical substations related to IEDs
- IEC 61850-7-1: Basic communication structure for substation and feeder equipment - Principles and models
- IEC 61850-7-2: Basic communication structure for substation and feeder equipment - Abstract communication service interface (ACSI)
- IEC 61850-7-3: Basic communication structure for substation and feeder equipment – Common data classes
- IEC 61850-7-4: Basic communication structure for substation and feeder equipment – Compatible logical node classes and data classes
- IEC 61850-8-1: Specific Communication Service Mapping (SCSM) – Mappings to MMS (ISO 9506-1 and ISO 9506-2) and to ISO/IEC 8802-3
- IEC 61850-9-1: Specific Communication Service Mapping (SCSM) – Sampled values over serial unidirectional multidrop point to point link
- IEC 61850-9-2: Specific Communication Service Mapping (SCSM) – Sampled values over ISO/IEC 8802-3
- IEC 61850-10: Conformance testing

These documents can be obtained from the IEC (http://www.iec.ch). It is strongly recommended that all those involved with any IEC 61850 implementation obtain this document set.

C.1.2 COMMUNICATION PROFILES

IEC 61850 specifies the use of the Manufacturing Message Specification (MMS) at the upper (application) layer for transfer of real-time data. This protocol has been in existence for several of years and provides a set of services suitable for the transfer of data within a substation LAN environment. Actual MMS protocol services are mapped to IEC 61850 abstract services in IEC 61850-8-1.

The L60 relay supports IEC 61850 server services over both TCP/IP and TP4/CLNP (OSI) communication protocol stacks. The TP4/CLNP profile requires the L60 to have a network address or Network Service Access Point (NSAP) to establish a communication link. The TCP/IP profile requires the L60 to have an IP address to establish communications. These addresses are located in the **SETTINGS** ⇨ **PRODUCT SETUP** ⇨⇩ **COMMUNICATIONS** ⇨⇩ **NETWORK** menu. Note that the L60 supports IEC 61850 over the TP4/CLNP or TCP/IP stacks, and also operation over both stacks simultaneously. It is possible to have up to five simultaneous connections (in addition to DNP and Modbus/TCP (non-IEC 61850) connections).

- **Client/server**: This is a connection-oriented type of communication. The connection is initiated by the client, and communication activity is controlled by the client. IEC 61850 clients are often substation computers running HMI programs or SOE logging software. Servers are usually substation equipment such as protection relays, meters, RTUs, transformer tap changers, or bay controllers.
- **Peer-to-peer**: This is a non-connection-oriented, high speed type of communication usually between substation equipment such as protection relays. GSSE and GOOSE are methods of peer-to-peer communication.
- **Substation configuration language (SCL)**: A substation configuration language is a number of files used to describe the configuration of substation equipment. Each configured device has an *IEC Capability Description* (ICD) file. The substation single line information is stored in a *System Specification Description* (SSD) file. The entire substation configuration is stored in a *Substation Configuration Description* (SCD) file. The SCD file is the combination of the individual ICD files and the SSD file.

C.2.1 OVERVIEW

IEC 61850 defines an object-oriented approach to data and services. An IEC 61850 *physical device* can contain one or more *logical device(s)*. Each logical device can contain many *logical nodes*. Each logical node can contain many *data objects*. Each data object is composed of *data attributes* and *data attribute components*. Services are available at each level for performing various functions, such as reading, writing, control commands, and reporting.

Each L60 IED represents one IEC 61850 physical device. The physical device contains one logical device, and the logical device contains many logical nodes. The logical node LPHD1 contains information about the L60 IED physical device. The logical node LLN0 contains information about the L60 IED logical device.

C.2.2 GGIO1: DIGITAL STATUS VALUES

The GGIO1 logical node is available in the L60 to provide access to as many 128 digital status points and associated time-stamps and quality flags. The data content must be configured before the data can be used. GGIO1 provides digital status points for access by clients.

It is intended that clients use GGIO1 in order to access digital status values from the L60. Configuration settings are provided to allow the selection of the number of digital status indications available in GGIO1 (8 to 128), and to allow the choice of the L60 FlexLogic™ operands that drive the status of the GGIO1 status indications. Clients can utilize the IEC 61850 buffered and unbuffered reporting features available from GGIO1 in order to build sequence of events (SOE) logs and HMI display screens. Buffered reporting should generally be used for SOE logs since the buffering capability reduces the chances of missing data state changes. Unbuffered reporting should generally be used for local status display.

C.2.3 GGIO2: DIGITAL CONTROL VALUES

The GGIO2 logical node is available to provide access to the L60 virtual inputs. Virtual inputs are single-point control (binary) values that can be written by clients. They are generally used as control inputs. GGIO2 provides access to the virtual inputs through the IEC 61850 standard control model (ctlModel) services:

- Status only
- Direct control with normal security
- SBO control with normal security

Configuration settings are available to select the control model for each point. Each virtual input used through GGIO2 should have its **VIRTUAL INPUT 1(64) FUNCTION** setting programmed as “Enabled” and its corresponding **GGIO2 CF SPSCO1(64) CTLMODEL** setting programmed to the appropriate control configuration.

C.2.4 GGIO3: DIGITAL STATUS AND ANALOG VALUES FROM RECEIVED GOOSE DATA

The GGIO3 logical node is available to provide access for clients to values received via configurable GOOSE messages. The values of the digital status indications and analog values in GGIO3 originate in GOOSE messages sent from other devices.

C.2.5 GGIO4: GENERIC ANALOG MEASURED VALUES

The GGIO4 logical node provides access to as many as 32 analog value points, as well as associated timestamps and quality flags. The data content must be configured before the data can be used. GGIO4 provides analog values for access by clients.

It is intended that clients use GGIO4 to access generic analog values from the L60. Configuration settings allow the selection of the number of analog values available in GGIO4 (4 to 32) and the choice of the FlexAnalog™ values that determine the value of the GGIO4 analog inputs. Clients can utilize polling or the IEC 61850 unbuffered reporting feature available from GGIO4 in order to obtain the analog values provided by GGIO4.

C.2.6 MMXU: ANALOG MEASURED VALUES

A limited number of measured analog values are available through the MMXU logical nodes.

Each MMXU logical node provides data from a L60 current and voltage source. There is one MMXU available for each configurable source (programmed in the **SETTINGS** ⇨⇩ **SYSTEM SETUP** ⇨⇩ **SIGNAL SOURCES** menu). MMXU1 provides data from L60 source 1, and MMXU2 provides data from L60 source 2.

MMXU data is provided in two forms: instantaneous and deadband. The instantaneous values are updated every time a read operation is performed by a client. The deadband values are calculated as described in IEC 61850 parts 7-1 and 7-3. The selection of appropriate deadband settings for the L60 is described in chapter 5 of this manual.

IEC 61850 buffered and unbuffered reporting capability is available in all MMXU logical nodes. MMXUx logical nodes provide the following data for each source:

- MMXU1.MX.TotW: three-phase real power
- MMXU1.MX.TotVAr: three-phase reactive power
- MMXU1.MX.TotVA: three-phase apparent power
- MMXU1.MX.TotPF: three-phase power factor
- MMXU1.MX.Hz: frequency
- MMXU1.MX.PPV.phsAB: phase AB voltage magnitude and angle
- MMXU1.MX.PPV.phsBC: phase BC voltage magnitude and angle
- MMXU1.MX.PPV.phsCA: Phase CA voltage magnitude and angle
- MMXU1.MX.PhV.phsA: phase AG voltage magnitude and angle
- MMXU1.MX.PhV.phsB: phase BG voltage magnitude and angle
- MMXU1.MX.PhV.phsC: phase CG voltage magnitude and angle
- MMXU1.MX.A.phsA: phase A current magnitude and angle
- MMXU1.MX.A.phsB: phase B current magnitude and angle
- MMXU1.MX.A.phsC: phase C current magnitude and angle
- MMXU1.MX.A.neut: ground current magnitude and angle
- MMXU1.MX.W.phsA: phase A real power
- MMXU1.MX.W.phsB: phase B real power
- MMXU1.MX.W.phsC: phase C real power
- MMXU1.MX.VAr.phsA: phase A reactive power
- MMXU1.MX.VAr.phsB: phase B reactive power
- MMXU1.MX.VAr.phsC: phase C reactive power
- MMXU1.MX.VA.phsA: phase A apparent power
- MMXU1.MX.VA.phsB: phase B apparent power
- MMXU1.MX.VA.phsC: phase C apparent power
- MMXU1.MX.PF.phsA: phase A power factor
- MMXU1.MX.PF.phsB: phase B power factor
- MMXU1.MX.PF.phsC: phase C power factor

C.2.7 PROTECTION AND OTHER LOGICAL NODES

The following list describes the protection elements for all UR-series relays. The L60 relay will contain a subset of protection elements from this list.

- PDIF: bus differential, transformer instantaneous differential, transformer percent differential

- PDIS: phase distance, ground distance
- PIOC: phase instantaneous overcurrent, neutral instantaneous overcurrent, ground instantaneous overcurrent, negative-sequence instantaneous overcurrent.
- PTOC: phase time overcurrent, neutral time overcurrent, ground time overcurrent, negative-sequence time overcurrent, neutral directional overcurrent, negative-sequence directional overcurrent
- PTUV: phase undervoltage, auxiliary undervoltage, third harmonic neutral undervoltage
- PTOV: phase overvoltage, neutral overvoltage, auxiliary overvoltage, negative sequence overvoltage
- RBRF: breaker failure
- RREC: autoreclosure
- RPSB: power swing detection
- RFLO: fault locator
- XCBR: breaker control

The protection elements listed above contain *start* (pickup) and *operate* flags. For example, the start flag for PIOC1 is PIOC1.ST.Str.general. The operate flag for PIOC1 is PIOC1.ST.Op.general. For the L60 protection elements, these flags take their values from the pickup and operate FlexLogic™ operands for the corresponding element.

Some protection elements listed above contain directional start values. For example, the directional start value for PDIS1 is PDIS1.ST.Str.dirGeneral. This value is built from the directional FlexLogic™ operands for the element.

The RFLO logical node contains the measurement of the distance to fault calculation in kilometers. This value originates in the fault locator function.

The XCBR logical node is directly associated with the breaker control feature.

- XCBR1.ST.Loc: This is the state of the XCBR1 local/remote switch. A setting is provided to assign a FlexLogic™ operand to determine the state. When local mode is true, IEC 61850 client commands will be rejected.
- XCBR1.ST.Opcnt: This is an operation counter as defined in IEC 61850. Command settings are provided to allow the counter to be cleared.
- XCBR1.ST.Pos: This is the position of the breaker. The breaker control FlexLogic™ operands are used to determine this state. If the breaker control logic indicates that the breaker, or any single pole of the breaker, is closed, then the breaker position state is “on”. If the breaker control logic indicates that the breaker is open, then the breaker position state is “off”.
- XCBR1.ST.BlkOpn: This is the state of the block open command logic. When true, breaker open commands from IEC 61850 clients will be rejected.
- XCBR1.ST.BlkCls: This is the state of the block close command logic. When true, breaker close commands from IEC 61850 clients will be rejected.
- XCBR1.CO.Pos: This is where IEC 61850 clients can issue open or close commands to the breaker. SBO control with normal security is the only supported IEC 61850 control model.
- XCBR1.CO.BlkOpn: This is where IEC 61850 clients can issue block open commands to the breaker. Direct control with normal security is the only supported IEC 61850 control model.
- XCBR1.CO.BlkCls: This is where IEC 61850 clients can issue block close commands to the breaker. Direct control with normal security is the only supported IEC 61850 control model.

C.3.1 BUFFERED/UNBUFFERED REPORTING

IEC 61850 buffered and unbuffered reporting is provided in the GGIO1 logical nodes (for binary status values) and MMXU1 to MMXU6 (for analog measured values). Report settings can be configured using the EnerVista UR Setup software, substation configurator software, or via an IEC 61850 client. The following items can be configured:

- **TrgOps**: Trigger options. The following bits are supported by the L60:
  - Bit 1: data-change
  - Bit 4: integrity
  - Bit 5: general interrogation
- **OptFlds**: Option Fields. The following bits are supported by the L60:
  - Bit 1: sequence-number
  - Bit 2: report-time-stamp
  - Bit 3: reason-for-inclusion
  - Bit 4: data-set-name
  - Bit 5: data-reference
  - Bit 6: buffer-overflow (for buffered reports only)
  - Bit 7: entryID (for buffered reports only)
  - Bit 8: conf-revision
  - Bit 9: segmentation
- **IntgPd**: Integrity period.
- **BufTm**: Buffer time.

C.3.2 FILE TRANSFER

MMS file services are supported to allow transfer of oscillography, event record, or other files from a L60 relay.

C.3.3 TIMESTAMPS AND SCANNING

The timestamp values associated with all IEC 61850 data items represent the *time of the last change* of either the value or quality flags of the data item. To accomplish this functionality, all IEC 61850 data items must be regularly scanned for data changes, and the timestamp updated when a change is detected, regardless of the connection status of any IEC 61850 clients. For applications where there is no IEC 61850 client in use, the IEC 61850 **SERVER SCANNING** setting can be programmed as "Disabled". If a client is in use, this setting should be programmed as "Enabled" to ensure the proper generation of IEC 61850 timestamps.

C.3.4 LOGICAL DEVICE NAME

The logical device name is used to identify the IEC 61850 logical device that exists within the L60. This name is composed of two parts: the IED name setting and the logical device instance. The complete logical device name is the combination of the two character strings programmed in the **IEDNAME** and **LD INST** settings. The default values for these strings are "IEDName" and "LDInst". These values should be changed to reflect a logical naming convention for all IEC 61850 logical devices in the system.

C.3.5 LOCATION

The LPHD1 logical node contains a data attribute called *location* (LPHD1.DC.PhyNam.location). This is a character string meant to describe the physical location of the L60. This attribute is programmed through the **LOCATION** setting and its default value is "Location". This value should be changed to describe the actual physical location of the L60.

C.3.6 LOGICAL NODE NAME PREFIXES

IEC 61850 specifies that each logical node can have a name with a total length of 11 characters. The name is composed of:

- a five or six-character name prefix.
- a four-character standard name (for example, MMXU, GGIO, PIOC, etc.).
- a one or two-character instantiation index.

Complete names are of the form `xxxxxxPIOC1`, where the `xxxxxx` character string is configurable. Details regarding the logical node naming rules are given in IEC 61850 parts 6 and 7-2. It is recommended that a consistent naming convention be used for an entire substation project.

C.3.7 CONNECTION TIMING

A built-in TCP/IP connection timeout of two minutes is employed by the L60 to detect 'dead' connections. If there is no data traffic on a TCP connection for greater than two minutes, the connection will be aborted by the L60. This frees up the connection to be used by other clients. Therefore, when using IEC 61850 reporting, clients should configure report control block items such that an integrity report will be issued at least every 2 minutes (120000 ms). This ensures that the L60 will not abort the connection. If other MMS data is being polled on the same connection at least once every 2 minutes, this timeout will not apply.

C.3.8 NON-IEC 61850 DATA

The L60 relay makes available a number of non-IEC 61850 data items. These data items can be accessed through the "UR" MMS domain. IEC 61850 data can be accessed through the standard IEC 61850 logical device. To access the non-IEC data items, the **INCLUDE NON-IEC DATA** setting must be "Enabled".

C.3.9 COMMUNICATION SOFTWARE UTILITIES

The exact structure and values of the supported IEC 61850 logical nodes can be seen by connecting to a L60 relay with an MMS browser, such as the "MMS Object Explorer and AXS4-MMS" DDE/OPC server from Sisco Inc.

C.4.1 OVERVIEW

IEC 61850 specifies two types of peer-to-peer data transfer services: Generic Substation State Events (GSSE) and Generic Object Oriented Substation Events (GOOSE). GSSE services are compatible with UCA 2.0 GOOSE. IEC 61850 GOOSE services provide virtual LAN (VLAN) support, Ethernet priority tagging, and Ethertype Application ID configuration. The support for VLANs and priority tagging allows for the optimization of Ethernet network traffic. GOOSE messages can be given a higher priority than standard Ethernet traffic, and they can be separated onto specific VLANs. Because of the additional features of GOOSE services versus GSSE services, it is recommended that GOOSE be used wherever backwards compatibility with GSSE (or UCA 2.0 GOOSE) is not required.

Devices that transmit GSSE and/or GOOSE messages also function as servers. Each GSSE publisher contains a "GSSE control block" to configure and control the transmission. Each GOOSE publisher contains a "GOOSE control block" to configure and control the transmission. The transmission is also controlled via device settings. These settings can be seen in the ICD and/or SCD files, or in the device configuration software or files.

IEC 61850 recommends a default priority value of 4 for GOOSE. Ethernet traffic that does not contain a priority tag has a default priority of 1. More details are specified in IEC 61850 part 8-1.

IEC 61850 recommends that the Ethertype Application ID number be configured according to the GOOSE source. In the L60, the transmitted GOOSE Application ID number must match the configured receive Application ID number in the receiver. A common number may be used for all GOOSE transmitters in a system. More details are specified in IEC 61850 part 8-1.

C.4.2 GSSE CONFIGURATION

IEC 61850 Generic Substation Status Event (GSSE) communication is compatible with UCA GOOSE communication. GSSE messages contain a number of double point status data items. These items are transmitted in two pre-defined data structures named DNA and UserSt. Each DNA and UserSt item is referred to as a 'bit pair'. GSSE messages are transmitted in response to state changes in any of the data points contained in the message. GSSE messages always contain the same number of DNA and UserSt bit pairs. Depending the on the configuration, only some of these bit pairs may have values that are of interest to receiving devices.

The **GSSE FUNCTION**, **GSSE ID**, and **GSSE DESTINATION MAC ADDRESS** settings are used to configure GSSE transmission. **GSSE FUNCTION** is set to "Enabled" to enable the transmission. If a valid multicast Ethernet MAC address is entered for the **GSSE DESTINATION MAC ADDRESS** setting, this address will be used as the destination MAC address for GSSE messages. If a valid multicast Ethernet MAC address is not entered (for example, 00 00 00 00 00 00), the L60 will use the source Ethernet MAC address as the destination, with the multicast bit set.

C.4.3 FIXED GOOSE

The L60 supports two types of IEC 61850 Generic Object Oriented Substation Event (GOOSE) communication: fixed GOOSE and configurable GOOSE. All GOOSE messages contain IEC 61850 data collected into a *dataset*. It is this dataset that is transferred using GOOSE message services. The dataset transferred using the L60 fixed GOOSE is the same data that is transferred using the GSSE feature; that is, the DNA and UserSt bit pairs. The FlexLogic™ operands that determine the state of the DNA and UserSt bit pairs are configurable via settings, but the fixed GOOSE dataset always contains the same DNA/UserSt data structure. Upgrading from GSSE to GOOSE services is simply a matter of enabling fixed GOOSE and disabling GSSE. The remote inputs and outputs are configured in the same manner for both GSSE and fixed GOOSE.

It is recommended that the fixed GOOSE be used for implementations that require GOOSE data transfer between UR-series IEDs. Configurable GOOSE may be used for implementations that require GOOSE data transfer between UR-series IEDs and devices from other manufacturers.

C.4.4 CONFIGURABLE GOOSE

The configurable GOOSE feature allows for the configuration of the datasets to be transmitted or received from the L60. The L60 supports the configuration of eight (8) transmission and reception datasets, allowing for the optimization of data transfer between devices.

Items programmed for dataset 1 will have changes in their status transmitted as soon as the change is detected. Dataset 1 should be used for high-speed transmission of data that is required for applications such as transfer tripping, blocking, and breaker fail initiate. At least one digital status value needs to be configured in dataset 1 to enable transmission of all data configured for dataset 1. Configuring analog data only to dataset 1 will not activate transmission.

Items programmed for datasets 2 through 8 will have changes in their status transmitted at a maximum rate of every 100 ms. Datasets 2 through 8 will regularly analyze each data item configured within them every 100 ms to identify if any changes have been made. If any changes in the data items are detected, these changes will be transmitted through a GOOSE message. If there are no changes detected during this 100 ms period, no GOOSE message will be sent.

For all datasets 1 through 8, the integrity GOOSE message will still continue to be sent at the pre-configured rate even if no changes in the data items are detected.

The GOOSE functionality was enhanced to prevent the relay from flooding a communications network with GOOSE messages due to an oscillation being created that is triggering a message.

The L60 has the ability of detecting if a data item in one of the GOOSE datasets is erroneously oscillating. This can be caused by events such as errors in logic programming, inputs improperly being asserted and de-asserted, or failed station components. If erroneously oscillation is detected, the L60 will stop sending GOOSE messages from the dataset for a minimum period of one second. Should the oscillation persist after the one second time-out period, the L60 will continue to block transmission of the dataset. The L60 will assert the **MAINTENANCE ALERT: GGIO Ind XXX oscill** self-test error message on the front panel display, where **XXX** denotes the data item detected as oscillating.

The configurable GOOSE feature is recommended for applications that require GOOSE data transfer between UR-series IEDs and devices from other manufacturers. Fixed GOOSE is recommended for applications that require GOOSE data transfer between UR-series IEDs.

IEC 61850 GOOSE messaging contains a number of configurable parameters, all of which must be correct to achieve the successful transfer of data. It is critical that the configured datasets at the transmission and reception devices are an exact match in terms of data structure, and that the GOOSE addresses and name strings match exactly. Manual configuration is possible, but third-party substation configuration software may be used to automate the process. The EnerVista UR Setup software can produce IEC 61850 ICD files and import IEC 61850 SCD files produced by a substation configurator (refer to the *IEC 61850 IED configuration* section later in this appendix).

The following example illustrates the configuration required to transfer IEC 61850 data items between two devices. The general steps required for transmission configuration are:

1. Configure the transmission dataset.
2. Configure the GOOSE service settings.
3. Configure the data.

The general steps required for reception configuration are:

1. Configure the reception dataset.
2. Configure the GOOSE service settings.
3. Configure the data.

This example shows how to configure the transmission and reception of three IEC 61850 data items: a single point status value, its associated quality flags, and a floating point analog value.

The following procedure illustrates the transmission configuration.

1. Configure the transmission dataset by making the following changes in the **PRODUCT SETUP** ⇨⇩ **COMMUNICATION** ⇨⇩ **IEC 61850 PROTOCOL** ⇨ **GSSE/GOOSE CONFIGURATION** ⇨ **TRANSMISSION** ⇨⇩ **CONFIGURABLE GOOSE** ⇨ **CONFIGURABLE GOOSE 1** ⇨⇩ **CONFIG GSE 1 DATASET ITEMS** settings menu:
   - Set **ITEM 1** to “GGIO1.ST.Ind1.q” to indicate quality flags for GGIO1 status indication 1.
   - Set **ITEM 2** to “GGIO1.ST.Ind1.stVal” to indicate the status value for GGIO1 status indication 1.

   The transmission dataset now contains a set of quality flags and a single point status Boolean value. The reception dataset on the receiving device must exactly match this structure.
2. Configure the GOOSE service settings by making the following changes in the **PRODUCT SETUP** ⇨⇩ **COMMUNICATION** ⇨⇩ **IEC 61850 PROTOCOL** ⇨ **GSSE/GOOSE CONFIGURATION** ⇨ **TRANSMISSION** ⇨⇩ **CONFIGURABLE GOOSE** ⇨ **CONFIGURABLE GOOSE 1** settings menu:

– Set **CONFIG GSE 1 FUNCTION** to “Enabled”.

– Set **CONFIG GSE 1 ID** to an appropriate descriptive string (the default value is “GOOSEOut_1”).

– Set **CONFIG GSE 1 DST MAC** to a multicast address (for example, 01 00 00 12 34 56).

– Set the **CONFIG GSE 1 VLAN PRIORITY**; the default value of “4” is OK for this example.

– Set the **CONFIG GSE 1 VLAN ID** value; the default value is “0”, but some switches may require this value to be “1”.

– Set the **CONFIG GSE 1 ETYPE APPID** value. This setting represents the Ethertype application ID and must match the configuration on the receiver (the default value is “0”).

– Set the **CONFIG GSE 1 CONFREV** value. This value changes automatically as described in IEC 61850 part 7-2. For this example it can be left at its default value.

3. Configure the data by making the following changes in the **PRODUCT SETUP ⇨⇩ COMMUNICATION ⇨⇩ IEC 61850 PROTOCOL ⇨ GGIO1 STATUS CONFIGURATION** settings menu:

   – Set **GGIO1 INDICATION 1** to a FlexLogic™ operand used to provide the status of GGIO1.ST.Ind1.stVal (for example, a contact input, virtual input, a protection element status, etc.).

The L60 must be rebooted (control power removed and re-applied) before these settings take effect.

The following procedure illustrates the reception configuration.

1. Configure the reception dataset by making the following changes in the **PRODUCT SETUP ⇨⇩ COMMUNICATION ⇨⇩ IEC 61850 PROTOCOL ⇨ GSSE/GOOSE CONFIGURATION ⇨⇩ RECEPTION ⇨⇩ CONFIGURABLE GOOSE ⇨ CONFIGURABLE GOOSE 1 ⇨⇩ CONFIG GSE 1 DATASET ITEMS** settings menu:

   – Set **ITEM 1** to “GGIO3.ST.Ind1.q” to indicate quality flags for GGIO3 status indication 1.

   – Set **ITEM 2** to “GGIO3.ST.Ind1.stVal” to indicate the status value for GGIO3 status indication 1.

   The reception dataset now contains a set of quality flags, a single point status Boolean value, and a floating point analog value. This matches the transmission dataset configuration above.

2. Configure the GOOSE service settings by making the following changes in the **INPUTS/OUTPUTS ⇨⇩ REMOTE DEVICES ⇨⇩ REMOTE DEVICE 1** settings menu:

   – Set **REMOTE DEVICE 1 ID** to match the GOOSE ID string for the transmitting device. Enter “GOOSEOut_1”.

   – Set **REMOTE DEVICE 1 ETYPE APPID** to match the Ethertype application ID from the transmitting device. This is “0” in the example above.

   – Set the **REMOTE DEVICE 1 DATASET** value. This value represents the dataset number in use. Since we are using configurable GOOSE 1 in this example, program this value as “GOOSEIn 1”.

3. Configure the data by making the following changes in the **INPUTS/OUTPUTS ⇨⇩ REMOTE INPUTS ⇨⇩ REMOTE INPUT 1** settings menu:

   – Set **REMOTE IN 1 DEVICE** to “GOOSEOut_1”.

   – Set **REMOTE IN 1 ITEM** to “Dataset Item 2”. This assigns the value of the GGIO3.ST.Ind1.stVal single point status item to remote input 1.

Remote input 1 can now be used in FlexLogic™ equations or other settings. The L60 must be rebooted (control power removed and re-applied) before these settings take effect.

The value of remote input 1 (Boolean on or off) in the receiving device will be determined by the GGIO1.ST.Ind1.stVal value in the sending device. The above settings will be automatically populated by the EnerVista UR Setup software when a complete SCD file is created by third party substation configurator software.

C.4.5 ETHERNET MAC ADDRESS FOR GSSE/GOOSE

Ethernet capable devices each contain a unique identifying address called a Media Access Control (MAC) address. This address cannot be changed and is unique for each Ethernet device produced worldwide. The address is six bytes in length and is usually represented as six hexadecimal values (for example, 00 A0 F4 01 02 03). It is used in all Ethernet frames as the ‘source’ address of the frame. Each Ethernet frame also contains a *destination* address. The destination address can be different for each Ethernet frame depending on the intended destination of the frame.

A special type of destination address called a *multicast* address is used when the Ethernet frame can be received by more than one device. An Ethernet MAC address is multicast when the least significant bit of the first byte is set (for example, 01 00 00 00 00 00 is a multicast address).

GSSE and GOOSE messages must have multicast destination MAC addresses.

By default, the L60 is configured to use an automated multicast MAC scheme. If the L60 destination MAC address setting is not a valid multicast address (that is, the least significant bit of the first byte is not set), the address used as the destination MAC will be the same as the local MAC address, but with the multicast bit set. Thus, if the local MAC address is 00 A0 F4 01 02 03, then the destination MAC address will be 01 A0 F4 01 02 03.

C.4.6 GSSE ID AND GOOSE ID SETTINGS

GSSE messages contain an identifier string used by receiving devices to identify the sender of the message, defined in IEC 61850 part 8-1 as GsID. This is a programmable 65-character string. This string should be chosen to provide a descriptive name of the originator of the GSSE message.

GOOSE messages contain an identifier string used by receiving devices to identify the sender of the message, defined in IEC 61850 part 8-1 as GoID. This programmable 65-character string should be a descriptive name of the originator of the GOOSE message. GOOSE messages also contain two additional character strings used for identification of the message: DatSet - the name of the associated dataset, and GoCBRef - the reference (name) of the associated GOOSE control block. These strings are automatically populated and interpreted by the L60; no settings are required.

C.5.1 OVERVIEW

The L60 can be configured for IEC 61850 via the EnerVista UR Setup software as follows.

1. An ICD file is generated for the L60 by the EnerVista UR Setup software that describe the capabilities of the IED.
2. The ICD file is then imported into a system configurator along with other ICD files for other IEDs (from GE or other vendors) for system configuration.
3. The result is saved to a SCD file, which is then imported back to EnerVista UR Setup to create one or more settings file(s). The settings file(s) can then be used to update the relay(s) with the new configuration information.

The configuration process is illustrated below.

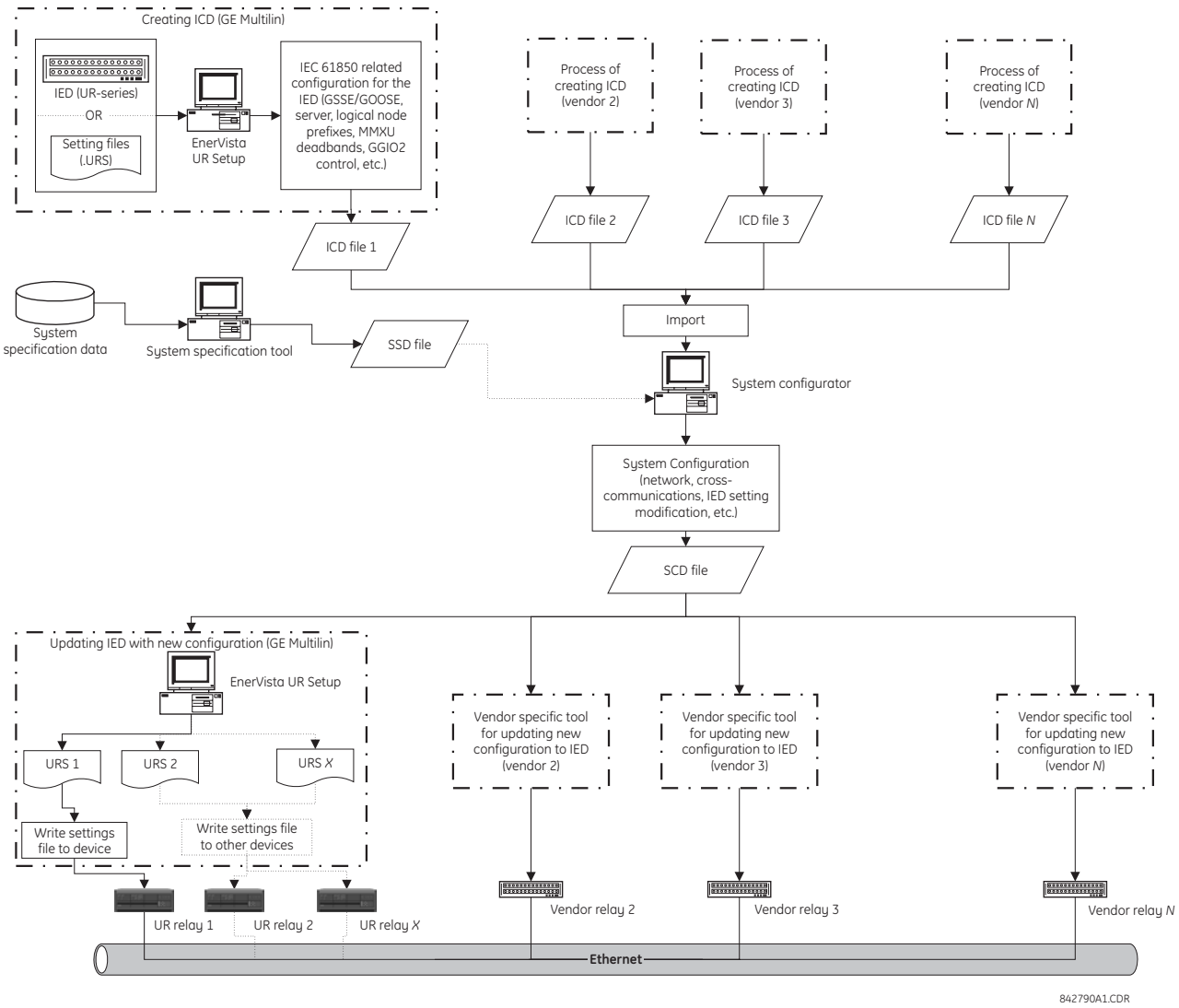


Figure 0–1: IED CONFIGURATION PROCESS

The following acronyms and abbreviations are used in the procedures describing the IED configuration process for IEC 61850:

- BDA: Basic Data Attribute, that is not structured
- DAI: Instantiated Data Attribute
- DO: Data Object type or instance, depending on the context

- DOI: Instantiated Data Object
- IED: Intelligent Electronic Device
- LDInst: Instantiated Logical Device
- LNInst: Instantiated Logical Node
- SCL: Substation Configuration Description Language. The configuration language is an application of the Extensible Markup Language (XML) version 1.0.
- SDI: Instantiated Sub DATA; middle name part of a structured DATA name
- UR: GE Multilin Universal Relay series
- URI: Universal Resource Identifier
- URS: UR-series relay setting file
- XML: Extensible Markup Language

The following SCL variants are also used:

- ICD: IED Capability Description
- CID: Configured IED Description
- SSD: System Specification Description
- SCD: Substation Configuration Description

The following IEC related tools are referenced in the procedures that describe the IED configuration process for IEC 61850:

- **System configurator** or **Substation configurator**: This is an IED independent system level tool that can import or export configuration files defined by IEC 61850-6. It can import configuration files (ICD) from several IEDs for system level engineering and is used to add system information shared by different IEDs. The system configuration generates a substation related configuration file (SCD) which is fed back to the IED configurator (for example, EnerVista UR Setup) for system related IED configuration. The system configurator should also be able to read a system specification file (SSD) to use as base for starting system engineering, or to compare it with an engineered system for the same substation.
- **IED configurator**: This is a vendor specific tool that can directly or indirectly generate an ICD file from the IED (for example, from a settings file). It can also import a system SCL file (SCD) to set communication configuration parameters (that is, required addresses, reception GOOSE datasets, IDs of incoming GOOSE datasets, etc.) for the IED. The IED configurator functionality is implemented in the GE Multilin EnerVista UR Setup software.

C.5.2 CONFIGURING IEC 61850 SETTINGS

Before creating an ICD file, the user can customize the IEC 61850 related settings for the IED. For example, the IED name and logical device instance can be specified to uniquely identify the IED within the substation, or transmission GOOSE datasets created so that the system configurator can configure the cross-communication links to send GOOSE messages from the IED. Once the IEC 61850 settings are configured, the ICD creation process will recognize the changes and generate an ICD file that contains the updated settings.

Some of the IED settings will be modified during they system configuration process. For example, a new IP address may be assigned, line items in a Transmission GOOSE dataset may be added or deleted, or prefixes of some logical nodes may be changed. While all new configurations will be mapped to the L60 settings file when importing an SCD file, all unchanged settings will preserve the same values in the new settings file.

These settings can be configured either directly through the relay panel or through the EnerVista UR Setup software (preferred method). The full list of IEC 61850 related settings for are as follows:

- Network configuration: IP address, IP subnet mask, and default gateway IP address (access through the **Settings > Product Setup > Communications > Network** menu tree in EnerVista UR Setup).
- Server configuration: IED name and logical device instance (access through the **Settings > Product Setup > Communications > IEC 61850 > Server Configuration** menu tree in EnerVista UR Setup).
- Logical node prefixes, which includes prefixes for all logical nodes except LLN0 (access through the **Settings > Product Setup > Communications > IEC 61850 > Logical Node Prefixes** menu tree in EnerVista UR Setup).

- MMXU deadbands, which includes deadbands for all available MMXUs. The number of MMXUs is related to the number of CT/VT modules in the relay. There are two MMXUs for each CT/VT module. For example, if a relay contains two CT/VT modules, there will be four MMXUs available (access through the **Settings > Product Setup > Communications > IEC 61850 > MMXU Deadbands** menu tree in EnerVista UR Setup).
- GGIO1 status configuration, which includes the number of status points in GGIO1 as well as the potential internal mappings for each GGIO1 indication. However only the number of status points will be used in the ICD creation process (access through the **Settings > Product Setup > Communications > IEC 61850 > GGIO1 Status Configuration** menu tree in EnerVista UR Setup).
- GGIO2 control configuration, which includes ctlModels for all SPCSOs within GGIO2 (access through the **Settings > Product Setup > Communications > IEC 61850 > GGIO2 Control Configuration** menu tree in EnerVista UR Setup).
- Configurable transmission GOOSE, which includes eight configurable datasets that can be used for GOOSE transmission. The GOOSE ID can be specified for each dataset (it must be unique within the IED as well as across the whole substation), as well as the destination MAC address, VLAN priority, VLAN ID, ETYPE APPID, and the dataset items. The selection of the dataset item is restricted by firmware version; for version 5.4x, only GGIO1.ST.Indx.stVal and GGIO1.ST.Indx.q are valid selection (where *x* is between 1 to *N*, and *N* is determined by number of GGIO1 status points). Although configurable transmission GOOSE can also be created and altered by some third-party system configurators, we recommend configuring transmission GOOSE for GE Multilin IEDs before creating the ICD, and strictly within EnerVista UR Setup software or the front panel display (access through the **Settings > Product Setup > Communications > IEC 61850 > GSSE/GOOSE Configuration > Transmission > Tx Configurable GOOSE** menu tree in EnerVista UR Setup).
- Configurable reception GOOSE, which includes eight configurable datasets that can be used for GOOSE reception. However, unlike datasets for transmission, datasets for reception only contains dataset items, and they are usually created automatically by process of importing the SCD file (access through the **Settings > Product Setup > Communications > IEC 61850 > GSSE/GOOSE Configuration > Reception > Rx Configurable GOOSE** menu tree in EnerVista UR Setup).
- Remote devices configuration, which includes remote device ID (GOOSE ID or GoID of the incoming transmission GOOSE dataset), ETYPE APPID (of the GSE communication block for the incoming transmission GOOSE), and DATASET (which is the name of the associated reception GOOSE dataset). These settings are usually done automatically by process of importing SCD file (access through the **Settings > Inputs/Outputs > Remote Devices** menu tree in EnerVista UR Setup).
- Remote inputs configuration, which includes device (remote device ID) and item (which dataset item in the associated reception GOOSE dataset to map) values. Only the items with cross-communication link created in SCD file should be mapped. These configurations are usually done automatically by process of importing SCD file (access through the **Settings > Inputs/Outputs > Remote Inputs** menu tree in EnerVista UR Setup).

C.5.3 ABOUT ICD FILES

The SCL language is based on XML, and its syntax definition is described as a W3C XML Schema. ICD is one type of SCL file (which also includes SSD, CID and SCD files). The ICD file describes the capabilities of an IED and consists of four major sections:

- Header
- Communication
- IEDs
- DataTypeTemplates

The root file structure of an ICD file is illustrated below.

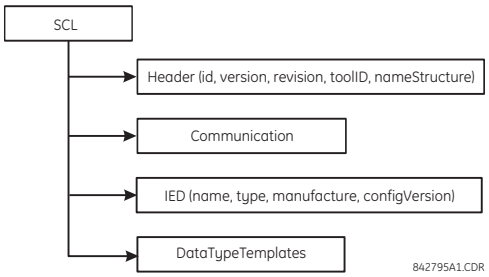


Figure 0–2: ICD FILE STRUCTURE, SCL (ROOT) NODE

The **Header** node identifies the ICD file and its version, and specifies options for the mapping of names to signals

The **Communication** node describes the direct communication connection possibilities between logical nodes by means of logical buses (sub-networks) and IED access ports. The communication section is structured as follows.

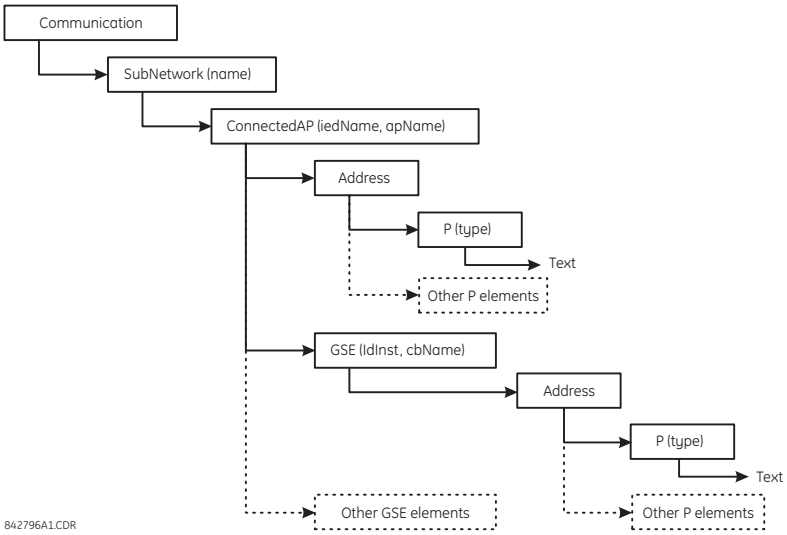


Figure 0–3: ICD FILE STRUCTURE, COMMUNICATIONS NODE

The **SubNetwork** node contains all access points which can (logically) communicate with the sub-network protocol and without the intervening router. The **ConnectedAP** node describes the IED access point connected to this sub-network. The **Address** node contains the address parameters of the access point. The **GSE** node provides the address element for stating the control block related address parameters, where **ldInst** is the instance identification of the logical device within the IED on which the control block is located, and **cbName** is the name of the control block.

The **IED** node describes the (pre-)configuration of an IED: its access points, the logical devices, and logical nodes instantiated on it. Furthermore, it defines the capabilities of an IED in terms of communication services offered and, together with its **LNType**, instantiated data (DO) and its default or configuration values. There should be only one IED section in an ICD since it only describes one IED.

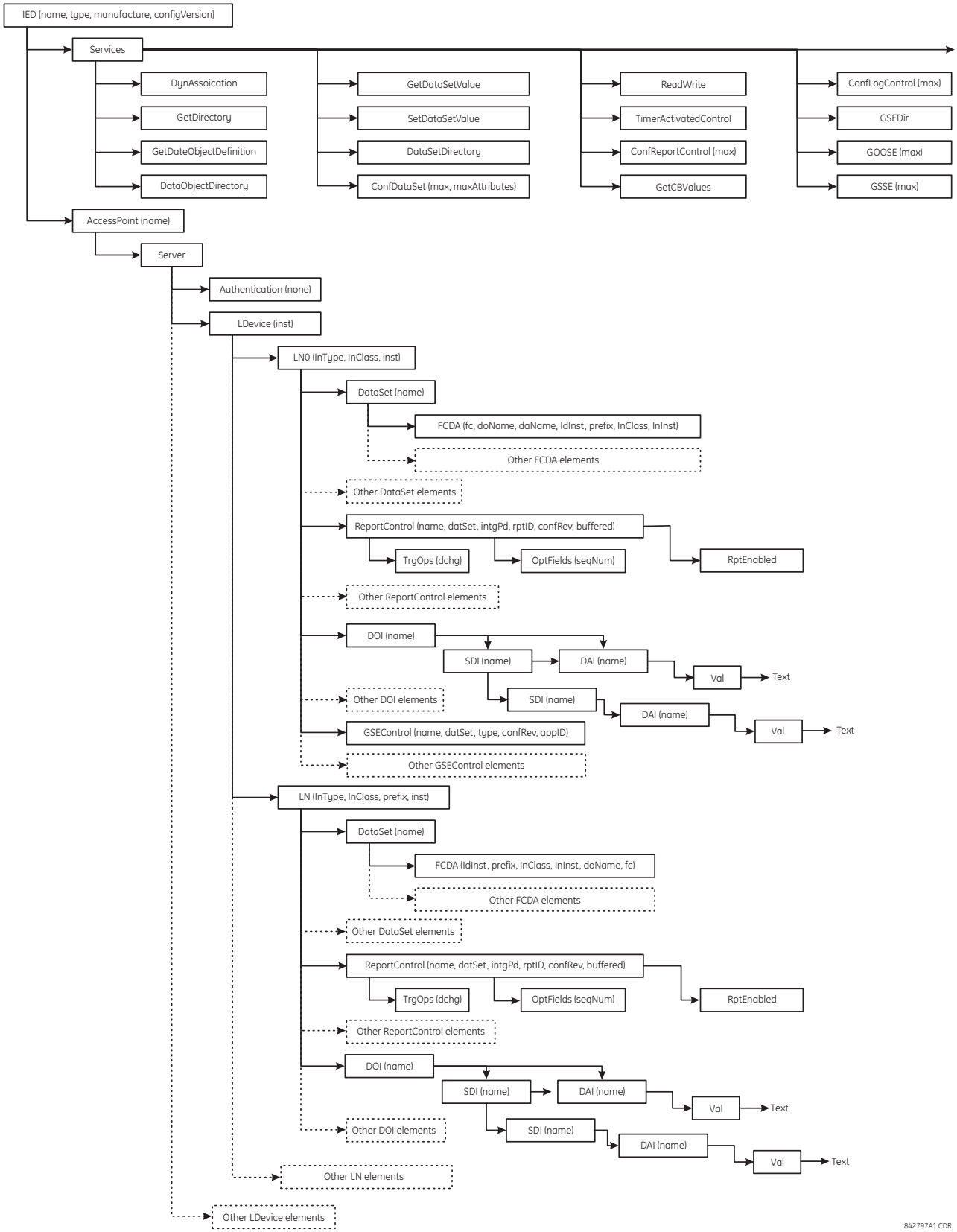


Figure 0–4: ICD FILE STRUCTURE, IED NODE

The **DataTypeTemplates** node defines instantiable logical node types. A logical node type is an instantiable template of the data of a logical node. A **LnodeType** is referenced each time that this instantiable type is needed with an IED. A logical node type template is built from DATA (DO) elements, which again have a DO type, which is derived from the DATA classes (CDC). DOs consist of attributes (DA) or of elements of already defined DO types (SDO). The attribute (DA) has a functional constraint, and can either have a basic type, be an enumeration, or a structure of a **DAType**. The DAType is built from BDA elements, defining the structure elements, which again can be **BDA** elements of have a base type such as DA.

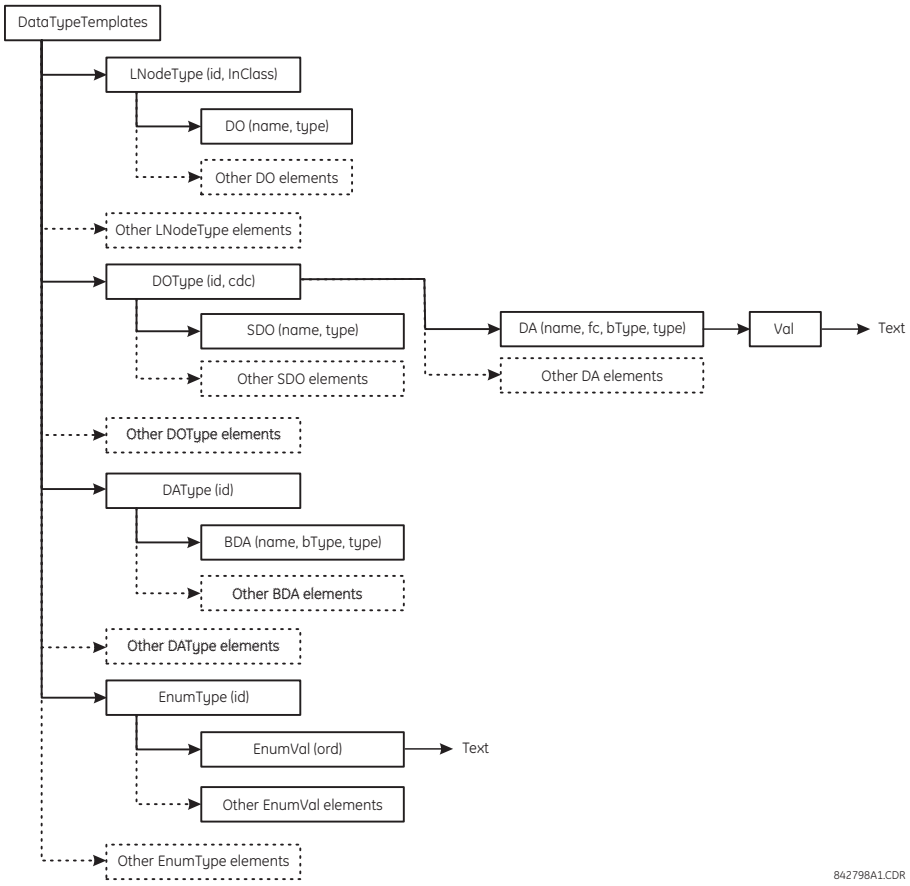
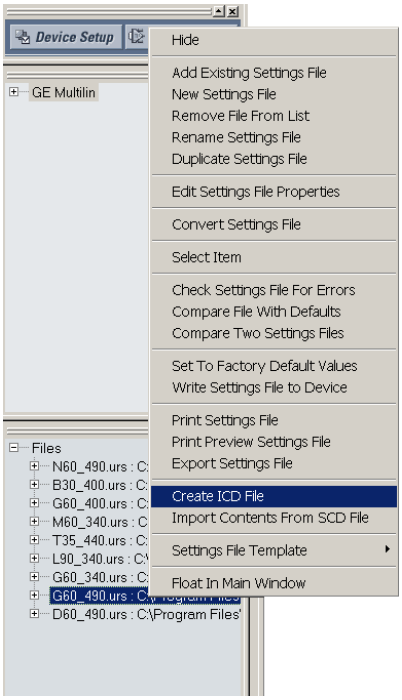


Figure 0–5: ICD FILE STRUCTURE, DATATYPETEMPLATES NODE

C.5.4 CREATING AN ICD FILE WITH ENERVISTA UR SETUP

An ICD file can be created directly from a connected L60 IED or from an offline L60 settings file with the EnerVista UR Setup software using the following procedure:

1. Right-click the connected UR-series relay or settings file and select **Create ICD File**.



2. The EnerVista UR Setup will prompt to save the file. Select the file path and enter the name for the ICD file, then click **OK** to generate the file.

The time to create an ICD file from the offline L60 settings file is typically much quicker than create an ICD file directly from the relay.

C.5.5 ABOUT SCD FILES

System configuration is performed in the system configurator. While many vendors (including GE Multilin) are working their own system configuration tools, there are some system configurators available in the market (for example, Siemens DIGSI version 4.6 or above and ASE Visual SCL Beta 0.12).

Although the configuration tools vary from one vendor to another, the procedure is pretty much the same. First, a substation project must be created, either as an empty template or with some system information by importing a system specification file (SSD). Then, IEDs are added to the substation. Since each IED is represented by its associated ICD, the ICD files are imported into the substation project, and the system configurator validates the ICD files during the importing process. If the ICD files are successfully imported into the substation project, it may be necessary to perform some additional minor steps to attach the IEDs to the substation (see the system configurator manual for details).

Once all IEDs are inserted into the substation, further configuration is possible, such as:

- assigning network addresses to individual IEDs
- customizing the prefixes of logical nodes
- creating cross-communication links (configuring GOOSE messages to send from one IED to others)

When system configurations are complete, the results are saved to an SCD file, which contains not only the configuration for each IED in the substation, but also the system configuration for the entire substation. Finally, the SCD file is passed back to the IED configurator (vendor specific tool) to update the new configuration into the IED.

The SCD file consists of at least five major sections:

- Header
- Substation
- Communication
- IED section (one or more)
- DataTypeTemplates

The root file structure of an SCD file is illustrated below.

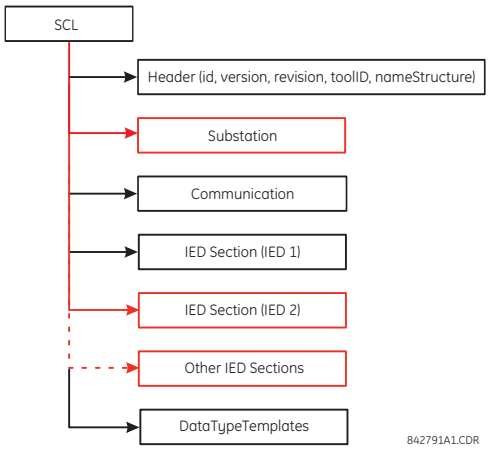


Figure 0–6: SCD FILE STRUCTURE, SCL (ROOT) NODE

Like ICD files, the **Header** node identifies the SCD file and its version, and specifies options for the mapping of names to signals.

The **Substation** node describes the substation parameters:

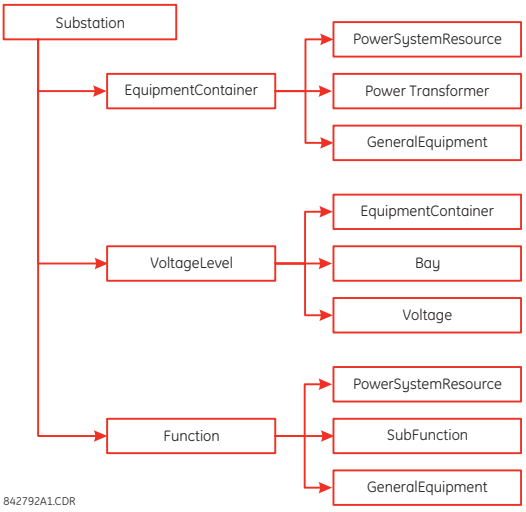


Figure 0–7: SCD FILE STRUCTURE, SUBSTATION NODE

The **Communication** node describes the direct communication connection possibilities between logical nodes by means of logical buses (sub-networks) and IED access ports. The communication section is structured as follows.

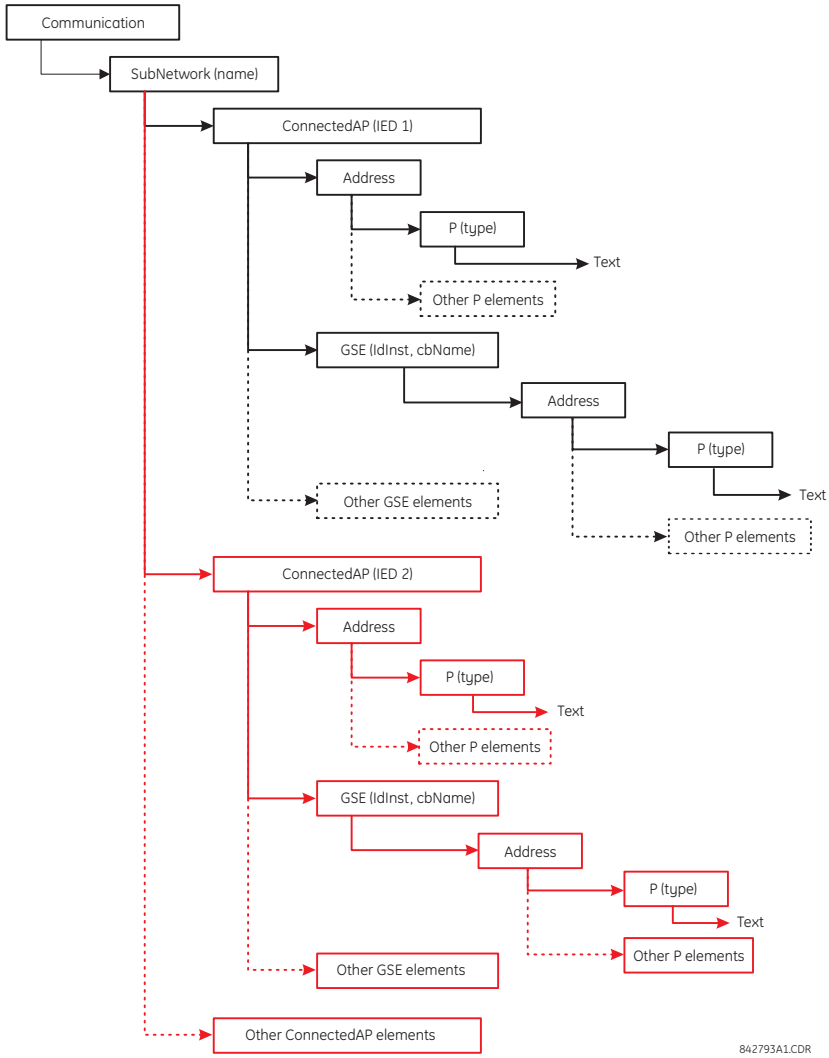


Figure 0–8: SCD FILE STRUCTURE, COMMUNICATIONS NODE

The **SubNetwork** node contains all access points which can (logically) communicate with the sub-network protocol and without the intervening router. The **ConnectedAP** node describes the IED access point connected to this sub-network. The **Address** node contains the address parameters of the access point. The **GSE** node provides the address element for stating the control block related address parameters, where **ldInst** is the instance identification of the logical device within the IED on which the control block is located, and **cbName** is the name of the control block.

The **IED Section** node describes the configuration of an IED.

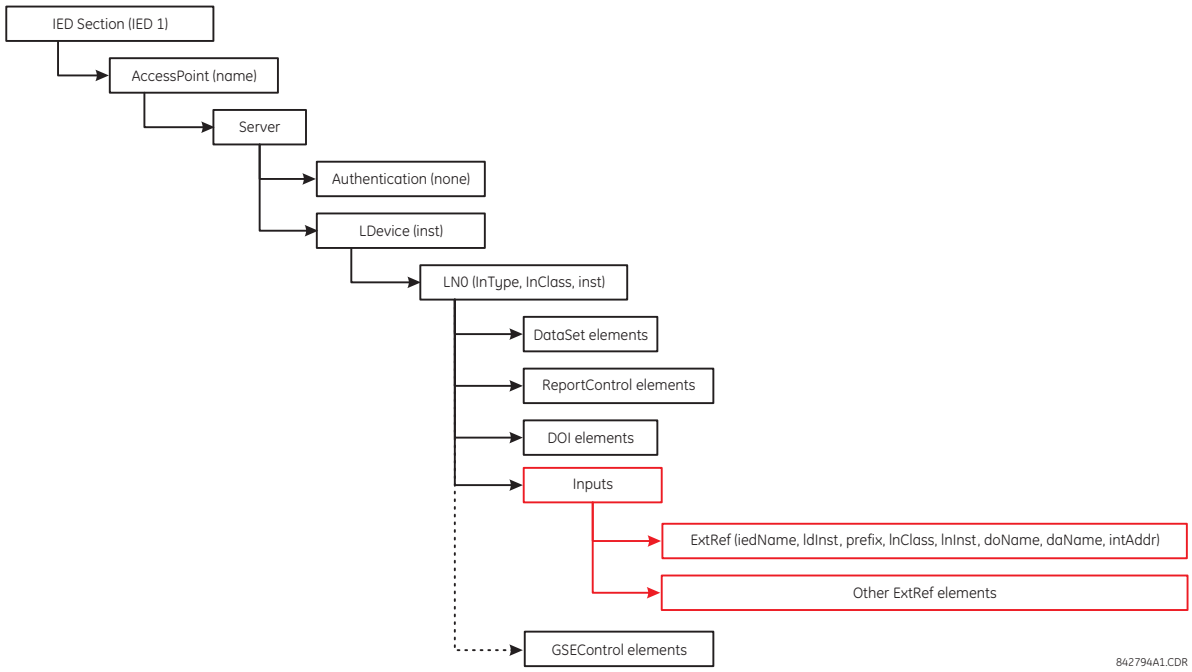
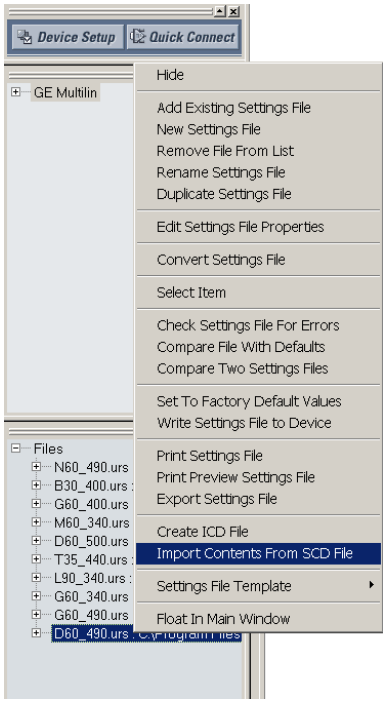


Figure 0–9: SCD FILE STRUCTURE, IED NODE

C.5.6 IMPORTING AN SCD FILE WITH ENERVISTA UR SETUP

The following procedure describes how to update the L60 with the new configuration from an SCD file with the EnerVista UR Setup software.

1. Right-click anywhere in the files panel and select the **Import Contents From SCD File** item.



2. Select the saved SCD file and click **Open**.

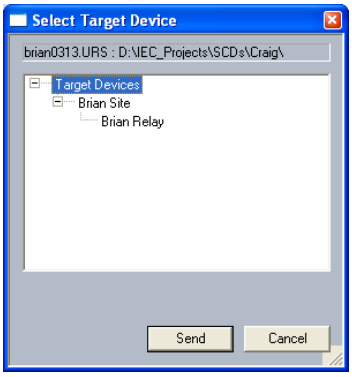
3. The software will open the SCD file and then prompt the user to save a UR-series settings file. Select a location and name for the URS (UR-series relay settings) file.

   If there is more than one GE Multilin IED defined in the SCD file, the software prompt the user to save a UR-series settings file for each IED.

4. After the URS file is created, modify any settings (if required).

5. To update the relay with the new settings, right-click on the settings file in the settings tree and select the **Write Settings File to Device** item.

6. The software will prompt for the target device. Select the target device from the list provided and click **Send**. The new settings will be updated to the selected device.



C.6.1 ACSI BASIC CONFORMANCE STATEMENT

SERVICES		SERVER/ PUBLISHER	UR-FAMILY
CLIENT-SERVER ROLES			
B11	**Server** side (of Two-party Application-Association)	**c1**	**Yes**
B12	**Client** side (of Two-party Application-Association)	**---**	
SCSMS SUPPORTED			
B21	**SCSM**: IEC 61850-8-1 used		**Yes**
B22	**SCSM**: IEC 61850-9-1 used		
B23	**SCSM**: IEC 61850-9-2 used		
B24	**SCSM**: other		
GENERIC SUBSTATION EVENT MODEL (GSE)			
B31	**Publisher** side	**O**	**Yes**
B32	**Subscriber** side	**---**	**Yes**
TRANSMISSION OF SAMPLED VALUE MODEL (SVC)			
B41	**Publisher** side	**O**	
B42	**Subscriber** side	**---**	

NOTE

c1: shall be "M" if support for LOGICAL-DEVICE model has been declared
O: Optional
M: Mandatory

C.6.2 ACSI MODELS CONFORMANCE STATEMENT

SERVICES		SERVER/ PUBLISHER	UR-FAMILY
IF SERVER SIDE (B11) SUPPORTED			
M1	**Logical device**	**c2**	**Yes**
M2	**Logical node**	**c3**	**Yes**
M3	**Data**	**c4**	**Yes**
M4	**Data set**	**c5**	**Yes**
M5	**Substitution**	**O**	
M6	**Setting group control**	**O**	
	REPORTING		
M7	**Buffered report control**	**O**	**Yes**
M7-1	sequence-number		
M7-2	report-time-stamp		
M7-3	reason-for-inclusion		
M7-4	data-set-name		
M7-5	data-reference		
M7-6	buffer-overflow		
M7-7	entryID		
M7-8	BufTm		
M7-9	IntgPd		
M7-10	GI		
M8	**Unbuffered report control**	**O**	**Yes**
M8-1	sequence-number		
M8-2	report-time-stamp		
M8-3	reason-for-inclusion		

SERVICES		SERVER/ PUBLISHER	UR-FAMILY
M8-4	data-set-name		
M8-5	data-reference		
M8-6	BufTm		
M8-7	IntgPd		
M8-8	GI		
	Logging	**O**	
M9	**Log control**	**O**	
M9-1	IntgPd		
M10	**Log**	**O**	
M11	**Control**	**M**	**Yes**
IF GSE (B31/32) IS SUPPORTED			
	GOOSE	**O**	**Yes**
M12-1	entryID		
M12-2	DataReflnc		
M13	**GSSE**	**O**	**Yes**
IF SVC (B41/B42) IS SUPPORTED			
M14	Multicast SVC	**O**	
M15	Unicast SVC	**O**	
M16	**Time**	**M**	**Yes**
M17	**File transfer**	**O**	**Yes**

NOTE

c2: shall be "M" if support for LOGICAL-NODE model has been declared
c3: shall be "M" if support for DATA model has been declared
c4: shall be "M" if support for DATA-SET, Substitution, Report, Log Control, or Time models has been declared
c5: shall be "M" if support for Report, GSE, or SMV models has been declared
M: Mandatory

C.6.3 ACSI SERVICES CONFORMANCE STATEMENT

In the table below, the acronym AA refers to Application Associations (TP: Two Party / MC: Multicast). The c6 to c10 entries are defined in the notes following the table.

SERVICES		AA: TP/MC	SERVER/ PUBLISHER	UR FAMILY
SERVER (CLAUSE 6)				
S1	ServerDirectory	TP	M	Yes
APPLICATION ASSOCIATION (CLAUSE 7)				
S2	Associate		M	Yes
S3	Abort		M	Yes
S4	Release		M	Yes
LOGICAL DEVICE (CLAUSE 8)				
S5	LogicalDeviceDirectory	TP	M	Yes
LOGICAL NODE (CLAUSE 9)				
S6	LogicalNodeDirectory	TP	M	Yes
S7	GetAllDataValues	TP	M	Yes
DATA (CLAUSE 10)				
S8	GetDataValues	TP	M	Yes
S9	SetDataValues	TP	O	Yes
S10	GetDataDirectory	TP	M	Yes
S11	GetDataDefinition	TP	M	Yes

SERVICES		AA: TP/MC	SERVER/ PUBLISHER	UR FAMILY
DATA SET (CLAUSE 11)				
S12	GetDataSetValues	TP	M	Yes
S13	SetDataSetValues	TP	O	
S14	CreateDataSet	TP	O	
S15	DeleteDataSet	TP	O	
S16	GetDataSetDirectory	TP	O	Yes
SUBSTITUTION (CLAUSE 12)				
S17	SetDataValues	TP	M	
SETTING GROUP CONTROL (CLAUSE 13)				
S18	SelectActiveSG	TP	O	
S19	SelectEditSG	TP	O	
S20	SetSGValues	TP	O	
S21	ConfirmEditSGValues	TP	O	
S22	GetSGValues	TP	O	
S23	GetSGCBValues	TP	O	
REPORTING (CLAUSE 14)				
	BUFFERED REPORT CONTROL BLOCK (BRCB)			
S24	Report	TP	c6	Yes
S24-1	data-change (dchg)			Yes
S24-2	qchg-change (qchg)			
S24-3	data-update (dupd)			
S25	GetBRCBValues	TP	c6	Yes
S26	SetBRCBValues	TP	c6	Yes
	UNBUFFERED REPORT CONTROL BLOCK (URCB)			
S27	Report	TP	c6	Yes
S27-1	data-change (dchg)			Yes
S27-2	qchg-change (qchg)			
S27-3	data-update (dupd)			
S28	GetURCBValues	TP	c6	Yes
S29	SetURCBValues	TP	c6	Yes
LOGGING (CLAUSE 14)				
	LOG CONTROL BLOCK			
S30	GetLCBValues	TP	M	
S31	SetLCBValues	TP	M	
	LOG			
S32	QueryLogByTime	TP	M	
S33	QueryLogByEntry	TP	M	
S34	GetLogStatusValues	TP	M	
GENERIC SUBSTATION EVENT MODEL (GSE) (CLAUSE 14.3.5.3.4)				
	GOOSE-CONTROL-BLOCK			
S35	SendGOOSEMessage	MC	c8	Yes
S36	GetReference	TP	c9	
S37	GetGOOSEElementNumber	TP	c9	
S38	GetGoCBValues	TP	O	Yes
S39	SetGoCBValues	TP	O	Yes
	GSSE-CONTROL-BLOCK			
S40	SendGSSEMessage	MC	c8	Yes
S41	GetReference	TP	c9	

SERVICES		AA: TP/MC	SERVER/ PUBLISHER	UR FAMILY
S42	GetGSSEElementNumber	TP	c9	
S43	GetGsCBValues	TP	O	Yes
S44	SetGsCBValues	TP	O	Yes
TRANSMISSION OF SAMPLE VALUE MODEL (SVC) (CLAUSE 16)				
	MULTICAST SVC			
S45	SendMSVMessage	MC	c10	
S46	GetMSVCBValues	TP	O	
S47	SetMSVCBValues	TP	O	
	UNICAST SVC			
S48	SendUSVMessage	MC	c10	
S49	GetUSVCBValues	TP	O	
S50	SetUSVCBValues	TP	O	
CONTROL (CLAUSE 16.4.8)				
S51	Select		O	Yes
S52	SelectWithValue	TP	O	
S53	Cancel	TP	O	Yes
S54	Operate	TP	M	Yes
S55	Command-Termination	TP	O	
S56	TimeActivated-Operate	TP	O	
FILE TRANSFER (CLAUSE 20)				
S57	GetFile	TP	M	Yes
S58	SetFile	TP	O	
S59	DeleteFile	TP	O	
S60	GetFileAttributeValues	TP	M	Yes
TIME (CLAUSE 5.5)				
T1	Time resolution of internal clock (nearest negative power of 2 in seconds)			20
T2	Time accuracy of internal clock			
T3	supported TimeStamp resolution (nearest value of 2^{-n} in seconds, accoridng to 5.5.3.7.3.3)			20

NOTE

c6: shall declare support for at least one (BRCB or URCB)
c7: shall declare support for at least one (QueryLogByTime or QueryLogAfter)
c8: shall declare support for at least one (SendGOOSEMessage or SendGSSEMessage)
c9: shall declare support if TP association is available
c10: shall declare support for at least one (SendMSVMessage or SendUSVMessage)

C.7.1 LOGICAL NODES TABLE

The UR-series of relays supports IEC 61850 logical nodes as indicated in the following table. Note that the actual instantiation of each logical node is determined by the product order code. For example. the logical node “PDIS” (distance protection) is available only in the D60 Line Distance Relay.

Table 0–1: IEC 61850 LOGICAL NODES (Sheet 1 of 3)

NODES	UR-FAMILY
L: SYSTEM LOGICAL NODES	
LPHD: Physical device information	**Yes**
LLN0: Logical node zero	**Yes**
P: LOGICAL NODES FOR PROTECTION FUNCTIONS	
PDIF: Differential	**Yes**
PDIR: Direction comparison	---
PDIS: Distance	**Yes**
PDOP: Directional overpower	---
PDUP: Directional underpower	---
PFRC: Rate of change of frequency	---
PHAR: Harmonic restraint	---
PHIZ: Ground detector	---
PIOC: Instantaneous overcurrent	**Yes**
PMRI Motor restart inhibition	---
PMSS: Motor starting time supervision	---
POPF: Over power factor	---
PPAM: Phase angle measuring	---
PSCH: Protection scheme	---
PSDE: Sensitive directional earth fault	---
PTEF: Transient earth fault	---
PTOC: Time overcurrent	**Yes**
PTOF: Overfrequency	---
PTOV: Overvoltage	**Yes**
PTRC: Protection trip conditioning	**Yes**
PTTR: Thermal overload	**Yes**
PTUC: Undercurrent	---
PTUV: Undervoltage	**Yes**
PUPF: Underpower factor	---
PTUF: Underfrequency	---
PVOC: Voltage controlled time overcurrent	---
PVPH: Volts per Hz	---
PZSU: Zero speed or underspeed	---
R: LOGICAL NODES FOR PROTECTION RELATED FUNCTIONS	
RDRE: Disturbance recorder function	---
RADR: Disturbance recorder channel analogue	---
RBDR: Disturbance recorder channel binary	---
RDRS: Disturbance record handling	---
RBRF: Breaker failure	**Yes**
RDIR: Directional element	---
RFLO: Fault locator	**Yes**
RPSB: Power swing detection/blocking	**Yes**
RREC: Autoreclosing	**Yes**

Table 0–1: IEC 61850 LOGICAL NODES (Sheet 2 of 3)

NODES	UR-FAMILY
RSYN: Synchronism-check or synchronizing	---
C: LOGICAL NODES FOR CONTROL	
CALH: Alarm handling	---
CCGR: Cooling group control	---
CILO: Interlocking	---
CPOW: Point-on-wave switching	---
CSWI: Switch controller	---
G: LOGICAL NODES FOR GENERIC REFERENCES	
GAPC: Generic automatic process control	---
GGIO: Generic process I/O	Yes
GSAL: Generic security application	---
I: LOGICAL NODES FOR INTERFACING AND ARCHIVING	
IARC: Archiving	---
IHMI: Human machine interface	---
ITCI: Telecontrol interface	---
ITMI: Telemonitoring interface	---
A: LOGICAL NODES FOR AUTOMATIC CONTROL	
ANCR: Neutral current regulator	---
ARCO: Reactive power control	---
ATCC: Automatic tap changer controller	---
AVCO: Voltage control	---
M: LOGICAL NODES FOR METERING AND MEASUREMENT	
MDIF: Differential measurements	---
MHAI: Harmonics or interharmonics	---
MHAN: Non phase related harmonics or interharmonic	---
MMTR: Metering	---
MMXN: Non phase related measurement	**Yes**
MMXU: Measurement	**Yes**
MSQI: Sequence and imbalance	---
MSTA: Metering statistics	---
S: LOGICAL NODES FOR SENSORS AND MONITORING	
SARC: Monitoring and diagnostics for arcs	---
SIMG: Insulation medium supervision (gas)	---
SIML: Insulation medium supervision (liquid)	---
SPDC: Monitoring and diagnostics for partial discharges	---
X: LOGICAL NODES FOR SWITCHGEAR	
XCBR: Circuit breaker	**Yes**
XSWI: Circuit switch	---
T: LOGICAL NODES FOR INSTRUMENT TRANSFORMERS	
TCTR: Current transformer	---
TVTR: Voltage transformer	---
Y: LOGICAL NODES FOR POWER TRANSFORMERS	
YEFN: Earth fault neutralizer (Peterson coil)	---
YLTC: Tap changer	---
YPSH: Power shunt	---
YPTR: Power transformer	---

Table 0–1: IEC 61850 LOGICAL NODES (Sheet 3 of 3)

NODES	UR-FAMILY
Z: LOGICAL NODES FOR FURTHER POWER SYSTEM EQUIPMENT	
ZAXN: Auxiliary network	---
ZBAT: Battery	---
ZBSH: Bushing	---
ZCAB: Power cable	---
ZCAP: Capacitor bank	---
ZCON: Converter	---
ZGEN: Generator	---
ZGIL: Gas insulated line	---
ZLIN: Power overhead line	---
ZMOT: Motor	---
ZREA: Reactor	---
ZRRC: Rotating reactive component	---
ZSAR: Surge arrestor	---
ZTCF: Thyristor controlled frequency converter	---
ZTRC: Thyristor controlled reactive component	---

D.1.1 INTEROPERABILITY DOCUMENT

This document is adapted from the IEC 60870-5-104 standard. For ths section the boxes indicate the following: ☒ – used in standard direction; ☐ – not used; ■ – cannot be selected in IEC 60870-5-104 standard.

1. SYSTEM OR DEVICE:

☐ System Definition

☐ Controlling Station Definition (Master)

☒ **Controlled Station Definition (Slave)**

2. NETWORK CONFIGURATION:

■ ~~Point-to-Point~~ ■ ~~Multipoint~~

■ ~~Multiple Point-to-Point~~ ■ ~~Multipoint Star~~

3. PHYSICAL LAYER

Transmission Speed (control direction):

Unbalanced Interchange Circuit V.24/V.28 Standard:	Unbalanced Interchange Circuit V.24/V.28 Recommended if >1200 bits/s:	Balanced Interchange Circuit X.24/X.27:
■ ~~100 bits/sec.~~	■ ~~2400 bits/sec.~~	■ ~~2400 bits/sec.~~
■ ~~200 bits/sec.~~	■ ~~4800 bits/sec.~~	■ ~~4800 bits/sec.~~
■ ~~300 bits/sec.~~	■ ~~9600 bits/sec.~~	■ ~~9600 bits/sec.~~
■ ~~600 bits/sec.~~		■ ~~19200 bits/sec.~~
■ ~~1200 bits/sec.~~		■ ~~38400 bits/sec.~~
		■ ~~56000 bits/sec.~~
		■ ~~64000 bits/sec.~~

Transmission Speed (monitor direction):

Unbalanced Interchange Circuit V.24/V.28 Standard:	Unbalanced Interchange Circuit V.24/V.28 Recommended if >1200 bits/s:	Balanced Interchange Circuit X.24/X.27:
■ ~~100 bits/sec.~~	■ ~~2400 bits/sec.~~	■ ~~2400 bits/sec.~~
■ ~~200 bits/sec.~~	■ ~~4800 bits/sec.~~	■ ~~4800 bits/sec.~~
■ ~~300 bits/sec.~~	■ ~~9600 bits/sec.~~	■ ~~9600 bits/sec.~~
■ ~~600 bits/sec.~~		■ ~~19200 bits/sec.~~
■ ~~1200 bits/sec.~~		■ ~~38400 bits/sec.~~
		■ ~~56000 bits/sec.~~
		■ ~~64000 bits/sec.~~

4. LINK LAYER

Link Transmission Procedure:	Address Field of the Link:
■ ~~Balanced Transmision~~	■ ~~Not Present (Balanced Transmission Only)~~
■ ~~Unbalanced Transmission~~	■ ~~One Octet~~
	■ ~~Two Octets~~
	■ ~~Structured~~
	■ ~~Unstructured~~
Frame Length (maximum length, number of octets): Not selectable in companion IEC 60870-5-104 standard	

When using an unbalanced link layer, the following ADSU types are returned in class 2 messages (low priority) with the indicated causes of transmission:

- ~~The standard assignment of ADSUs to class 2 messages is used as follows~~:

- ~~A special assignment of ADSUs to class 2 messages is used as follows~~:

5. APPLICATION LAYER

Transmission Mode for Application Data:
Mode 1 (least significant octet first), as defined in Clause 4.10 of IEC 60870-5-4, is used exclusively in this companion stanadard.

Common Address of ADSU:

- ~~One Octet~~
- ☒ Two Octets

Information Object Address:

- ~~One Octet~~
- ~~Two Octets~~
- ☒ Three Octets
- ☒ Structured
- ☒ Unstructured

Cause of Transmission:

- ~~One Octet~~
- ☒ Two Octets (with originator address). Originator address is set to zero if not used.

Maximum Length of APDU: 253 (the maximum length may be reduced by the system.

Selection of standard ASDUs:

For the following lists, the boxes indicate the following: ☒ – used in standard direction; ☐ – not used; ■ – cannot be selected in IEC 60870-5-104 standard.

Process information in monitor direction

☒ <1> := Single-point information	M_SP_NA_1
~~■ <2> := Single-point information with time tag~~	~~M_SP_TA_1~~
☐ <3> := Double-point information	M_DP_NA_1
~~■ <4> := Double-point information with time tag~~	~~M_DP_TA_1~~
☐ <5> := Step position information	M_ST_NA_1
~~■ <6> := Step position information with time tag~~	~~M_ST_TA_1~~
☐ <7> := Bitstring of 32 bits	M_BO_NA_1
~~■ <8> := Bitstring of 32 bits with time tag~~	~~M_BO_TA_1~~
☐ <9> := Measured value, normalized value	M_ME_NA_1
~~■ <10> := Measured value, normalized value with time tag~~	~~M_NE_TA_1~~
☐ <11> := Measured value, scaled value	M_ME_NB_1
~~■ <12> := Measured value, scaled value with time tag~~	~~M_NE_TB_1~~
☒ <13> := Measured value, short floating point value	M_ME_NC_1
~~■ <14> := Measured value, short floating point value with time tag~~	~~M_NE_TC_1~~
☒ <15> := Integrated totals	M_IT_NA_1
~~■ <16> := Integrated totals with time tag~~	~~M_IT_TA_1~~
~~■ <17> := Event of protection equipment with time tag~~	~~M_EP_TA_1~~
~~■ <18> := Packed start events of protection equipment with time tag~~	~~M_EP_TB_1~~
~~■ <19> := Packed output circuit information of protection equipment with time tag~~	~~M_EP_TC_1~~
☐ <20> := Packed single-point information with status change detection	M_SP_NA_1

☐ <21> := Measured value, normalized value without quantity descriptor	M_ME_ND_1
☒ <30> := Single-point information with time tag CP56Time2a	M_SP_TB_1
☐ <31> := Double-point information wiht time tag CP56Time2a	M_DP_TB_1
☐ <32> := Step position information with time tag CP56Time2a	M_ST_TB_1
☐ <33> := Bitstring of 32 bits with time tag CP56Time2a	M_BO_TB_1
☐ <34> := Measured value, normalized value with time tag CP56Time2a	M_ME_TD_1
☐ <35> := Measured value, scaled value with time tag CP56Time2a	M_ME_TE_1
☐ <36> := Measured value, short floating point value with time tag CP56Time2a	M_ME_TF_1
☒ <37> := Integrated totals with time tag CP56Time2a	M_IT_TB_1
☐ <38> := Event of protection equipment with time tag CP56Time2a	M_EP_TD_1
☐ <39> := Packed start events of protection equipment with time tag CP56Time2a	M_EP_TE_1
☐ <40> := Packed output circuit information of protection equipment with time tag CP56Time2a	M_EP_TF_1

Either the ASDUs of the set <2>, <4>, <6>, <8>, <10>, <12>, <14>, <16>, <17>, <18>, and <19> or of the set <30> to <40> are used.

Process information in control direction

☒ <45> := Single command	C_SC_NA_1
☐ <46> := Double command	C_DC_NA_1
☐ <47> := Regulating step command	C_RC_NA_1
☐ <48> := Set point command, normalized value	C_SE_NA_1
☐ <49> := Set point command, scaled value	C_SE_NB_1
☐ <50> := Set point command, short floating point value	C_SE_NC_1
☐ <51> := Bitstring of 32 bits	C_BO_NA_1
☒ <58> := Single command with time tag CP56Time2a	C_SC_TA_1
☐ <59> := Double command with time tag CP56Time2a	C_DC_TA_1
☐ <60> := Regulating step command with time tag CP56Time2a	C_RC_TA_1
☐ <61> := Set point command, normalized value with time tag CP56Time2a	C_SE_TA_1
☐ <62> := Set point command, scaled value with time tag CP56Time2a	C_SE_TB_1
☐ <63> := Set point command, short floating point value with time tag CP56Time2a	C_SE_TC_1
☐ <64> := Bitstring of 32 bits with time tag CP56Time2a	C_BO_TA_1

Either the ASDUs of the set <45> to <51> or of the set <58> to <64> are used.

System information in monitor direction

☒ <70> := End of initialization	M_EI_NA_1

System information in control direction

☒ <100> := Interrogation command	C_IC_NA_1
☒ <101> := Counter interrogation command	C_CI_NA_1
☒ <102> := Read command	C_RD_NA_1
☒ <103> := Clock synchronization command (see Clause 7.6 in standard)	C_CS_NA_1
■ ~~<104> := Test command~~	~~C_TS_NA_1~~
☒ <105> := Reset process command	C_RP_NA_1
■ <106> := Delay acquisition command	C_CD_NA_1
☒ <107> := Test command with time tag CP56Time2a	C_TS_TA_1

Parameter in control direction

☐ <110> := Parameter of measured value, normalized value	PE_ME_NA_1
☐ <111> := Parameter of measured value, scaled value	PE_ME_NB_1
☒ <112> := Parameter of measured value, short floating point value	PE_ME_NC_1
☐ <113> := Parameter activation	PE_AC_NA_1

File transfer

☐ <120> := File Ready	F_FR_NA_1
☐ <121> := Section Ready	F_SR_NA_1
☐ <122> := Call directory, select file, call file, call section	F_SC_NA_1
☐ <123> := Last section, last segment	F_LS_NA_1
☐ <124> := Ack file, ack section	F_AF_NA_1
☐ <125> := Segment	F_SG_NA_1
☐ <126> := Directory (blank or X, available only in monitor [standard] direction)	C_CD_NA_1

Type identifier and cause of transmission assignments
(station-specific parameters)

In the following table:

•Shaded boxes are not required.

•Black boxes are not permitted in this companion standard.

•Blank boxes indicate functions or ASDU not used.

•'**X**' if only used in the standard direction

TYPE IDENTIFICATION		CAUSE OF TRANSMISSION																		
		PERIODIC, CYCLIC	BACKGROUND SCAN	SPONTANEOUS	INITIALIZED	REQUEST OR REQUESTED	ACTIVATION	ACTIVATION CONFIRMATION	DEACTIVATION	DEACTIVATION CONFIRMATION	ACTIVATION TERMINATION	RETURN INFO CAUSED BY LOCAL CMD	FILE TRANSFER	INTERROGATED BY GROUP <NUMBER>	REQUEST BY GROUP <N> COUNTER REQ	UNKNOWN TYPE IDENTIFICATION	UNKNOWN CAUSE OF TRANSMISSION	UNKNOWN COMMON ADDRESS OF ADSU	UNKNOWN INFORMATION OBJECT ADDR	UNKNOWN INFORMATION OBJECT ADDR
NO.	MNEMONIC	1	2	3	4	5	6	7	8	9	10	11	12	13	20 to 36	37 to 41	44	45	46	47
<1>	M_SP_NA_1			X		X						X	X		X					
<2>	M_SP_TA_1																			
<3>	M_DP_NA_1																			
<4>	M_DP_TA_1																			
<5>	M_ST_NA_1																			
<6>	M_ST_TA_1																			
<7>	M_BO_NA_1																			
<8>	M_BO_TA_1																			
<9>	M_ME_NA_1																			

TYPE IDENTIFICATION		CAUSE OF TRANSMISSION																		
		PERIODIC, CYCLIC	BACKGROUND SCAN	SPONTANEOUS	INITIALIZED	REQUEST OR REQUESTED	ACTIVATION	ACTIVATION CONFIRMATION	DEACTIVATION	DEACTIVATION CONFIRMATION	ACTIVATION TERMINATION	RETURN INFO CAUSED BY LOCAL CMD	FILE TRANSFER	INTERROGATED BY GROUP <NUMBER>	REQUEST BY GROUP <N> COUNTER REQ	UNKNOWN TYPE IDENTIFICATION	UNKNOWN CAUSE OF TRANSMISSION	UNKNOWN COMMON ADDRESS OF ADSU	UNKNOWN INFORMATION OBJECT ADDR	UNKNOWN INFORMATION OBJECT ADDR
NO.	MNEMONIC	1	2	3	4	5	6	7	8	9	10	11	12	13	20 to 36	37 to 41	44	45	46	47
<10>	M_ME_TA_1																			
<11>	M_ME_NB_1																			
<12>	M_ME_TB_1																			
<13>	M_ME_NC_1	X		X		X									X					
<14>	M_ME_TC_1																			
<15>	M_IT_NA_1			X												X				
<16>	M_IT_TA_1																			
<17>	M_EP_TA_1																			
<18>	M_EP_TB_1																			
<19>	M_EP_TC_1																			
<20>	M_PS_NA_1																			
<21>	M_ME_ND_1																			
<30>	M_SP_TB_1			X								X	X							
<31>	M_DP_TB_1																			
<32>	M_ST_TB_1																			
<33>	M_BO_TB_1																			
<34>	M_ME_TD_1																			
<35>	M_ME_TE_1																			
<36>	M_ME_TF_1																			
<37>	M_IT_TB_1			X												X				
<38>	M_EP_TD_1																			
<39>	M_EP_TE_1																			
<40>	M_EP_TF_1																			
<45>	C_SC_NA_1						X	X	X	X	X									
<46>	C_DC_NA_1																			
<47>	C_RC_NA_1																			
<48>	C_SE_NA_1																			
<49>	C_SE_NB_1																			
<50>	C_SE_NC_1																			
<51>	C_BO_NA_1																			
<58>	C_SC_TA_1						X	X	X	X	X									
<59>	C_DC_TA_1																			
<60>	C_RC_TA_1																			

D

TYPE IDENTIFICATION		CAUSE OF TRANSMISSION																		
		PERIODIC, CYCLIC	BACKGROUND SCAN	SPONTANEOUS	INITIALIZED	REQUEST OR REQUESTED	ACTIVATION	ACTIVATION CONFIRMATION	DEACTIVATION	DEACTIVATION CONFIRMATION	ACTIVATION TERMINATION	RETURN INFO CAUSED BY LOCAL CMD	FILE TRANSFER	INTERROGATED BY GROUP <NUMBER>	REQUEST BY GROUP <N> COUNTER REQ	UNKNOWN TYPE IDENTIFICATION	UNKNOWN CAUSE OF TRANSMISSION	UNKNOWN COMMON ADDRESS OF ADSU	UNKNOWN INFORMATION OBJECT ADDR	UNKNOWN INFORMATION OBJECT ADDR
NO.	MNEMONIC	1	2	3	4	5	6	7	8	9	10	11	12	13	20 to 36	37 to 41	44	45	46	47
<61>	C_SE_TA_1																			
<62>	C_SE_TB_1																			
<63>	C_SE_TC_1																			
<64>	C_BO_TA_1																			
<70>	M_EI_NA_1*)				X															
<100>	C_IC_NA_1						X	X	X	X	X									
<101>	C_CI_NA_1						X	X			X									
<102>	C_RD_NA_1					X														
<103>	C_CS_NA_1			X			X	X												
<104>	C_TS_NA_1																			
<105>	C_RP_NA_1						X	X												
<106>	C_CD_NA_1																			
<107>	C_TS_TA_1																			
<110>	P_ME_NA_1																			
<111>	P_ME_NB_1																			
<112>	P_ME_NC_1						X	X							X					
<113>	P_AC_NA_1																			
<120>	F_FR_NA_1																			
<121>	F_SR_NA_1																			
<122>	F_SC_NA_1																			
<123>	F_LS_NA_1																			
<124>	F_AF_NA_1																			
<125>	F_SG_NA_1																			
<126>	F_DR_TA_1*)																			

6. BASIC APPLICATION FUNCTIONS

Station Initialization:

☒ Remote initialization

Cyclic Data Transmission:

☒ Cyclic data transmission

Read Procedure:

☒ Read procedure

Spontaneous Transmission:

☒ Spontaneous transmission

Double transmission of information objects with cause of transmission spontaneous:

The following type identifications may be transmitted in succession caused by a single status change of an information object. The particular information object addresses for which double transmission is enabled are defined in a project-specific list.

☐ Single point information: M_SP_NA_1, M_SP_TA_1, M_SP_TB_1, and M_PS_NA_1

☐ Double point information: M_DP_NA_1, M_DP_TA_1, and M_DP_TB_1

☐ Step position information: M_ST_NA_1, M_ST_TA_1, and M_ST_TB_1

☐ Bitstring of 32 bits: M_BO_NA_1, M_BO_TA_1, and M_BO_TB_1 (if defined for a specific project)

☐ Measured value, normalized value: M_ME_NA_1, M_ME_TA_1, M_ME_ND_1, and M_ME_TD_1

☐ Measured value, scaled value: M_ME_NB_1, M_ME_TB_1, and M_ME_TE_1

☐ Measured value, short floating point number: M_ME_NC_1, M_ME_TC_1, and M_ME_TF_1

Station interrogation:

☒ Global

☒ Group 1	☒ Group 5	☒ Group 9	☒ Group 13
☒ Group 2	☒ Group 6	☒ Group 10	☒ Group 14
☒ Group 3	☒ Group 7	☒ Group 11	☒ Group 15
☒ Group 4	☒ Group 8	☒ Group 12	☒ Group 16

Clock synchronization:

☒ Clock synchronization (optional, see Clause 7.6)

Command transmission:

☒ Direct command transmission

☐ Direct setpoint command transmission

☒ Select and execute command

☐ Select and execute setpoint command

☒ C_SE ACTTERM used

☒ No additional definition

☒ Short pulse duration (duration determined by a system parameter in the outstation)

☒ Long pulse duration (duration determined by a system parameter in the outstation)

☒ Persistent output

☒ Supervision of maximum delay in command direction of commands and setpoint commands

Maximum allowable delay of commands and setpoint commands: **10 s**

Transmission of integrated totals:

☒ Mode A: Local freeze with spontaneous transmission

☒ Mode B: Local freeze with counter interrogation

☒ Mode C: Freeze and transmit by counter-interrogation commands

☒ Mode D: Freeze by counter-interrogation command, frozen values reported simultaneously

☒ Counter read

☒ Counter freeze without reset

☒ Counter freeze with reset

☒ Counter reset

☒ General request counter

☒ Request counter group 1

☒ Request counter group 2

☒ Request counter group 3

☒ Request counter group 4

Parameter loading:

☒ Threshold value

☐ Smoothing factor

☐ Low limit for transmission of measured values

☐ High limit for transmission of measured values

Parameter activation:

☐ Activation/deactivation of persistent cyclic or periodic transmission of the addressed object

Test procedure:

☐ Test procedure

File transfer:

File transfer in monitor direction:

☐ Transparent file

☐ Transmission of disturbance data of protection equipment

☐ Transmission of sequences of events

☐ Transmission of sequences of recorded analog values

File transfer in control direction:

☐ Transparent file

Background scan:

☐ Background scan

Acquisition of transmission delay:

■ ~~Acquisition of transmission delay~~

Definition of time outs:

PARAMETER	DEFAULT VALUE	REMARKS	SELECTED VALUE
t_0	30 s	Timeout of connection establishment	120 s
t_1	15 s	Timeout of send or test APDUs	15 s
t_2	10 s	Timeout for acknowlegements in case of no data messages $t_2 < t_1$	10 s
t_3	20 s	Timeout for sending test frames in case of a long idle state	20 s

Maximum range of values for all time outs: 1 to 255 s, accuracy 1 s

Maximum number of outstanding I-format APDUs *k* and latest acknowledge APDUs (*w*):

PARAMETER	DEFAULT VALUE	REMARKS	SELECTED VALUE
k	12 APDUs	Maximum difference receive sequence number to send state variable	12 APDUs
w	8 APDUs	Latest acknowledge after receiving *w* I-format APDUs	8 APDUs

Maximum range of values *k*: 1 to 32767 (2^{15} – 1) APDUs, accuracy 1 APDU

Maximum range of values *w*: 1 to 32767 APDUs, accuracy 1 APDU
Recommendation: *w* should not exceed two-thirds of *k*.

Portnumber:

PARAMETER	VALUE	REMARKS
Portnumber	2404	In all cases

RFC 2200 suite:

RFC 2200 is an official Internet Standard which describes the state of standardization of protocols used in the Internet as determined by the Internet Architecture Board (IAB). It offers a broad spectrum of actual standards used in the Internet. The suitable selection of documents from RFC 2200 defined in this standard for given projects has to be chosen by the user of this standard.

☒ Ethernet 802.3

☐ Serial X.21 interface

☐ Other selection(s) from RFC 2200 (list below if selected)

D.1.2 POINT LIST

The IEC 60870-5-104 data points are configured through the **SETTINGS** ⇨ **PRODUCT SETUP** ⇨⇩ **COMMUNICATIONS** ⇨⇩ **DNP / IEC104 POINT LISTS** menu. Refer to the *Communications* section of Chapter 5 for additional details.

D

E.1.1 DNP V3.00 DEVICE PROFILE

The following table provides a 'Device Profile Document' in the standard format defined in the DNP 3.0 Subset Definitions Document.

Table E–1: DNP V3.00 DEVICE PROFILE (Sheet 1 of 3)

<table>
<tr><td colspan="2">(Also see the IMPLEMENTATION TABLE in the following section)</td></tr>
<tr><td colspan="2">Vendor Name: General Electric Multilin</td></tr>
<tr><td colspan="2">Device Name: UR Series Relay</td></tr>
<tr><td>Highest DNP Level Supported:
For Requests: Level 2
For Responses: Level 2</td><td>Device Function:
☐ Master
☒ Slave</td></tr>
<tr><td colspan="2">Notable objects, functions, and/or qualifiers supported in addition to the Highest DNP Levels Supported (the complete list is described in the attached table):
Binary Inputs (Object 1)
Binary Input Changes (Object 2)
Binary Outputs (Object 10)
Control Relay Output Block (Object 12)
Binary Counters (Object 20)
Frozen Counters (Object 21)
Counter Change Event (Object 22)
Frozen Counter Event (Object 23)
Analog Inputs (Object 30)
Analog Input Changes (Object 32)
Analog Deadbands (Object 34)
Time and Date (Object 50)
File Transfer (Object 70)
Internal Indications (Object 80)</td></tr>
<tr><td>Maximum Data Link Frame Size (octets):
Transmitted: 292
Received: 292</td><td>Maximum Application Fragment Size (octets):
Transmitted: configurable up to 2048
Received: 2048</td></tr>
<tr><td>Maximum Data Link Re-tries:
☒ None
☐ Fixed at 3
☐ Configurable</td><td>Maximum Application Layer Re-tries:
☒ None
☐ Configurable</td></tr>
<tr><td colspan="2">Requires Data Link Layer Confirmation:
☒ Never
☐ Always
☐ Sometimes
☐ Configurable</td></tr>
</table>

Table E–1: DNP V3.00 DEVICE PROFILE (Sheet 2 of 3)

Requires Application Layer Confirmation:

- ☐ Never
- ☐ Always
- ☒ When reporting Event Data
- ☒ When sending multi-fragment responses
- ☐ Sometimes
- ☐ Configurable

Timeouts while waiting for:

Data Link Confirm:	☒ None	☐ Fixed at ____	☐ Variable	☐ Configurable
Complete Appl. Fragment:	☒ **None**	☐ Fixed at ____	☐ Variable	☐ Configurable
Application Confirm:	☐ None	☒ **Fixed at 10 s**	☐ Variable	☐ Configurable
Complete Appl. Response:	☒ **None**	☐ Fixed at ____	☐ Variable	☐ Configurable

Others:

Transmission Delay:	**No intentional delay**
Need Time Interval:	**Configurable (default = 24 hrs.)**
Select/Operate Arm Timeout:	**10 s**
Binary input change scanning period:	**8 times per power system cycle**
Analog input change scanning period:	**500 ms**
Counter change scanning period:	**500 ms**
Frozen counter event scanning period:	**500 ms**
Unsolicited response notification delay:	**100 ms**
Unsolicited response retry delay	**configurable 0 to 60 sec.**

Sends/Executes Control Operations:

WRITE Binary Outputs	☒ **Never**	☐ Always	☐ Sometimes	☐ Configurable
SELECT/OPERATE	☐ Never	☒ **Always**	☐ Sometimes	☐ Configurable
DIRECT OPERATE	☐ Never	☒ **Always**	☐ Sometimes	☐ Configurable
DIRECT OPERATE – NO ACK	☐ Never	☒ **Always**	☐ Sometimes	☐ Configurable

Count > 1	☒ **Never**	☐ Always	☐ Sometimes	☐ Configurable
Pulse On	☐ Never	☐ Always	☒ **Sometimes**	☐ Configurable
Pulse Off	☐ Never	☐ Always	☒ **Sometimes**	☐ Configurable
Latch On	☐ Never	☐ Always	☒ **Sometimes**	☐ Configurable
Latch Off	☐ Never	☐ Always	☒ **Sometimes**	☐ Configurable
Queue	☒ **Never**	☐ Always	☐ Sometimes	☐ Configurable
Clear Queue	☒ **Never**	☐ Always	☐ Sometimes	☐ Configurable

Explanation of 'Sometimes': Object 12 points are mapped to UR Virtual Inputs. The persistence of Virtual Inputs is determined by the **VIRTUAL INPUT X TYPE** settings. Both "Pulse On" and "Latch On" operations perform the same function in the UR; that is, the appropriate Virtual Input is put into the "On" state. If the Virtual Input is set to "Self-Reset", it will reset after one pass of FlexLogic™. The On/Off times and Count value are ignored. "Pulse Off" and "Latch Off" operations put the appropriate Virtual Input into the "Off" state. "Trip" and "Close" operations both put the appropriate Virtual Input into the "On" state.

Table E–1: DNP V3.00 DEVICE PROFILE (Sheet 3 of 3)

Reports Binary Input Change Events when no specific variation requested: ☐ Never ☒ **Only time-tagged** ☐ Only non-time-tagged ☐ Configurable	**Reports time-tagged Binary Input Change Events when no specific variation requested:** ☐ Never ☒ Binary Input Change With Time ☐ Binary Input Change With Relative Time ☐ Configurable (attach explanation)
Sends Unsolicited Responses: ☐ **Never** ☒ Configurable ☐ Only certain objects ☐ Sometimes (attach explanation) ☒ ENABLE/DISABLE unsolicited Function codes supported	**Sends Static Data in Unsolicited Responses:** ☒ Never ☐ When Device Restarts ☐ When Status Flags Change No other options are permitted.
Default Counter Object/Variation: ☐ No Counters Reported ☐ Configurable (attach explanation) ☒ **Default Object: 20** **Default Variation: 1** ☒ **Point-by-point list attached**	**Counters Roll Over at:** ☐ No Counters Reported ☐ Configurable (attach explanation) ☒ **16 Bits (Counter 8)** ☒ **32 Bits (Counters 0 to 7, 9)** ☐ Other Value: _____ ☒ **Point-by-point list attached**
Sends Multi-Fragment Responses: ☒ **Yes** ☐ No	

The following table identifies the variations, function codes, and qualifiers supported by the L60 in both request messages and in response messages. For static (non-change-event) objects, requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01. Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28. For change-event objects, qualifiers 17 or 28 are always responded.

Table E–2: IMPLEMENTATION TABLE (Sheet 1 of 4)

OBJECT			REQUEST		RESPONSE	
OBJECT NO.	VARIATION NO.	DESCRIPTION	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)
1	0	Binary Input (Variation 0 is used to request default variation)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)		
	1	Binary Input	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	2	Binary Input with Status	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
2	0	Binary Input Change (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited quantity)		
	1	Binary Input Change without Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	2	Binary Input Change with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response 130 (unsol. resp.)	17, 28 (index)
	3	Binary Input Change with Relative Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)		
10	0	Binary Output Status (Variation 0 is used to request default variation)	1 (read)	00, 01(start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)		
	2	Binary Output Status	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
12	1	Control Relay Output Block	3 (select) 4 (operate) 5 (direct op) 6 (dir. op, noack)	00, 01 (start-stop) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	echo of request
20	0	Binary Counter (Variation 0 is used to request default variation)	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01(start-stop) 06(no range, or all) 07, 08(limited quantity) 17, 28(index)		
	1	32-Bit Binary Counter	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*

Note 1: A default variation refers to the variation responded when variation 0 is requested and/or in class 0, 1, 2, or 3 scans. The default variations for object types 1, 2, 20, 21, 22, 23, 30, and 32 are selected via relay settings. Refer to the *Communications* section in Chapter 5 for details. This optimizes the class 0 poll data size.

Note 2: For static (non-change-event) objects, qualifiers 17 or 28 are only responded when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01 (for change-event objects, qualifiers 17 or 28 are always responded.)

Note 3: Cold restarts are implemented the same as warm restarts – the L60 is not restarted, but the DNP process is restarted.

Table E–2: IMPLEMENTATION TABLE (Sheet 2 of 4)

OBJECT			REQUEST		RESPONSE	
OBJECT NO.	VARIATION NO.	DESCRIPTION	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)
20 cont'd	2	16-Bit Binary Counter	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	5	32-Bit Binary Counter without Flag	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	6	16-Bit Binary Counter without Flag	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
21	0	Frozen Counter (Variation 0 is used to request default variation)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)		
	1	32-Bit Frozen Counter	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	2	16-Bit Frozen Counter	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	9	32-Bit Frozen Counter without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	10	16-Bit Frozen Counter without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
22	0	Counter Change Event (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited quantity)		
	1	32-Bit Counter Change Event	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	2	16-Bit Counter Change Event	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	5	32-Bit Counter Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	6	16-Bit Counter Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited quantity)		
	1	32-Bit Frozen Counter Event	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	2	16-Bit Frozen Counter Event	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)

Note 1: A default variation refers to the variation responded when variation 0 is requested and/or in class 0, 1, 2, or 3 scans. The default variations for object types 1, 2, 20, 21, 22, 23, 30, and 32 are selected via relay settings. Refer to the *Communications* section in Chapter 5 for details. This optimizes the class 0 poll data size.

Note 2: For static (non-change-event) objects, qualifiers 17 or 28 are only responded when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01 (for change-event objects, qualifiers 17 or 28 are always responded.)

Note 3: Cold restarts are implemented the same as warm restarts – the L60 is not restarted, but the DNP process is restarted.

Table E–2: IMPLEMENTATION TABLE (Sheet 3 of 4)

OBJECT			REQUEST		RESPONSE	
OBJECT NO.	VARIATION NO.	DESCRIPTION	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)
23 cont'd	5	32-Bit Frozen Counter Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	6	16-Bit Frozen Counter Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
30	0	Analog Input (Variation 0 is used to request default variation)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)		
	1	32-Bit Analog Input	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	2	16-Bit Analog Input	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	3	32-Bit Analog Input without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	4	16-Bit Analog Input without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
	5	short floating point	1 (read) 22 (assign class)	00, 01 (start-stop) 06(no range, or all) 07, 08(limited quantity) 17, 28(index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
32	0	Analog Change Event (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited quantity)		
	1	32-Bit Analog Change Event without Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	2	16-Bit Analog Change Event without Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	3	32-Bit Analog Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	4	16-Bit Analog Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	5	short floating point Analog Change Event without Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	7	short floating point Analog Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited quantity)	129 (response) 130 (unsol. resp.)	17, 28 (index)
34	0	Analog Input Reporting Deadband (Variation 0 is used to request default variation)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)		
	1	16-bit Analog Input Reporting Deadband (default – see Note 1)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
			2 (write)	00, 01 (start-stop) 07, 08 (limited quantity) 17, 28 (index)		

Note 1: A default variation refers to the variation responded when variation 0 is requested and/or in class 0, 1, 2, or 3 scans. The default variations for object types 1, 2, 20, 21, 22, 23, 30, and 32 are selected via relay settings. Refer to the *Communications* section in Chapter 5 for details. This optimizes the class 0 poll data size.

Note 2: For static (non-change-event) objects, qualifiers 17 or 28 are only responded when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01 (for change-event objects, qualifiers 17 or 28 are always responded.)

Note 3: Cold restarts are implemented the same as warm restarts – the L60 is not restarted, but the DNP process is restarted.

Table E–2: IMPLEMENTATION TABLE (Sheet 4 of 4)

OBJECT			REQUEST		RESPONSE	
OBJECT NO.	VARIATION NO.	DESCRIPTION	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)	FUNCTION CODES (DEC)	QUALIFIER CODES (HEX)
34 cont'd	2	32-bit Analog Input Reporting Deadband	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
			2 (write)	00, 01 (start-stop) 07, 08 (limited quantity) 17, 28 (index)		
	3	Short floating point Analog Input Reporting Deadband	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
50	1	Time and Date (default – see Note 1)	1 (read) 2 (write)	00, 01 (start-stop) 06 (no range, or all) 07 (limited qty=1) 08 (limited quantity) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) *(see Note 2)*
52	2	Time Delay Fine			129 (response)	07 (limited quantity) (quantity = 1)
60	0	Class 0, 1, 2, and 3 Data	1 (read) 20 (enable unsol) 21 (disable unsol) 22 (assign class)	06 (no range, or all)		
	1	Class 0 Data	1 (read) 22 (assign class)	06 (no range, or all)		
	2	Class 1 Data	1 (read) 20 (enable unsol) 21 (disable unsol) 22 (assign class)	06 (no range, or all) 07, 08 (limited quantity)		
	3	Class 2 Data				
	4	Class 3 Data				
70	0	File event - any variation	1 (read)	06 (no range, or all) 07, 08 (limited quantity)		
			22 (assign class)	06 (no range, or all)		
	2	File authentication	29 (authenticate)	5b (free format)	129 (response)	5b (free format)
	3	File command	25 (open) 27 (delete)	5b (free format)		
	4	File command status	26 (close) 30 (abort)	5b (free format)	129 (response) 130 (unsol. resp.)	5b (free format)
	5	File transfer	1 (read) 2 (write)	5b (free format)	129 (response) 130 (unsol. resp.)	5b (free format)
	6	File transfer status			129 (response) 130 (unsol. resp.)	5b (free format)
	7	File descriptor	28 (get file info.)	5b (free format)	129 (response) 130 (unsol. resp.)	5b (free format)
80	1	Internal Indications	1 (read)	00, 01 (start-stop) (index =7)	129 (response)	00, 01 (start-stop)
			2 (write) *(see Note 3)*	00 (start-stop) (index =7)		
---		No Object (function code only) *see Note 3*	13 (cold restart)			
---		No Object (function code only)	14 (warm restart)			
---		No Object (function code only)	23 (delay meas.)			

Note 1: A default variation refers to the variation responded when variation 0 is requested and/or in class 0, 1, 2, or 3 scans. The default variations for object types 1, 2, 20, 21, 22, 23, 30, and 32 are selected via relay settings. Refer to the *Communications* section in Chapter 5 for details. This optimizes the class 0 poll data size.

Note 2: For static (non-change-event) objects, qualifiers 17 or 28 are only responded when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01 (for change-event objects, qualifiers 17 or 28 are always responded.)

Note 3: Cold restarts are implemented the same as warm restarts – the L60 is not restarted, but the DNP process is restarted.

E.2.1 BINARY INPUT POINTS

The DNP binary input data points are configured through the **PRODUCT SETUP** ⇨⇩ **COMMUNICATIONS** ⇨⇩ **DNP / IEC104 POINT LISTS** ⇨ **BINARY INPUT / MSP POINTS** menu. Refer to the *Communications* section of Chapter 5 for additional details. When a freeze function is performed on a binary counter point, the frozen value is available in the corresponding frozen counter point.

BINARY INPUT POINTS

Static (Steady-State) Object Number: **1**

Change Event Object Number: **2**

Request Function Codes supported: **1 (read), 22 (assign class)**

Static Variation reported when variation 0 requested: **2 (Binary Input with status), Configurable**

Change Event Variation reported when variation 0 requested: **2 (Binary Input Change with Time), Configurable**

Change Event Scan Rate: **8 times per power system cycle**

Change Event Buffer Size: **500**

Default Class for All Points: **1**

E.2.2 BINARY AND CONTROL RELAY OUTPUT

Supported Control Relay Output Block fields: Pulse On, Pulse Off, Latch On, Latch Off, Paired Trip, Paired Close.

BINARY OUTPUT STATUS POINTS

Object Number: **10**

Request Function Codes supported: **1 (read)**

Default Variation reported when Variation 0 requested: **2 (Binary Output Status)**

CONTROL RELAY OUTPUT BLOCKS

Object Number: **12**

Request Function Codes supported: **3 (select), 4 (operate), 5 (direct operate), 6 (direct operate, noack)**

Table E–3: BINARY/CONTROL OUTPUTS

POINT	NAME/DESCRIPTION
0	Virtual Input 1
1	Virtual Input 2
2	Virtual Input 3
3	Virtual Input 4
4	Virtual Input 5
5	Virtual Input 6
6	Virtual Input 7
7	Virtual Input 8
8	Virtual Input 9
9	Virtual Input 10
10	Virtual Input 11
11	Virtual Input 12
12	Virtual Input 13
13	Virtual Input 14
14	Virtual Input 15
15	Virtual Input 16
16	Virtual Input 17
17	Virtual Input 18
18	Virtual Input 19
19	Virtual Input 20
20	Virtual Input 21
21	Virtual Input 22
22	Virtual Input 23
23	Virtual Input 24
24	Virtual Input 25
25	Virtual Input 26
26	Virtual Input 27
27	Virtual Input 28
28	Virtual Input 29
29	Virtual Input 30
30	Virtual Input 31
31	Virtual Input 32

Table E–3: BINARY/CONTROL OUTPUTS

POINT	NAME/DESCRIPTION
32	Virtual Input 33
33	Virtual Input 34
34	Virtual Input 35
35	Virtual Input 36
36	Virtual Input 37
37	Virtual Input 38
38	Virtual Input 39
39	Virtual Input 40
40	Virtual Input 41
41	Virtual Input 42
42	Virtual Input 43
43	Virtual Input 44
44	Virtual Input 45
45	Virtual Input 46
46	Virtual Input 47
47	Virtual Input 48
48	Virtual Input 49
49	Virtual Input 50
50	Virtual Input 51
51	Virtual Input 52
52	Virtual Input 53
53	Virtual Input 54
54	Virtual Input 55
55	Virtual Input 56
56	Virtual Input 57
57	Virtual Input 58
58	Virtual Input 59
59	Virtual Input 60
60	Virtual Input 61
61	Virtual Input 62
62	Virtual Input 63
63	Virtual Input 64

E.2.3 COUNTERS

The following table lists both Binary Counters (Object 20) and Frozen Counters (Object 21). When a freeze function is performed on a Binary Counter point, the frozen value is available in the corresponding Frozen Counter point.

BINARY COUNTERS

Static (Steady-State) Object Number: **20**

Change Event Object Number: **22**

Request Function Codes supported: **1 (read), 7 (freeze), 8 (freeze noack), 9 (freeze and clear), 10 (freeze and clear, noack), 22 (assign class)**

Static Variation reported when variation 0 requested: **1 (32-Bit Binary Counter with Flag)**

Change Event Variation reported when variation 0 requested: **1 (32-Bit Counter Change Event without time)**

Change Event Buffer Size: **10**

Default Class for all points: **3**

FROZEN COUNTERS

Static (Steady-State) Object Number: **21**

Change Event Object Number: **23**

Request Function Codes supported: **1 (read)**

Static Variation reported when variation 0 requested: **1 (32-Bit Frozen Counter with Flag)**

Change Event Variation reported when variation 0 requested: **1 (32-Bit Frozen Counter Event without time)**

Change Event Buffer Size: **10**

Default Class for all points: **3**

Table E–4: BINARY AND FROZEN COUNTERS

POINT INDEX	NAME/DESCRIPTION
0	Digital Counter 1
1	Digital Counter 2
2	Digital Counter 3
3	Digital Counter 4
4	Digital Counter 5
5	Digital Counter 6
6	Digital Counter 7
7	Digital Counter 8
8	Oscillography Trigger Count
9	Events Since Last Clear

A counter freeze command has no meaning for counters 8 and 9. L60 Digital Counter values are represented as 32-bit integers. The DNP 3.0 protocol defines counters to be unsigned integers. Care should be taken when interpreting negative counter values.

E.2.4 ANALOG INPUTS

The DNP analog input data points are configured through the **PRODUCT SETUP** ⇨⇩ **COMMUNICATIONS** ⇨⇩ **DNP / IEC104 POINT LISTS** ⇨ **ANALOG INPUT / MME POINTS** menu. Refer to the *Communications* section of Chapter 5 for additional details.

It is important to note that 16-bit and 32-bit variations of analog inputs are transmitted through DNP as signed numbers. Even for analog input points that are not valid as negative values, the maximum positive representation is 32767 for 16-bit values and 2147483647 for 32-bit values. This is a DNP requirement.

The deadbands for all Analog Input points are in the same units as the Analog Input quantity. For example, an Analog Input quantity measured in volts has a corresponding deadband in units of volts. This is in conformance with DNP Technical Bulletin 9809-001: Analog Input Reporting Deadband. Relay settings are available to set default deadband values according to data type. Deadbands for individual Analog Input Points can be set using DNP Object 34.

Static (Steady-State) Object Number: **30**

Change Event Object Number: **32**

Request Function Codes supported: **1 (read), 2 (write, deadbands only), 22 (assign class)**

Static Variation reported when variation 0 requested: **1 (32-Bit Analog Input)**

Change Event Variation reported when variation 0 requested: **1 (Analog Change Event without Time)**

Change Event Scan Rate: defaults to **500 ms**

Change Event Buffer Size: **256**

Default Class for all Points: **2**

F.1.1 REVISION HISTORY

Table F–1: REVISION HISTORY

MANUAL P/N	L60 REVISION	RELEASE DATE	ECO
1601-0082-A1	1.5x	04 November 1998	N/A
1601-0082-A2	1.5x	25 June 1999	URL-054
1601-0082-A3	1.5x	19 August 1999	URL-056
1601-0082-A4	2.0x	26 January 2000	URL-062
1601-0082-A5	2.2x	12 May 2000	URL-066
1601-0082-A6	2.2x	14 June 2000	URL-069
1601-0082-A6a	2.2x	28 June 2000	URL-069a
1601-0082-B1	2.4x	08 September 2000	URL-074
1601-0082-B2	2.4x	03 November 2000	URL-076
1601-0082-B3	2.6x	09 March 2001	URL-080
1601-0082-B4	2.8x	12 October 2001	URL-089
1601-0082-B5	2.9x	03 December 2001	URL-091
1601-0082-C1	3.0x	02 July 2002	URL-093
1601-0082-C2	3.1x	30 August 2002	URL-097
1601-0082-C3	3.0x	18 November 2002	URL-099
1601-0082-C4	3.1x	18 November 2002	URL-100
1601-0082-C5	3.0x	11 February 2003	URL-103
1601-0082-C6	3.1x	11 February 2003	URL-104
1601-0082-D1	3.2x	11 February 2003	URL-107
1601-0082-E1	3.3x	01 May 2003	URX-080
1601-0082-E2	3.3x	29 May 2003	URX-083
1601-0082-K1	4.6x	15 March 2005	URX-176
1601-0082-L1	4.8x	05 August 2005	URX-202
1601-0082-M1	4.9x	15 December 2005	URX-208
1601-0082-M2	4.9x	27 February 2006	URX-214
1601-0082-N1	5.0x	31 March 2006	URX-217
1601-0082-N2	5.0x	26 May 2006	URX-220
1601-0082-P1	5.2x	23 October 2006	URX-230
1601-0082-P2	5.2x	24 January 2007	URX-232
1601-0082-R1	5.4x	26 June 2007	URX-242

F.1.2 CHANGES TO THE L60 MANUAL

Table F–2: MAJOR UPDATES FOR L60 MANUAL REVISION R1 (Sheet 1 of 2)

PAGE (P2)	PAGE (R1)	CHANGE	DESCRIPTION
Title	Title	Update	Manual part number to 1601-0082-R1
2-4	2-4	Update	Updated ORDERING section
2-9	2-9	Update	Updated PROTECTION ELEMENTS specifications section
3-1	3-1	Update	Updated PANEL CUTOUT section
3-4	3-5	Update	Updated MODULE WITHDRAWAL AND INSERTION section
3-6	3-9	Update	Updated TYPICAL WIRING section
4-4	4-4	Update	Updated FACEPLATE section

Table F–2: MAJOR UPDATES FOR L60 MANUAL REVISION R1 (Sheet 2 of 2)

PAGE (P2)	PAGE (R1)	CHANGE	DESCRIPTION
4-5	4-5	Update	Updated LED INDICATORS section
4-7	4-8	Update	Updated CUSTOM LABELING OF LEDS section
4-13	4-21	Update	Updated ENTERING INITIAL PASSWORDS section
5-8	5-8	Update	Updated PASSWORD SECURITY section
5-35	5-36	Update	Updated USER-PROGRAMMABLE LEDS section
5-39	5-40	Update	Updated CONTROL PUSHBUTTONS section
5-40	5-41	Update	Updated USER-PROGRAMMABLE PUSHBUTTONS section
5-46	5-48	Update	Updated DIRECT INPUTS AND OUTPUTS section
5-69	5-73	Update	Updated FLEXLOGIC™ OPERANDS table
5-186	5-193	Update	Updated TRIP OUTPUT section
---	5-234	Add	Added TRIP BUS section
6-18	6-18	Update	Updated FAULT REPORT section
7-3	7-3	Update	Updated RELAY SELF-TESTS section
---	8-37	Add	Added FAULT TYPE DETERMINATION section
9-10	9-10	Update	Updated PHASE DISTANCE section
9-10	9-11	Update	Updated GROUND DISTANCE section
B-7	B-8	Update	Updated MODBUS PASSWORD OPERATION section
B-8	B-9	Update	Updated MODBUS MEMORY MAP section
---	C-2	Add	Added GGIO4: GENERIC ANALOG MEASURED VALUES section
C-7	C-7	Update	Updated CONFIGURABLE GOOSE section

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Table F–3: MAJOR UPDATES FOR L60 MANUAL REVISION P2

PAGE (P1)	PAGE (P2)	CHANGE	DESCRIPTION
Title	Title	Update	Manual part number to 1601-0082-P2
2-4	2-4	Update	Updated ORDERING section
2-9	2-9	Update	Updated PROTECTION ELEMENTS specifications section
3-20	3-20	Update	Updated CPU MODULE COMMUNICATIONS WIRING diagram to 842765A2
---	4-8	Add	Added BREAKER CONTROL section
5-122	5-122	Update	Updated GROUND DISTANCE ZONE 2 TO 3 OP SCHEME diagram to 837019A7
5-154	5-153	Update	Updated WATTMETRIC ZERO-SEQUENCE LOGIC diagram to 837033A4
5-176	5-176	Update	Updated NEGATIVE-SEQUENCE OVERVOLTAGE SCHEME LOGIC diagram to 827839A3
6-15	6-15	Update	Updated TRACKING FREQUENCY section
---	6-16	Add	Added IEC 61850 GOOSE ANALOG VALUES section
7-4	7-4	Update	Updated SELF-TEST ERROR MESSAGES table
A-1	A-1	Update	Updated FLEXANALOG PARAMETERS table
B-8	B-8	Update	Updated MODBUS MEMORY MAP table

Table F–4: MAJOR UPDATES FOR L60 MANUAL REVISION P1

PAGE (N2)	PAGE (P1)	CHANGE	DESCRIPTION
Title	Title	Update	Manual part number to 1601-0082-P1
2-3	2-3	Update	Updated SINGLE LINE DIAGRAM to 831707AT
2-4	2-4	Update	Updated ORDERING section
2-9	2-9	Update	Updated PROTECTION ELEMENTS specifications section
3-23	3-23	Update	Updated L60 CHANNEL COMMUNICATIONS section
5-14	5-14	Update	Updated DNP PROTOCOL sub-section
5-18	5-18	Update	Updated IEC 61850 PROTOCOL sub-section
5-67	5-69	Update	Updated FLEXLOGIC™ OPERANDS table
5-87	5-89	Update	Updated 87PC SCHEME settings sub-section
---	5-95	Add	Added ADVANCED FAULT DETECTORS settings sub-section
---	5-95	Add	Added NEGATIVE-SEQUENCE VOLTAGE settings sub-section
---	5-97	Add	Added NEGATIVE-SEQUENCE CURRENT RATE OF CHANGE settings sub-section
---	5-98	Add	Added POSITIVE-SEQUENCE CURRENT RATE OF CHANGE settings sub-section
---	5-99	Add	Added CHARGE CURRENT COMPENSATION settings sub-section
5-142	5-151	Update	Updated WATTMETRIC ZERO-SEQUENCE DIRECTIONAL section
5-164	5-173	Update	Updated PHASE OVERVOLTAGE sub-section
---	5-175	Add	Added NEGATIVE-SEQUENCE OVERVOLTAGE sub-section
---	8-23	Add	Added CHARGING CURRENT COMPENSATION theory section
---	8-25	Add	Added L60 SIGNAL PROCESSING theory section
B-8	B-8	Update	Updated MODBUS MEMORY MAP section
C-1	C-1	Update	Updated Appendix C: IEC 61850 COMMUNICATIONS
E-1	E-1	Update	Updated DNP V3.00 DEVICE PROFILE section
E-4	E-4	Update	Updated DNP IMPLEMENTATION TABLE section
E-8	E-8	Update	Updated BINARY INPUT POINTS section
E-10	E-10	Update	Updated COUNTERS section

F.2.1 STANDARD ABBREVIATIONS

A..... Ampere
AC ..... Alternating Current
A/D ..... Analog to Digital
AE ..... Accidental Energization, Application Entity
AMP ..... Ampere
ANG ..... Angle
ANSI..... American National Standards Institute
AR ..... Automatic Reclosure
ASDU ..... Application-layer Service Data Unit
ASYM..... Asymmetry
AUTO ..... Automatic
AUX..... Auxiliary
AVG..... Average

BER..... Bit Error Rate
BF..... Breaker Fail
BFI..... Breaker Failure Initiate
BKR..... Breaker
BLK ..... Block
BLKG..... Blocking
BPNT..... Breakpoint of a characteristic
BRKR ..... Breaker

CAP..... Capacitor
CC ..... Coupling Capacitor
CCVT ..... Coupling Capacitor Voltage Transformer
CFG..... Configure / Configurable
.CFG..... Filename extension for oscillography files
CHK..... Check
CHNL ..... Channel
CLS ..... Close
CLSD..... Closed
CMND ..... Command
CMPRSN..... Comparison
CO..... Contact Output
COM..... Communication
COMM..... Communications
COMP ..... Compensated, Comparison
CONN..... Connection
CONT ..... Continuous, Contact
CO-ORD..... Coordination
CPU..... Central Processing Unit
CRC ..... Cyclic Redundancy Code
CRT, CRNT .... Current
CSA..... Canadian Standards Association
CT ..... Current Transformer
CVT..... Capacitive Voltage Transformer

D/A ..... Digital to Analog
DC (dc)..... Direct Current
DD ..... Disturbance Detector
DFLT ..... Default
DGNST..... Diagnostics
DI..... Digital Input
DIFF ..... Differential
DIR ..... Directional
DISCREP ..... Discrepancy
DIST ..... Distance
DMD ..... Demand
DNP..... Distributed Network Protocol
DPO ..... Dropout
DSP..... Digital Signal Processor
dt ..... Rate of Change
DTT ..... Direct Transfer Trip
DUTT..... Direct Under-reaching Transfer Trip

ENCRMNT ..... Encroachment
EPRI..... Electric Power Research Institute
.EVT ..... Filename extension for event recorder files
EXT ..... Extension, External

F..... Field
FAIL..... Failure
FD ..... Fault Detector
FDH..... Fault Detector high-set
FDL ..... Fault Detector low-set
FLA..... Full Load Current
FO ..... Fiber Optic
FREQ..... Frequency
FSK..... Frequency-Shift Keying
FTP..... File Transfer Protocol
FxE ..... FlexElement™
FWD..... Forward

G ..... Generator
GE..... General Electric
GND..... Ground
GNTR..... Generator
GOOSE..... General Object Oriented Substation Event
GPS ..... Global Positioning System

HARM ..... Harmonic / Harmonics
HCT ..... High Current Time
HGF ..... High-Impedance Ground Fault (CT)
HIZ..... High-Impedance and Arcing Ground
HMI ..... Human-Machine Interface
HTTP ..... Hyper Text Transfer Protocol
HYB ..... Hybrid

I..... Instantaneous
I_0..... Zero Sequence current
I_1..... Positive Sequence current
I_2..... Negative Sequence current
IA ..... Phase A current
IAB..... Phase A minus B current
IB ..... Phase B current
IBC..... Phase B minus C current
IC ..... Phase C current
ICA..... Phase C minus A current
ID ..... Identification
IED..... Intelligent Electronic Device
IEC..... International Electrotechnical Commission
IEEE..... Institute of Electrical and Electronic Engineers
IG ..... Ground (not residual) current
Igd..... Differential Ground current
IN ..... CT Residual Current (3Io) or Input
INC SEQ..... Incomplete Sequence
INIT..... Initiate
INST..... Instantaneous
INV..... Inverse
I/O ..... Input/Output
IOC ..... Instantaneous Overcurrent
IOV..... Instantaneous Overvoltage
IRIG ..... Inter-Range Instrumentation Group
ISO..... International Standards Organization
IUV..... Instantaneous Undervoltage

K0 ..... Zero Sequence Current Compensation
kA..... kiloAmpere
kV..... kiloVolt

LED..... Light Emitting Diode
LEO..... Line End Open
LFT BLD ..... Left Blinder
LOOP..... Loopback
LPU..... Line Pickup
LRA..... Locked-Rotor Current
LTC ..... Load Tap-Changer

M..... Machine
mA ..... MilliAmpere
MAG..... Magnitude
MAN..... Manual / Manually
MAX..... Maximum
MIC ..... Model Implementation Conformance
MIN ..... Minimum, Minutes
MMI..... Man Machine Interface
MMS ..... Manufacturing Message Specification
MRT ..... Minimum Response Time
MSG..... Message
MTA..... Maximum Torque Angle
MTR ..... Motor
MVA ..... MegaVolt-Ampere (total 3-phase)
MVA_A..... MegaVolt-Ampere (phase A)
MVA_B..... MegaVolt-Ampere (phase B)
MVA_C..... MegaVolt-Ampere (phase C)

MVAR ..... MegaVar (total 3-phase)
MVAR_A..... MegaVar (phase A)
MVAR_B..... MegaVar (phase B)
MVAR_C ..... MegaVar (phase C)
MVARH ..... MegaVar-Hour
MW..... MegaWatt (total 3-phase)
MW_A ..... MegaWatt (phase A)
MW_B ..... MegaWatt (phase B)
MW_C ..... MegaWatt (phase C)
MWH ..... MegaWatt-Hour

N..... Neutral
N/A, n/a ..... Not Applicable
NEG ..... Negative
NMPLT ..... Nameplate
NOM..... Nominal
NSAP ..... Network Service Access Protocol
NTR..... Neutral

O ..... Over
OC, O/C ..... Overcurrent
O/P, Op..... Output
OP ..... Operate
OPER ..... Operate
OPERATG..... Operating
O/S ..... Operating System
OSI..... Open Systems Interconnect
OSB..... Out-of-Step Blocking
OUT..... Output
OV..... Overvoltage
OVERFREQ... Overfrequency
OVLD ..... Overload

P..... Phase
PC ..... Phase Comparison, Personal Computer
PCNT ..... Percent
PF..... Power Factor (total 3-phase)
PF_A ..... Power Factor (phase A)
PF_B ..... Power Factor (phase B)
PF_C ..... Power Factor (phase C)
PFLL..... Phase and Frequency Lock Loop
PHS..... Phase
PICS..... Protocol Implementation & Conformance Statement
PKP ..... Pickup
PLC ..... Power Line Carrier
POS..... Positive
POTT..... Permissive Over-reaching Transfer Trip
PRESS..... Pressure
PRI ..... Primary
PROT ..... Protection
PSEL..... Presentation Selector
pu ..... Per Unit
PUIB..... Pickup Current Block
PUIT..... Pickup Current Trip
PUSHBTN..... Pushbutton
PUTT..... Permissive Under-reaching Transfer Trip
PWM ..... Pulse Width Modulated
PWR..... Power

QUAD..... Quadrilateral

R..... Rate, Reverse
RCA..... Reach Characteristic Angle
REF..... Reference
REM ..... Remote
REV..... Reverse
RI..... Reclose Initiate
RIP ..... Reclose In Progress
RGT BLD..... Right Blinder
ROD ..... Remote Open Detector
RST ..... Reset
RSTR ..... Restrained
RTD..... Resistance Temperature Detector
RTU..... Remote Terminal Unit
RX (Rx) ..... Receive, Receiver

s ..... second
S..... Sensitive

SAT .....CT Saturation
SBO .....Select Before Operate
SCADA .....Supervisory Control and Data Acquisition
SEC .....Secondary
SEL .....Select / Selector / Selection
SENS.....Sensitive
SEQ .....Sequence
SIR.....Source Impedance Ratio
SNTP .....Simple Network Time Protocol
SRC .....Source
SSB.....Single Side Band
SSEL.....Session Selector
STATS.....Statistics
SUPN.....Supervision
SUPV.....Supervise / Supervision
SV .....Supervision, Service
SYNC.....Synchrocheck
SYNCHCHK....Synchrocheck

T.....Time, transformer
TC .....Thermal Capacity
TCP.....Transmission Control Protocol
TCU .....Thermal Capacity Used
TD MULT .....Time Dial Multiplier
TEMP.....Temperature
TFTP.....Trivial File Transfer Protocol
THD .....Total Harmonic Distortion
TMR .....Timer
TOC .....Time Overcurrent
TOV .....Time Overvoltage
TRANS.....Transient
TRANSF .....Transfer
TSEL.....Transport Selector
TUC .....Time Undercurrent
TUV.....Time Undervoltage
TX (Tx).....Transmit, Transmitter

U .....Under
UC.....Undercurrent
UCA .....Utility Communications Architecture
UDP .....User Datagram Protocol
UL .....Underwriters Laboratories
UNBAL.....Unbalance
UR.....Universal Relay
URC .....Universal Recloser Control
.URS .....Filename extension for settings files
UV.....Undervoltage

V/Hz .....Volts per Hertz
V_0 .....Zero Sequence voltage
V_1 .....Positive Sequence voltage
V_2 .....Negative Sequence voltage
VA .....Phase A voltage
VAB.....Phase A to B voltage
VAG .....Phase A to Ground voltage
VARH .....Var-hour voltage
VB .....Phase B voltage
VBA.....Phase B to A voltage
VBG .....Phase B to Ground voltage
VC.....Phase C voltage
VCA .....Phase C to A voltage
VCG .....Phase C to Ground voltage
VF .....Variable Frequency
VIBR .....Vibration
VT .....Voltage Transformer
VTFF.....Voltage Transformer Fuse Failure
VTLOS.....Voltage Transformer Loss Of Signal

WDG .....Winding
WH.....Watt-hour
w/ opt .....With Option
WRT.....With Respect To

X .....Reactance
XDUCER.....Transducer
XFMR.....Transformer

Z.....Impedance, Zone

F

GE MULTILIN RELAY WARRANTY

General Electric Multilin Inc. (GE Multilin) warrants each relay it manufactures to be free from defects in material and workmanship under normal use and service for a period of 24 months from date of shipment from factory.

In the event of a failure covered by warranty, GE Multilin will undertake to repair or replace the relay providing the warrantor determined that it is defective and it is returned with all transportation charges prepaid to an authorized service centre or the factory. Repairs or replacement under warranty will be made without charge.

Warranty shall not apply to any relay which has been subject to misuse, negligence, accident, incorrect installation or use not in accordance with instructions nor any unit that has been altered outside a GE Multilin authorized factory outlet.

GE Multilin is not liable for special, indirect or consequential damages or for loss of profit or for expenses sustained as a result of a relay malfunction, incorrect application or adjustment.

For complete text of Warranty (including limitations and disclaimers), refer to GE Multilin Standard Conditions of Sale.

Numerics

A

B

C

D

E

F

G

H

I

K

L

M

N

O

P

Q

R

S

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U

V

W

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