



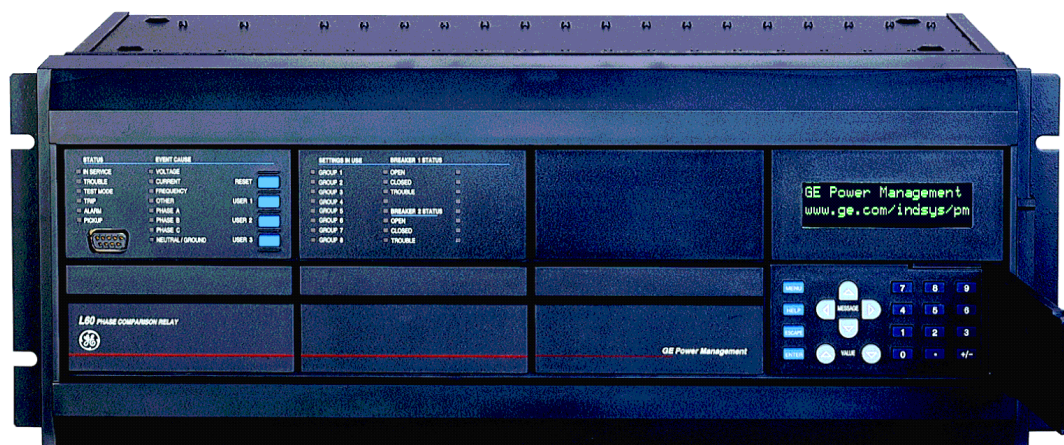
L60 Line Phase Comparison Relay

UR Series Instruction Manual

L60 Revision: 2.6X

Manual P/N: 1601-0082-**B3** (GEK-106320)

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NOTE

This relay is shipped from the factory with preset LED Panel indicators – see the ‘Settings \ Product Setup \ User-Programmable LEDs’ section for details and user options.

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Manufactured under an
ISO9000 Registered system.



ADDENDUM

This Addendum contains information that relates to the L60 relay, version 2.6X. This addendum lists a number of information items that appear in the instruction manual GEK-106320 (1601-0082-B3) but are not included in the current L60 operations.

The following functions/items are not yet available with the current version of the L60 relay:

- Phase Comparison schemes 3TL-PT-SPC-3FC and 3TL-BL-SPC-3FC
- RTD inputs
- Signal Sources SRC 3 to SRC 6 (availability is pending for this release)

NOTE:

- The UCA2 specifications are not yet finalized. There will be changes to the object models described in the Appendix - UCA/MMS.

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H. WARRANTY

H.1 WARRANTY INFORMATION

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Please read this chapter for information to help guide you through the initial steps of organizing the setting up of your new relay.

1.1.1 CAUTIONS AND WARNINGS



WARNING



CAUTION

Before attempting to install or use the relay, it is imperative that all WARNINGS and CAUTIONS in this manual are reviewed to help prevent personal injury, equipment damage, and/or downtime.

1.1.2 INSPECTION CHECKLIST

- Open the relay packaging and inspect the relay for physical damage.
- Check that the battery tab is intact on the power supply module (for more details, see the section BATTERY TAB in this chapter).
- View the rear name-plate and verify that the relay is the correct model ordered.

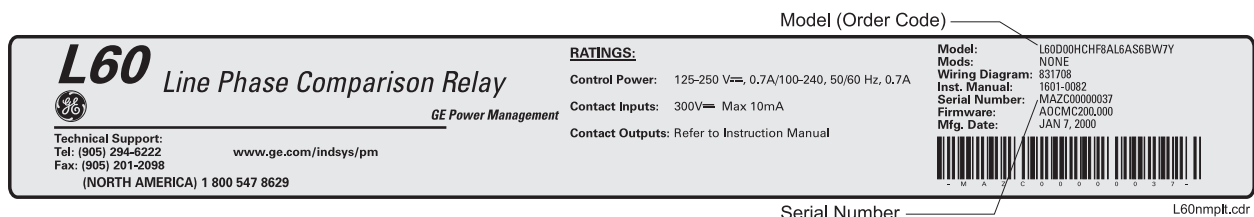


Figure 1-1: REAR NAME-PLATE (Example)

- Ensure that the following items have been included with the relay:
 - Instruction Manual
 - Products CD (includes UR PC software)
 - mounting screws
 - registration card (attached as the last page of the manual)
- Fill out the registration form and mail it back to GE Power Management (include the serial number located on the rear name-plate).
- For product information, instruction manual updates, and the latest software updates, please visit the GE Power Management Home Page.



NOTE

If there is any physical damage noticed on the relay, or any of the contents listed are missing, please contact GE Power Management immediately.

GE Power Management contact information and Call Center for product support:

GE Power Management
215 Anderson Avenue
Markham, Ontario
Canada L6E 1B3

Telephone: (905) 294-6222, 1-800-547-8629 (North America only)
Fax: (905) 201-2098
Email: info.pm@indsys.ge.com
Home Page: <http://www.ge.com/indsys/pm> or <http://www.GEindustrial.com/pm>

1.2.1 INTRODUCTION TO THE UR RELAY

Historically substations were designed with protection, control and metering functions performed by electro-mechanical equipment. This first generation of equipment was in time replaced in various degrees by analog electronic equipment, most of which emulated the single function approach required in the electromechanical precursors. Both of these technologies require a lot of expensive cabling and auxiliary equipment to produce functioning systems.

Recently digital electronic equipment has been applied to the purposes outlined above. Initially this equipment was either single function or had very limited multi-function capability, and did not significantly reduce the amount of cabling and auxiliary equipment required. Recent digital relays have become quite multi-functional, reducing cabling and auxiliaries even more. These devices also transfer data to central control facilities and Human Machine Interfaces, using electronic communications. The functions performed by these products have become so broad that many users now prefer the term IED (Intelligent Electronic Device).

It is obvious to station designers that the amount of cabling and auxiliary equipment installed in stations can be even further reduced, to 20% to 70% of the levels common in 1990, to achieve large cost reductions. This requires placing even more functions in the IEDs.

Users of power equipment are also interested in reducing cost by improving power quality and personnel productivity, and as always, in increasing system reliability and efficiency. These objectives are realized through software which is used to perform functions at both the station and supervisory levels. The use of these systems is growing rapidly.

High speed communications are required to meet the data transfer rates required by the automatic control and monitoring systems of today. In the near future, very high speed communications will be required to perform protection signaling with a performance target response time for a command signal between two IEDs, from transmission to reception, of less than 5 milliseconds as has been established by the Electric Power Research Institute, a collective body of many American and Canadian power utilities, in their Utilities Communications Architecture 2 (MMS/UCA2) project. In late 1998 some European utilities began to show an interest in this ongoing initiative.

IEDs with the capabilities outlined will also provide a lot more data on the power system than is presently available, enhance operations and maintenance, and permit the use of adaptive system configuration for protection and control systems. This new generation of equipment must also be easily incorporated into automation systems, at both the station and enterprise levels. The Universal Relay (UR) has been developed to meet these goals.

1.2.2 UR HARDWARE ARCHITECTURE

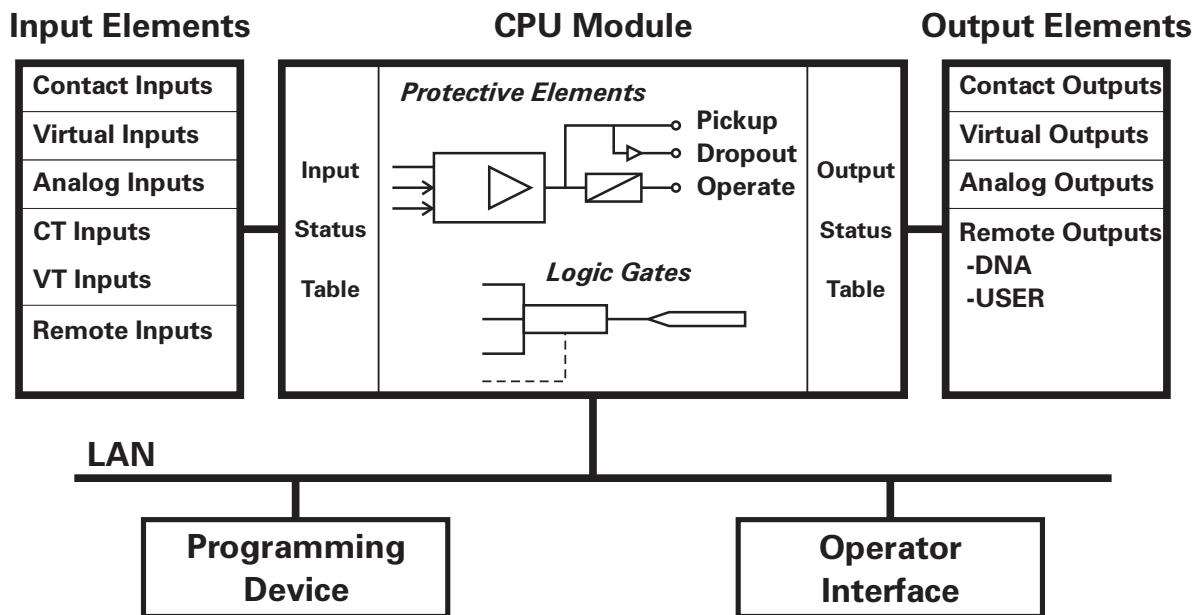


Figure 1-2: UR CONCEPT BLOCK DIAGRAM

827822A1.CDR

a) UR BASIC DESIGN

The UR is a digital-based device containing a central processing unit (CPU) which handles multiple types of input and output signals. The UR device can communicate over a local area network (LAN) with an operator interface, a programming device, or another UR device.

The **CPU module** contains firmware which provides protection elements in the form of logic algorithms, and programmable logic gates, timers, and latches for control features.

Input elements accept a variety of analog or digital signals from the field, isolate and convert the signals into logic signals which can be used by the relay.

Output elements convert and isolate the logic signals generated by the relay, into digital or analog signals that can be used to control field devices.

b) UR SIGNAL TYPES

The **contact inputs and outputs** are digital signals associated with connections to hard-wired contacts. Both 'wet' and 'dry' contacts are supported.

The **virtual inputs and outputs** are digital signals associated with the UR internal logic signals. Virtual inputs include signals generated by the local user interface. The virtual outputs are outputs of FlexLogic™ equations used to customize the UR device. Virtual outputs can also serve as virtual inputs to FlexLogic™ equations.

The **analog inputs and outputs** are signals that are associated with transducers such as Resistance Temperature Detectors (RTDs), etc.

The **CT and VT inputs** refer to analog current transformer and voltage transformer signals used to monitor AC power lines. The UR supports 1 A or 5 A CTs.

The **remote inputs and outputs** provide a means of sharing digital point state information between remote UR devices. The remote outputs interface to the remote inputs of other UR devices. Remote outputs are FlexLogic™ operands inserted into UCA2 GOOSE messages and are of two assignment types; DNA standard functions and USER defined functions.

c) UR SCAN OPERATION

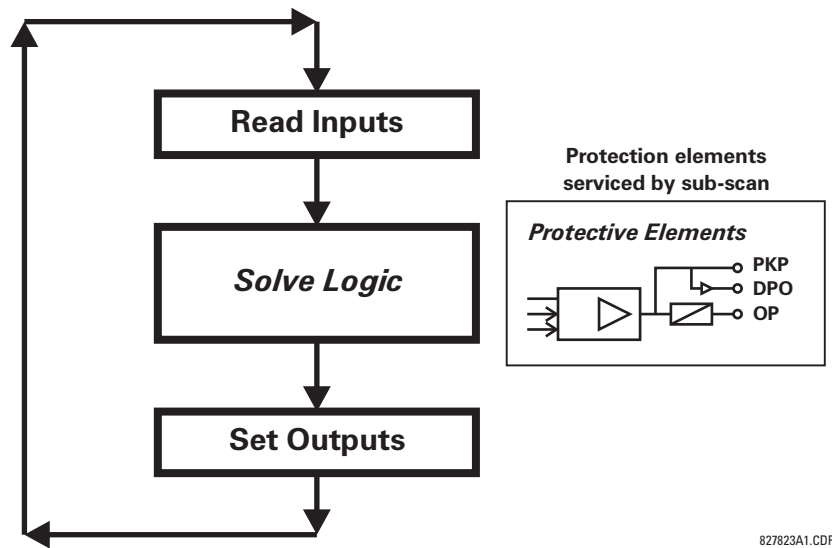


Figure 1–3: UR SCAN OPERATION

The UR device operates in a cyclic scan fashion. The UR reads the inputs into an input status table, solves the logic program (FlexLogic™ equation), and then sets each output to the appropriate state in an output status table. Any resulting task execution is priority interrupt-driven.

1.2.3 UR SOFTWARE ARCHITECTURE

The firmware (software embedded in the relay) is designed in functional modules which can be installed in any relay as required. This is achieved with Object-Oriented Design and Programming (OOD/OOP) techniques.

Object-Oriented techniques involve the use of 'objects' and 'classes'. An 'object' is defined as "a logical entity that contains both data and code that manipulates that data". A 'class' is the generalized form of similar objects. By using this concept, one can create a Protection Class with the Protection Elements as objects of the class such as Time Overcurrent, Instantaneous Overcurrent, Current Differential, Undervoltage, Overvoltage, Underfrequency, Distance, etc. These objects represent software modules that are completely self-contained. The same object-class concept can be used for Metering, I/O Control, HMI, Communications, or for any functional entity in the system.

Employing OOD/OOP in the software architecture of the Universal Relay achieves the same features as for the hardware architecture; modularity, scalability, and flexibility. The application software for any Universal Relay (e.g. Feeder Protection, Transformer Protection, Distance Protection, etc.) is constructed by combining objects from the various functionality classes. This results in a 'common look and feel' across the entire family of UR platform-based applications.

1.2.4 IMPORTANT UR CONCEPTS

As described above, the architecture of the UR relay is different from previous devices. In order to achieve a general understanding of this device, some sections of Chapter 5 are quite helpful. The most important functions of the relay are contained in "Elements". A description of UR elements can be found in the INTRODUCTION TO ELEMENTS section. An example of a simple element, and some of the organization of this manual, can be found in the DIGITAL ELEMENTS MENU section. An explanation of the use of inputs from CTs and VTs is in the INTRODUCTION TO AC SOURCES section. A description of how digital signals are used and routed within the relay is contained in the INTRODUCTION TO FLEXLOGIC™ section.

1.3.1 PC REQUIREMENTS

1

The Faceplate keypad and display or the URPC software interface can be used to communicate with the relay.

The URPC software interface is the preferred method to edit settings and view actual values because the PC monitor can display more information in a simple comprehensible format.

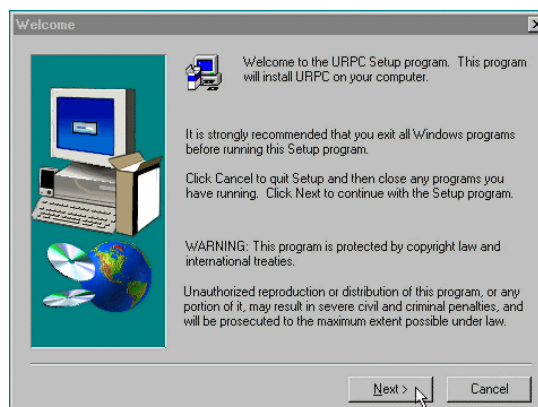
The following minimum requirements must be met for the URPC software to properly operate on a PC.

Processor:	Intel® Pentium 200 MMX
RAM Memory:	32 Mb (64 Mb recommended)
Hard Disk:	20 Mb free space required before installation of URPC software
O/S:	Windows® NT 4.x or Windows® 9x
Device:	CD ROM drive
Port:	COM1(2) / Ethernet

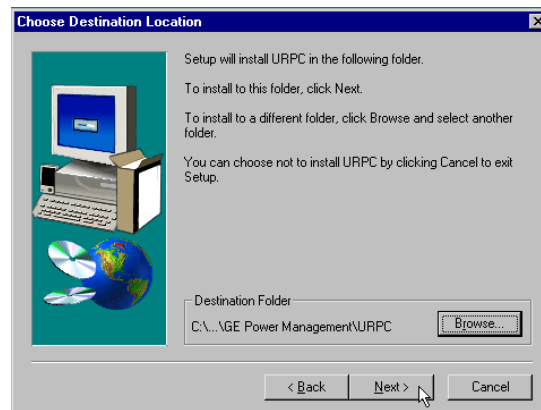
1.3.2 SOFTWARE INSTALLATION

Refer to the following instructions to install the URPC software onto a PC:

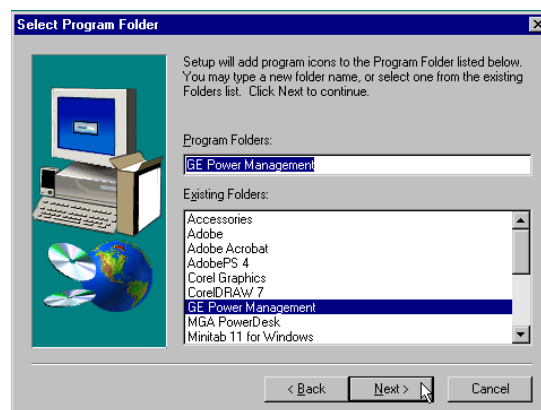
1. **Start** the **Windows®** program.
2. **Insert** the URPC software CD into the CD ROM drive.
3. If the installation program does not start automatically, choose **Run** from the Windows® **Start** menu and type D:\SETUP.EXE. Press Enter to start the installation.
4. Follow the on-screen instructions to install the URPC software. When the **Welcome** window appears, click on **Next** to continue with the installation procedure.



5. When the **Choose Destination Location** window appears and if the software is not to be located in the default directory, click **Browse** and type in the complete path name including the new directory name.
6. Click **Next** to continue with the installation procedure.



7. The default program group where the application will be added to is shown in the **Select Program Folder** window. If it is desired that the application be added to an already existing program group, choose the group name from the list shown.
8. Click **Next** to begin the installation process.



9. To launch the URPC application, click Finish in the Setup Complete window.
10. Subsequently, double click on the URPC software icon to activate the application.



NOTE

Refer to the **HUMAN INTERFACES** chapter in this manual and the URPC Software Help program for more information about the URPC software interface.

1.3.3 CONNECTING URPC® WITH THE L60

1

This section is intended as a quick start guide to using the URPC software. Please refer to the URPC Help File and the HUMAN INTERFACES chapter for more information.

a) CONFIGURING AN ETHERNET CONNECTION

Before starting, verify that the Ethernet network cable is properly connected to the Ethernet port on the back of the relay.

1. Start the URPC software. Enter the password "URPC" at the login password box.
2. Select the **Help > Connection Wizard** menu item to open the Connection Wizard. Click "Next" to continue.
3. Click the "New Interface" button to open the Edit New Interface window.
 - Enter the desired interface name in the **Enter Interface Name** field.
 - Select the "Ethernet" interface from the drop down list and press "Next" to continue.
4. Click the "New Device" button to open the Edit New Device Window.
 - Enter the desired name in the **Enter Interface Name** field.
 - Enter the Modbus address of the relay (from **S1 PRODUCT SETUP \ COMMUNICATIONS \ MODBUS PROTOCOL \ MODBUS SLAVE ADDRESS**) in the **Enter Modbus Address** field.
 - Enter the IP address (from **S1 PRODUCT SETUP \ COMMUNICATIONS \ NETWORK \ IP ADDRESS**) in the **Enter TCPIP Address** field.
5. Click the "4.1 Read Device Information" button then "OK" when the relay information has been received. Click "Next" to continue.
6. Click the "New Site" button to open the Edit Site Name window.
 - Enter the desired site name in the **Enter Site Name** field.
7. Click the "OK" button then click "Finish". The new Site List tree will be added to the Site List window (or Online window) located in the top left corner of the main URPC window.

The Site Device has now been configured for Ethernet communications. Proceed to Section c) CONNECTING TO THE RELAY below to begin communications.

b) CONFIGURING AN RS232 CONNECTION

Before starting, verify that the RS232 serial cable is properly connected to the RS232 port on the front panel of the relay.

1. Start the URPC software. Enter the password "URPC" at the login password box.
2. Select the **Help > Connection Wizard** menu item to open the Connection Wizard. Click "Next" to continue.
3. Click the "New Interface" button to open the Edit New Interface window.
 - Enter the desired interface name in the **Enter Interface Name** field.
 - Select the "RS232" interface from the drop down list and press "Next" to continue.
4. Click the "New Device" button to open the Edit New Device Window.
 - Enter the desired name in the **Enter Interface Name** field.
 - Enter the PC COM port number in the **COM Port** field.
5. Click "OK" then click "Next" to continue.

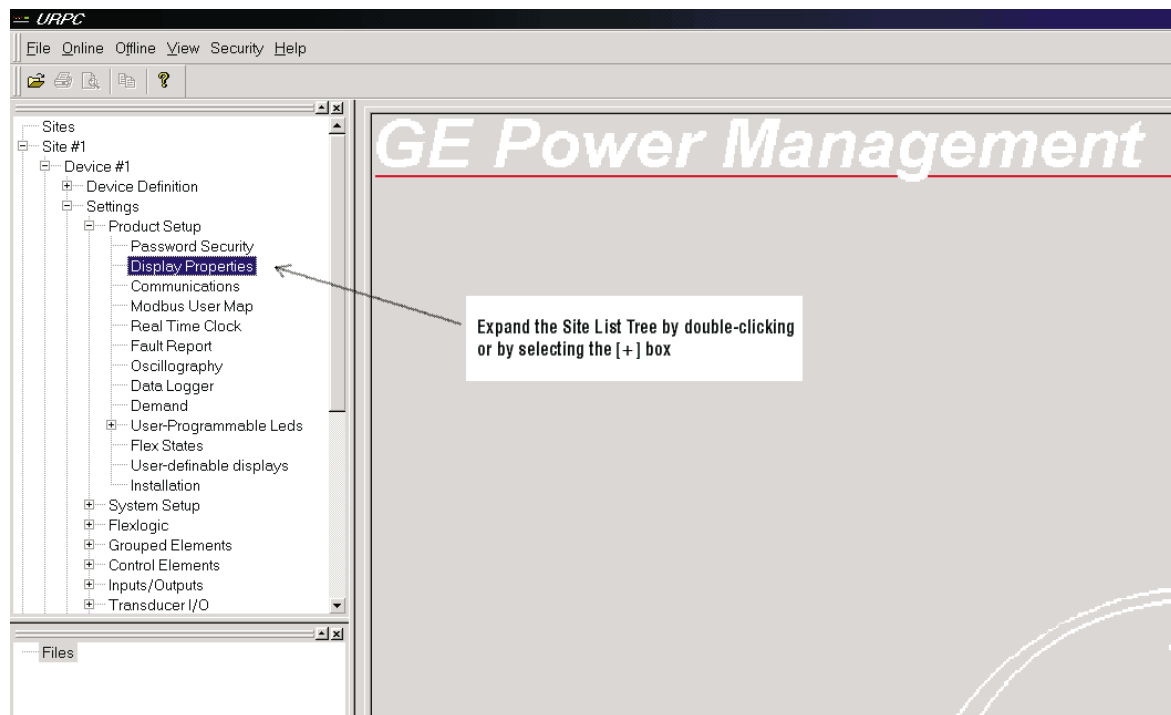
1

6. Click the "New Site" button to open the Edit Site Name window.
 - Enter the desired site name in the **Enter Site Name** field.
7. Click the "OK" button then click "Finish". The new Site List tree will be added to the Site List window (or Online window) located in the top left corner of the main URPC window.

The Site Device has now been configured for RS232 communications. Proceed to Section c) CONNECTING TO THE RELAY below to begin communications.

c) CONNECTING TO THE RELAY

1. Select the Display Properties window through the Site List tree as shown below:



2. The Display Properties window will open with a flashing status indicator.
 - If the indicator is red, click the Connect button (the lightning bolt) in the menu bar of the Displayed Properties window.
3. In a few moments, the flashing light should turn green, indicating that URPC is communicating with the relay.



NOTE

Refer to the HUMAN INTERFACES chapter in this manual and the URPC Software Help program for more information about the URPC software interface.

1.4.1 MOUNTING AND WIRING

Please refer to the HARDWARE chapter for detailed relay mounting and wiring instructions. Review all **WARNINGS** and **CAUTIONS**.

1.4.2 COMMUNICATIONS

The URPC software can communicate to the relay via the faceplate RS232 port, or the rear panel RS485 or Ethernet ports. To communicate with the relay via the faceplate RS232 port, a standard "straight through" serial cable is used. The DB-9 male end is connected to the relay and the DB-9 or DB-25 female end is connected to the PC COM1 or COM2 port as described in the HARDWARE chapter.

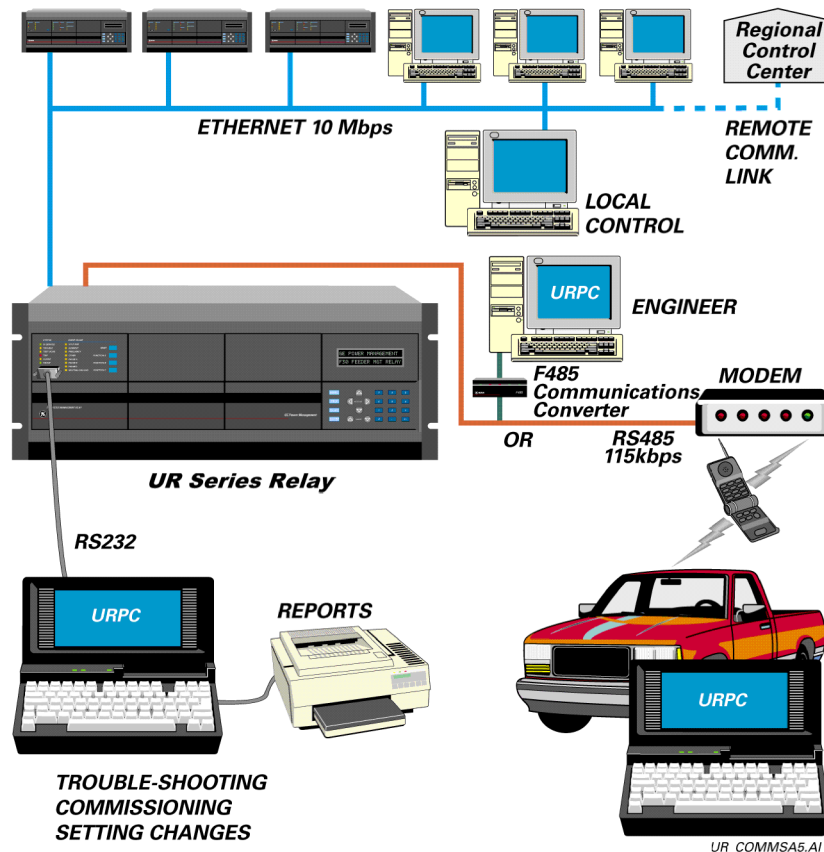


Figure 1–4: RELAY COMMUNICATIONS OPTIONS

To communicate through the relay's rear RS485 port from a PC RS232 port, the GE Power Management RS232/RS485 converter box is required. This device (catalog number F485) connects to the computer using a "straight-through" serial cable. A shielded twisted-pair (20, 22, or 24 AWG) connects the F485 converter to the UR rear communications port. The converter terminals (+, –, GND) are connected to the UR communication module (+, –, COM) terminals. Refer to the CPU COMMUNICATION PORTS section in the HARDWARE chapter for option details. The line should be terminated with an R-C network (i.e. 120 Ω , 1 nF) as described in the HARDWARE chapter.

1.4.3 FACEPLATE DISPLAY

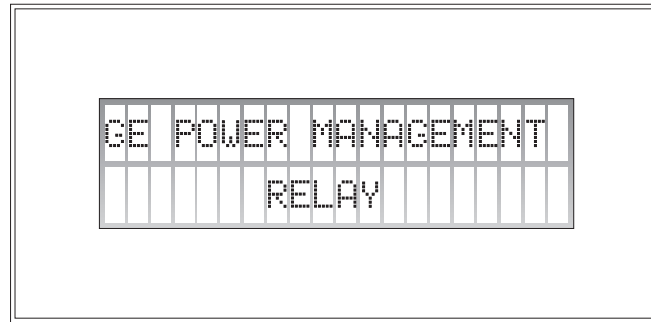


Figure 1-5: DISPLAY

All messages are displayed on a 2 × 20 character vacuum fluorescent display to make them visible under poor lighting conditions. Messages are displayed in English and do not require the aid of an instruction manual for deciphering. While the keypad and display are not actively being used, the display will default to defined messages. Any high priority event driven message will automatically override the default message and appear on the display.

1.4.4 FACEPLATE KEYPAD

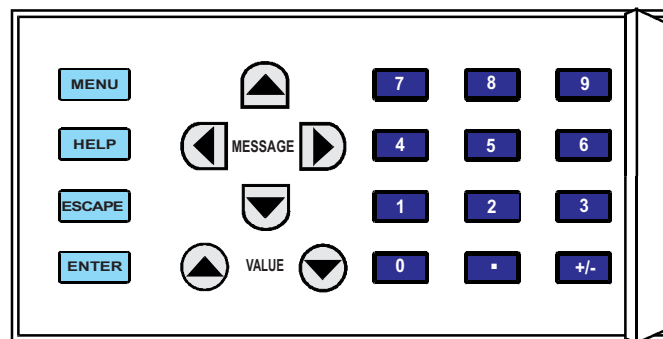


Figure 1-6: KEYPAD

Display messages are organized into 'pages' under the main headings, Actual Values, Settings, Commands, and Targets. The **MENU** key is used to navigate through the main heading pages. Each main heading page is further broken down into logical subgroup messages.

The **▲** **◀** **MESSAGE** **▶** **▼** keys are used to navigate through the subgroups.

The **▲** **VALUE** **▼** keys are used to scroll through variables in the settings programming mode to increment or decrement numerical setting values. These keys are also used to scroll through alphanumeric values in the text edit mode. Alternatively, values may be entered with the numeric keypad.

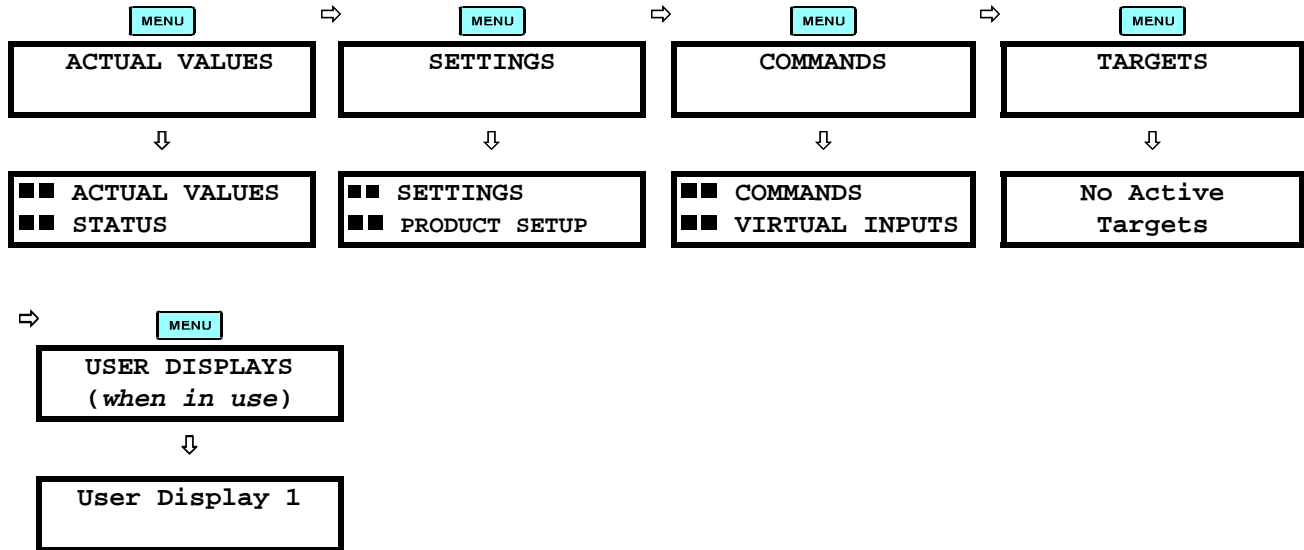
The **■** key is used to initiate and advance to the next character in text edit mode or to enter a decimal point.

The **HELP** key may be pressed at any time for context sensitive help messages. The **ENTER** key is used to store altered setting values.

1.5.1 MENU NAVIGATION

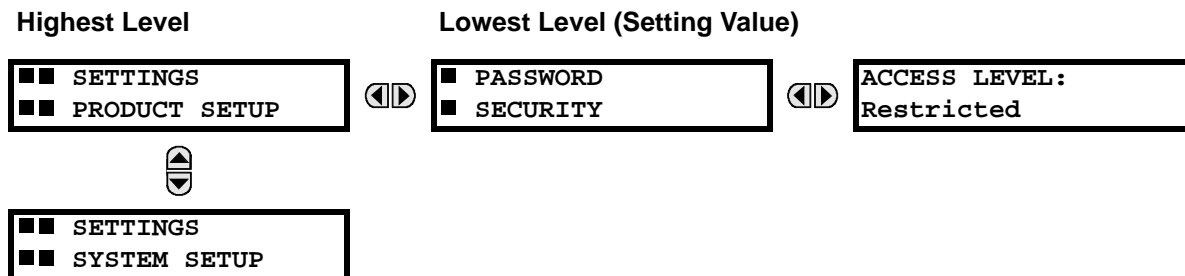
1

Press the **MENU** key to select the desired header display page (top-level menu). The header title will appear momentarily and then a header display page menu item will appear on the display. Each press of the **MENU** key advances through the main heading pages as illustrated below.



a) MENU HIERARCHY

The setting and actual value messages are set up in a hierarchical format. The header display pages are indicated by the double scroll bar characters (■■), while sub-header pages are indicated by a single scroll bar character (■). The header display pages are at the highest level of the hierarchy and the sub-header display pages fall below this level. The MESSAGE and MESSAGE keys are used to move within a group of headers, sub-headers, setting values or actual values. Continually pressing the MESSAGE key from a header display, displays more specific information for the header category. Conversely, continually pressing the MESSAGE key from a setting value or actual value display will return to the header display.






1.5.2 RELAY ACTIVATION

The relay is defaulted to the 'Not Programmed' state before it leaves the factory. This safeguards against the installation of a relay whose settings have not been entered. When powered up successfully, the TROUBLE indicator will be on and the IN SERVICE indicator off. The relay in the 'Not Programmed' state will block signaling of any output relay. These conditions will remain until the relay is explicitly put in the 'Programmed' state.

Select the menu message SETTINGS PRODUCT SETUP \ INSTALLATION \ RELAY SETTINGS:

RELAY SETTINGS: Not Programmed
--

To put the relay in the 'Programmed' state, press either of the  VALUE  keys once and then press . The faceplate TROUBLE indicator will turn off and the IN SERVICE indicator will turn on.

The settings for the relay can be set up manually (refer to the SETTINGS chapter) via the Faceplate Interface or remotely (refer to the URPC Help program) via the URPC Software Interface.

1.5.3 BATTERY TAB

The battery tab is installed in the power supply module before it is shipped from the factory. The purpose of the battery tab is to prolong the life of the battery in the event the relay is powered down for long periods of time before installation. The battery is responsible for backing up event records, oscillography, data logger, and real-time clock information when the relay is powered off. The battery failure self-test error generated by the relay is a minor self-test error and should not affect the functionality of the relay. When the relay is installed and ready for commissioning, the tab should be removed. If required, contact the factory for a replacement battery.

1.5.4 RELAY PASSWORDS

It is recommended that passwords be set up on the relay for each security level and assigned to specific personnel. There are two user password SECURITY access levels:

1. COMMAND

The COMMAND access level restricts the user from making any settings changes, but allows the user to perform the following operations:

- operate breakers via faceplate pushbuttons
- change state of virtual inputs
- clear event records
- clear oscillography records

2. SETTING

The SETTING access level allows the user to make any changes to any of the setting values.

Refer to the HUMAN INTERFACES chapter, CHANGING SETTINGS section for complete instructions on setting up security level passwords.

1.5.5 FLEXLOGIC™ CUSTOMIZATION

FlexLogic™ equation editing is required for setting up user-defined logic for customizing the relay operations. See section FLEXLOGIC™ in the SETTINGS chapter.

1.5.6 COMMISSIONING

Templated tables for charting all the required settings before entering them via the keypad are available in the COMMISSIONING chapter.

2.1.1 OVERVIEW

The L60 relay is a high-speed digital phase comparison protection relay system for HV and EHV transmission lines.

In addition to phase comparison protection, the L60 relay provides instantaneous and time overcurrent backup protection for phase, neutral, and negative sequence faults. Distance, breaker failure, undervoltage and over-voltage protection is also built in. The time overcurrent curves may be selected from a selection of standard curve shapes or a custom FlexCurve™ for optimum co-ordination.

Control features include synchrocheck, autoreclosure, and control for two breakers. Monitoring features include CT failure detector, VT fuse failure detector, breaker arcing current, disturbance detector and continuous monitor.

Diagnostic features include a sequence of records capable of storing 1024 time-tagged events. The internal clock used for time-tagging can be synchronized with an IRIG-B signal. This precise time stamping allows the sequence of events to be determined throughout the system. Events can also be programmed (via FlexLogic™ equations) to trigger oscillography data capture which may be set to record the measured parameters before and after the event for viewing on a portable computer (PC). These tools will significantly reduce troubleshooting time and simplify report generation in the event of a system fault.

A faceplate RS232 port may be used to connect to a PC for the programming of settings and for the monitoring of actual values. A variety of communications modules are available. Two rear RS485 ports are standard to allow independent access by operating and engineering staff. All serial ports use the Modbus® RTU protocol. The RS485 ports may be connected to system computers with baud rates up to 115.2 kbps. The RS232 port has a fixed baud rate of 19.2 kbps. Optional communications modules include a 10BaseF Ethernet interface which can be used to provide fast, reliable communications in noisy environments. Another option provides two 10BaseF fiber optic ports for redundancy. The Ethernet port supports MMS/UCA2, Modbus®/TCP, and TFTP protocols, and allows access to the relay via any standard web browser (UR web pages). The DNP 3.0 protocol is supported on a user-specified port, including serial and Ethernet ports.

The relay uses flash memory technology which allows field upgrading as new features are added.

The following SINGLE LINE DIAGRAM illustrates the relay functionality using ANSI (American National Standards Institute) device numbers.

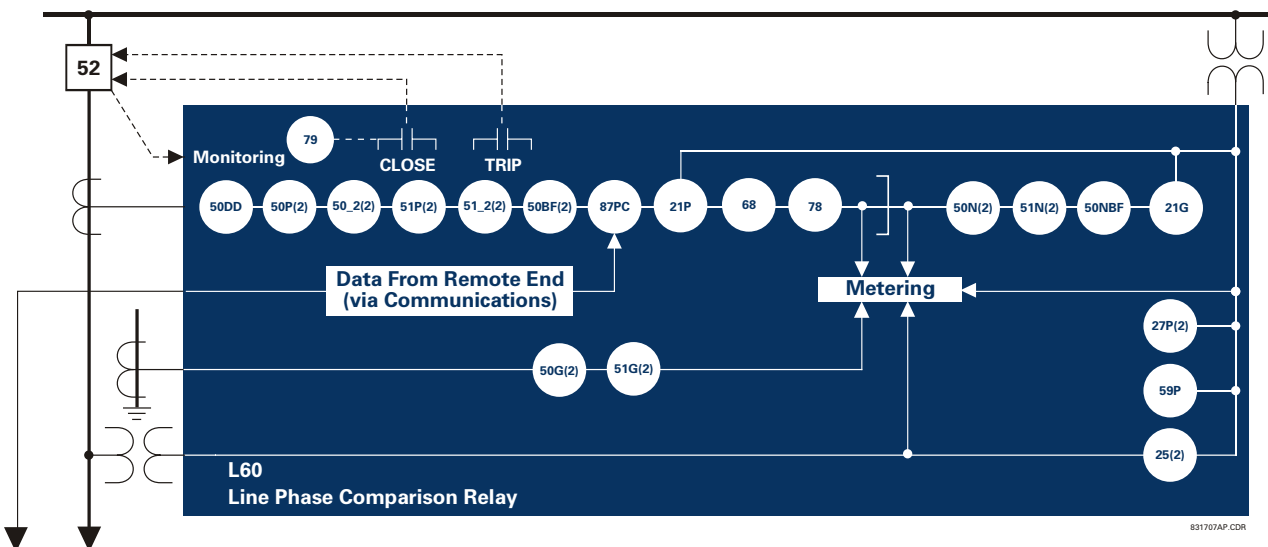


Figure 2–1: SINGLE LINE DIAGRAM

Table 2-1: DEVICE NUMBERS AND FUNCTIONS

DEVICE NUMBER	FUNCTION
21G	Ground Distance
21P	Phase Distance
25	Synchrocheck
27P	Phase Undervoltage
50BF	Breaker Failure
50DD	Disturbance Detector
50G	Ground Instantaneous Overcurrent
50N	Neutral Instantaneous Overcurrent
50P	Phase Instantaneous Overcurrent
50_2	Negative Sequence Instantaneous Overcurrent
51G	Ground Time Overcurrent
51N	Neutral Time Overcurrent
51P	Phase Time Overcurrent
51_2	Negative Sequence Time Overcurrent
52	AC Circuit Breaker
59P	Phase Overvoltage
68	Power Swing Blocking
78	Out-of-step Tripping
79	Automatic Recloser
87PC	Phase Comparison

Table 2-2: OTHER DEVICE FUNCTIONS

FUNCTION	FUNCTION	FUNCTION
Breaker Arcing Current (I^2t)	Event Recorder	Open Breaker Echo
Breaker Control	Fault Location	Oscillography
Contact Inputs (up to 96)	FlexLogic Equations	Pilot Scheme (POTT)
Contact Outputs (up to 64)	Line Pickup	Setting Groups (8)
CT Failure Detector	Metering: Current, Voltage, Power Frequency	Transducer I/O
Data Logger	MMS/UCA Communications	User Definable LEDs
Digital Counters (8)	MMS/UCA Remote I/O ("GOOSE")	Virtual Inputs (32)
Digital Elements (16)	ModBus Communications	Virtual Outputs (64)
DNP 3.0	ModBus User Map	VT Fuse Failure

2.1.2 ORDERING

The relay is available as a 19 inch rack horizontal mount unit or as a reduced size (3/4) vertical mount unit, and consists of the following UR module functions: Power Supply, CPU, CT/VT DSP, Digital Input/Output, Transducer I/O, and L60 Communications. Each of these modules can be supplied in a number of configurations which must be specified at the time of ordering. The information required to completely specify the relay is provided in the following table (full details of the modules that are available for the relay are contained in the HARDWARE chapter.)

Table 2-3: ORDER CODES

L60 - * 00 - HC * - F ** - H ** - L ** - N ** - S ** - U ** - W **												For Full Sized Horizontal Mount
L60 - * 00 - V F * - F ** - H ** - L ** - N ** - R **												For Reduced Size Vertical Mount
Base Unit	L60											Base Unit
CPU	A											RS485 + RS485 (ModBus RTU, DNP)
	C											RS485 + 10BaseF (MMS/UC2, Modbus TCP/IP, DNP)
	D											RS485 + Redundant 10BaseF (MMS/UC2, Modbus TCP/IP, DNP)
Software Options	00											No Software Options
Mount / Faceplate	H C											Horizontal (19" rack)
	V F											Vertical (3/4 size)
Power Supply	H											125 / 250 V AC/DC
	L											24 - 48 V (DC only)
CT/VT DSP	8A											Standard 4CT/4VT
	8C											Standard 8CT
Digital I/O ¹												No Module
	6A		6A		6A		6A		6A			2 Form-A (Voltage w/ opt Current) & 2 Form-C Outputs, 8 Digital Inputs
	6B		6B		6B		6B		6B			2 Form-A (Voltage w/ opt Current) & 4 Form-C Outputs, 4 Digital Inputs
	6C		6C		6C		6C		6C			8 Form-C Outputs
	6D		6D		6D		6D		6D			16 Digital Inputs
	6E		6E		6E		6E		6E			4 Form-C Outputs, 8 Digital Inputs
	6F		6F		6F		6F		6F			8 Fast Form-C Outputs
	6G		6G		6G		6G		6G			4 Form-A (Voltage w/ opt Current) Outputs, 8 Digital Inputs
	6H		6H		6H		6H		6H			6 Form-A (Voltage w/ opt Current) Outputs, 4 Digital Inputs
	6K		6K		6K		6K		6K			4 Form-C & 4 Fast Form-C Outputs
	6L		6L		6L		6L		6L			2 Form-A (Current w/ opt Voltage) & 2 Form-C Outputs, 8 Digital Inputs
	6M		6M		6M		6M		6M			2 Form-A (Current w/ opt Voltage) & 4 Form-C Outputs, 4 Digital Inputs
	6N		6N		6N		6N		6N			4 Form-A (Current w/ opt Voltage) Outputs, 8 Digital Inputs
	6P		6P		6P		6P		6P			6 Form-A (Current w/ opt Voltage) Outputs, 4 Digital Inputs
	6R		6R		6R		6R		6R			2 Form-A (No Monitoring) & 2 Form-C Outputs, 8 Digital Inputs
	6S		6S		6S		6S		6S			2 Form-A (No Monitoring) & 4 Form-C Outputs, 4 Digital Inputs
	6T		6T		6T		6T		6T			4 Form-A (No Monitoring) Outputs, 8 Digital Inputs
	6U		6U		6U		6U		6U			6 Form-A (No Monitoring) Outputs, 4 Digital Inputs
Transducer I/O ¹ (max of 4 per unit)	5C		5C		5C		5C		5C			8 RTD Inputs
	5E		5E		5E		5E		5E			4 RTD Inputs, 4 dcmA Inputs
	5F		5F		5F		5F		5F			8 dcmA Inputs
Inter-Relay Communications												7Y 125 V Input, 5V Output, 20 mA Channel Interface
												7Z 5 V Input, 5V Output, 20 mA Channel Interface
												7V 48/60 V, 20 mA Input/Output Channel Interface
												7U 110/125 V, 20 mA Input/Output Channel Interface

¹Custom I/O configurations available. Consult factory with requirements.

The following table displays the appropriate order codes of individual modules if replacement modules need to be ordered separately.



When ordering a replacement CPU module or Faceplate, please provide the serial number of your existing unit.

Table 2–4: ORDER CODES FOR ORDERING REPLACEMENT MODULES

	UR - ** -	
Power Supply	1H	125 / 250 V AC/DC
	1L	24 - 48 V (DC only)
CPU	9A	RS485 + RS485 (ModBus RTU, DNP 3.0)
	9C	RS485 + 10BaseF (MMS/UCA2, ModBus TCP/IP, DNP 3.0)
	9D	RS485 + Redundant 10BaseF (MMS/UCA2, ModBus TCP/IP, DNP 3.0)
Faceplate	3C	Horizontal Faceplate with Display & Keypad
	3F	Vertical Faceplate with Display & Keypad
Digital I/O	6A	2 Form-A (Voltage w/ opt Current) & 2 Form-C Outputs, 8 Digital Inputs
	6B	2 Form-A (Voltage w/ opt Current) & 4 Form-C Outputs, 4 Digital Inputs
	6C	8 Form-C Outputs
	6D	16 Digital Inputs
	6E	4 Form-C Outputs, 8 Digital Inputs
	6F	8 Fast Form-C Outputs
	6G	4 Form-A (Voltage w/ opt Current) Outputs, 8 Digital Inputs
	6H	6 Form-A (Voltage w/ opt Current) Outputs, 4 Digital Inputs
	6K	4 Form-C & 4 Fast Form-C Outputs
	6L	2 Form-A (Current w/ opt Voltage) & 2 Form-C Outputs, 8 Digital Inputs
	6M	2 Form-A (Current w/ opt Voltage) & 4 Form-C Outputs, 4 Digital Inputs
	6N	4 Form-A (Current w/ opt Voltage) Outputs, 8 Digital Inputs
	6P	6 Form-A (Current w/ opt Voltage) Outputs, 4 Digital Inputs
	6R	2 Form-A (No Monitoring) & 2 Form-C Outputs, 8 Digital Inputs
	6S	2 Form-A (No Monitoring) & 4 Form-C Outputs, 4 Digital Inputs
	6T	4 Form-A (No Monitoring) Outputs, 8 Digital Inputs
CT/VT DSP	6U	6 Form-A (No Monitoring) Outputs, 4 Digital Inputs
	8A	Standard 4CT/4VT
	8B	Sensitive Ground 4CT/4VT
	8C	Standard 8CT
	8Z	HI-Z 4CT
L60 Inter-Relay Communications	7U	110/125 V, 20 mA Input/Output Channel Interface
	7V	48/60 V, 20 mA Input/Output Channel Interface
	7Y	125 V Input, 5V Output, 20 mA Channel Interface
	7Z	5 V Input, 5V Output, 20 mA Channel Interface
L90 Inter-Relay Communications	7A	820 nm, multi-mode, LED, 1 Channel
	7B	1300 nm, multi-mode, LED, 1 Channel
	7C	1300 nm, single-mode, ELED, 1 Channel
	7D	1300 nm, single-mode, LASER, 1 Channel
	7H	820 nm, multi-mode, LED, 2 Channels
	7I	1300 nm, multi-mode, LED, 2 Channels
	7J	1300 nm, single-mode, ELED, 2 Channels
	7K	1300 nm, single-mode, LASER, 2 Channels
	7L	Channel 1 - RS422; Channel 2 - 820 nm, multi-mode, LED
	7M	Channel 1 - RS422; Channel 2 - 1300 nm, multi-mode, LED
	7N	Channel 1 - RS422; Channel 2 - 1300 nm, single-mode, ELED
	7P	Channel 1 - RS422; Channel 2 - 1300 nm, single-mode, LASER
	7R	G.703, 1 Channel
	7S	G.703, 2 Channels
	7T	RS422, 1 Channel
	7W	RS422, 2 Channels
Transducer I/O	5C	8 RTD Inputs
	5E	4 dcmA Inputs, 4 RTD Inputs
	5F	8 dcmA Inputs

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

2.2.1 PROTECTION ELEMENTS



The operating times published below include the activation time of a trip rated Form-A output contact unless otherwise indicated. FlexLogic™ operands representing operation of a given element are available 4 ms faster. This should be taken into account when using FlexLogic™ operands to interconnect with other protection or control elements of the relay, building FlexLogic™ equations, or interfacing with other IEDs or power system devices via communications or different output contacts.

2

87PC SCHEME

Signal Selection: Mixed I₂ - K*I₁
(K = 0.00 to 0.25 in steps of 0.01),
or 3I₀

Fault Detector Low: 0.01 to 5.00 pu in steps of 0.01

Fault Detector High: 0.01 to 5.00 pu in steps of 0.01

Signal Symmetry Adjustment: -20.0 to 20.0 ms in steps of 0.1

Channel Delay Adjustment: 0.000 to 65.535 ms in steps of 0.001

Channel Adjustments: Channel delay and signal symmetry automatic measurements

OPEN BREAKER ECHO

Keying of the transmitter in case one end of the line is open or weak-infeed at the terminal.

LINE PICKUP

Phase IOC: 0.000 to 30.000 pu

Pos. Seq. UV: 0.000 to 3.000 pu

Pos. Seq. OV Delay: 0.000 to 65.535 s

PHASE DISTANCE

Characteristic: Dynamic (100% memory-polarized) MHO

Number of Zones: 1

Directionality: Reversible

Reach (secondary ohms):

1 A CT: 0.10 to 250.00 Ω in steps of 0.01

5 A CT: 0.02 to 250.00 Ω in steps of 0.01

Reach Accuracy: ± 5% at steady state (higher during transients)

Characteristic Angle: 25 to 90° in steps of 1 (common for phase and ground elements)

Comparator Limit Angle: 60 to 90° in steps of 1 (lens shaping)

Time Delay: 0.000 to 65.535 s in steps of 0.001

Timing Accuracy: ±3% or 4 ms (whichever is greater)

Current Supervision

Level: Line-to-line current

Pickup: 0.050 to 30.000 pu in steps of 0.001

Dropout: 97 to 98%

Memory Duration: 5 to 25 cycles in steps of 1

Operation Time: 1 to 1.5 cycles (typical)

Reset Time: 1 power cycle (typical)

GROUND DISTANCE

Characteristic:	Dynamic (100% memory-polarized) MHO
Number of Zones:	1
Directionality:	Reversible
Reach (secondary ohms):	
1 A CT:	0.10 to 250.00 Ω in steps of 0.01
5 A CT:	0.02 to 250.00 Ω in steps of 0.01
Reach Accuracy:	$\pm 5\%$ at steady state (higher during transients)
Characteristic Angle:	25 to 90° in steps of 1° (common for phase and ground elements)
Zero Sequence Factor:	calculated automatically from line impedances
Comparator Limit Angle:	60 to 90° in steps of 1° (lens shaping)
Time Delay:	0.000 to 65.535 s in steps of 0.001
Timing Accuracy:	$\pm 3\%$ or 4 ms (whichever is greater)
Current Supervision	
Level:	Neutral current (3I ₀)
Pickup:	0.050 to 30.000 pu in steps of 0.001
Dropout:	97 to 98%
Memory Duration:	5 to 25 cycles in steps of 1
Operation Time:	1 to 1.5 cycles (typical)
Reset Time:	1 power cycle (typical)

PHASE/NEUTRAL/GROUND TOC

Current:	Phasor or RMS
Pickup Level:	0.000 to 30.000 pu in steps of 0.001
Dropout Level:	97% to 98% of Pickup
Level Accuracy:	$\pm 0.5\%$ of reading or $\pm 1\%$ of rated (whichever is greater) from 0.1 to 2.0 x CT rating $\pm 1.5\%$ of reading > 2.0 x CT rating
Curve Shapes:	IEEE Moderately/Very/Extremely Inverse IEC (and B.S.) A/B/C and Short Inverse GE IAC Inverse, Short/Very/Extremely Inverse I ² t FlexCurve™ (Programmable) Definite Time (0.01s base curve)
Curve Multiplier:	Time Dial = 0.00 to 600.00 in steps of 0.01
Reset Type:	Instantaneous/Timed (per IEEE)
Timing Accuracy:	Operate @ > 1.03 x Actual Pickup $\pm 3.5\%$ of operate time or $\pm 1/2$ cycle (whichever is greater)

PHASE/NEUTRAL/GROUND IOC

Current:	Phasor only
Pickup Level:	0.000 to 30.000 pu in steps of 0.001
Dropout Level:	97% to 98% of Pickup
Level Accuracy:	$\pm 0.5\%$ of reading or $\pm 1\%$ of rated (whichever is greater) from 0.1 to 2.0 x CT rating $\pm 1.5\%$ of reading > 2.0 x CT rating
Overreach:	< 2 %
Pickup Delay:	0.00 to 600.00 s in steps of 0.01
Reset Delay:	0.00 to 600.00 s in steps of 0.01
Operate Time:	< 20 ms @ 3 x Pickup @ 60 Hz
Timing Accuracy:	Operate @ 1.5 x Pickup $\pm 3\%$ or ± 4 ms (whichever is greater)

NEGATIVE SEQUENCE TOC

Current:	Phasor
Pickup Level:	0.000 to 30.000 pu in steps of 0.001
Dropout Level:	97% to 98% of Pickup
Level Accuracy:	$\pm 0.5\%$ of reading or $\pm 1\%$ of rated (whichever is greater) from 0.1 to 2.0 x CT rating $\pm 1.5\%$ of reading > 2.0 x CT rating
Curve Shapes:	IEEE Moderately/Very/Extremely Inverse IEC (and B.S.) A/B/C and Short Inverse GE IAC Inverse, Short/Very/Extremely Inverse I ² t FlexCurve™ (Programmable) Definite Time (0.01s base curve)
Curve Multiplier:	Time Dial = 0.00 to 600.00 in steps of 0.01
Reset Type:	Instantaneous/Timed (per IEEE)
Timing Accuracy:	Operate @ > 1.03 x Actual Pickup $\pm 3.5\%$ of operate time or $\pm 1/2$ cycle (whichever is greater)

NEGATIVE SEQUENCE IOC

Current:	Phasor
Pickup Level:	0.000 to 30.000 pu in steps of 0.001
Dropout Level:	97% to 98% of Pickup
Level Accuracy:	±0.5% of reading or ±1% of rated (whichever is greater) from 0.1 to 2.0 x CT rating ±1.5% of reading > 2.0 x CT rating
Overreach:	< 2 %
Pickup Delay:	0.00 to 600.00 s in steps of 0.01
Reset Delay:	0.00 to 600.00 s in steps of 0.01
Operate Time:	< 20 ms @ 3 x Pickup @ 60Hz
Timing Accuracy:	Operate @ 1.5 x Pickup ±3% or ± 4 ms (whichever is greater)

BREAKER FAILURE

Mode:	1-pole, 3-pole
Current Supv. Level:	Phase, Neutral
Current Supv. Pickup:	0.001 to 30.000 pu in steps of 0.001
Current Supv. DPO:	97 to 98% of Pickup
Current Supv. Accuracy:	0.1 to 2.0 x CT rating: ±0.75% of reading or ±1% of rated (whichever is greater) > 2 x CT rating: ±1.5% of reading

PHASE UNDERVOLTAGE

Voltage:	Phasor only
Pickup Level:	0.000 to 3.000 pu in steps of 0.001
Dropout Level:	102 to 103% of Pickup
Level Accuracy:	±0.5% of reading from 10 to 208 V
Curve Shapes:	GE IAV Inverse Definite Time (0.1s base curve)
Curve Multiplier:	Time Dial = 0.00 to 600.00 in steps of 0.01
Timing Accuracy:	Operate at < 0.90 x Pickup ±3.5% of operate time or ±4 ms (whichever is greater)

SYNCHROCHECK

Max Volt Difference:	0 to 100,000 V in steps of 1
Max Angle Difference:	0 to 100° in steps of 1°
Max Freq Difference:	0.00 to 2.00 Hz in steps of 0.01
Dead Source Function:	None, LV1 & DV2, DV1 & LV2, DV1 or DV2, DV1 xor DV2, DV1 & DV2 (L=Live, D=Dead)

AUTORECLOSURE

Single breaker applications, 3-pole tripping schemes.
Up to 4 reclose attempts before lockout.
Independent dead time setting before each shot.
Possibility of changing protection settings after each shot,
using FlexLogic™.

POWER SWING DETECT

Functions:	Power Swing Blocking, Out-of-Step Tripping
Measured Impedance:	Positive-sequence
Blocking & Tripping Modes:	2-step or 3-step
Tripping Mode:	Early or Delayed
Current Supervision:	
Pickup Level:	0.050 to 30.000 pu in steps of 0.001
Dropout Level:	97 to 98% of Pickup
Forward and Reverse Reach (sec. ohms):	
1 A CT:	0.50 to 500.00 Ω in steps of 0.05
5 A CT:	0.10 to 100.00 Ω in steps of 0.01
Impedance Accuracy:	±5%
Forward and Reverse Angle Impedances:	40° to 90° in steps of 1°
Angle Accuracy:	±2°
Characteristic Limit Angles:	40 to 140° in steps of 1
Timers:	0.000 to 65.535 s in steps of 0.001
Timing Accuracy:	±3% or 4 ms, whichever is greater

2.2.2 MONITORING

OSCILLOGRAPHY

Max. No. of Records: 64

Sampling Rate: 64 samples per power cycle

Triggers: Any element pickup, dropout or operate
 Digital input change of state
 Digital output change of state
 FlexLogic™ equation

Triggers: DV, DI, DF, digital points

Data: AC input channels
 Element state
 Digital input state
 Digital output state

Data Storage: In non-volatile memory

EVENT RECORDER

Capacity: 1024 events

Time-tag: To 1 microsecond

Triggers: Any element pickup, dropout or operate
 Digital input change of state
 Digital output change of state
 Self-test events

Data Storage: In non-volatile memory

DATA LOGGER

Number of Channels: 1 to 16

Parameters: Any analog Actual Value available in the relay

Sampling Rate: 1 sec.; 1, 5, 10, 15, 20, 30, 60 min.

Storage Capacity: (NN is dependent on memory)

1-second rate: 01 channel for NN days
 16 channels for NN days

:

60-minute rate: 01 channel for NN days
 16 channels for NN days

FAULT LOCATOR

Method: Single-ended

Maximum accuracy if: Fault resistance is zero or fault currents from all line terminals are in phase

Relay Accuracy: $\pm 1.5\%$ ($V > 10\text{ V}$, $I > 0.1\text{ pu}$)

Total Location Accuracy:

 $VT_{\%error} +$ (user data) $CT_{\%error} +$ (user data) $Z_{Line\%error} +$ (user data)METHOD $_{\%error} +$ (Chapter 6)RELAY ACCURACY $_{\%error} +$ (1.5%)

2.2.3 METERING

RMS CURRENT: Phase, Neutral, and Ground

Accuracy at

0.1 to 2.0 x CT rating: $\pm 0.25\%$ of reading or $\pm 0.1\%$ of rated (whichever is greater)> 2.0 x CT rating: $\pm 1.0\%$ of reading**RMS VOLTAGE**Accuracy: $\pm 0.5\%$ of reading from 10 to 208 V**APPARENT POWER VA**Accuracy: $\pm 1.0\%$ of reading**REAL POWER WATT**

Accuracy: $\pm 1.0\%$ of reading
 at PF between ± 0.8 and 1.0

REACTIVE POWER var

Accuracy: $\pm 1.0\%$ of reading
 at PF between ± 0.2 and 0.0

REACTIVE POWER var

Accuracy: $\pm 1.0\%$ of reading
 at PF between ± 0.2 and 0.0

FREQUENCY

Accuracy at

V = 0.8 to 1.2 pu: $\pm 0.01\text{ Hz}$ (when voltage signal is used for frequency measurement).I = 0.1 to 0.25 pu: $\pm 0.05\text{ Hz}$,I > 0.25 pu: $\pm 0.02\text{ Hz}$ (when current signal is used for frequency measurement)

2.2.4 INPUTS

AC CURRENT

CT Rated Primary: 1 to 50000 A
 CT Rated Secondary: 1 A or 5 A by connection
 Nominal Frequency: 20 to 65 Hz
 Relay Burden: < 0.2 VA at rated secondary
 Conversion Range:
 Standard CT Module: 0.02 to 46 x CT rating
 RMS symmetrical
 Sensitive Ground Module: 0.002 to 4.6 x CT rating
 RMS symmetrical
 Current Withstand: 20 ms at 250 times rated
 1 sec. at 100 times rated
 Cont. at 3 times rated

AC VOLTAGE

VT Rated Secondary: 50.0 to 240.0 V
 VT Ratio: 0.1 to 24000.0
 Nominal Frequency: 20 to 65 Hz
 Relay Burden: < 0.25 VA at 120 V
 Conversion Range: 1 to 275 V
 Voltage Withstand: cont. at 260 V to neutral
 1 min./hr at 420 V to neutral

CONTACT INPUTS

Dry Contacts: 1000 Ω Maximum
 Wet Contacts: 300 V DC Maximum
 Selectable Thresholds: 16 V, 30 V, 80 V, 140 V
 Recognition Time: < 5 ms

IRIG-B INPUT

Amplitude Modulation: 1 to 10 Vp-p
 DC Shift: TTL
 Input Impedance: 22 kOhms

DCMA INPUTS

Current Input (mA_{dc}): 0 to -1, 0 to +1, -1 to +1, 0 to 5, 0 to 10, 0 to 20, 4 to 20 (programmable)
 Input Impedance: 379 Ω \pm 10%
 Conversion Range: -1 to + 20 mA_{dc}
 Accuracy: \pm 0.2% of full scale
 Type: Passive

2.2.5 POWER SUPPLY

LOW RANGE

Nominal DC Voltage: 24 to 48 at 3 A
 Min./Max. DC Voltage: 20 / 60
 NOTE: Low range is DC only.

HIGH RANGE

Nominal DC Voltage: 125 to 250 at 0.7 A
 Min./Max. DC Voltage: 88 / 300
 Nominal AC Voltage: 100 to 240 at 50/60 Hz, 0.7 A
 Min./Max. AC Voltage: 88 / 265 at 48 to 62 Hz

ALL RANGES

Volt Withstand: 2 x Highest Nominal Voltage
 for 10 ms
 Voltage Loss Hold-Up: 50 ms duration at nominal
 Power Consumption: Typical = 35 VA, Max. = 75 VA

INTERNAL FUSE**RATINGS**

Low Range Power Supply: 7.5A/600V
 High Range Power Supply: 5A/600V

INTERRUPTING CAPACITY

AC: 100,000 A RMS symmetrical
 DC: 10,000 A

2.2.6 OUTPUTS

FORM-A RELAY

Make and Carry for 0.2 sec: 30 A as per ANSI C37.90

Carry Continuous: 6 A

Break @ L/R of 40 ms: 0.25 A DC max.

Operate Time: < 4 ms

Contact Material: Silver alloy

FORM-A VOLTAGE MONITOR

Applicable Voltage: approx. 15 to 250 V DC

Trickle Current: approx. 1 to 2.5 mA

FORM-A CURRENT MONITOR

Threshold Current: approx. 80 to 100 mA

FORM-C AND CRITICAL FAILURE RELAY

Make and Carry for 0.2 sec: 10 A

Carry Continuous: 6 A

Break @ L/R of 40 ms: 0.1 ADC max.

Operate Time: < 8 ms

Contact Material: Silver alloy

FAST FORM-C RELAY

Make and Carry: 40 mA @ 48 V DC

Operate Time: < 0.6 ms

INTERNAL LIMITING RESISTOR:

Power: 2 Watts

Resistance: 100 ohms

**CONTROL POWER EXTERNAL OUTPUT
(for Dry Contact Input)**

Capacity: 100 mA DC at 48 VDC

Isolation: ± 300 Vpk

2.2.7 COMMUNICATIONS

RS232

Front Port: 19.2 kbps, Modbus® RTU

RS485

1 or 2 Rear Ports: Up to 115 kbps, Modbus® RTU, isolated together at 36 Vpk

Typical Distance: 1200 m

ETHERNET PORT

10BaseF: 820 nm, multi-mode, half-duplex fiber optic with ST connector

Redundant 10BaseF: 820 nm, multi-mode, half-duplex fiber optic with ST connector

Power Budget: 10 db

Max Optical Ip Power: -7.6 dBm

Typical Distance: 1.65 km

2.2.8 ENVIRONMENTAL

Operating Temperatures:

-10°C to +60°C

Ambient Storage Temperatures:

-40° C to +80° C

Humidity (noncondensing):

Up to 95%

Altitude:

Up to 2000 m

Installation Category: II

2.2.9 TYPE TESTS

Electrical Fast Transient:

ANSI/IEEE C37.90.1

EN 61000-4-4

Oscillatory Transient: ANSI/IEEE C37.90.1

Insulation Resistance: IEC 255-5

Dielectric Strength: IEC 255-6, Series C 2240V
ANSI/IEEE C37.90

Electrostatic Discharge:

EN 61000-4-2

Surge Immunity: EN 61000-4-5

RFI Susceptibility: ANSI/IEEE C37.90.2

EN 61000-4-3



NOTE

Type test report available upon request.

2.2.10 PRODUCTION TESTS

DIELECTRIC STRENGTH

ANSI/IEEE C37.90:

AC: CT, VT, Control Power, and Contact Inputs

DC: Contact Outputs

2

2.2.11 APPROVALS

APPROVALS

UL Certification applied for.

CSA Certification applied for.

Manufactured under an ISO9000 Registered system.

CE: 73/23/EEC, 89/336/EEC
IEC 947-1
IEC 1010-1:1990+ A 1:1992+ A 2:1995
CISPR 11 / EN 55011:1997
EN 50082-2:1997
IEC 1000-4-3 / EN 61000-4-3
EN 61000-4-6

2.2.12 MAINTENANCE

CLEANING

Normally, cleaning is not required; but for situations where dust has accumulated on the faceplate display, a dry cloth can be used.

3.1.1 PANEL CUTOUT

The relay is available as a 19 inch rack horizontal mount unit or as a reduced size ($\frac{3}{4}$) vertical mount unit, with a removable faceplate. The modular design allows the relay to be easily upgraded or repaired by a qualified service person. The faceplate is hinged to allow easy access to the removable modules, and is itself removable to allow mounting on doors with limited rear depth. There is also a removable dust cover that fits over the faceplate, which must be removed when attempting to access the keypad or RS232 communications port.

The vertical and horizontal case dimensions are as shown in the dimension drawings below, along with panel cutout details for panel mounting. When planning the location of your panel cutout, ensure that provision is made for the faceplate to swing open without interference to or from adjacent equipment.

The relay must be mounted such that the faceplate sits semi-flush with the panel or switchgear door, allowing the operator access to the keypad and the RS232 communications port. The relay is secured to the panel with the use of four screws supplied with the relay.

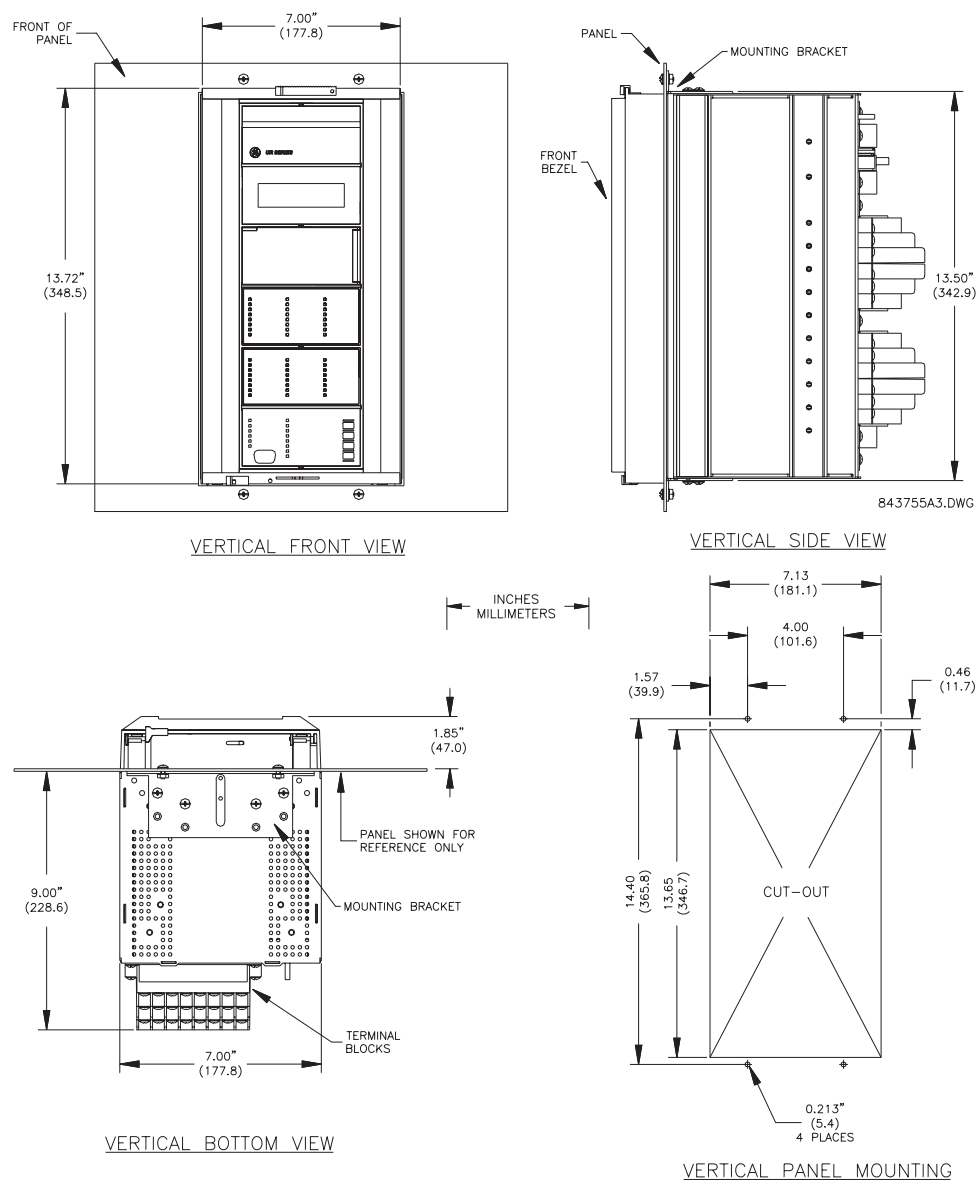


Figure 3-1: UR VERTICAL MOUNTING AND DIMENSIONS

3

STEP 1 – CREATE THE HOLES AND CUT-OUT INTO THE PANEL
AS PER DRAWING 843753.

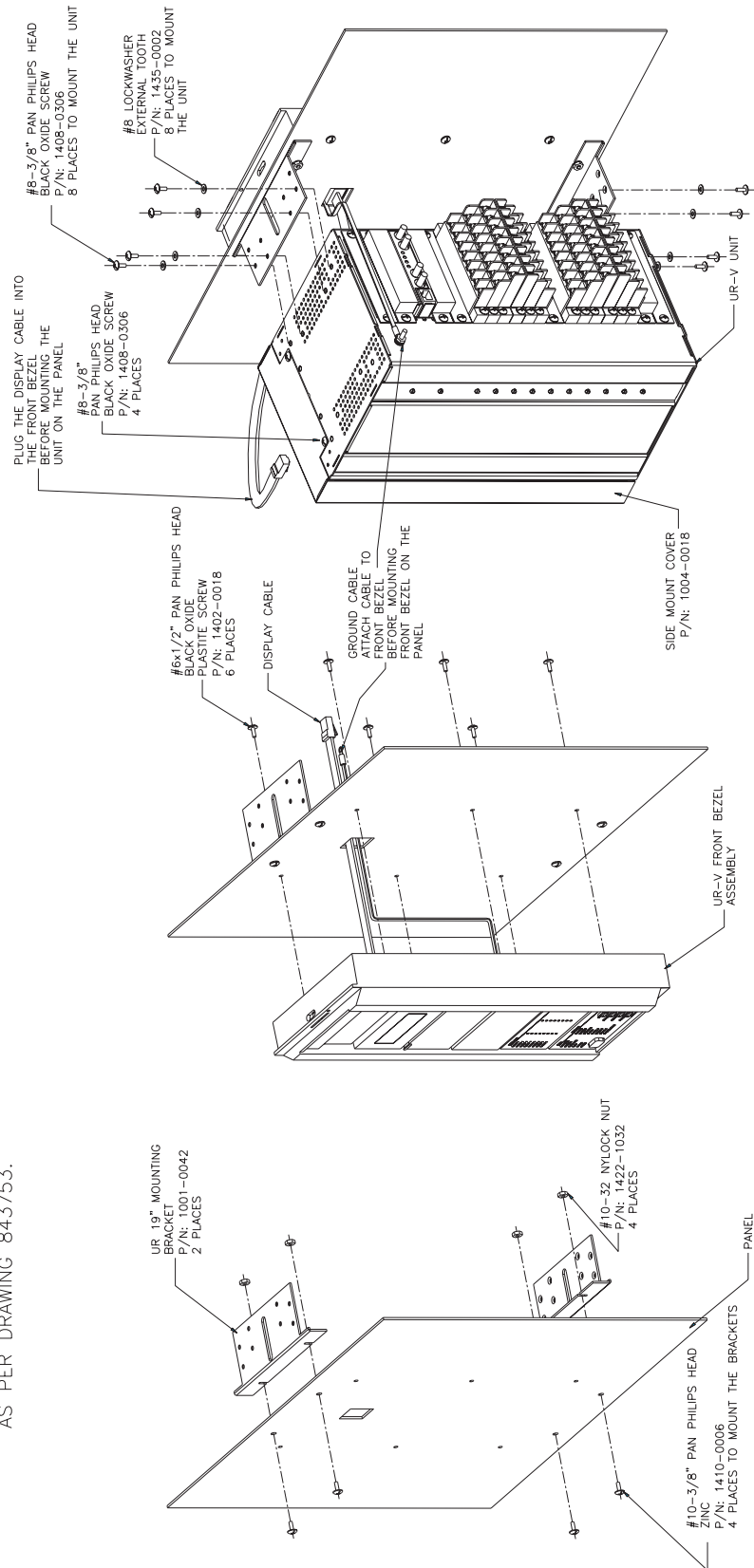


Figure 3-2: UR VERTICAL SIDE MOUNTING INSTALLATION

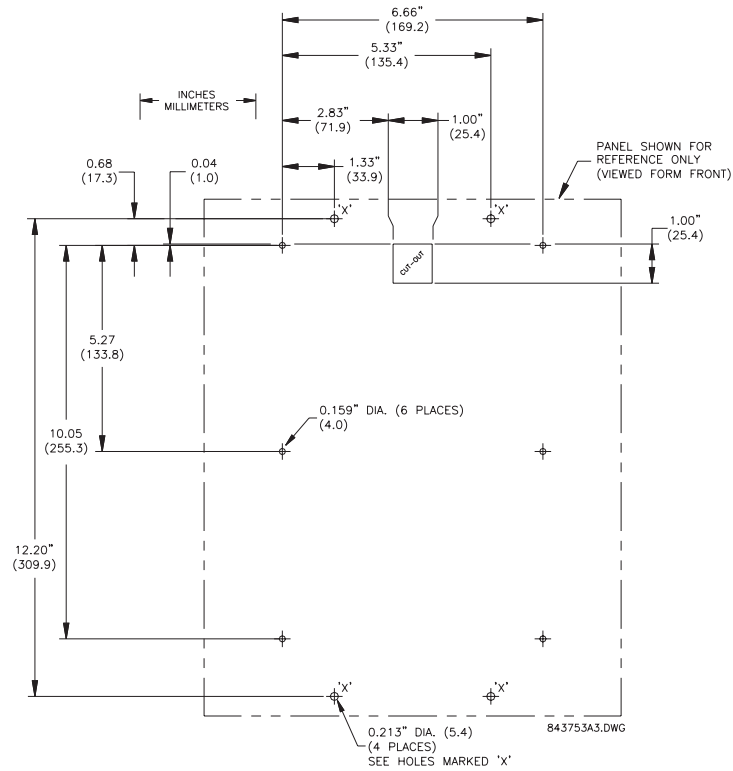


Figure 3-3: UR VERTICAL SIDE MOUNTING REAR DIMENSIONS

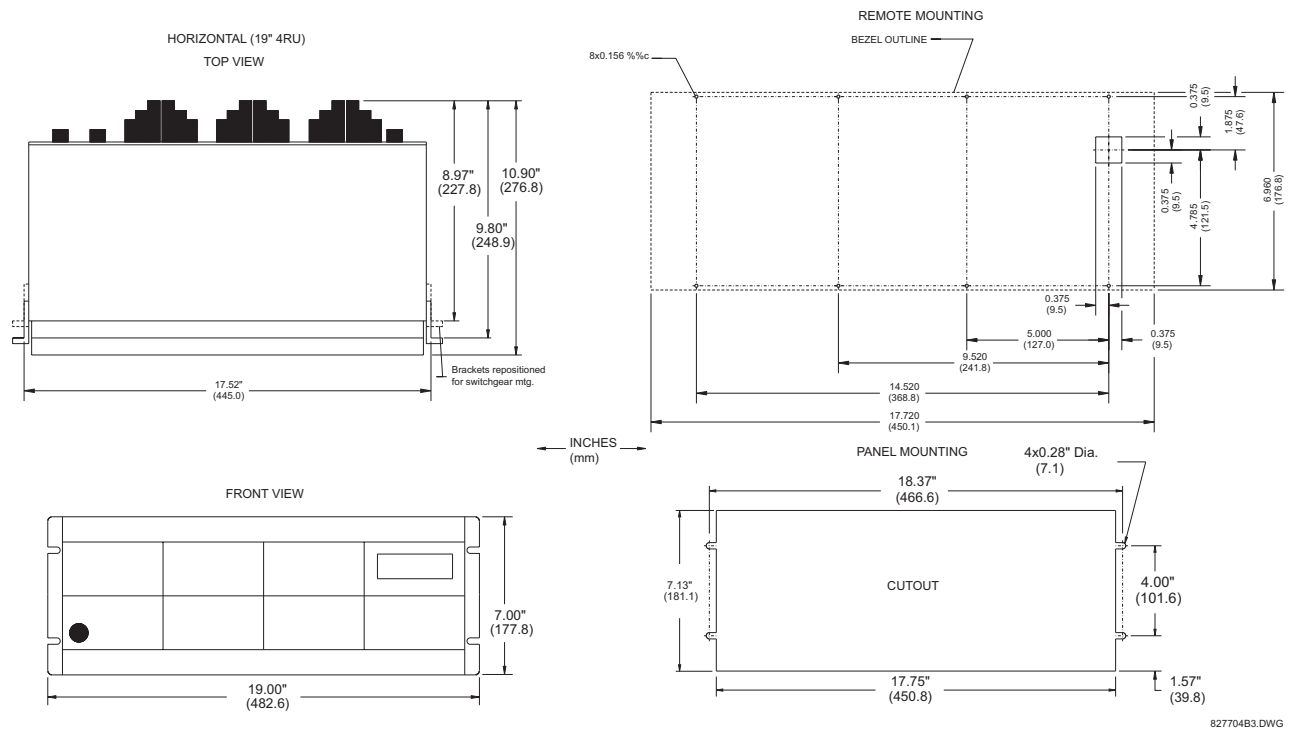


Figure 3-4: UR HORIZONTAL MOUNTING AND DIMENSIONS

3.1.2 MODULE WITHDRAWAL / INSERTION



Module withdrawal and insertion may only be performed when control power has been removed from the unit. Inserting an incorrect module type into a slot may result in personal injury, damage to the unit or connected equipment, or undesired operation!



Proper electrostatic discharge protection (i.e. static strap) must be used when coming in contact with modules while the relay is energized!

3

The relay, being modular in design, allows for the withdrawal and insertion of modules. Modules must only be replaced with like modules in their original factory configured slots.

The faceplate can be opened to the left, once the sliding latch on the right side has been pushed up, as shown in the figure below. This allows for easy accessibility of the modules for withdrawal.



Figure 3-5: UR MODULE WITHDRAWAL/INSERTION

WITHDRAWAL: The ejector/inserter clips, located at the top and bottom of each module, must be pulled simultaneously to release the module for removal. Before performing this action, **control power must be removed from the relay**. Record the original location of the module to ensure that the same or replacement module is inserted into the correct slot.

INSERTION: Ensure that the **correct** module type is inserted into the **correct** slot position. The ejector/insert clips located at the top and at the bottom of each module must be in the disengaged position as the module is smoothly inserted into the slot. Once the clips have cleared the raised edge of the chassis, engage the clips simultaneously. When the clips have locked into position, the module will be fully inserted.



Type 9C and 9D CPU modules are equipped with 10BaseT and 10BaseF Ethernet connectors for communications. These connectors must be individually disconnected from the module before the module can be removed from the chassis.

3.1.3 REAR TERMINAL LAYOUT

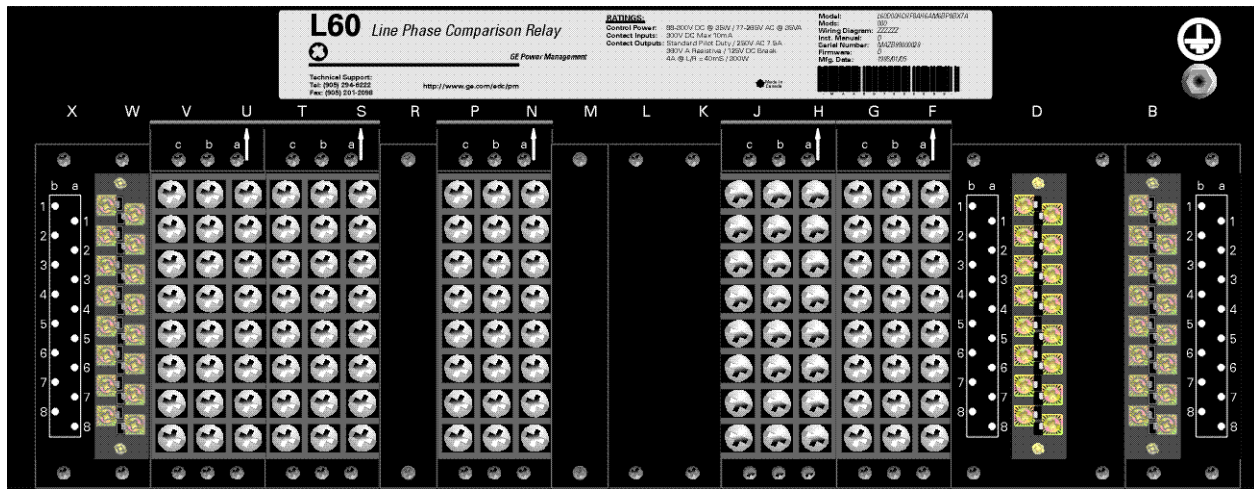


Figure 3-6: REAR TERMINAL VIEW



Do not touch any rear terminals while the relay is energized!

a) REAR TERMINAL ASSIGNMENTS

The relay follows a convention with respect to terminal number assignments which are three characters long assigned in order by module slot position, row number, and column letter. Two-slot wide modules take their slot designation from the first slot position (nearest to CPU module) which is indicated by an arrow marker on the terminal block. See the following figure for an example of rear terminal assignments.

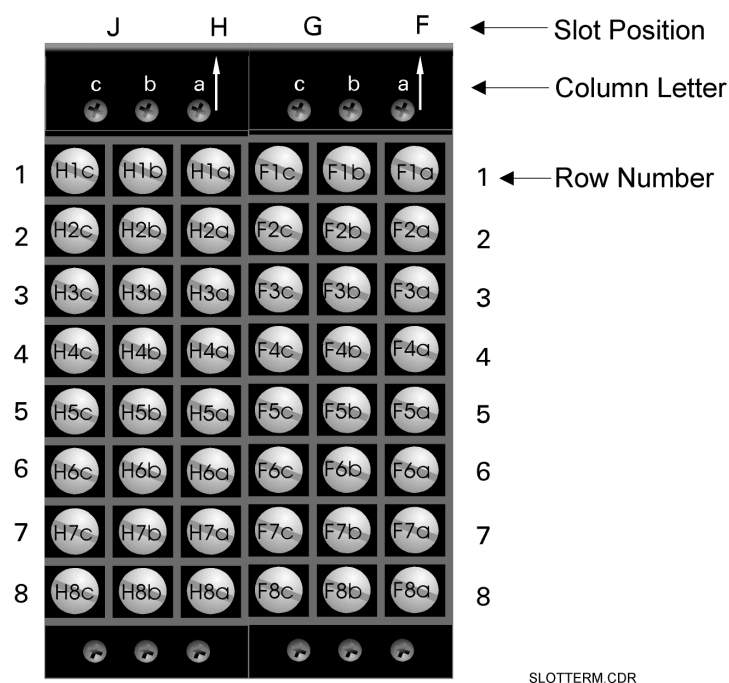


Figure 3-7: EXAMPLE OF MODULES IN F & H SLOTS

3.2.2 DIELECTRIC STRENGTH RATINGS AND TESTING

a) RATINGS

The dielectric strength of UR module hardware is shown in the following table:

Table 3–1: DIELECTRIC STRENGTH OF UR MODULE HARDWARE

MODULE TYPE	MODULE FUNCTION	TERMINALS		DIELECTRIC STRENGTH (AC)
		FROM	TO	
1	Power Supply	High(+); Low(+); (–)	Chassis	2000 V AC for 1 min. (See Precaution 1)
1	Power Supply	48 VDC (+) and (–)	Chassis	2000 V AC for 1 min. (See Precaution 1)
1	Power Supply	Relay Terminals	Chassis	2000 VAC for 1 min. (See Precaution 1)
2	Reserved for Future	N/A	N/A	N/A
3	Reserved for Future	N/A	N/A	N/A
4	Reserved for Future	N/A	N/A	N/A
5	Analog I/O	All except 8b	Chassis	< 50 V DC
6	Digital I/O	All (See Precaution 2)	Chassis	2000 V AC for 1 min.
7R	L90 G.703	All except 2b,3a,7b,8a	Chassis	2000 V AC for 1 min.
7T	L90 RS422	All except 6a, 7b, 8a	Chassis	< 50 V DC
8	CT/VT	All	Chassis	2000 V AC for 1 min.
9	CPU	All except 7b	Chassis	< 50 VDC

b) TESTING

Filter networks and transient protection clamps are used in module hardware to prevent damage caused by high peak voltage transients, radio frequency interference (RFI) and electromagnetic interference (EMI). These protective components **can be damaged** by application of the ANSI/IEEE C37.90 specified test voltage for a period longer than the specified one minute. For testing of dielectric strength where the test interval may exceed one minute, always observe the following precautions:

Test Precautions:

1. The connection from ground to the Filter Ground (terminal 8b) and Surge Ground (terminal 8a) must be removed before testing.
2. Some versions of the digital I/O module have a Surge Ground connection on terminal 8b. On these module types, this connection must be removed before testing.

3.2.3 CONTROL POWER



CONTROL POWER SUPPLIED TO THE RELAY MUST BE CONNECTED TO THE MATCHING POWER SUPPLY RANGE OF THE RELAY. IF THE VOLTAGE IS APPLIED TO THE WRONG TERMINALS, DAMAGE MAY OCCUR!

The power supply module can be ordered with either of two possible voltage ranges. Each range has a dedicated input connection for proper operation. The ranges are as shown below (see the Technical Specifications section for details).

Table 3–2: CONTROL POWER VOLTAGE RANGE

RANGE	NOMINAL VOLTAGE
LO	24 to 48 V (DC only)
HI	125 to 250 V

The power supply module provides power to the relay and supplies power for dry contact input connections.

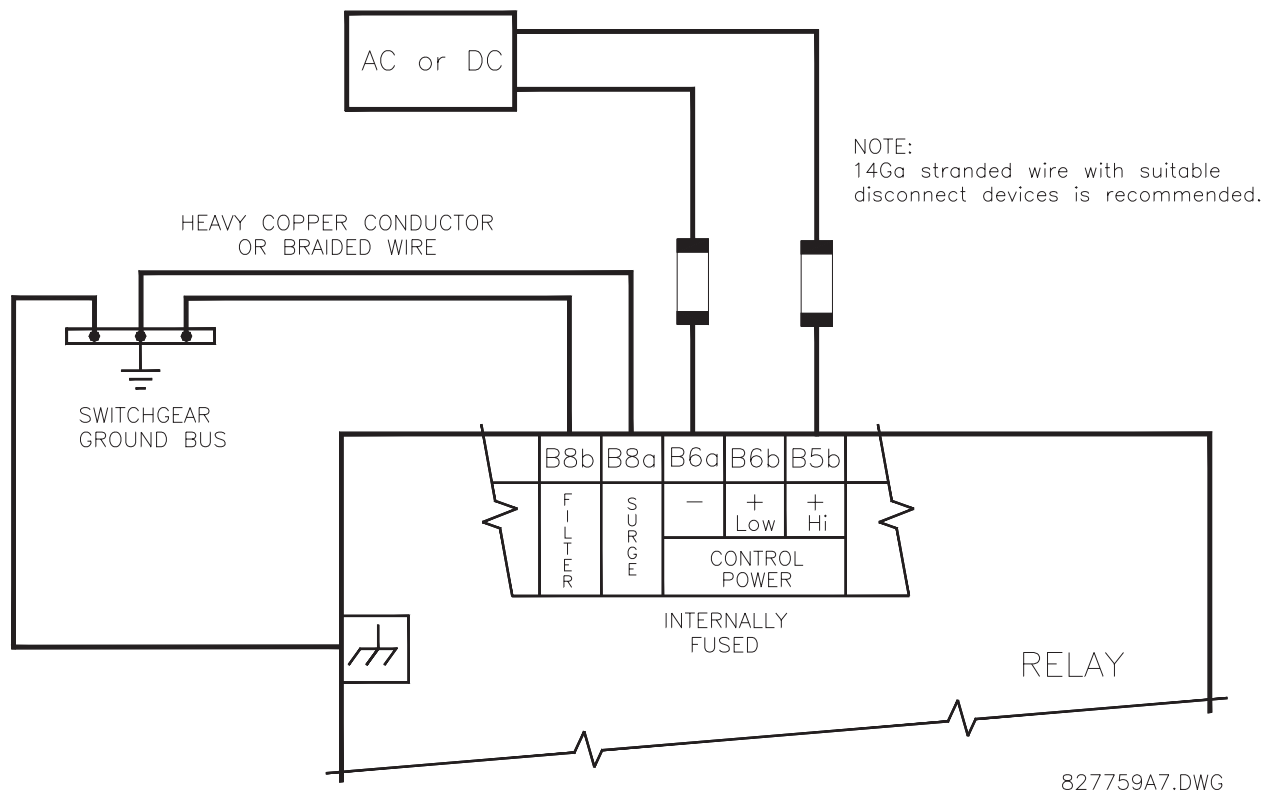


Figure 3–9: CONTROL POWER CONNECTION

The power supply module provides 48 V DC power for dry contact input connections and a critical failure relay (see TYPICAL WIRING DIAGRAM). The critical failure relay is a Form-C that will be energized once control power is applied and the relay has successfully booted up with no critical self-test failures. If any of the on-going self-test features detect a critical failure or control power is lost, the relay will de-energize.

3.2.4 AC CURRENT TRANSFORMER INPUTS



VERIFY THAT THE CONNECTION MADE TO THE RELAY NOMINAL CURRENT OF 1A OR 5A MATCHES THE SECONDARY RATING OF THE CONNECTED CTS. UNMATCHED CTS MAY RESULT IN EQUIPMENT DAMAGE OR INADEQUATE PROTECTION.

The CT/VT module may be ordered with a standard ground current input that is the same as the phase current inputs (type 8A) or with a sensitive ground input (type 8B) which is 10 times more sensitive (see the Technical Specifications section for more details). Each AC current input has an isolating transformer and an automatic shorting mechanism that shorts the input when the module is withdrawn from the chassis. There are no internal ground connections on the current inputs. Current transformers with 1 to 50000 A primaries and 1 A or 5 A secondaries may be used.

CT connections for both ABC and ACB phase rotations are identical as shown in the TYPICAL WIRING DIAGRAM.

The exact placement of a zero sequence CT so that ground fault current will be detected is shown below. Twisted pair cabling on the zero sequence CT is recommended.

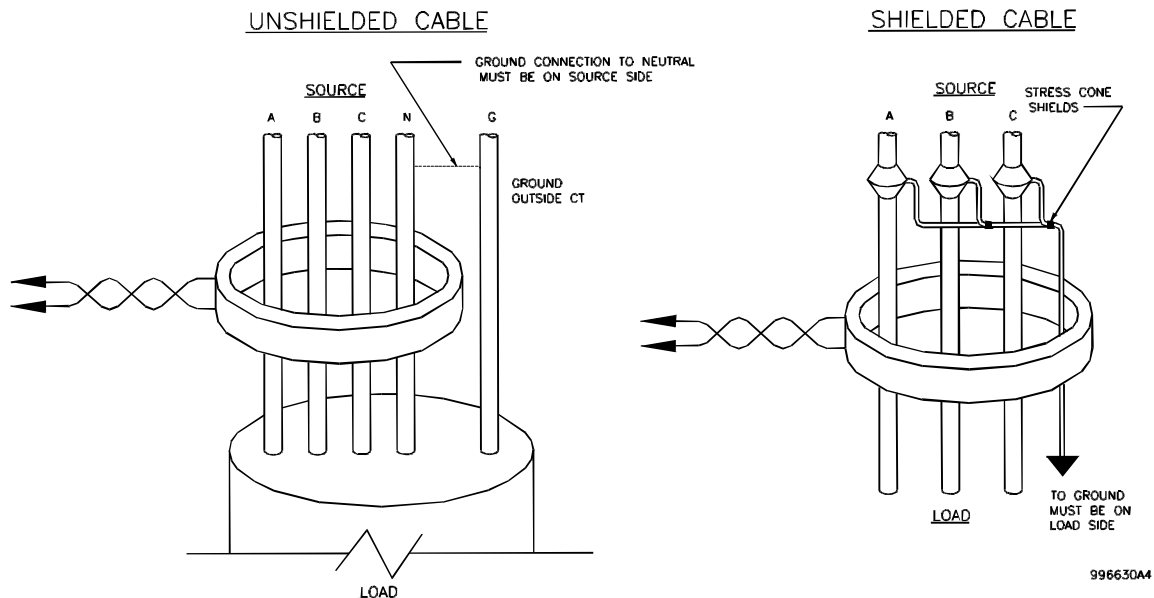


Figure 3-10: ZERO SEQUENCE CORE BALANCE CT INSTALLATION

3.2.5 CT/VT MODULE ASSIGNMENTS

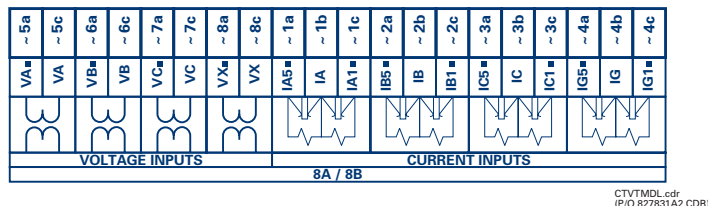


Figure 3-11: CT/VT MODULE WIRING



NOTE

Wherever a tilde “~” symbol appears, substitute with the Slot Position of the module.

3.2.6 CONTACT INPUTS/OUTPUTS

Every digital I/O module has 24 terminal connections. They are arranged as 3 terminals per row, with 8 rows in total. A given row of three terminals may be used for the outputs of one relay. For example, for Form-C relay outputs, the terminals connect to the normally open (NO), normally closed (NC), and common contacts of the relay. For a Form-A output, there are options of using current or voltage detection for feature supervision, depending on the module ordered. The terminal configuration for contact inputs is different for the two applications. When a digital I/O module is ordered with contact inputs, they are arranged in groups of four and use two rows of three terminals. Ideally, each input would be totally isolated from any other input. However, this would require that every input have two dedicated terminals and limit the available number of contacts based on the available number of terminals. So, although each input is individually optically isolated, each group of four inputs uses a single common as a reasonable compromise. This allows each group of four outputs to be supplied by wet contacts from different voltage sources (if required) or a mix of wet and dry contacts.

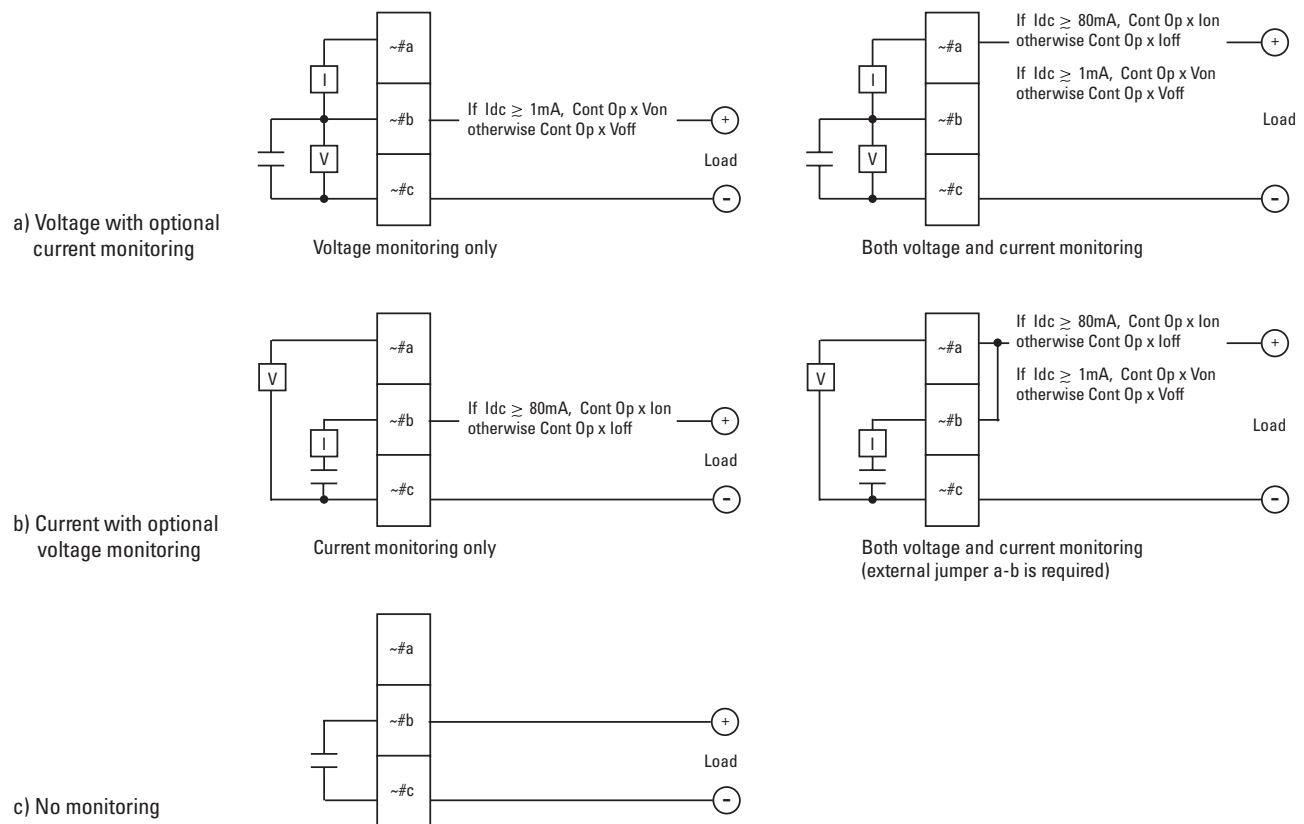
The following tables and diagrams below illustrate the module types (6A, etc.) and contact arrangements that may be ordered for the relay. Since an entire row is used for a single contact output, the name is assigned using the module slot position and row number. However, since there are two contact inputs per row, these names are assigned by module slot position, row number, and column position.

UR RELAY FORM-A OUTPUT CONTACTS

Some Form-A outputs include circuits to monitor the DC voltage across the output contact when it is open, and the DC current through the output contact when it is closed. Each of the monitors contains a level detector whose output is set to logic “On = 1” when the current in the circuit is above the threshold setting. The voltage monitor is set to “On = 1” when the current is above about 1 to 2.5 mA, and the current monitor is set to “On = 1” when the current exceeds about 80 to 100 mA. The voltage monitor is intended to check the health of the overall trip circuit, and the current monitor can be used to seal-in the output contact until an external contact has interrupted current flow. The block diagrams of the circuits are shown below for the Form-A outputs with:

- a) optional voltage monitor
- b) optional current monitor
- c) with no monitoring

The operation of voltage and current monitors is reflected with the corresponding FlexLogic™ operands (Cont Op # Von, Cont Op # Voff, Cont Op # Ion, and Cont Op # Ioff) which can be used in protection, control and alarm logic. The typical application of the voltage monitor is Breaker Trip Circuit Integrity monitoring; a typical application of the Current monitor is seal-in of the control command. Refer DIGITAL ELEMENTS section for an example of how Form A contacts can be applied for Breaker Trip Circuit Integrity Monitoring.



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Figure 3-12: FORM-A CONTACT FUNCTIONS

NOTE: Use of Form-A Outputs in High Impedance Circuits

For Form-A output contacts that are internally equipped with a voltage measuring circuit across the contact, the circuit has an impedance that can cause a problem when used in conjunction with external high input impedance monitoring equipment such as modern relay test set trigger circuits. These monitoring circuits may continue to read the Form-A contact as being closed after it has closed and subsequently opened, when measured as an impedance.

The solution to this problem is to use the voltage measuring trigger input of the relay test set, and connect the Form-A contact through a voltage-dropping resistor to a DC voltage source. If the 48 V DC output of the power supply is used as a source, a 500 Ω , 10 W resistor is appropriate. In this configuration, the voltage across either the Form-A contact or the resistor can be used to monitor the state of the output.



Wherever a tilde “~” symbol appears, substitute with the Slot Position of the module.

Table 3–3: DIGITAL I/O MODULE ASSIGNMENTS

~6A I/O MODULE		~6B I/O MODULE		~6C I/O MODULE	
Terminal Assignment	Output or Input	Terminal Assignment	Output or Input	Terminal Assignment	Output
~1	Form-A	~1	Form-A	~1	Form-C
~2	Form-A	~2	Form-A	~2	Form-C
~3	Form-C	~3	Form-C	~3	Form-C
~4	Form-C	~4	Form-C	~4	Form-C
~5a, ~5c	2 Inputs	~5	Form-C	~5	Form-C
~6a, ~6c	2 Inputs	~6	Form-C	~6	Form-C
~7a, ~7c	2 Inputs	~7a, ~7c	2 Inputs	~7	Form-C
~8a, ~8c	2 Inputs	~8a, ~8c	2 Inputs	~8	Form-C

~6D I/O MODULE		~6E I/O MODULE		~6F I/O MODULE	
Terminal Assignment	Input	Terminal Assignment	Output or Input	Terminal Assignment	Output
~1a, ~1c	2 Inputs	~1	Form-C	~1	Fast Form-C
~2a, ~2c	2 Inputs	~2	Form-C	~2	Fast Form-C
~3a, ~3c	2 Inputs	~3	Form-C	~3	Fast Form-C
~4a, ~4c	2 Inputs	~4	Form-C	~4	Fast Form-C
~5a, ~5c	2 Inputs	~5a, ~5c	2 Inputs	~5	Fast Form-C
~6a, ~6c	2 Inputs	~6a, ~6c	2 Inputs	~6	Fast Form-C
~7a, ~7c	2 Inputs	~7a, ~7c	2 Inputs	~7	Fast Form-C
~8a, ~8c	2 Inputs	~8a, ~8c	2 Inputs	~8	Fast Form-C

~6G I/O MODULE		~6H I/O MODULE		~6K I/O MODULE	
Terminal Assignment	Output or Input	Terminal Assignment	Output or Input	Terminal Assignment	Output
~1	Form-A	~1	Form-A	~1	Form-C
~2	Form-A	~2	Form-A	~2	Form-C
~3	Form-A	~3	Form-A	~3	Form-C
~4	Form-A	~4	Form-A	~4	Form-C
~5a, ~5c	2 Inputs	~5	Form-A	~5	Fast Form-C
~6a, ~6c	2 Inputs	~6	Form-A	~6	Fast Form-C
~7a, ~7c	2 Inputs	~7a, ~7c	2 Inputs	~7	Fast Form-C
~8a, ~8c	2 Inputs	~8a, ~8c	2 Inputs	~8	Fast Form-C

~6L I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6M I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5	Form-C
~6	Form-C
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6N I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6P I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5	Form-A
~6	Form-A
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6R I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6S I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-C
~4	Form-C
~5	Form-C
~6	Form-C
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6T I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5a, ~5c	2 Inputs
~6a, ~6c	2 Inputs
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

~6U I/O MODULE	
Terminal Assignment	Output or Input
~1	Form-A
~2	Form-A
~3	Form-A
~4	Form-A
~5	Form-A
~6	Form-A
~7a, ~7c	2 Inputs
~8a, ~8c	2 Inputs

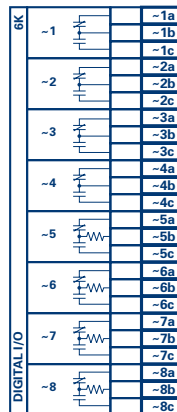
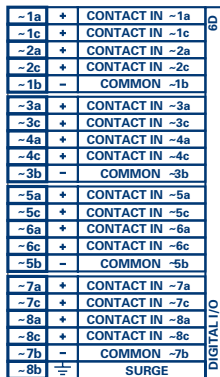
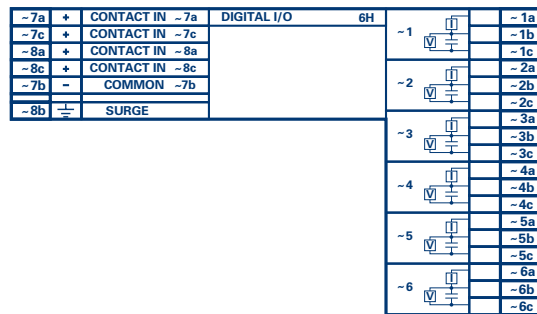
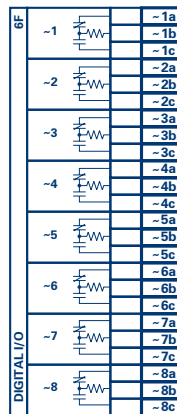
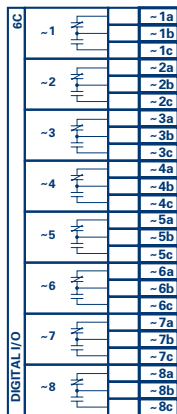
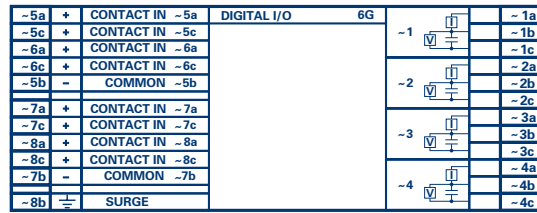
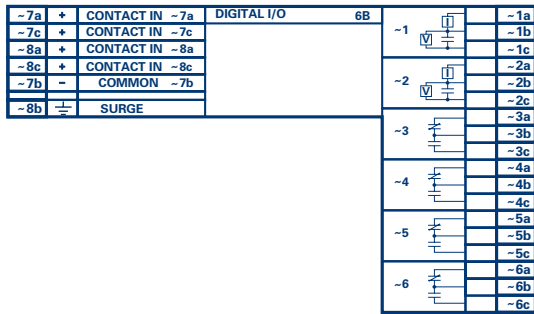
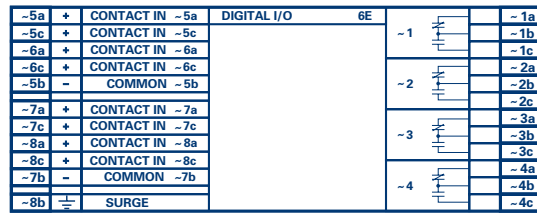
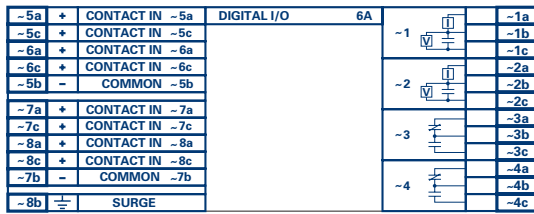
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sheet 1 of 2

Figure 3–13: DIGITAL I/O MODULE WIRING (Sheet 1 of 2)

~5a	+	CONTACT IN ~5a	DIGITAL I/O	6L	~1		~1a
~5c	+	CONTACT IN ~5c			~1		~1b
~6a	+	CONTACT IN ~6a			~1		~1c
~6c	+	CONTACT IN ~6c			~2		~2a
~5b	-	COMMON ~5b			~2		~2b
~7a	+	CONTACT IN ~7a			~2		~2c
~7c	+	CONTACT IN ~7c			~3		~3a
~8a	+	CONTACT IN ~8a			~3		~3b
~8c	+	CONTACT IN ~8c			~3		~3c
~7b	-	COMMON ~7b			~4		~4a
~8b	-	SURGE			~4		~4b
~8b	-	SURGE			~4		~4c

~5a	+	CONTACT IN ~5a	DIGITAL I/O	6R	~1		~1a
~5c	+	CONTACT IN ~5c			~1		~1b
~6a	+	CONTACT IN ~6a			~1		~1c
~6c	+	CONTACT IN ~6c			~2		~2a
~5b	-	COMMON ~5b			~2		~2b
~7a	+	CONTACT IN ~7a			~2		~2c
~7c	+	CONTACT IN ~7c			~3		~3a
~8a	+	CONTACT IN ~8a			~3		~3b
~8c	+	CONTACT IN ~8c			~3		~3c
~7b	-	COMMON ~7b			~4		~4a
~8b	-	SURGE			~4		~4b
~8b	-	SURGE			~4		~4c

~7a	+	CONTACT IN ~7a	DIGITAL I/O	6M	~1		~1a
~7c	+	CONTACT IN ~7c			~1		~1b
~8a	+	CONTACT IN ~8a			~1		~1c
~8c	+	CONTACT IN ~8c			~2		~2a
~7b	-	COMMON ~7b			~2		~2b
~8b	-	SURGE			~2		~2c
~7a	+	CONTACT IN ~7a			~3		~3a
~7c	+	CONTACT IN ~7c			~3		~3b
~8a	+	CONTACT IN ~8a			~3		~3c
~8c	+	CONTACT IN ~8c			~4		~4a
~7b	-	COMMON ~7b			~4		~4b
~8b	-	SURGE			~4		~4c
~7a	+	CONTACT IN ~7a			~5		~5a
~7c	+	CONTACT IN ~7c			~5		~5b
~8a	+	CONTACT IN ~8a			~5		~5c
~8c	+	CONTACT IN ~8c			~6		~6a
~7b	-	COMMON ~7b			~6		~6b
~8b	-	SURGE			~6		~6c

~7a	+	CONTACT IN ~7a	DIGITAL I/O	6S	~1		~1a
~7c	+	CONTACT IN ~7c			~1		~1b
~8a	+	CONTACT IN ~8a			~1		~1c
~8c	+	CONTACT IN ~8c			~2		~2a
~7b	-	COMMON ~7b			~2		~2b
~8b	-	SURGE			~2		~2c
~7a	+	CONTACT IN ~7a			~3		~3a
~7c	+	CONTACT IN ~7c			~3		~3b
~8a	+	CONTACT IN ~8a			~3		~3c
~8c	+	CONTACT IN ~8c			~4		~4a
~7b	-	COMMON ~7b			~4		~4b
~8b	-	SURGE			~4		~4c
~7a	+	CONTACT IN ~7a			~5		~5a
~7c	+	CONTACT IN ~7c			~5		~5b
~8a	+	CONTACT IN ~8a			~5		~5c
~8c	+	CONTACT IN ~8c			~6		~6a
~7b	-	COMMON ~7b			~6		~6b
~8b	-	SURGE			~6		~6c

~5a	+	CONTACT IN ~5a	DIGITAL I/O	6N	~1		~1a
~5c	+	CONTACT IN ~5c			~1		~1b
~6a	+	CONTACT IN ~6a			~1		~1c
~6c	+	CONTACT IN ~6c			~2		~2a
~5b	-	COMMON ~5b			~2		~2b
~7a	+	CONTACT IN ~7a			~2		~2c
~7c	+	CONTACT IN ~7c			~3		~3a
~8a	+	CONTACT IN ~8a			~3		~3b
~8c	+	CONTACT IN ~8c			~3		~3c
~7b	-	COMMON ~7b			~4		~4a
~8b	-	SURGE			~4		~4b
~8b	-	SURGE			~4		~4c

~5a	+	CONTACT IN ~5a	DIGITAL I/O	6T	~1		~1a
~5c	+	CONTACT IN ~5c			~1		~1b
~6a	+	CONTACT IN ~6a			~1		~1c
~6c	+	CONTACT IN ~6c			~2		~2a
~5b	-	COMMON ~5b			~2		~2b
~7a	+	CONTACT IN ~7a			~2		~2c
~7c	+	CONTACT IN ~7c			~3		~3a
~8a	+	CONTACT IN ~8a			~3		~3b
~8c	+	CONTACT IN ~8c			~3		~3c
~7b	-	COMMON ~7b			~4		~4a
~8b	-	SURGE			~4		~4b
~8b	-	SURGE			~4		~4c

~7a	+	CONTACT IN ~7a	DIGITAL I/O	6P	~1		~1a
~7c	+	CONTACT IN ~7c			~1		~1b
~8a	+	CONTACT IN ~8a			~1		~1c
~8c	+	CONTACT IN ~8c			~2		~2a
~7b	-	COMMON ~7b			~2		~2b
~8b	-	SURGE			~2		~2c
~7a	+	CONTACT IN ~7a			~3		~3a
~7c	+	CONTACT IN ~7c			~3		~3b
~8a	+	CONTACT IN ~8a			~3		~3c
~8c	+	CONTACT IN ~8c			~4		~4a
~7b	-	COMMON ~7b			~4		~4b
~8b	-	SURGE			~4		~4c
~7a	+	CONTACT IN ~7a			~5		~5a
~7c	+	CONTACT IN ~7c			~5		~5b
~8a	+	CONTACT IN ~8a			~5		~5c
~8c	+	CONTACT IN ~8c			~6		~6a
~7b	-	COMMON ~7b			~6		~6b
~8b	-	SURGE			~6		~6c

~7a	+	CONTACT IN ~7a	DIGITAL I/O	6U	~1		~1a
~7c	+	CONTACT IN ~7c			~1		~1b
~8a	+	CONTACT IN ~8a			~1		~1c
~8c	+	CONTACT IN ~8c			~2		~2a
~7b	-	COMMON ~7b			~2		~2b
~8b	-	SURGE			~2		~2c
~7a	+	CONTACT IN ~7a			~3		~3a
~7c	+	CONTACT IN ~7c			~3		~3b
~8a	+	CONTACT IN ~8a			~3		~3c
~8c	+	CONTACT IN ~8c			~4		~4a
~7b	-	COMMON ~7b			~4		~4b
~8b	-	SURGE			~4		~4c
~7a	+	CONTACT IN ~7a			~5		~5a
~7c	+	CONTACT IN ~7c			~5		~5b
~8a	+	CONTACT IN ~8a			~5		~5c
~8c	+	CONTACT IN ~8c			~6		~6a
~7b	-	COMMON ~7b			~6		~6b
~8b	-	SURGE			~6		~6c

827719sp.CDR
sheet 2 of 2

Figure 3–14: DIGITAL I/O MODULE WIRING (Sheet 2 of 2)



CORRECT POLARITY MUST BE OBSERVED FOR ALL CONTACT INPUT CONNECTIONS OR EQUIPMENT DAMAGE MAY RESULT.

A dry contact has one side connected to terminal B3b. This is the positive 48 VDC voltage rail supplied by the power supply module. The other side of the dry contact is connected to the required contact input terminal. Each contact input group has its own common (negative) terminal which must be connected to the DC negative terminal (B3a) of the power supply module. When a dry contact closes, a current of 1 to 3 mA will flow through the associated circuit.

A wet contact has one side connected to the positive terminal of an external DC power supply. The other side of this contact is connected to the required contact input terminal. In addition, the negative side of the external source must be connected to the relay common (negative) terminal of each contact input group. The maximum external source voltage for this arrangement is 300 V DC.

The voltage threshold at which each group of four contact inputs will detect a closed contact input is programmable as 16 V DC for 24 V sources, 30 V DC for 48 V sources, 80 V DC for 110 to 125 V sources, and 140 V DC for 250 V sources.

3

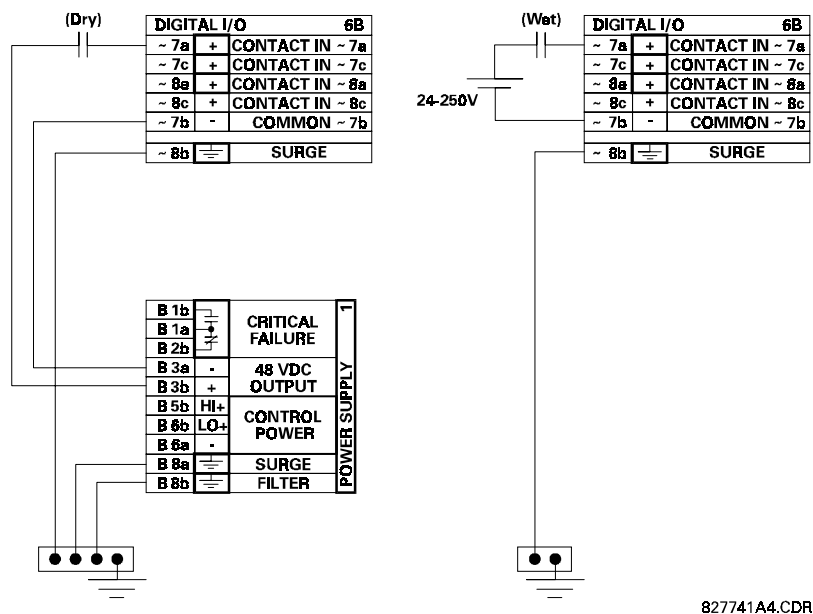


Figure 3-15: DRY AND WET CONTACT INPUT CONNECTIONS



NOTE

Wherever a tilde “~” symbol appears, substitute with the Slot Position of the module.

Contact outputs may be ordered as Form-A or Form-C. The Form A contacts may be connected for external circuit supervision. These contacts are provided with voltage and current monitoring circuits used to detect the loss of DC voltage in the circuit, and the presence of DC current flowing through the contacts when the Form-A contact closes. If enabled, the current monitoring can be used as a seal-in signal to ensure that the Form-A contact does not attempt to break the energized inductive coil circuit and weld the output contacts.

3.2.7 TRANSDUCER INPUTS/OUTPUTS

Transducer input/output modules can receive input signals from external dcmA output transducers (DCMA INPUT) or resistance temperature detectors (RTD INPUT). Hardware and software is provided to receive signals from these external transducers and convert these signals into a digital format for use as required.

Every transducer input/output module has a total of 24 terminal connections. These connections are arranged as three terminals per row with a total of eight rows. A given row may be used for either inputs or outputs, with terminals in column "a" having positive polarity and terminals in column "c" having negative polarity. Since an entire row is used for a single input/output channel, the name of the channel is assigned using the module slot position and row number.

Each module also requires that a connection from an external ground bus be made to terminal 8b.

The figure below illustrates the transducer module types (5F, etc.) and channel arrangements that may be ordered for the relay.



Wherever a tilde “~” symbol appears, substitute with the Slot Position of the module.

~1a	Hot	RTD ~ 1	5C
~1c	Comp		
~1b	Return	for RTD ~1 & ~2	
~2a	Hot	RTD ~ 2	
~2c	Comp		
~3a	Hot	RTD ~ 3	
~3c	Comp		
~3b	Return	for RTD ~ 3 & ~4	
~4a	Hot	RTD ~ 4	
~4c	Comp		
~5a	Hot	RTD ~ 5	
~5c	Comp		
~5b	Return	for RTD ~ 5 & ~6	
~6a	Hot	RTD ~ 6	
~6c	Comp		
~7a	Hot	RTD ~ 7	
~7c	Comp		
~7b	Return	for RTD ~ 7 & ~8	
~8a	Hot	RTD ~ 8	
~8c	Comp		
~8b		SURGE	ANALOG I/O

~1a	+	dcmA In ~ 1	5F
~1c	-		
~2a	+	dcmA In ~ 2	
~2c	-		
~3a	+	dcmA In ~ 3	
~3c	-		
~4a	+	dcmA In ~ 4	
~4c	-		
~5a	+	dcmA In ~ 5	
~5c	-		
~6a	+	dcmA In ~ 6	
~6c	-		
~7a	+	dcmA In ~ 7	
~7c	-		
~8a	+	dcmA In ~ 8	
~8c	-		
~8b		SURGE	ANALOG I/O

ANALOGIO.CDR
P/O: 827719CD.CDR

Figure 3–16: TRANSDUCER I/O MODULE WIRING

3.2.8 RS232 FACEPLATE PROGRAM PORT

A 9 pin RS232C serial port is located on the relay's faceplate for programming with a portable (personal) computer. All that is required to use this interface is a personal computer running the URPC software provided with the relay. Cabling for the RS232 port is shown in the following figure for both 9 pin and 25 pin connectors.

Note that the baud rate for this port is fixed at **19200 bps**.

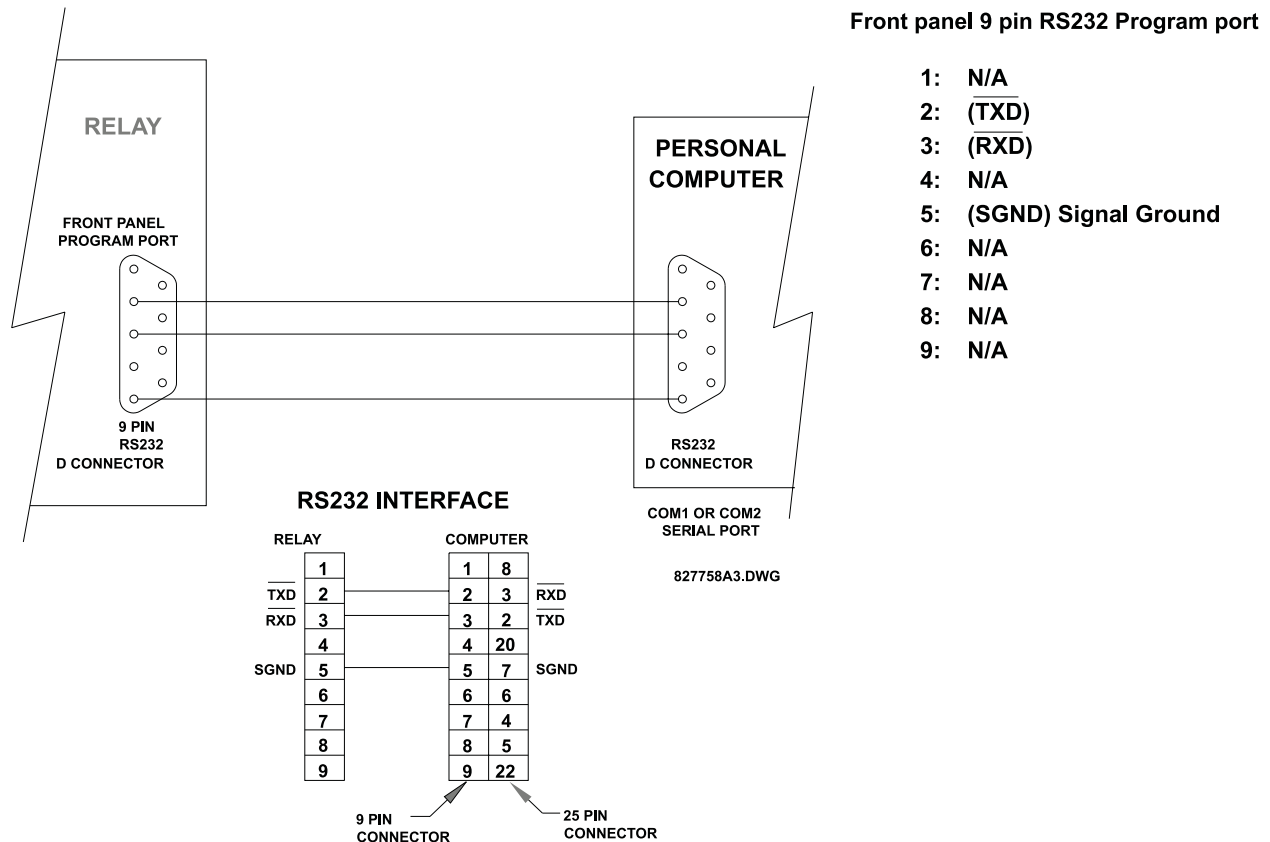



Figure 3-17: RS232 FACEPLATE PORT CONNECTION

3.2.9 CPU COMMUNICATION PORTS







In addition to the RS232 port on the faceplate, the relay provides the user with two additional communication port(s) depending on the CPU module installed.

Table 3–4: CPU COMMUNICATION PORT OPTIONS

CPU TYPE	COM 1	COM 2
9A	RS485	RS485
9C	10BASE-F	RS485
9D	Redundant 10BASE-F	RS485

D2a	+	RS485 COM 1	9A CPU
D3a	-		
D4a	COM		
D3b	+	RS485 COM 2	
D4b	-		
D5b	COM		
D5a	+	IRIG-B	
D6a	-		
D7b		SURGE	

<div><div><div>Tx</div><div>Rx</div></div></div> 10BaseF		NORMAL	COM 1	9C CPU
<div><div></div></div> 10BaseT		TEST ONLY		
D3b	+	RS485 COM 2		
D4b	-			
D5b	COM			
D5a	+	IRIG-B		
D6a	-			
D7b	<div><div></div></div>	SURGE		

  10BaseF	NORMAL	COM 1	9D CPU	
  10BaseF	ALTERNATE			
 10BaseT	TEST ONLY			
D3b	+	RS485 COM 2		
D4b	-			
D5b	COM			
D5a	+	IRIG-B		
D6a	-			
D7b		SURGE GROUND		

COMMODO.CDR
P/O 827719C2.CDR

Figure 3–18: CPU MODULE COMMUNICATIONS WIRING

a) RS485 PORTS

RS485 data transmission and reception are accomplished over a single twisted pair with transmit and receive data alternating over the same two wires. Through the use of these port(s), continuous monitoring and control from a remote computer, SCADA system or PLC is possible.

To minimize errors from noise, the use of shielded twisted pair wire is recommended. Correct polarity must also be observed. For instance, the relays must be connected with all RS485 “+” terminals connected together, and all RS485 “-” terminals connected together. The COM terminal should be connected to the common wire inside the shield, when provided. To avoid loop currents, the shield should be grounded at one point only. Each relay should also be daisy chained to the next one in the link. A maximum of 32 relays can be connected in this manner without exceeding driver capability. For larger systems, additional serial channels must be added. It is also possible to use commercially available repeaters to increase the number of relays on a single channel to more than 32. Star or stub connections should be avoided entirely.

Lightning strikes and ground surge currents can cause large momentary voltage differences between remote ends of the communication link. For this reason, surge protection devices are internally provided at both communication ports. An isolated power supply with an optocoupled data interface also acts to reduce noise coupling. To ensure maximum reliability, all equipment should have similar transient protection devices installed.

Both ends of the RS485 circuit should also be terminated with an impedance as shown in the figure: RS485 SERIAL CONNECTION.

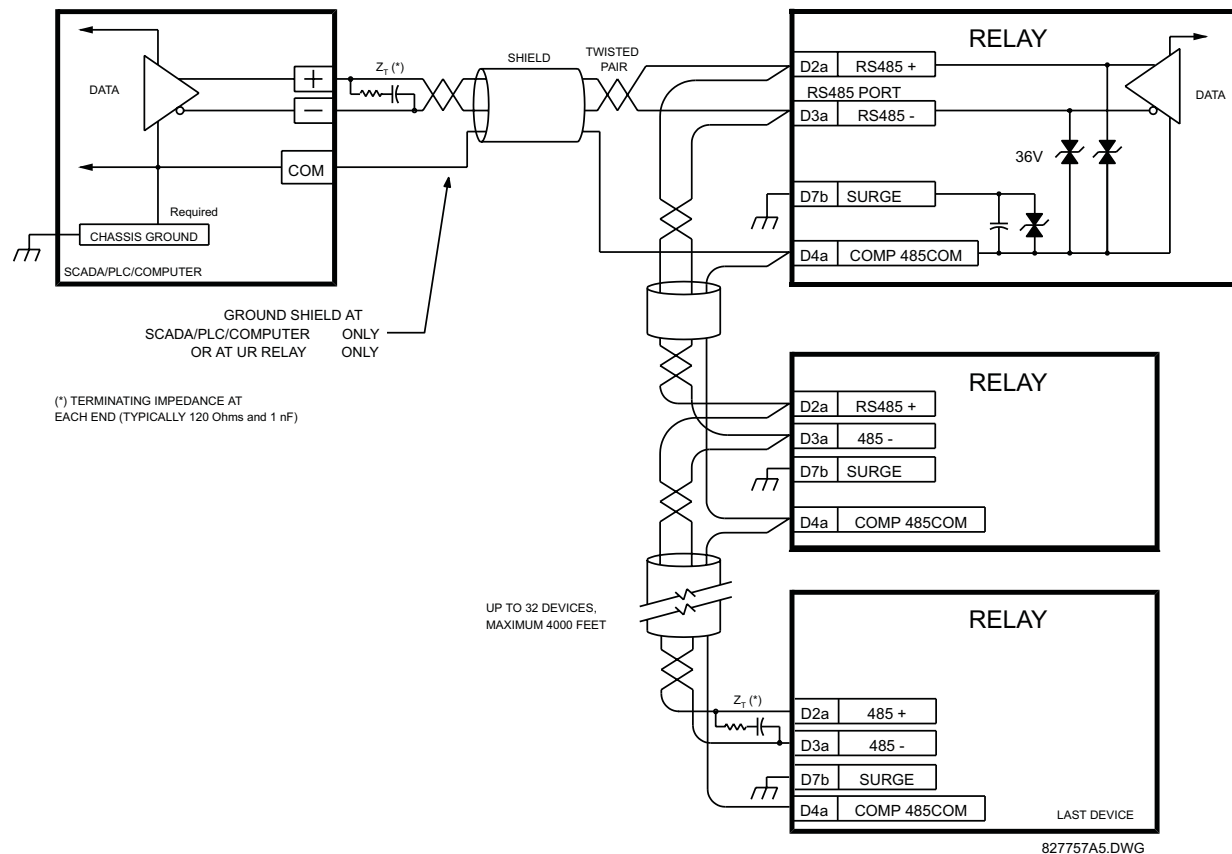


Figure 3-19: RS485 SERIAL CONNECTION

b) 10BASE-F FIBER OPTIC PORT



ENSURE THE DUST COVERS ARE INSTALLED WHEN THE FIBER IS NOT IN USE. DIRTY OR SCRATCHED CONNECTORS CAN LEAD TO HIGH LOSSES ON A FIBER LINK.



OBSERVING ANY FIBER TRANSMITTER OUTPUT MAY CAUSE INJURY TO THE EYE.

The fiber optic communication ports allow for fast and efficient communications between relays at 10 Mbps. Optical fiber may be connected to the relay supporting a wavelength of 820 nanometers in multimode. Optical fiber is only available for CPU types 9C and 9D. The 9D CPU has a 10BaseF transmitter and receiver for optical fiber communications and a second pair of identical optical fiber transmitter and receiver for redundancy.

The optical fiber sizes supported include 50/125 μm , 62.5/125 μm and 100/140 μm . The fiber optic port is designed such that the response times will not vary for any core that is 100 μm or less in diameter. For optical power budgeting, splices are required every 1 km for the transmitter/receiver pair (the ST type connector contributes for a connector loss of 0.2 dB). When splicing optical fibers, the diameter and numerical aperture of each fiber must be the same. In order to engage or disengage the ST type connector, only a quarter turn of the coupling is required.

3.2.10 IRIG-B

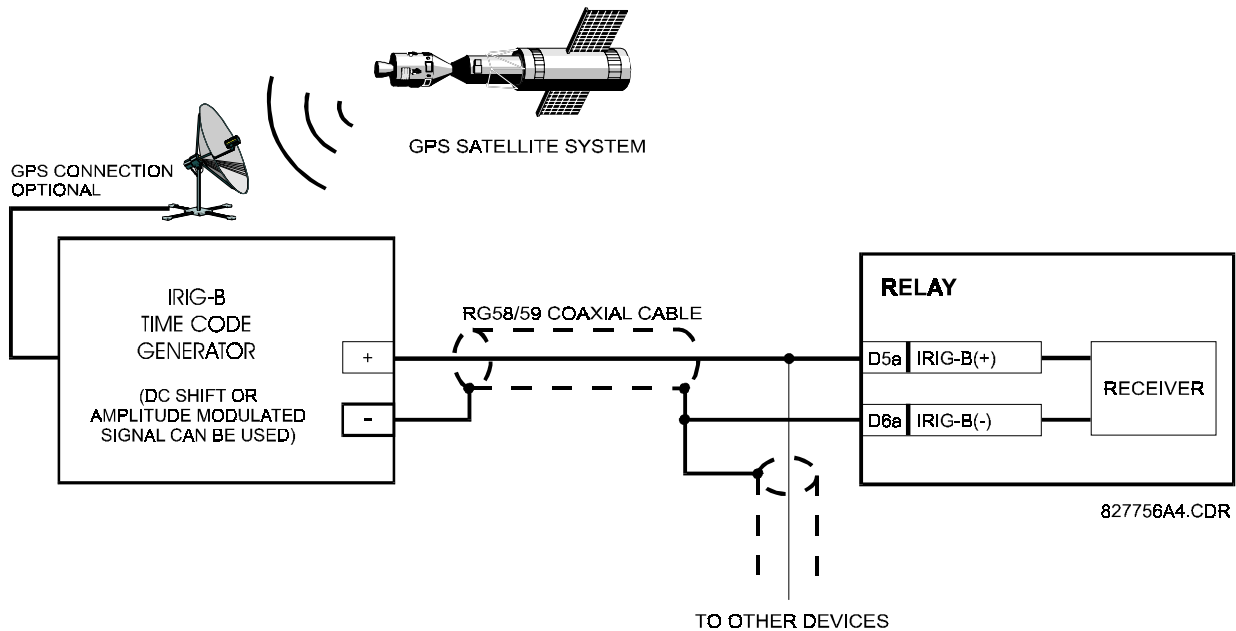


Figure 3–20: IRIG-B CONNECTION

IRIG-B is a standard time code format that allows stamping of events to be synchronized among connected devices within 1 millisecond. The IRIG time code formats are serial, width-modulated codes which can be either DC level shifted or amplitude modulated (AM). Third party equipment is available for generating the IRIG-B signal; this equipment may use a GPS satellite system to obtain the time reference so that devices at different geographic locations can also be synchronized.

3.2.11 L60 CHANNEL COMMUNICATIONS

To exchange phase comparison signals with a remote relay, the L60 requires a special module which is plugged into slot “W” as viewed from the front. This module is available in several varieties depending on the PLC type and station battery voltage. The “W” module shares phase comparison signals (squares) between relays via PLCs or other appropriate interfaces. Interconnections between the L60 and some typical market PLCs are shown below. One- or two-channel connections are required (the second channel is shown with dashed lines), depending on the L60 module chosen.

Some PLCs can be directly connected to the L60; others require interconnections with a station battery. Connections for W7Y(Z) and W7V(U) for the Trench CS22A, RFL 9780, and Pulsar TCF10 PLCs are shown below.

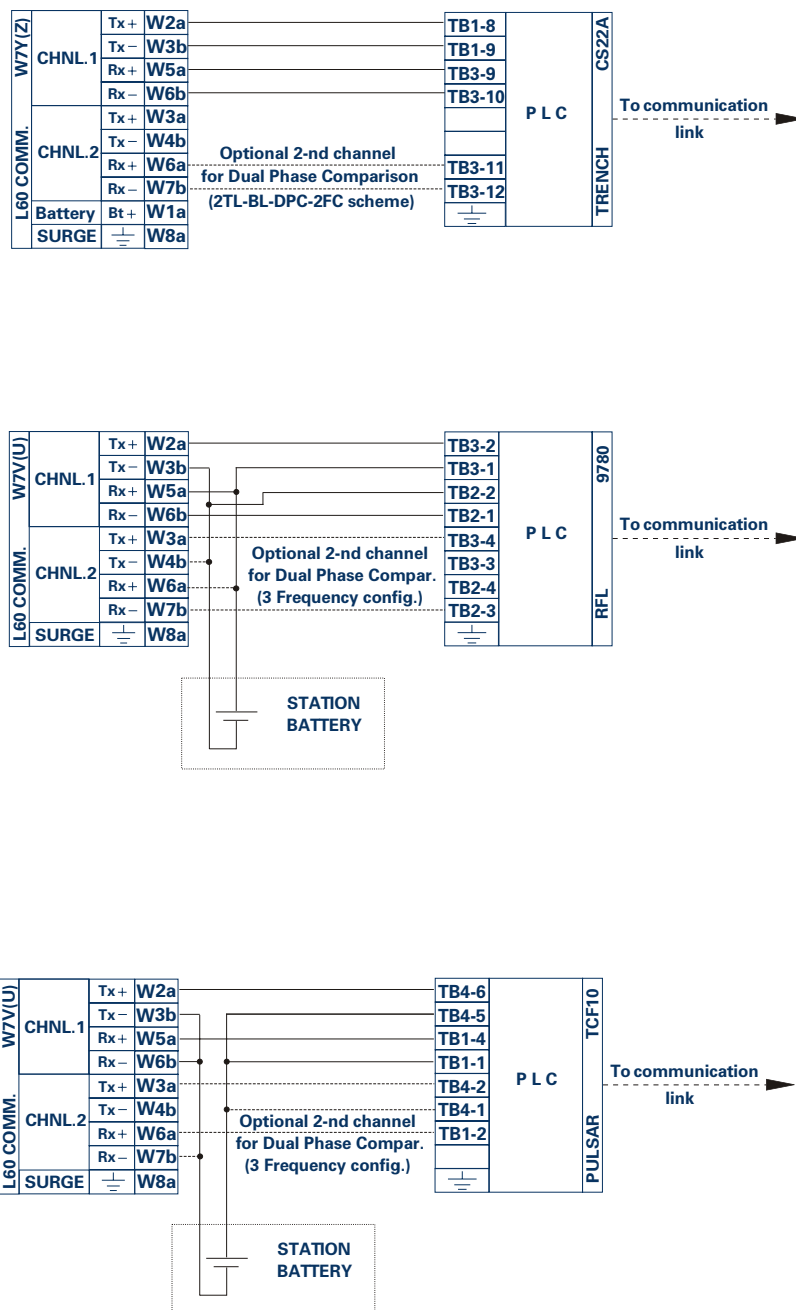


Figure 3-21: L60 INTERCONNECTIONS TO PLC

4.1.1 GRAPHICAL USER INTERFACE

The URPC software provides a graphical user interface (GUI) as one of two human interfaces to a UR device. The alternate human interface is implemented via the device's faceplate keypad and display (see FACEPLATE INTERFACE section in this chapter).

The URPC software program provides users with a single facility to configure, monitor, maintain and trouble-shoot the operation of relay functions, connected over local or wide area communication networks.

The URPC software interface can be used while disconnected (i.e. off-line) or connected (i.e. on-line) to a UR device. In off-line mode, you can prepare a file of the device's parameter settings for eventual downloading to the device. In on-line mode, you can communicate with the device in real-time.

The URPC® software, provided with every UR device, can be run from any computer supporting Microsoft® Windows® 95, 98, or NT.

The following figure illustrates an example URPC software screen showing example Site List and Settings List control bar tree menus, and the URPC Help window. This chapter provides a summary of the basic URPC® software interface features. The URPC Help program provides details for getting started and using the URPC® software interface.

a) CREATING A SITE LIST

To start using the URPC program, a Site List must first be created. See the instructions in the URPC Help program under the topic "Creating a Site List".

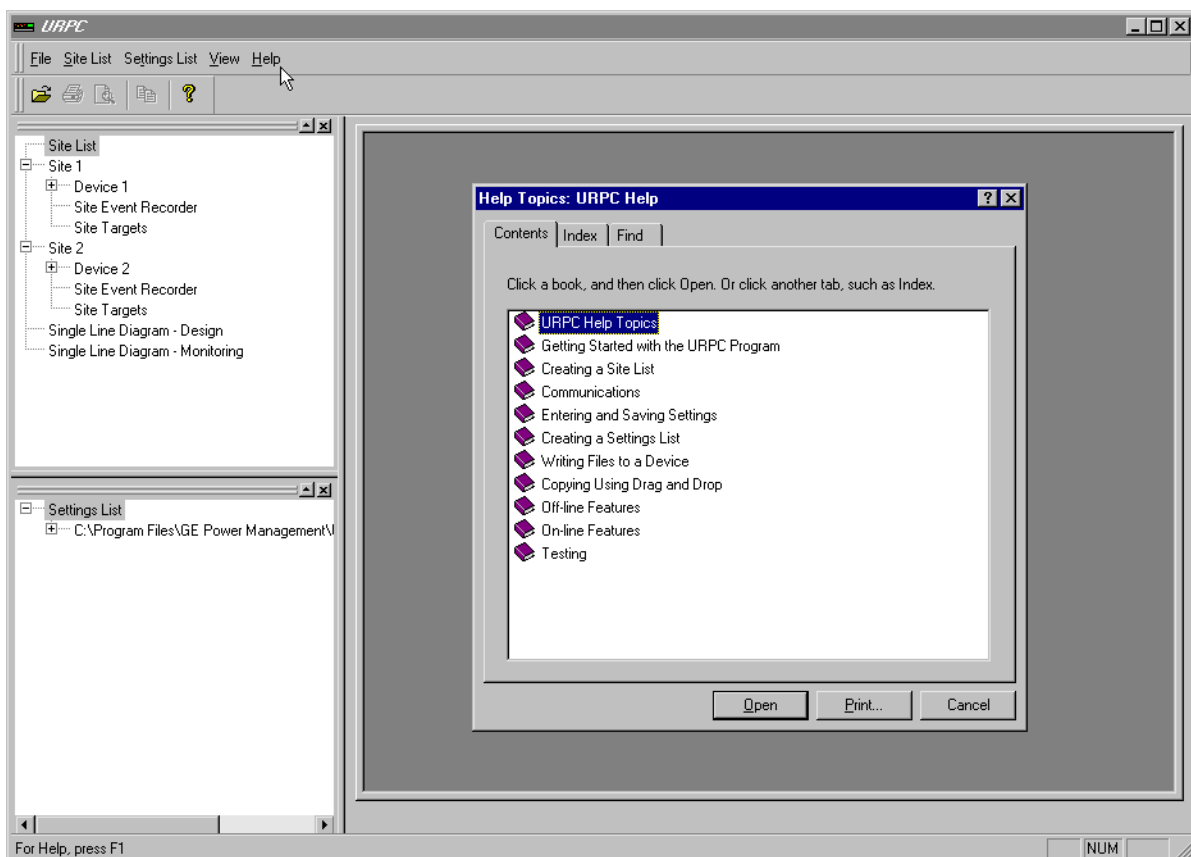


Figure 4–1: EXAMPLE URPC SOFTWARE SCREEN

4.1.2 URPC® SOFTWARE OVERVIEW

a) ENGAGING A COMMUNICATING DEVICE

You can use the URPC® software interface in on-line mode (relay connected) to directly communicate with a UR relay.

Communicating relays are organized and grouped by communication interfaces and into sites. Sites may contain any number of relays selected from the UR product series.

b) USING SETTINGS FILES

The URPC® software interface supports three ways of handling changes to relay settings:

- You can initially use the URPC software interface in off-line mode (relay disconnected) to create or edit relay settings files for later writing to communicating relays.
- You can use the interface while connected to a communicating relay to directly modify any relay settings via relay data view windows, and then save the settings to the relay.
- You can create/edit settings files and then write them to the relay while the interface is connected to the relay.

Settings files are organized on the basis of file names assigned by the user. A settings file contains data pertaining to the following types of relay settings:

- Device Definition
- Product Setup
- System Setup
- FlexLogic
- Grouped Elements
- Control Elements
- Inputs/Outputs
- Testing

Factory default values are supplied and can be restored after any changes.

c) CREATING / EDITING FLEXLOGIC™ EQUATIONS

You can create or edit a FlexLogic™ equation in order to customize the relay. You can subsequently view the automatically generated logic diagram.

d) VIEWING ACTUAL VALUES

You can view real-time relay data such as input/output status and measured parameters.

e) VIEWING TRIGGERED EVENTS

While the interface is in either on-line or off-line mode, you can view and analyze data generated by triggered specified parameters, via:

- **Event Recorder facility**

The event recorder captures contextual data associated with the last 1024 events, listed in chronological order from most recent to oldest.

- **Oscillography facility**

The oscillography waveform traces and digital states are used to provide a visual display of power system and relay operation data captured during specific triggered events.

f) CREATING INTERACTIVE SINGLE LINE DIAGRAMS

The URPC® software provides an icon-based interface facility for designing and monitoring electrical schematic diagrams of sites employing UR relays.

g) FILE SUPPORT

- **Execution**

Any URPC file which is double clicked or opened will launch the application, or provide focus to the already opened application. If the file was a settings file (*.urs) which had been removed from the Settings List tree menu, it will be added back to the Settings List tree menu.

- **Drag and Drop**

The Site List and Settings List control bar windows are each mutually a drag source and a drop target for device-order-code-compatible files or individual menu items. Also, the Settings List control bar window and any Windows Explorer directory folder are each mutually a file drag source and drop target.

New files which are dropped into the Settings List window are added to the tree which is automatically sorted alphabetically with respect to settings file names.

Files or individual menu items which are dropped in the selected device menu in the Site List window will automatically be sent to the on-line communicating device.

h) UR FIRMWARE UPGRADES

The firmware of a UR device can be upgraded, locally or remotely, via the URPC® software. The corresponding instructions are provided by the URPC® Help program under the topic “Upgrading Firmware”.

4.1.3 URPC[®] SOFTWARE MAIN WINDOW

The URPC software main window supports the following primary display components:

- a. Title bar which shows the pathname of the active data view
- b. Main window menu bar
- c. Main window tool bar
- d. Site List control bar window
- e. Settings List control bar window
- f. Device data view window(s), with common tool bar
- g. Settings File data view window(s), with common tool bar
- h. Workspace area with data view tabs
- i. Status bar

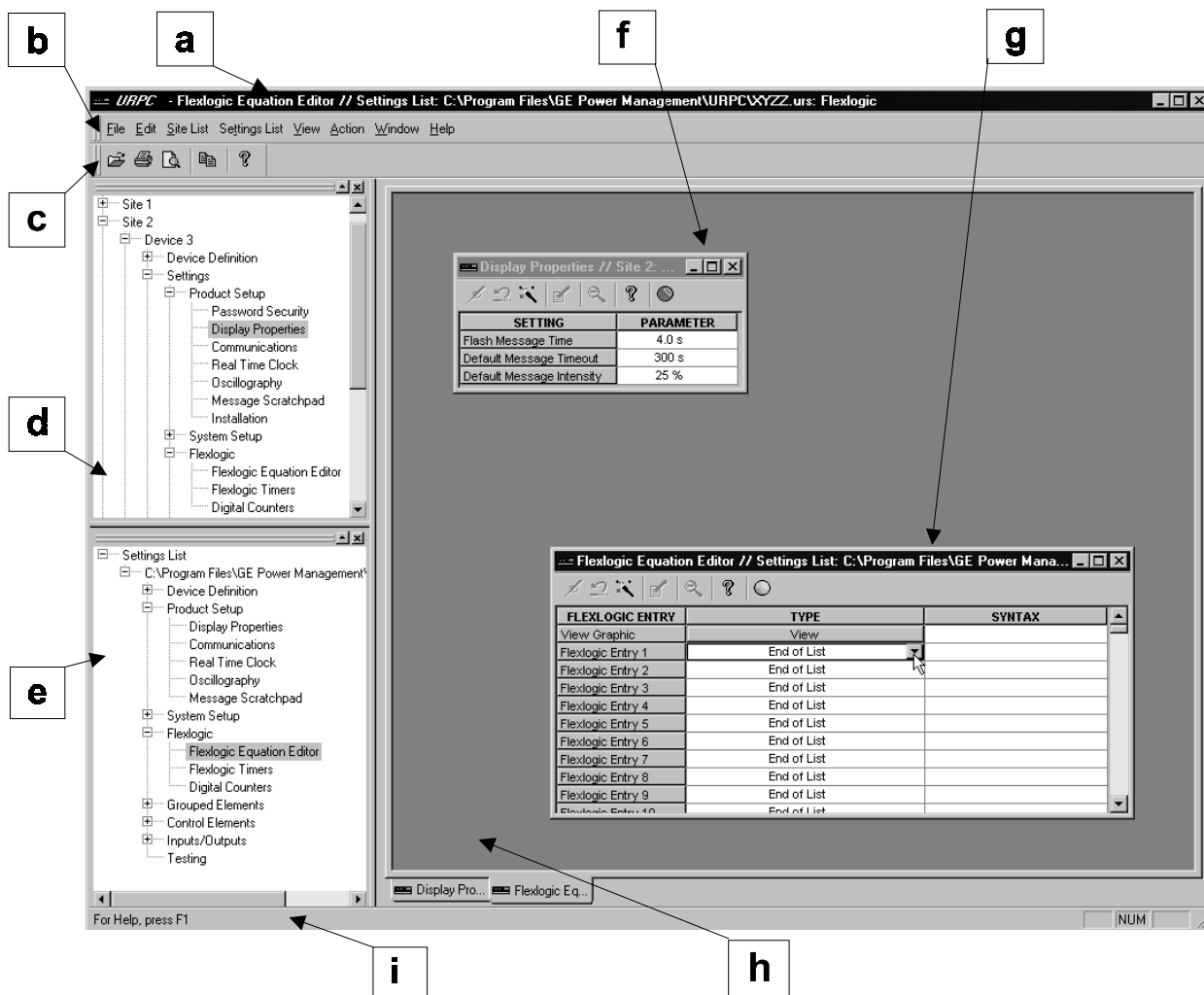


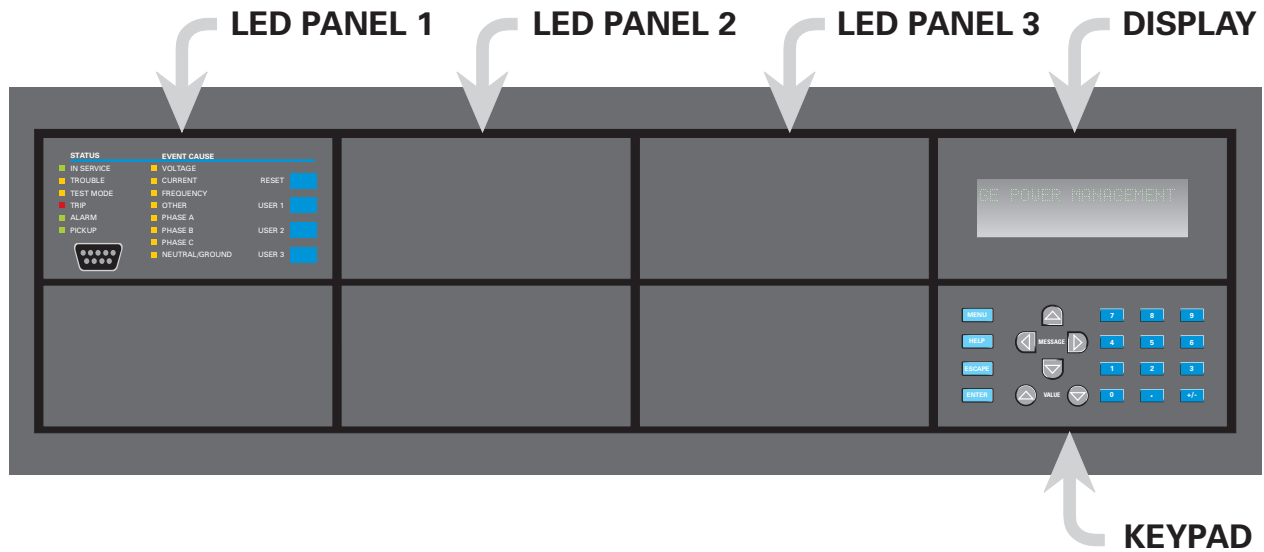
Figure 4-2: URPC SOFTWARE MAIN WINDOW

4.2.1 FACEPLATE

The UR faceplate Keypad/Display/LEDs interface is one of two alternate human interfaces supported. The alternate human interface is implemented via the URPC software. The UR faceplate interface is available in either of two configurations; horizontal or vertical. The faceplate interface consists of several functional panels.

The faceplate is hinged to allow easy access to the removable modules. There is also a removable dust cover that fits over the faceplate which must be removed in order to access the keypad panel.

The following two figures show the horizontal and vertical arrangements of faceplate panels.



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Figure 4-3: UR HORIZONTAL FACEPLATE PANELS

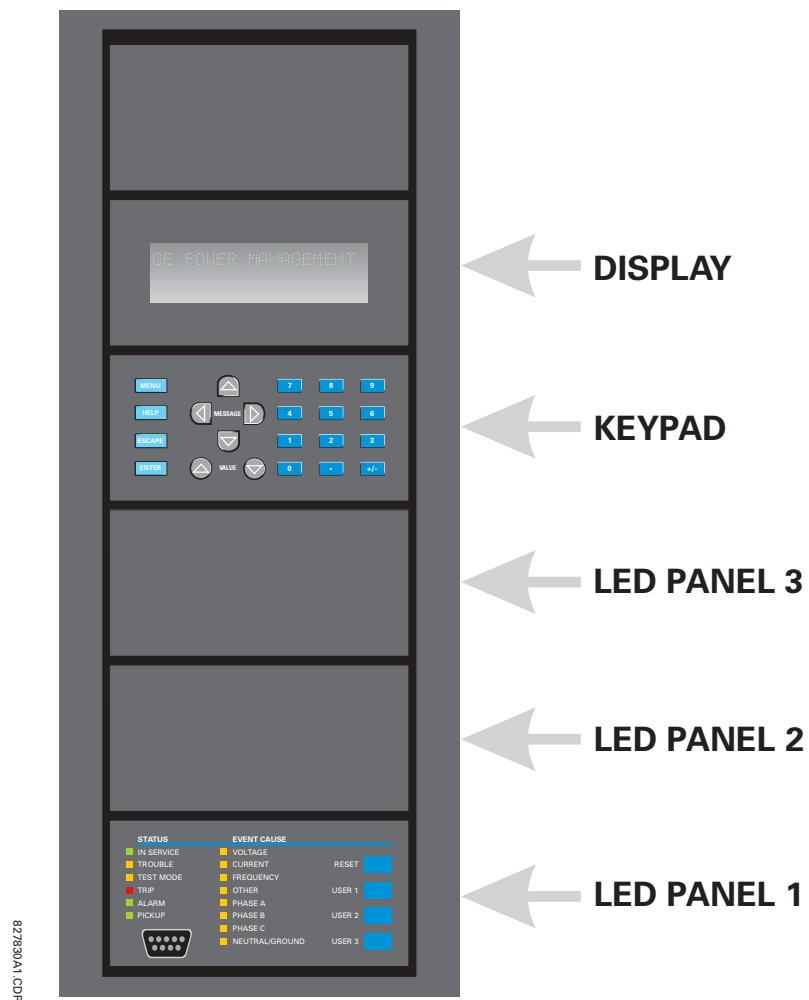


Figure 4-4: UR VERTICAL FACEPLATE PANELS

4.2.2 LED INDICATORS

a) LED PANEL 1

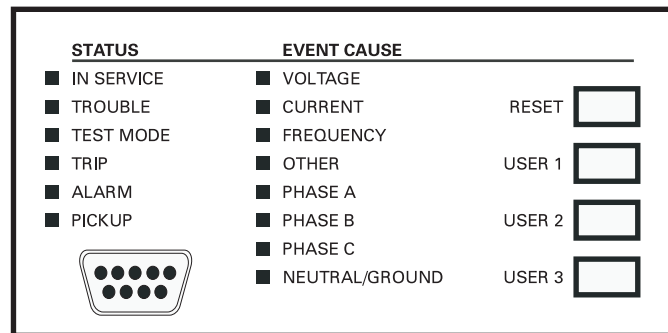


Figure 4–5: LED PANEL 1

This panel provides several groups of LED indicators, several keys, and a communications port. The RESET key is used to reset any latched LED indicator or target message, once the condition has been cleared (these latched conditions can also be reset via the SETTINGS \ INPUT/OUTPUTS \ RESETTING menu). The USER keys are used by the Breaker Control feature. The RS232 port is intended for connection to a portable PC.

STATUS INDICATORS:

- **IN SERVICE:** Indicates that control power is applied; all monitored I/O and internal systems are OK; the relay has been programmed.
- **TROUBLE:** Indicates that the relay has detected an internal problem.
- **TEST MODE:** Indicates that the relay is in test mode.
- **TRIP:** Indicates that the selected FlexLogic™ operand serving as a Trip switch has operated. This indicator always latches; the RESET command must be initiated to allow the latch to be reset.
- **ALARM:** Indicates that the selected FlexLogic™ operand serving as an Alarm switch has operated. This indicator is never latched.
- **PICKUP:** Indicates that an element is picked up. This indicator is never latched.

EVENT CAUSE INDICATORS:

These indicate the input type that was involved in a condition detected by an element that is operated or has a latched flag waiting to be reset.

- **VOLTAGE:** Indicates voltage was involved.
- **CURRENT:** Indicates current was involved.
- **FREQUENCY:** Indicates frequency was involved.
- **OTHER:** Indicates a composite function was involved.
- **PHASE A:** Indicates phase A was involved.
- **PHASE B:** Indicates phase B was involved.
- **PHASE C:** Indicates phase C was involved.
- **NEUTRAL/GROUND:** Indicates neutral or ground was involved.

b) LED PANELS 2 & 3

USER-PROGRAMMABLE LEDS		
■ (1)	■ (9)	■ (17)
■ (2)	■ (10)	■ (18)
■ (3)	■ (11)	■ (19)
■ (4)	■ (12)	■ (20)
■ (5)	■ (13)	■ (21)
■ (6)	■ (14)	■ (22)
■ (7)	■ (15)	■ (23)
■ (8)	■ (16)	■ (24)

Figure 4–6: LED PANEL 2 (INDEX TEMPLATE)

USER-PROGRAMMABLE LEDS		
■ (25)	■ (33)	■ (41)
■ (26)	■ (34)	■ (42)
■ (27)	■ (35)	■ (43)
■ (28)	■ (36)	■ (44)
■ (29)	■ (37)	■ (45)
■ (30)	■ (38)	■ (46)
■ (31)	■ (39)	■ (47)
■ (32)	■ (40)	■ (48)

Figure 4–7: LED PANEL 3 (INDEX TEMPLATE)

These panels provide 48 amber LED indicators whose operation is controlled by the user. When shipped from the factory, the LEDs on these panels will have been labeled and programmed with defaults to operate appropriately for each specific type of UR relay. The default settings controlling LED operation can be changed by the end user; and as well, support for applying a customized label beside every LED is provided.

User customization of LED operation is of maximum benefit in installations where languages other than English are used to communicate with operators.

Refer to the ‘SETTINGS \ PRODUCT SETUP \ USER-PROGRAMMABLE LEDS’ section in Chapter 5 for the settings used to program the operation of the LEDs on these panels, and for factory preset LED panel settings.

c) DEFAULT LABELS FOR LED PANEL 2

<u>SETTINGS IN USE</u>	<u>BREAKER 1</u>	<u>SYNCHROCHECK</u>
GROUP 1	OPEN	NO1 IN-SYNCH
GROUP 2	CLOSED	NO2 IN-SYNCH
GROUP 3	TROUBLE	
GROUP 4		<u>RECLOSE</u>
GROUP 5	<u>BREAKER 2</u>	ENABLED
GROUP 6	OPEN	DISABLED
GROUP 7	CLOSED	IN PROGRESS
GROUP 8	TROUBLE	LOCKED OUT

The default indications represent:

FACEPLATE LABEL	FUNCTION
GROUP 1...8	The illuminated GROUP is the active settings group.
BREAKER n OPEN	The breaker is open.
BREAKER n CLOSED	The breaker is closed.
BREAKER n TROUBLE	A problem related to the breaker has been detected.
SYNCHROCHECK NO _n IN-SYNCH	Voltages have satisfied the synchrocheck element.
RECLOSE ENABLED	The recloser is operational.
RECLOSE DISABLED	The recloser is not operational.
RECLOSE IN PROGRESS	A reclose operation is in progress.
RECLOSE LOCKED OUT	The recloser is not operational and requires a reset.

None of the above functions are latched in either the 'on' or 'off' state.

d) DEFAULT LABELS FOR LED PANEL 3

PHASE COMP	NEG SEQ TOC1	
	NEUTRAL TOC1	
	PHASE TOC1	
NEUTRAL IOC1		
PHASE IOC1		

The default indications represent:

FACEPLATE LABEL	FUNCTION
PHASE COMP	The phase comparison element has operated.
NEUTRAL IOC1	The neutral instantaneous overcurrent element No.1 has operated.
PHASE IOC1	The phase instantaneous overcurrent element No.1 has operated.
NEG SEQ TOC1	The negative sequence time overcurrent element No.1 has operated.
NEUTRAL TOC1	The neutral time overcurrent element No.1 has operated.
PHASE TOC1	The phase time overcurrent element No.1 has operated.

After one of the elements listed above has operated, the corresponding LED is latched 'on' and will remain illuminated until a RESET command is received by the relay.

Some FlexLogic™ equations have been programmed at the factory to provide operation of the faceplate LEDs for the functions shown above. The user can modify these equations which are shown in the FLEXLOGIC EQUATION EDITOR section of the SETTINGS chapter.

e) CUSTOM LABELING OF LEDs

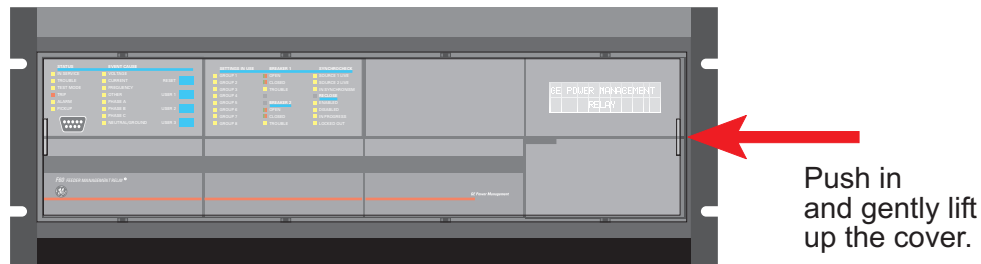
Custom labeling of an LED-only panel is facilitated by downloading a 'zip' file from

<http://www.ge.com/indsys/pm/drawings/ur/custmod.zip>.

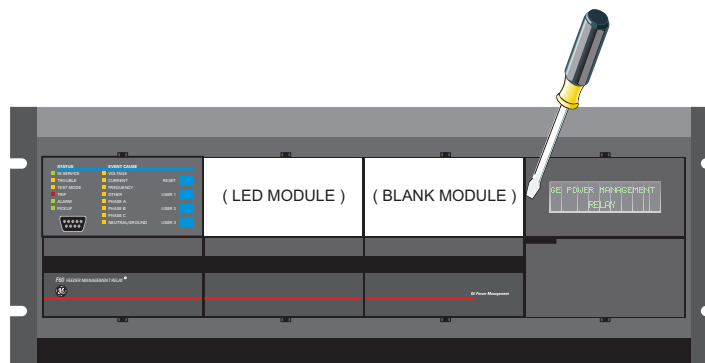
Opening this file will provide templates and instructions for creating appropriate labeling for the LED panel. The following three figures show the information in the downloadable file. The 'CorelDRAW' panel-templates provide relative LED locations and located example-text (x) edit boxes. The figure below shows how to install/uninstall the custom panel labeling.

HOW TO INSTALL THE UR CUSTOMIZED DISPLAY MODULE ON THE FRONT PANEL:

1-Remove the clear LEXAN FRONT COVER (P/N:1502-0014)



2-Pop out LED MODULE and/or BLANK MODULE with a screwdriver as the picture shows. (Be careful not to damage the plastic)



3-First place the left side of the customized module back to the front panel frame, then snap back the right side.

4-Put the clear LEXAN FRONT PANEL back to its place.

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Figure 4-8: CUSTOMIZED LED PANEL INSTALLATION

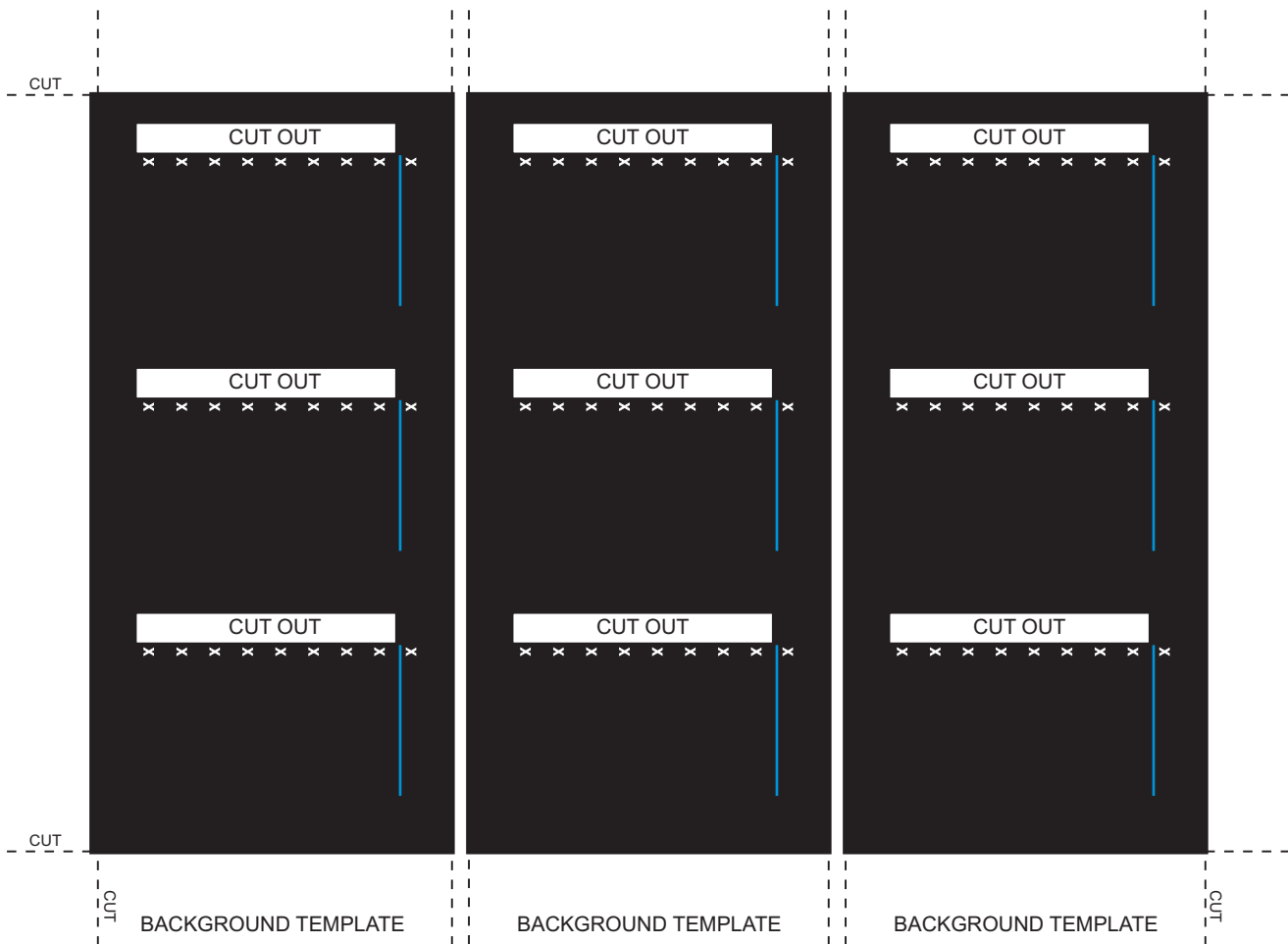


Figure 4-9: LED PANEL CUSTOMIZATION TEMPLATES

Instruction for how to customize the UR Display module

YOU NEED:

- Access to black and white or color printer (color preferred).
- CorelDRAW version 5 or later software package

Quantity	Material
1	8.5"x11" White paper
1	Exacto knife
1	Ruler
1	Custom display module (P/N: 1513-0069)
1	Custom module cover (P/N: 1502-0015)

HOW TO EDIT:

Add text in place of the Xs on the TEMPLATE(S) with **Edit Text...** from **Text** pull down menu. Delete the X place holders as required.

HOW TO PRINT:

Print one copy on the **White paper**.

- 1-Select **File** pull down menu.
- 2-Select **Print** from pull down menu.
- 3-Select the appropriate color printer.
- 4-Press **Properties...** button. On **Page Setup** tab for
 - Paper Size:** choose
 - Orientation:** choose ☒ **Landscape**
 - Press **OK**
- 5-Press **Options...** button. On **Layout** tab for
 - Position and size:** choose ☒ **Center image**
and ☒ **Maintain aspect ratio**
 - Press **OK**
- 6-And **OK** again.

HOW TO CUT:

- 1-From the print out cut out the **BACKGROUND TEMPLATE** and the **3 WINDOWS** (Using the cropmarks as a guide).

HOW TO ASSEMBLE:

- 1-Put the **BACKGROUND TEMPLATE** on top of the **Custom display module**.
- 2-Snap the clear **Custom module cover (P/N:1502-0015)** over the **Custom display module (P/N:1513-0069)** and templates.

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Figure 4–10: LED PANEL CUSTOMIZATION DETAILED INSTRUCTIONS

4.2.3 DISPLAY

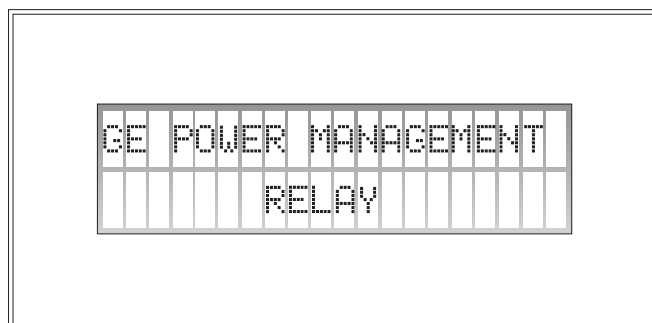


Figure 4-11: DISPLAY

All messages are displayed on a 2 × 20 character vacuum fluorescent display to make them visible under poor lighting conditions. Messages are displayed in English and do not require the aid of an instruction manual for deciphering. While the keypad and display are not actively being used, the display will default to defined messages. Any high priority event driven message will automatically override the default message and appear on the display.

4.2.4 KEYPAD

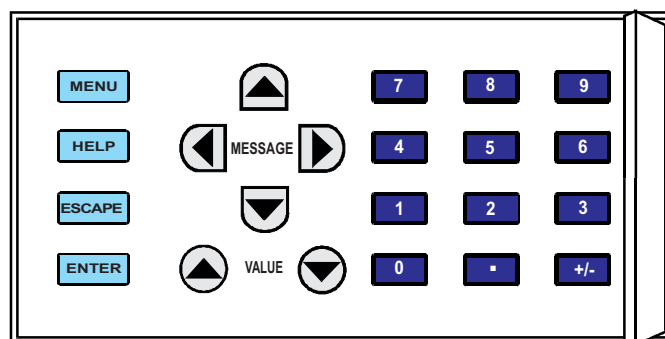


Figure 4-12: KEYPAD

Display messages are organized into 'pages' under the main headings, Actual Values, Settings, Commands, and Targets. The **MENU** key is used to navigate through the main heading pages. Each main heading page is further broken down into logical subgroup messages.

The **▲** **◀** **MESSAGE** **▶** **▼** keys are used to navigate through the subgroups.

The **▲** **VALUE** **▼** keys are used to scroll through variables in the settings programming mode to increment or decrement numerical setting values. These keys are also used to scroll through alphanumeric values in the text edit mode. Alternatively, values may be entered with the numeric keypad.

The **■** key is used to initiate and advance to the next character in text edit mode or to enter a decimal point.

The **HELP** key may be pressed at any time for context sensitive help messages. The **ENTER** key is used to store altered setting values.

4.2.5 BREAKER CONTROL

UR relays provide a feature to interface with circuit breakers that are associated with the relay. In many cases the application will monitor the state of the breaker, which can be presented on faceplate LEDs, along with a breaker trouble indication. Breaker operations can be manually initiated from faceplate PUSHBUTTON (USER) keys, or automatically initiated from a FlexLogic™ operand. A setting is provided for a user to assign a name to each breaker; the user-assigned name will be used for the display of related flash messages. These features are provided for two breakers; a user may of course use only those portions of the design relevant to a single breaker, which must be breaker No. 1.

For all of the following discussion it is assumed that the SETTINGS \ SYSTEM SETUP \ BREAKERS > BREAKER FUNCTION setting is Enabled for each breaker.

a) CONTROL MODE SELECTION & MONITORING

Installations may require that a breaker is operated in the three-pole only mode (3-Pole), or in the one and three-pole (1-Pole) mode, selected by setting. If the mode is selected as 3-pole, a single input is used to track the breaker open or closed position. If the mode is selected as 1-Pole, all three breaker pole states must be input to the relay. These inputs must be in agreement to indicate the position of the breaker.

For all of the following discussion it is assumed that the SETTINGS \ SYSTEM SETUP \ BREAKERS > BREAKER PUSH BUTTON CONTROL setting is Enabled for each breaker.

b) FACEPLATE PUSHBUTTON (USER KEY) CONTROL

After the 30 minute interval during which command functions are permitted after a correct command password has been entered, the user cannot open or close a breaker via the PUSHBUTTON (USER) keys, and the following discussions begin from the not-permitted state.

c) CONTROL OF TWO BREAKERS**NOTE**

For the following example setup, the symbol “(Name)” is used to represent the variable name that can be programmed by the user.

For this application (setup shown below), the relay is connected and programmed for both breaker No. 1 and breaker No. 2. The USER 1 key performs the selection of which breaker is to be operated by the USER 2 and USER 3 keys. The USER 2 key is used to manually close the breaker and the USER 3 key is used to manually open the breaker.

BREAKER CONTROL SETUP EXAMPLE:

ENTER COMMAND
PASSWORD

This message appears when the USER 1, USER 2, or USER 3 key is pressed and a COMMAND PASSWORD is required; i.e. if COMMAND PASSWORD is enabled and no commands have been issued within the last 30 minutes.

Press USER 1
To Select Breaker

This message appears if the correct password is entered or if none is required. This message will be maintained for 30 seconds or until the USER 1 key is pressed again.

BKR1-(Name) SELECTED
USER 2=CLS/USER 3=OP

This message is displayed after the USER 1 key is pressed for the second time. Three possible actions can be performed from this state within 30 seconds as per items **(1)**, **(2)** and **(3)** below:

(1)

USER 2 OFF/ON
To Close BKR1-(Name)

If the USER 2 key is pressed, this message appears for 20 seconds. If the USER 2 key is pressed again within that time, a signal is created that can be programmed to operate an output relay to close breaker No. 1.

(2)

USER 3 OFF/ON
To Open BKR1-(Name)

If the USER 3 key is pressed, this message appears for 20 seconds. If the USER 3 key is pressed again within that time, a signal is created that can be programmed to operate an output relay to open breaker No. 1.

(3)

BKR2-(Name) SELECTED
USER 2=CLS/USER 3=OP

If the USER 1 key is pressed at this step, this message appears showing that a different breaker is selected. Three possible actions can be performed from this state as per items **(1)**, **(2)** and **(3)**.

Repeatedly pressing the USER 1 key alternates between available breakers. Pressing a key other than USER 1, USER 2 or USER 3 key at any time will abort the breaker control function.

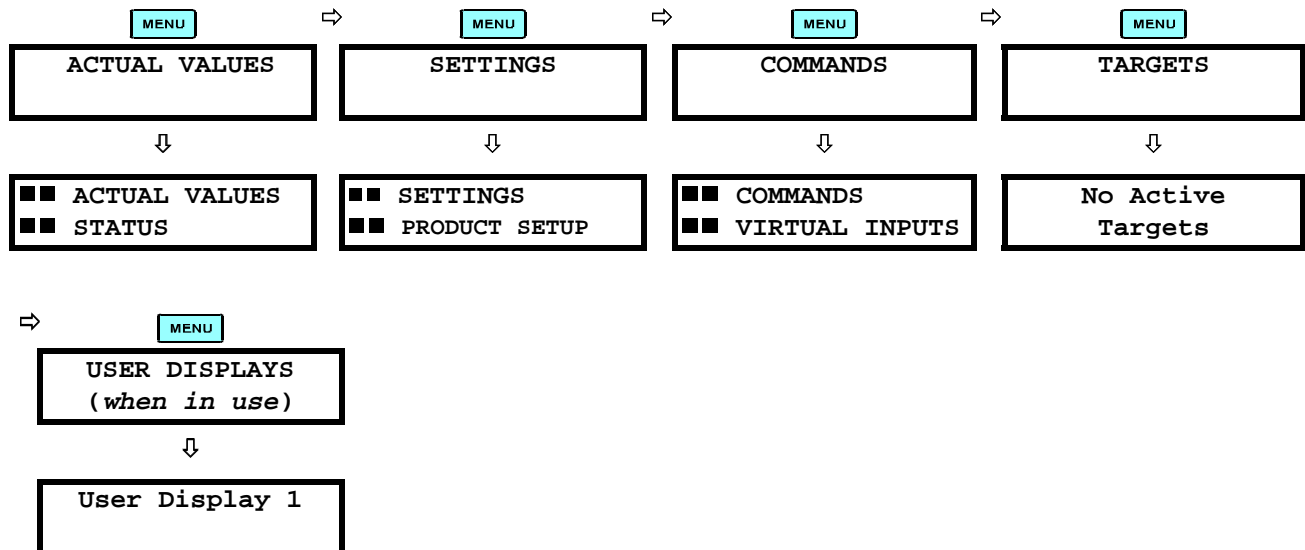
d) CONTROL OF ONE BREAKER

For this application the relay is connected and programmed for breaker No. 1 only. Operation for this application is identical to that described for two breakers.

4.2.6 MENUS

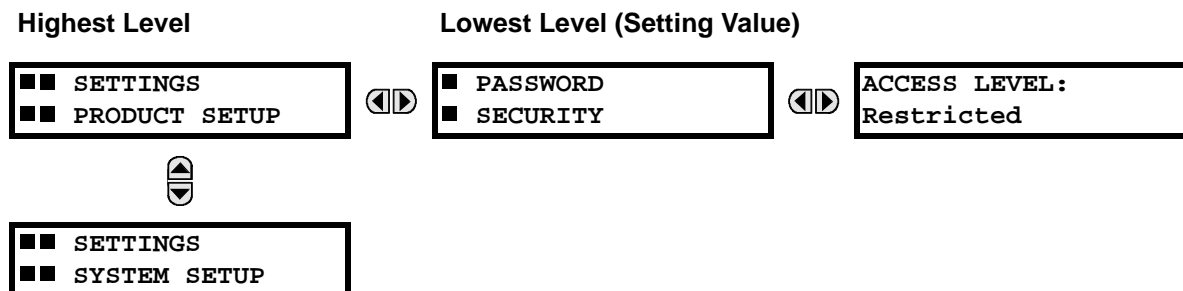
a) NAVIGATION

Press the **MENU** key to select the desired header display page (top-level menu). The header title will appear momentarily and then a header display page menu item will appear on the display. Each press of the **MENU** key advances through the main heading pages as illustrated below.

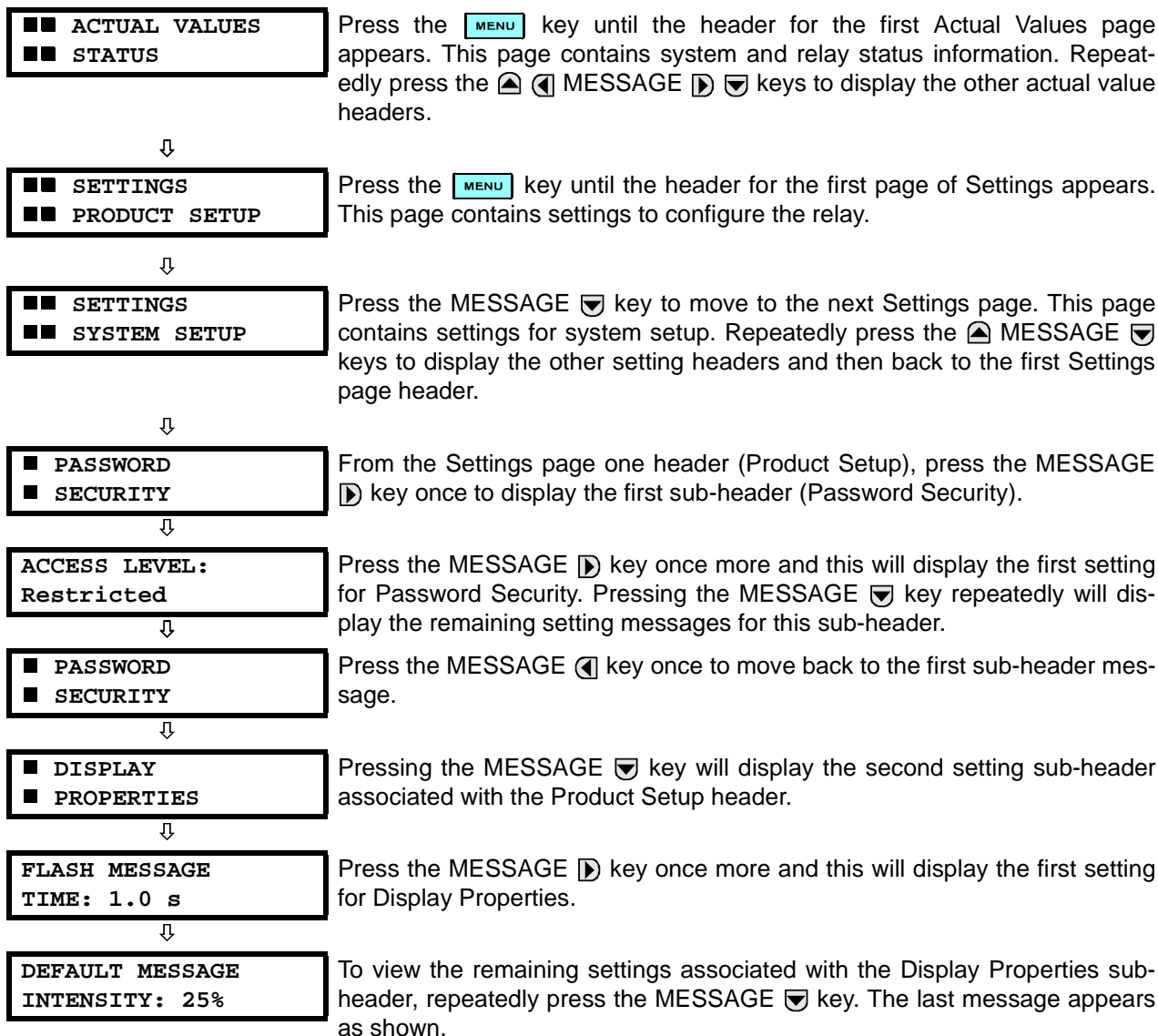


b) HIERARCHY

The setting and actual value messages are set up in a hierarchical format. The header display pages are indicated by the double scroll bar characters (■ ■), while sub-header pages are indicated by a single scroll bar character (■). The MESSAGE and MESSAGE keys are used to move within a group of headers, sub-headers, setting values or actual values. Continually pressing the MESSAGE key from a header display, displays more specific information for the header category. Conversely, continually pressing the MESSAGE key from a setting value or actual value display will return to the header display.



EXAMPLE MENU NAVIGATION SCENARIO:



4.2.7 CHANGING SETTINGS

a) ENTERING NUMERICAL DATA

Each numerical setting has its own minimum, maximum, and increment value associated with it. These parameters define what values are acceptable for a setting.

FLASH MESSAGE TIME: 1.0 s	For example, select the message PRODUCT SETUP \ DISPLAY PROPERTIES \ FLASH MESSAGE TIME.
↓	
MINIMUM: 0.5 MAXIMUM: 10.0	Press the HELP key to view the minimum and maximum values. Press the HELP key again to view the next context sensitive help message.

Two methods of editing and storing a numerical setting value are available.

- **0 to 9** and **.** (decimal point): The relay numeric keypad works the same as that of any electronic calculator. A number is entered one digit at a time. The leftmost digit is entered first and the rightmost digit is entered last. Pressing the MESSAGE **⏏** key or pressing the ESCAPE key, returns the original value to the display.
- **VALUE** **▲** **▼**: The VALUE **▲** key increments the displayed value by the step value, up to the maximum value allowed. While at the maximum value, pressing the VALUE **▲** key again will allow the setting selection to continue upward from the minimum value. The VALUE **▼** key decrements the displayed value by the step value, down to the minimum value. While at the minimum value, pressing the VALUE **▼** key again will allow the setting selection to continue downward from the maximum value.




FLASH MESSAGE TIME: 2.5 s	As an example, set the flash message time setting to 2.5 seconds. Press the appropriate numeric keys in the sequence '2 . 5'. The display message will change as the digits are being entered.
↓	
NEW SETTING HAS BEEN STORED	Until the ENTER key is pressed, editing changes are not registered by the relay. Therefore, press the ENTER key to store the new value in memory. This flash message will momentarily appear as confirmation of the storing process. Numerical values which contain decimal places will be rounded-off if more decimal place digits are entered than specified by the step value.

b) ENTERING ENUMERATION DATA



Enumeration settings have data values which are part of a set, whose members are explicitly defined by a name. A set is comprised of two or more members.

ACCESS LEVEL: Restricted	For example, the selections available for the PASSWORD SECURITY \ ACCESS LEVEL are 'Restricted', 'Command', 'Setting', and 'Factory Service'.
-----------------------------	---

Enumeration type values are changed using the  VALUE  keys. The VALUE  key displays the next selection while the VALUE  key displays the previous selection.

ACCESS LEVEL: Setting	If the ACCESS LEVEL needs to be set to 'Setting', press the  VALUE  keys until the proper selection is displayed. Press the  key at any time for the context sensitive help messages.
--------------------------	--



NEW SETTING HAS BEEN STORED	Until the  key is pressed, editing changes are not registered by the relay. Therefore, press the  key to store the new value in memory. This flash message will momentarily appear as confirmation of the storing process.
--------------------------------	--








4

c) ENTERING ALPHANUMERIC TEXT

Text settings have data values which are fixed in length, but user-defined in character. They may be comprised of upper case letters, lower case letters, numerals, and a selection of special characters.

In order to allow the relay to be customized for specific applications, there are several places where text messages may be programmed. One example is the MESSAGE SCRATCHPAD. To enter alphanumeric text messages, the following procedure should be followed:

Example: to enter the text, "Breaker #1"

1. Press  to enter text edit mode.
2. Press the VALUE  or VALUE  key until the character 'B' appears; press  to advance the cursor to the next position.
3. Repeat step 2 for the remaining characters: r,e,a,k,e,r, ,#,1.
4. Press  to store the text.
5. If you have any problem, press the  key to view the context sensitive help. Flash messages will sequentially appear for several seconds each. For the case of a text setting message, the  key displays how to edit and store a new value.

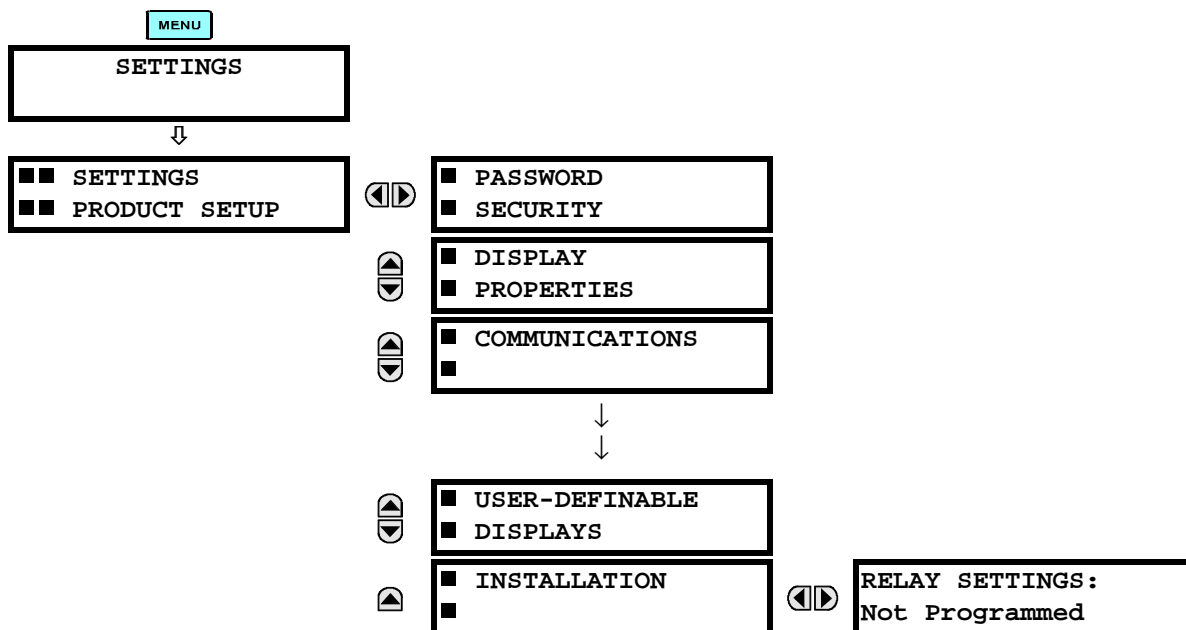
d) ACTIVATING THE RELAY

RELAY SETTINGS:
Not Programmed

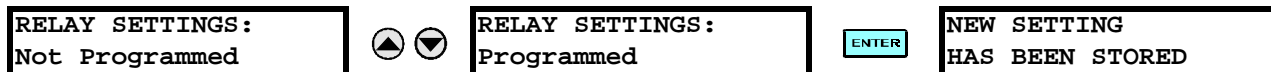
When the relay is powered up, the TROUBLE indicator will be on, the IN SERVICE indicator off, and this message displayed. This indicates that the relay is in the 'Not Programmed' state and is safeguarding (output relays blocked) against the installation of a relay whose settings have not been entered. This message will remain until the relay is explicitly put in the 'Programmed' state.

To change the 'RELAY SETTINGS: Not Programmed' mode to 'Programmed', proceed as follows:

1. Press the **MENU** key until the 'SETTINGS' header flashes momentarily and the 'SETTINGS PRODUCT SETUP' message appears on the display.
2. Press the MESSAGE **▶** key until the 'PASSWORD SECURITY' message appears on the display.
3. Press the MESSAGE **▼** key until the 'INSTALLATION' message appears on the display.
4. Press the MESSAGE **▶** key until the 'RELAY SETTINGS: Not Programmed' message is displayed.



5. After the 'RELAY SETTINGS: Not Programmed' message appears on the display, press the VALUE **▲** key or the VALUE **▼** key to change the selection to 'Programmed'.
6. Press the **ENTER** key.

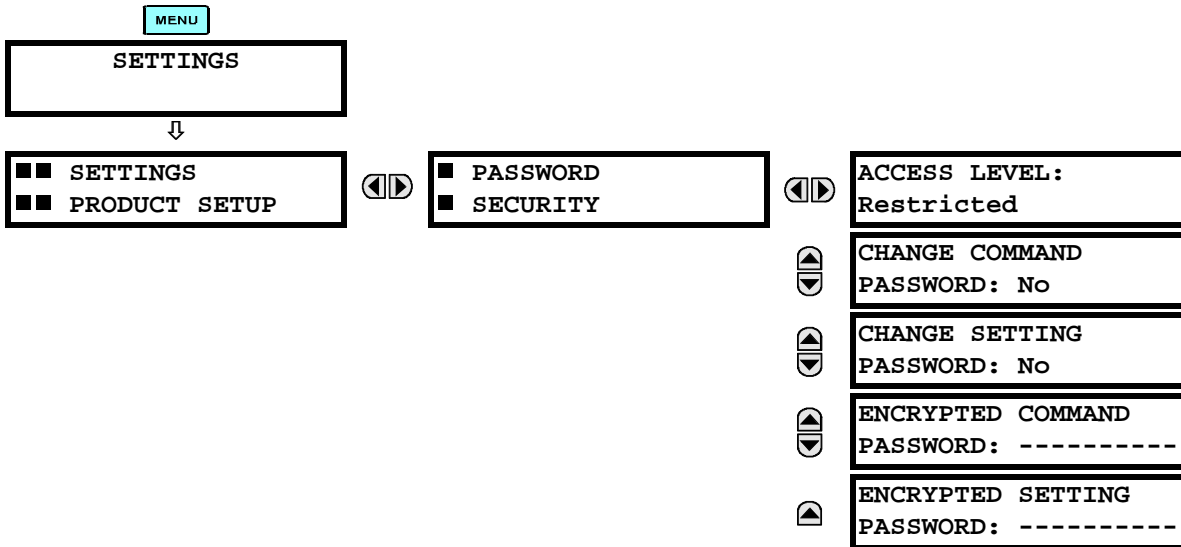


7. When the 'NEW SETTING HAS BEEN STORED' message appears, the relay will be in 'Programmed' state and the 'IN SERVICE' indicator will turn on.

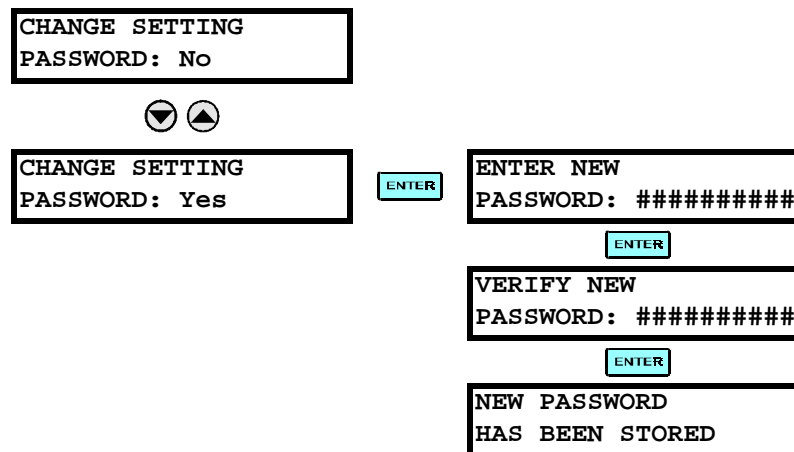
e) ENTERING INITIAL PASSWORDS

To enter the initial SETTING (or COMMAND) PASSWORD, proceed as follows:

1. Press the **MENU** key until the 'SETTINGS' header flashes momentarily and the 'SETTINGS PRODUCT SETUP' message appears on the display.
2. Press the MESSAGE **▶** key until the 'ACCESS LEVEL:' message appears on the display.
3. Press the MESSAGE **▼** key until the 'CHANGE SETTING (or COMMAND) PASSWORD:' message appears on the display.



4. After the 'CHANGE...PASSWORD' message appears on the display, press the VALUE **▲** key or the VALUE **▼** key to change the selection to Yes.
5. Press the **ENTER** key and the display will prompt you to 'ENTER NEW PASSWORD'.
6. Type in a numerical password (up to 10 characters) and press the **ENTER** key.
7. When the 'VERIFY NEW PASSWORD' is displayed, re-type in the same password and press **ENTER**.



8. When the 'NEW PASSWORD HAS BEEN STORED' message appears, your new SETTING (or COMMAND) PASSWORD will be active.

f) CHANGING EXISTING PASSWORD

To change an existing password, follow the instructions in the previous section with the following exception. A message will prompt you to type in the existing password (for each security level) before a new password can be entered.

In the event that a password has been lost (forgotten), submit the corresponding Encrypted Password from the PASSWORD SECURITY menu to the Factory for decoding.

5.1.1 SETTINGS MAIN MENU

<div> <div>■ ■ SETTINGS</div> <div>■ ■ PRODUCT SETUP</div> </div>		<div> <div>■ PASSWORD</div> <div>■ SECURITY</div> </div>	See page 5-9.
		<div> <div>■ DISPLAY</div> <div>■ PROPERTIES</div> </div>	See page 5-10.
		<div> <div>■ COMMUNICATIONS</div> <div>■</div> </div>	See page 5-11.
		<div> <div>■ MODBUS USER MAP</div> <div>■</div> </div>	See page 5-14.
		<div> <div>■ REAL TIME</div> <div>■ CLOCK</div> </div>	See page 5-14.
		<div> <div>■ FAULT REPORT</div> <div>■</div> </div>	See page 5-15.
		<div> <div>■ OSCILLOGRAPHY</div> <div>■</div> </div>	See page 5-16.
		<div> <div>■ DATA LOGGER</div> <div>■</div> </div>	See page 5-18.
		<div> <div>■ USER-PROGRAMMABLE</div> <div>■ LEDS</div> </div>	See page 5-19.
		<div> <div>■ FLEX STATE</div> <div>■ PARAMETERS</div> </div>	See page 5-21.
		<div> <div>■ USER-DEFINABLE</div> <div>■ DISPLAYS</div> </div>	See page 5-22.
		<div> <div>■ INSTALLATION</div> <div>■</div> </div>	See page 5-24.
		<div> <div>■ AC INPUTS</div> <div>■</div> </div>	See page 5-25.
		<div> <div>■ POWER SYSTEM</div> <div>■</div> </div>	See page 5-27.
		<div> <div>■ SIGNAL SOURCES</div> <div>■</div> </div>	See page 5-28.
		<div> <div>■ L60 POWER SYSTEM</div> <div>■</div> </div>	See page 5-31.
		<div> <div>■ LINE</div> <div>■</div> </div>	See page 5-31.
		<div> <div>■ BREAKERS</div> <div>■</div> </div>	See page 5-32.
		<div> <div>■ FLEXCURVES</div> <div>■</div> </div>	See page 5-35.

<div> <div>■ ■ SETTINGS</div> <div>■ ■ FLEXLOGIC</div> <div>▼</div> <div>▲</div> </div>	◀▶	<div> <div>■ FLEXLOGIC</div> <div>■ EQUATION EDITOR</div> </div>	See page 5-52.
<div> <div>■ ■ SETTINGS</div> <div>■ ■ GROUPED ELEMENTS</div> <div>▼</div> </div>	▲	<div> <div>■ FLEXLOGIC</div> <div>■ TIMERS</div> </div>	See page 5-53.
	◀▶	<div> <div>■ SETTING GROUP 1</div> <div>■</div> </div>	See page 5-54.
	▲▼	<div> <div>■ SETTING GROUP 2</div> <div>■</div> </div>	
	▲▼	<div> <div>■ SETTING GROUP 3</div> <div>■</div> </div>	
	▲▼	<div> <div>■ SETTING GROUP 4</div> <div>■</div> </div>	
	▲▼	<div> <div>■ SETTING GROUP 5</div> <div>■</div> </div>	
	▲▼	<div> <div>■ SETTING GROUP 6</div> <div>■</div> </div>	
	▲▼	<div> <div>■ SETTING GROUP 7</div> <div>■</div> </div>	
	▲	<div> <div>■ SETTING GROUP 8</div> <div>■</div> </div>	
<div> <div>■ ■ SETTINGS</div> <div>■ ■ CONTROL ELEMENTS</div> <div>▼</div> </div>	◀▶	<div> <div>■ SETTING GROUPS</div> <div>■</div> </div>	See page 5-108.
	▲▼	<div> <div>■ SYNCHROCHECK</div> <div>■</div> </div>	See page 5-110.
	▲▼	<div> <div>■ AUTORECLOSE</div> <div>■</div> </div>	See page 5-114.
	▲▼	<div> <div>■ DIGITAL ELEMENTS</div> <div>■</div> </div>	See page 5-122.
	▲▼	<div> <div>■ DIGITAL COUNTERS</div> <div>■</div> </div>	See page 5-126.
	▲▼	<div> <div>■ MONITORING</div> <div>■ ELEMENTS</div> </div>	See page 5-129.
	▲▼	<div> <div>■ PILOT SCHEMES</div> <div>■</div> </div>	See page 5-136.
	▲	<div> <div>■ PHASE COMPARISON</div> <div>■ ELEMENTS</div> </div>	See page 5-140.
<div> <div>■ ■ SETTINGS</div> <div>■ ■ INPUTS / OUTPUTS</div> <div>▼</div> </div>	◀▶	<div> <div>■ CONTACT INPUTS</div> <div>■</div> </div>	See page 5-149.
	▲▼	<div> <div>■ VIRTUAL INPUTS</div> <div>■</div> </div>	See page 5-151.

	▲▼	■ CONTACT OUTPUTS ■	See page 5-153.
	▲▼	■ VIRTUAL OUTPUTS ■	See page 5-154.
	▲▼	■ REMOTE DEVICES ■	See page 5-155.
	▲▼	■ REMOTE INPUTS ■	See page 5-156.
	▲▼	■ REMOTE OUTPUTS ■ DNA BIT PAIRS	See page 5-157.
	▲▼	■ REMOTE OUTPUTS ■ UserSt BIT PAIRS	See page 5-158.
	▲	■ RESETTING ■	See page 5-158.
▲	◀▶	■ DCMA INPUTS ■	See page 5-159.
▼	▲	■ RTD INPUTS ■	See page 5-160.
▲	◀▶	TEST MODE FUNCTION:	See page 5-161.
■ ■ SETTINGS ■ ■ TRANSDUCER I/O	▲▼	■ FORCE CONTACT ■ INPUTS	See page 5-161.
	▲	■ FORCE CONTACT ■ OUTPUTS	See page 5-161.
■ ■ SETTINGS ■ ■ TESTING	▲	■ CHANNEL TESTS ■	See page 5-162.

5.1.2 INTRODUCTION TO ELEMENTS

In the design of UR relays, the term “element” is used to describe a feature that is based around a comparator. The comparator is provided with an input (or set of inputs) that is tested against a programmed setting (or group of settings) to determine if the input is within the defined range that will set the output to logic 1, also referred to as “setting the flag”. A single comparator may make multiple tests and provide multiple outputs; for example, the time overcurrent comparator sets a Pickup flag when the current input is above the setting and sets an Operate flag when the input current has been at a level above the pickup setting for the time specified by the time-current curve settings. All comparators, except the Digital Element which uses a logic state as the input, use analog parameter actual values as the input.

Elements are arranged into two classes, GROUPED and CONTROL. Each element classed as a GROUPED element is provided with eight alternate sets of settings, in setting groups numbered 1 through 8. The performance of a GROUPED element is defined by the setting group that is active at a given time. The performance of a CONTROL element is independent of the selected active setting group.

The main characteristics of an element are shown on the element scheme logic diagram. This includes the input(s), settings, fixed logic, and the output operands that are generated (abbreviations used on scheme logic diagrams are defined in the ABBREVIATIONS Appendix).

Some settings for current and voltage elements are specified in per-unit (pu) calculated quantities:

pu quantity = (actual quantity) / (base quantity)

- For current elements, the ‘base quantity’ is the nominal secondary or primary current of the CT. Where the current source is the sum of two CTs with different ratios, the ‘base quantity’ will be the common secondary or primary current to which the sum is scaled (i.e. normalized to the larger of the 2 rated CT inputs). For example, if CT1 = 300 / 5 A and CT2 = 100 / 5 A, then in order to sum these, CT2 is scaled to the CT1 ratio. In this case, the ‘base quantity’ will be 5 A secondary or 300 A primary.
- For voltage elements, the ‘base quantity’ is the nominal secondary or primary voltage of the VT.

Some settings are common to most elements and are discussed below:

FUNCTION Setting

This setting is used to program the element to be operational when selected as Enabled. The factory default is Disabled. Once programmed to Enabled, any element associated with the Function becomes active and all options become available.

NAME Setting

This setting is used to uniquely identify the element.

SOURCE Setting

This setting is used to select the parameter or set of parameters to be monitored.

PICKUP Setting

For simple elements, this setting is used to program the level of the measured parameter above or below which the pickup state is established. In more complex elements, a set of settings may be provided to define the range of the measured parameters which will cause the element to pickup.

PICKUP DELAY Setting

This setting is used to set a time-delay-on-pickup, or on-delay, for the duration between the Pickup and Operate output states.

RESET DELAY Setting

This setting is used to set a time-delay-on-dropout, or off-delay, for the duration between the Operate output state and the return to logic 0 after the input transits outside the defined pickup range.

BLOCK Setting

The default output operand state of all comparators is a logic 0 or “flag not set”. The comparator remains in this default state until a logic 1 is asserted at the RUN input, allowing the test to be performed. If the RUN input changes to logic 0 at any time, the comparator returns to the default state. The RUN input is used to supervise the comparator. The BLOCK input is used as one of the inputs to RUN control.

TARGET Setting

This setting is used to define the operation of an element target message. When set to Disabled, no target message or illumination of a faceplate LED indicator is issued upon operation of the element. When set to Self-Reset, the target message and LED indication follow the Operate state of the element, and self-resets once the operate element condition clears. When set to Latched, the target message and LED indication will remain visible after the element output returns to logic 0 - until a RESET command is received by the relay.

EVENTS Setting

This setting is used to control whether the Pickup, Dropout or Operate states are recorded by the event recorder. When set to Disabled, element pickup, dropout or operate are not recorded as events.

When set to Enabled, an event is created for:

- (Element) PKP (pickup)
- (Element) DPO (dropout)
- (Element) OP (operate)

The DPO event is created when the measure and decide comparator output transits from the pickup state (logic 1) to the dropout state (logic 0). This could happen when the element is in the operate state if the reset delay time is not '0'.

5.1.3 INTRODUCTION TO AC SOURCES

a) BACKGROUND

UR relays may be used on systems with either breaker-and-a-half or ring bus configurations. In these applications, each of the two three-phase sets of individual phase currents (one associated with each breaker) could be used as an input to a breaker failure element. The sum of both breaker phase currents and 3I₀ residual currents may be required for the circuit relaying and metering functions. For a three-winding transformer application, it may be required to calculate watts and vars for each of three windings, using voltage from different sets of VTs. All of these requirements can be satisfied with a single UR relay, which is equipped with sufficient CT and VT input channels, by selecting the parameter to be measured. A mechanism is provided for users to specify the AC parameter (or group of parameters) to be used as the input to protection/control comparators and some metering elements.

Selection of the parameter(s) to be measured is partially performed by the design of a measuring element or protection/control comparator, by identifying the type of parameter (fundamental frequency phasor, harmonic phasor, symmetrical component, total waveform RMS magnitude, phase-phase or phase-ground voltage, etc.) to be measured. The user completes the selection process by selecting the instrument transformer input channels to be used and some of the parameters calculated from these channels. The input parameters available include the summation of currents from multiple input channels. For the summed currents of phase, 3I₀ and ground current, current from CTs with different ratios are adjusted to a single ratio before the summation.

A mechanism called a "Source" is used to configure the routing of input CT and VT channels to measurement sub-systems. Sources, in the context of the UR family of relays, refers to the logical grouping of current and voltage signals such that one Source will contain all of the signals required to measure the load or fault in a particular power apparatus. A given Source could contain all or some of the following signals: three-phase currents, single-phase ground current, three-phase voltages and an auxiliary voltage from a single VT for checking for synchronism.

A simple example to illustrate the concept of Sources, as applied to current inputs only, is in breaker-and-a-half schemes as illustrated in the following figure, BREAKER-AND-A-HALF SCHEME. In this application, the current flow could be as shown by the labeled arrows. Some current flows through the upper bus bar to some other location or power equipment, and some of the current flows into transformer winding 1. The current into winding 1 of the power transformer is the phasor sum (or difference) of the currents in CT1 and CT2 (whether the sum or difference is used, depends on the relative polarity of the CT connections). The same considerations apply to transformer winding 2. The protection elements need access to the net current for the protection of the transformer, but some elements may need access to the individual currents from CT1 and CT2.

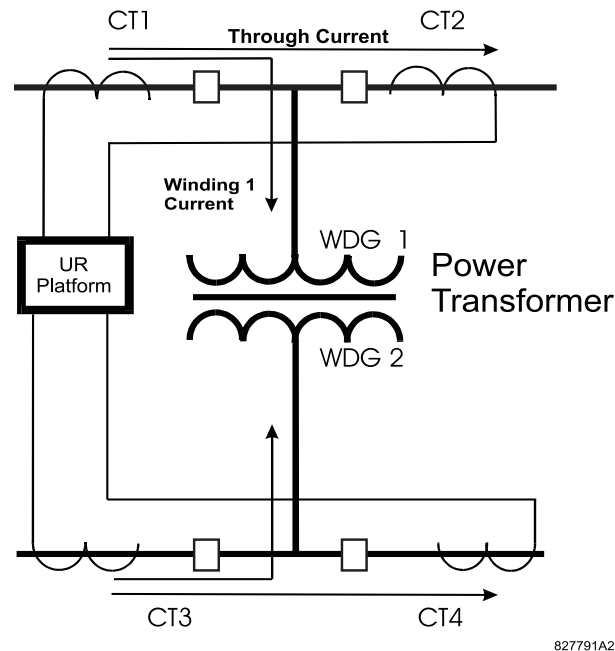


Figure 5-1: BREAKER-AND-A-HALF SCHEME

In conventional analogue or electronic relays, the sum of the currents is obtained from an appropriate external connection of all the CTs through which any portion of the current for the element being protected could flow. Auxiliary CTs are required to perform ratio matching if the ratios of the primary CTs to be summed are not identical. In the UR platform, provisions have been included for all the current signals to be brought to the UR device where grouping, ratio correction and summation are applied internally via configuration settings.

A major advantage of using internal summation is that the individual currents are available to the protection device, as additional information to calculate a restraint current, for example, or to allow the provision of additional protection features that operate on the individual currents such as breaker failure.

Given the flexibility of this approach, it becomes necessary to add configuration settings to the platform to allow the user to select which sets of CT inputs will be added to form the net current into the protected device.

The internal grouping of current and voltage signals forms an internal Source. This Source can be given a specific name through the settings, and becomes available to protection and metering elements in the UR platform. Individual names can be given to each Source to help identify them more clearly for later use. For example, in the scheme shown in the above figure, BREAKER-AND-A-HALF SCHEME, the user would configure one Source to be the sum of CT1 and CT2 and could name this Source as 'Wdg 1 Current'.

Once the Sources have been configured, the user has them available as selections for the choice of input signal for the protection elements and as metered quantities.

b) CT/VT MODULE CONFIGURATIONS

CT and VT input channels are contained in CT/VT modules in UR products. The type of input channel can be phase/neutral/other voltage, phase/ground current, or sensitive ground current. The CT/VT modules calculate total waveform RMS levels, fundamental frequency phasors, symmetrical components and harmonics for voltage or current, as allowed by the hardware in each channel. These modules may calculate other parameters as directed by the CPU module.

A CT/VT module can contain up to eight input channels numbered 1 through 8. The numbering of channels in a CT/VT module corresponds to the module terminal numbering of 1 through 8 and is arranged as follows; channels 1, 2, 3 and 4 are always provided as a group, hereafter called a "bank," and all four are either current or voltage, as are channels 5, 6, 7 and 8. Channels 1, 2, 3 and 5, 6, 7 are arranged as phase A, B and C respectively. Channels 4 and 8 are either another current or voltage.

Banks are ordered sequentially from the block of lower-numbered channels to the block of higher-numbered channels, and from the CT/VT module with the lowest slot position letter to the module with the highest slot position letter, as follows:

Increasing Slot Position Letter -->		
CT/VT MODULE 1	CT/VT MODULE 2	CT/VT MODULE 3
< bank 1 >	< bank 3 >	< bank 5 >
< bank 2 >	< bank 4 >	< bank 6 >

The UR platform allows for a maximum of three sets of three-phase voltages and six sets of three-phase currents. The result of these restrictions leads to the maximum number of CT/VT modules in a chassis to three. The maximum number of Sources is six. A summary of CT/VT module configurations is shown below.

ITEM	MAXIMUM NUMBER
CT/VT Module	3
CT Bank (3 phase channels, 1 ground channel)	6
VT Bank (3 phase channels, 1 auxiliary channel)	3

c) CT/VT INPUT CHANNEL CONFIGURATION SETTINGS

Upon startup of the relay, configuration settings for every bank of current or voltage input channels in the relay are automatically generated, as determined from the order code. Within each bank, a channel identification label is automatically assigned to each bank of channels in a given product. The 'bank' naming convention is based on the physical location of the channels, required by the user to know how to connect the relay to external circuits. Bank identification consists of the letter designation of the slot in which the CT/VT module is mounted as the first character, followed by numbers indicating the channel, either 1 or 5.

For three phase sets of channels, the number of the lowest numbered channel will identify the set. For example, F1 represents the three-phase channel set of F1/F2/F3, where F is the slot letter and 1 is the first channel of the set of three channels.

Upon startup, the CPU configures the settings required to characterize the current and voltage inputs, and will display them in the appropriate section in the sequence of the banks (as described above) as shown below for a maximum configuration:

F1, F5, L1, L5, S1, S5.

The above section explains how the input channels are identified and configured to the specific application instrument transformers and the connections of these transformers. The specific parameters to be used by each measuring element and comparator, and some actual values are controlled by selecting a specific Source. The Source is a group of current and voltage input channels selected by the user to facilitate this selection. With this mechanism, a user does not have to make multiple selections of voltage and current for those elements that need both parameters, such as a distance element or a watt calculation. It also gathers associated parameters for display purposes.

The basic idea of arranging a Source is to select a point on the power system where information is of interest. An application example of the grouping of parameters in a Source is a transformer winding, on which a three phase voltage is measured, and the sum of the currents from CTs on each of two breakers is required to measure the winding current flow.

5.2.1 PASSWORD SECURITY

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ PASSWORD SECURITY

<div> <div>■ PASSWORD</div> <div>■ SECURITY</div> </div>	◀▶	ACCESS LEVEL: Restricted	Range: Restricted, Command, Setting, Factory Service (for factory use only)
	MESSAGE ▲▼	CHANGE COMMAND PASSWORD: No	Range: No, Yes
	MESSAGE ▲▼	CHANGE SETTING PASSWORD: No	Range: No, Yes
	MESSAGE ▲▼	ENCRYPTED COMMAND PASSWORD: -----	Range: 0-9999999999 Note: ----- indicates no password
	MESSAGE ▲	ENCRYPTED SETTING PASSWORD: -----	Range: 0-9999999999 Note: ----- indicates no password

There are two user levels of password security in the relay; Command and Setting. Operations under the supervision of the passwords are:

COMMAND:

- Operating the breakers via faceplate pushbuttons
- Changing the state of virtual inputs,
- Clearing the event records,
- Clearing the oscillography records.

SETTING:

- Changing any setting.

When the relay is shipped from the factory, the Command and Setting passwords are defaulted to 'Null'. When a password is 'Null', the password security feature is disabled.

Programming a password code is required to enable each access level. A password consists of 1 to 10 numerical characters. When a 'CHANGE ... PASSWORD' message is set to 'Yes', the following message sequence is invoked:

1. ENTER NEW PASSWORD: _____
2. VERIFY NEW PASSWORD: _____
3. NEW PASSWORD HAS BEEN STORED

To gain write access to a 'Restricted' setting, select the ACCESS LEVEL 'Setting' value and then change the setting, or attempt to change the setting, and follow the prompt to enter the programmed password. If the password is correctly entered, access will be allowed. If no keys are pressed for longer than 30 minutes or control power is cycled, accessibility will automatically revert to the 'Restricted' level.

If an entered password is lost (or forgotten), consult the factory service department with the corresponding Encrypted Password number from the PASSWORD SECURITY menu.



NOTE

If the Setting password and Command password are set the same, the one password will allow access to commands and settings.

5.2.2 DISPLAY PROPERTIES

PATH: SETTINGS ↴ PRODUCT SETUP ⇨ ↴ DISPLAY PROPERTIES

■ DISPLAY

■ PROPERTIES

⏮

⏭

FLASH MESSAGE

TIME: 1.0 s

Range: 0.5 to 10.0 in steps of 0.1

MESSAGE

⏮

⏭

DEFAULT MESSAGE

TIMEOUT: 300 s

Range: 10 to 900 in steps of 1

MESSAGE

⏮

⏭

DEFAULT MESSAGE

INTENSITY: 25 %

Range: 25 %, 50 %, 75 %, 100 %

Some of the relay messaging characteristics can be modified to suit different situations using the display properties settings.

Flash messages are status, warning, error, or information messages displayed for several seconds in response to certain key presses during setting programming. These messages override any normal messages. The time a flash message remains on the display can be changed to accommodate different reading rates.

If no keys are pressed for a period of time, the relay will automatically display a default message. This time can be modified to ensure messages remain on the screen long enough during programming or reading of actual values.

To extend the life of the phosphor in the vacuum fluorescent display, the brightness of the display can be attenuated when default messages are being displayed. When interacting with the display using the faceplate keys, the display will always operate at full brightness.

5.2.3 COMMUNICATIONS

PATH: SETTINGS ↓ PRODUCT SETUP ⇨ ↓ COMMUNICATIONS

<div> <div>■ COMMUNICATIONS</div> <div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> </div> </div>		<div> <div>◀▶</div> <div> <div>■ SERIAL PORTS</div> <div>■ NETWORK</div> <div>■ MODBUS PROTOCOL</div> <div>■ DNP PROTOCOL</div> <div>■ UCA/MMS PROTOCOL</div> <div>■ WEB SERVER</div> <div>■ HTTP PROTOCOL</div> <div>■ TFTP PROTOCOL</div> </div> </div>	
<div> <div>■ SERIAL PORTS</div> <div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> </div> </div>		<div> <div>◀▶</div> <div> <div>RS485 COM1 BAUD RATE: 19200</div> <div>RS485 COM1 PARITY: None</div> <div>RS485 COM1 RESPONSE MIN TIME: 0 ms</div> <div>RS485 COM2 BAUD RATE: 19200</div> <div>RS485 COM2 PARITY: None</div> <div>RS485 COM2 RESPONSE MIN TIME: 0 ms</div> </div> </div>	<div>Range: 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200; Only active if CPU type 9A is ordered</div> <div>Range: None, Odd, Even Only active if CPU type 9A is ordered</div> <div>Range: 0 to 1000 in steps of 10 Only active if CPU type 9A is ordered</div> <div>Range: 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200</div> <div>Range: None, Odd, Even</div> <div>Range: 0 to 1000 in steps of 10 Only active if CPU type 9A is ordered</div>
<div> <div>■ NETWORK</div> <div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> </div> </div>		<div> <div>◀▶</div> <div> <div>IP ADDRESS: 0.0.0.0</div> <div>SUBNET IP MASK: 0.0.0.0</div> <div>GATEWAY IP ADDRESS: 0.0.0.0</div> <div>■ OSI NETWORK ADDRESS (NSAP)</div> <div>ETHERNET PRI LINK MONITOR: Disabled</div> <div>ETHERNET SEC LINK MONITOR: Disabled</div> </div> </div>	<div>Only active if CPU type 9C or 9D is ordered</div> <div>Only active if CPU type 9C or 9D is ordered</div> <div>Only active if CPU type 9C or 9D is ordered</div> <div>Note: Click the 'MESSAGE ⇨' key to enter address. Only active if CPU type 9C or 9D is ordered</div> <div>Range: Disabled, Enabled Only active if CPU type 9C or 9D is ordered</div> <div>Range: Disabled, Enabled Only active if CPU type 9C or 9D is ordered</div>

<div>■ MODBUS PROTOCOL</div>	<div>◀▶</div>	<div>MODBUS SLAVE ADDRESS: 254</div>	Range: 1 to 254 in steps of 1
<div>MESSAGE</div>	<div>▲</div>	<div>MODBUS IP PORT NUMBER: 502</div>	Range: 1 to 65535 in steps of 1
<div>■ DNP PROTOCOL</div>	<div>◀▶</div>	<div>DNP PORT: NONE</div>	Range: NONE, COM1 - RS485, COM2 - RS485, FRONT PANEL - RS232, NETWORK
<div>MESSAGE</div>	<div>▲▼</div>	<div>DNP ADDRESS: 255</div>	Range: 0 to 65534 in steps of 1
<div>MESSAGE</div>	<div>▲▼</div>	<div>■ DNP NETWORK ■ CLIENT ADDRESSES</div>	Note: Click the 'MESSAGE ⇌' key to enter addresses.
<div>MESSAGE</div>	<div>▲▼</div>	<div>DNP IP PORT NUMBER: 20000</div>	Range: 1 to 65535 in steps of 1
<div>MESSAGE</div>	<div>▲▼</div>	<div>DNP UNSOL RESPONSE FUNCTION: Disabled</div>	Range: Enabled, Disabled
<div>MESSAGE</div>	<div>▲▼</div>	<div>DNP UNSOL RESPONSE TIMEOUT: 0 s</div>	Range: 0 to 60 sec. in steps of 1
<div>MESSAGE</div>	<div>▲▼</div>	<div>DNP UNSOL RESPONSE MAX RETRIES: 10</div>	Range: 1 to 255 in steps of 1
<div>MESSAGE</div>	<div>▲▼</div>	<div>DNP UNSOL RESPONSE DEST ADDRESS: 1</div>	Range: 0 to 65519 in steps of 1
<div>MESSAGE</div>	<div>▲</div>	<div>USER MAP FOR DNP ANALOGS: Disabled</div>	Range: Enabled, Disabled
<div>■ UCA/MMS PROTOCOL</div>	<div>◀▶</div>	<div>DEFAULT GOOSE UPDATE TIME: 60 s</div>	Range: 1 to 60 in steps of 1 second (see Section: REMOTE OUTPUTS UserSt BIT PAIRS)
<div>MESSAGE</div>	<div>▲▼</div>	<div>UCA LOGICAL DEVICE: UCADevice</div>	Range: Name of UCA logical device Up to 16 alphanumeric characters
<div>MESSAGE</div>	<div>▲</div>	<div>UCA/MMS IP PORT NUMBER: 102</div>	Range: 1 to 65535 in steps of 1
<div>■ WEB SERVER ■ HTTP PROTOCOL</div>	<div>◀▶</div>	<div>HTTP IP PORT NUMBER: 80</div>	Range: 1 to 65535 in steps of 1
<div>■ TFTP PROTOCOL</div>	<div>◀▶</div>	<div>TFTP MAIN IP PORT NUMBER: 69</div>	Range: 1 to 65535 in steps of 1
<div>MESSAGE</div>	<div>▲▼</div>	<div>TFTP DATA IP PORT 1 NUMBER: 0</div>	Range: 0 to 65535 in steps of 1
<div>MESSAGE</div>	<div>▲</div>	<div>TFTP DATA IP PORT 2 NUMBER: 0</div>	Range: 0 to 65535 in steps of 1

The relay is equipped with up to 3 independent serial ports. The faceplate **RS232** port is intended for local use and will respond regardless of the slave address programmed. The rear COM1 port type will depend on the CPU type ordered - it may be either an Ethernet port or an RS485 port. The rear COM2 port is RS485.

The **RS232** port may be connected to a personal computer running URPC. Its baud rate is fixed at **19200** and parity is fixed as '**None**'. The software may be used for downloading or uploading setting files, viewing measured parameters, and upgrading the relay firmware to the latest revision.

For **RS485** communications (supporting a subset of the **Modbus® RTU Protocol**), each relay must have a unique address from 1 to 254. Address 0 is the broadcast address which all relays listen to. Addresses do not have to be sequential, but no two relays can have the same address or conflicts resulting in errors will occur. Generally, each relay added to the link will use the next higher address starting at 1. A maximum of 32 relays can be daisy-chained and connected to a DCS, PLC or PC using the RS485 ports.



For each RS485 port, the minimum time before the port will transmit after receiving data from a host can be set. This feature allows operation with hosts which hold the RS485 transmitter active for some time after each transmission.

The IP address setting messages will only appear if a relay is ordered with an **Ethernet** card. The Ethernet PRI & SEC Link Monitor settings refer to the Primary & Secondary Fibre Channel link monitors. The IP addresses are used with DNP/Network, Modbus/TCP/IP and MMS/UCIA2 protocols. The NSAP address is used with MMS/UCIA2 protocol over the OSI(CLN/TP4) stack only.

Each TCP/IP protocol has a setting for the **IP PORT NUMBER**. These settings are only used in advanced network configurations. They should normally be left at their default values, but may be changed if required; for example, to allow access to multiple URs behind a router. By setting a different IP port number for a given protocol on each UR, the router can map the URs to the same external IP address. The client software (URPC, for example) must be configured to use the correct port number if these settings are used.



Do not set more than one protocol to use the same IP Port Number, as this will result in unreliable operation of those protocols.



When the NSAP address, any IP Port Number, or any User Map setting (when used with DNP) is changed, it will not become active until power to the relay has been cycled (OFF - ON).

DNP PROTOCOL:

The **DNP PORT** setting is used to select the communications port assigned to the DNP protocol. DNP can be assigned to a single port. Once DNP is assigned to a serial port, the Modbus protocol is disabled on that port. Note that COM1 can be used only in non-Ethernet UR relays.

The **DNP ADDRESS** setting is the DNP slave address. This number identifies the UR on a DNP communications link. Each DNP slave on a communications link should be assigned a unique address.

The **DNP NETWORK CLIENT ADDRESS** settings can be used to force the UR to respond only to specific DNP masters.

The **DNP UNSOL RESPONSE TIMEOUT** setting sets the time that the relay waits for a DNP master to confirm an unsolicited response.

The **DNP UNSOL RESPONSE FUNCTION** setting should be set to "Disabled" for RS485 applications since there is no collision avoidance mechanism.

The **DNP UNSOL RESPONSE DEST ADDRESS** setting is the DNP address to which all unsolicited responses are sent. The IP address to which unsolicited responses are sent is determined from either the current DNP TCP connection or the most recent UDP message.

The **DNP UNSOL RESPONSE MAX RETRIES** setting determines the number of times the relay will retransmit an unsolicited response without receiving a confirmation from the master. A value of 255 allows infinite re-tries. See Appendix E for a description of the **USER MAP FOR DNP ANALOGS** setting.

5.2.4 MODBUS USER MAP

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ MODBUS USER MAP

MODBUS USER MAP

ADDRESS 1 :

0

VALUE:

0

Range: 0 to 65535 in steps of 1

↓

MESSAGE

ADDRESS 256 :

0

VALUE:

0

Range: 0 to 65535 in steps of 1

The Modbus® User Map provides up to 256 REGISTERS with read only access.

To obtain a value for a memory map address at a specific location, enter the desired location in the **ADDRESS** line (value must be converted from hex to decimal format). The corresponding value from the Modbus® Memory Map will be displayed in the **VALUE** line. A value of “0” in subsequent register **ADDRESS** lines will automatically return a value for the previous **ADDRESS** line incremented by “1”. An address value of “0” in the initial register means “none” and values of “0” will be displayed for all registers.

Different **ADDRESS** values can be entered as required in any of the register positions.



These settings can also be used with the DNP protocol. See the DNP ANALOG INPUT POINTS section in Appendix E for details.

NOTE

5.2.5 REAL TIME CLOCK

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ REAL TIME CLOCK

REAL TIME

CLOCK

IRIG-B SIGNAL TYPE:

None

Range: None, DC Shift, Amplitude Modulated

The date and time for the relay clock can be synchronized to other relays using an IRIG-B signal. It has the same accuracy as an electronic watch, approximately ± 1 minute per month.

An IRIG-B signal may be connected to the relay to synchronize the clock to a known time base and to other relays. If an IRIG-B signal is used, only the current year needs to be entered.

If the relay serial communication link is used, then all the relays can keep time in synchronization with each other. A new clock time is loaded into the relay via the communications port by a remote computer broadcast (address 0) for all the relays connected on the communications channel. Then all relays in the system begin timing at approximately the same instant (\pm a few milliseconds).

See also the **COMMANDS ↓ SET DATE AND TIME** menu for manually setting the relay clock.

5.2.6 FAULT REPORT

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ ↓ FAULT REPORT

<div>■ FAULT REPORT</div> <div>■</div>	<div>◀▶</div>	<div>FAULT REPORT</div> <div>SOURCE: SRC 1</div>	Range: SRC 1, ..., SRC 6
MESSAGE	▲	<div>FAULT REPORT TRIG:</div> <div>Off</div>	Range: FlexLogic™ Operand

The fault report stores data, in non-volatile memory, pertinent to an event when triggered. The captured data will include:

- Name of the relay, programmed by the user
- Date and time of trigger
- Name of trigger (specific operand)
- Active setting group
- Pre-fault current and voltage phasors (one-quarter cycle before the trigger)
- Fault current and voltage phasors (three-quarter cycle after the trigger)
- Target Messages that are set at the time of triggering
- Events (8 before trigger and 8 after trigger).

If the relay is equipped with a fault locator, the captured data will also include the fault type and the distance to the fault location. If the relay is equipped with a recloser, the captured data will include the reclose shot number.

The trigger can be any FlexLogic™ operand, but in most applications it is expected to be the same operand, usually a virtual output, that is used to drive an output relay to trip a breaker. The disturbance detector should not be used to trigger a fault report, to eliminate over-writing fault events.

Each fault report is stored as a file; the relay capacity is ten files. An eleventh trigger will over-write the oldest file. The operand selected as the fault report trigger will automatically trigger an oscillography record, which can also be triggered independently.

URPC is required to view all captured data.

The relay faceplate display can be used to view:

- Date and time of trigger
- Fault type (where applicable)
- Distance location of fault (where applicable)
- Reclose shot number (where applicable)

The **FAULT REPORT SOURCE** setting is used to select the Source for input currents and voltages and disturbance detection.

The **FAULT REPORT TRIG** setting is used to assign the FlexLogic™ operand representing the protection element/elements requiring operational fault location calculations. The calculations of the distance to fault are initiated by this signal.

See also SETTINGS \ SYSTEM SETUP \ LINE menu for specifying line characteristics.

See also ACTUAL VALUES \ RECORDS \ FAULT REPORTS section.

5.2.7 OSCILLOGRAPHY

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ OSCILLOGRAPHY

<div>■ OSCILLOGRAPHY</div> <div>■</div>		NUMBER OF RECORDS:	15	Range: 1 to 64 in steps of 1	
	MESSAGE	▲▼	TRIGGER MODE:	Automatic Overwrite	Range: Automatic Overwrite, Protected
	MESSAGE	▲▼	TRIGGER POSITION:	50%	Range: 0 to 100 in steps of 1
	MESSAGE	▲▼	TRIGGER SOURCE:	Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	AC INPUT WAVEFORMS:	16 samples/cycle	Range: Off, 8 samples/cycle, 16 samples/cycle, 32 samples/cycle, 64 samples/cycle
	MESSAGE	▲▼	■ DIGITAL CHANNELS	■	(1 to 64 channels)
	MESSAGE	▲	■ ANALOG CHANNELS	■	(1 to 16 channels)

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ OSCILLOGRAPHY ⇒ DIGITAL CHANNELS

<div>■ DIGITAL CHANNELS</div> <div>■</div>		DIGITAL CHANNEL 2:	Off	Range: FlexLogic™ Operand
	MESSAGE	▲	DIGITAL CHANNEL 63:	Off

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ OSCILLOGRAPHY ⇒ ANALOG CHANNELS

<div>■ ANALOG CHANNELS</div> <div>■</div>		ANALOG CHANNEL 1:	Off	Range: Off, any analog Actual Value parameter
	MESSAGE	▲	ANALOG CHANNEL 16:	Off

Oscillography records contain waveforms captured at the sampling rate as well as other relay data at the point of trigger. Oscillography records are triggered by a programmable FlexLogic™ operand. Multiple oscillography records may be captured simultaneously.

The **NUMBER OF RECORDS** is selectable, but the number of cycles captured in a single record varies considerably based on other factors such as sample rate and the number of operational CT/VT modules. There is a fixed amount of data storage for oscillography; the more data captured, the less the number of cycles captured

per record. See the **ACTUAL VALUES \ RECORDS \ OSCILLOGRAPHY** menu to view the number of cycles captured per record. The following table provides sample configurations with corresponding cycles/record.

Table 5-1: OSCILLOGRAPHY CYCLES/RECORD EXAMPLE

# RECORDS	# CT/VTs	SAMPLE RATE	# DIGITALS	# ANALOGS	CYCLES/RECORD
1	1	8	0	0	1872.0
1	1	16	16	0	1685.0
8	1	16	16	0	266.0
8	1	16	16	4	219.5
8	2	16	16	4	93.5
8	2	16	64	16	93.5
8	2	32	64	16	57.6
8	2	64	64	16	32.3
32	2	64	64	16	9.5

A new record may automatically overwrite an older record if **TRIGGER MODE** is set to 'Automatic Overwrite'.

The **TRIGGER POSITION** is programmable as a percent of the total buffer size (e.g. 10%, 50%, 75%, etc.). A trigger position of 25% consists of 25% pre- and 75% post- trigger data.

The **TRIGGER SOURCE** is always captured in oscillography and may be any FlexLogic™ parameter (element state, contact input, virtual output, etc.). The relay sampling rate is 64 samples per cycle.

The **AC INPUT WAVEFORMS** setting determines the sampling rate at which AC input signals (i.e. current and voltage) are stored. Reducing the sampling rate allows longer records to be stored. This setting has no effect on the internal sampling rate of the relay which is always 64 samples per cycle, i.e. it has no effect on the fundamental calculations of the device.

An **ANALOG CHANNEL** setting selects the metering actual value recorded in an oscillography trace. The length of each oscillography trace depends in part on the number of parameters selected here. Parameters set to 'Off' are ignored. The parameters available in a given relay are dependent on: (a) the type of relay, (b) the type and number of CT/VT hardware modules installed, and (c) the type and number of Analog Input hardware modules installed. Upon startup, the relay will automatically prepare the parameter list. Tables of all possible analog metering actual value parameters are presented in Appendix A: FLEXANALOG PARAMETERS. The parameter index number shown in any of the tables is used to expedite the selection of the parameter on the relay display. It can be quite time-consuming to scan through the list of parameters via the relay keypad/display - entering this number via the relay keypad will cause the corresponding parameter to be displayed.

All eight channels per CT/VT module are stored in the oscillography file. The CT/VT module analog channels are named '<slot letter><terminal number>-<I or V><phase A, B, or C; or 4th input>'. The fourth current input in a bank is called IG, and the fourth voltage input in a bank is called VX. For example, F2-IB designates the IB signal on terminal 2 of the CT/VT module in slot F.

If there are no CT/VT modules and Analog Input modules, no analog traces will appear in the file; only the digital traces will appear.



When the NUMBER OF RECORDS setting is altered, all oscillography records will be CLEARED.

5.2.8 DATA LOGGER

PATH: SETTINGS ↓ PRODUCT SETUP ⇨ DATA LOGGER

■ DATA LOGGER	◀▶	DATA LOGGER RATE:	Range: 1 sec; 1 min, 5 min, 10 min, 15 min, 20 min, 30 min, 60 min
	▲▼	DATA LOGGER CHNL 1:	Range: Off, any analog Actual Value parameter
MESSAGE		Off	
	▲▼	DATA LOGGER CHNL 2:	Range: Off, any analog Actual Value parameter
MESSAGE		Off	
		↓	
	▲▼	DATA LOGGER CHNL 16:	Range: Off, any analog Actual Value parameter
MESSAGE		Off	
	▲	DATA LOGGER CONFIG:	Range: Not applicable - shows computed data only
MESSAGE		0 CHNL x 0.0 DAYS	

The data logger is used to sample and record up to sixteen analog parameters at a sampling rate that is defined by the user. This recorded data may be downloaded to the URPC software where it is displayed with 'parameters' on the vertical axis and 'time' on the horizontal axis. All data is stored in non-volatile memory which means that the information is retained when power to the relay is lost.

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For a fixed sampling rate, the data logger can be configured with a few channels over a long period or a larger number of channels for a shorter period. The relay will automatically partition the available memory between the channels that are in use.



Changing any setting affecting Data Logger operation will clear any data that is currently in the log.

NOTE

a) SETTINGS

DATA LOGGER RATE:

This setting selects the time interval at which the actual value data will be recorded.

DATA LOGGER CHNL 1(16):

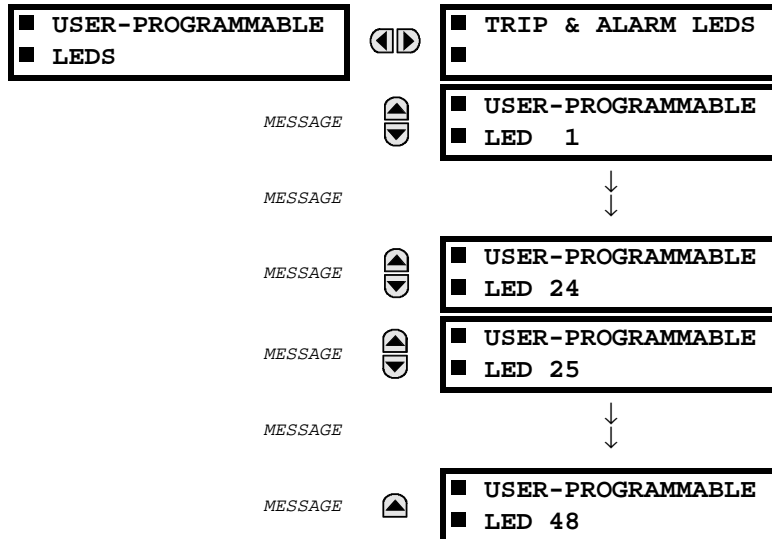
This setting selects the metering actual value that is to be recorded in channel 1(16) of the data log. The parameters available in a given relay are dependent on: (a) the type of relay, (b) the type and number of CT/VT hardware modules installed, and (c) the type and number of Analog Input hardware modules installed. Upon startup, the relay will automatically prepare the parameter list. Tables of all possible analog metering actual value parameters are presented in Appendix A: FLEXANALOG PARAMETERS. The parameter index number shown in any of the tables is used to expedite the selection of the parameter on the relay display. It can be quite time-consuming to scan through the list of parameters via the relay keypad/display – entering this number via the relay keypad will cause the corresponding parameter to be displayed.

DATA LOGGER CONFIG:

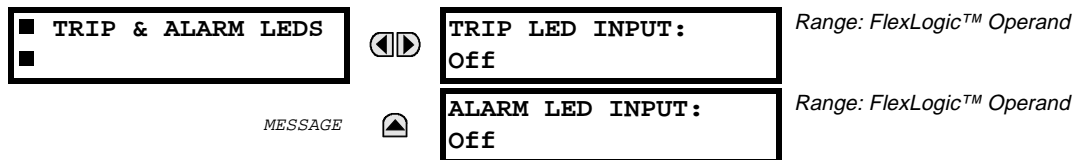
This display presents the total amount of time the Data Logger can record the channels not selected to "Off" without over-writing old data.

5.2.9 USER-PROGRAMMABLE LEDS

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ USER-PROGRAMMABLE LEDS

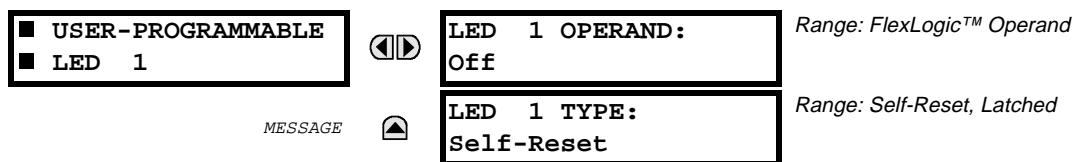


PATH: SETTINGS ↓ PRODUCT SETUP ⇒ USER-PROGRAMMABLE LEDS ⇒ TRIP & ALARM LEDS



The TRIP and ALARM LEDs are on the faceplate LED panel 1. Each of these indicators can be programmed to become illuminated when the selected FlexLogic™ operand is in the logic 1 state.

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ USER-PROGRAMMABLE LEDS ⇒ USER PROGRAMABLE LED 1(48)



There are 48 amber LEDs across 2 relay faceplate LED panels. Each of these indicators can be programmed to become illuminated when the selected FlexLogic™ operand is in the logic 1 state.

LEDs 1 through 24 inclusive are on LED panel 2.

LEDs 25 through 48 inclusive are on LED panel 3.

Refer to Chapter 4 on Human Interfaces (LED INDICATORS section) for the locations of these indexed LEDs.

This menu is used to individually select the operands that control these LEDs. Support for applying user-customized labels to these LEDs is provided - see the LED INDICATORS section for details.

If the LED TYPE setting is 'Self-Reset' (default setting), the LED illumination will track the state of the selected LED operand. If the LED TYPE setting is 'Latched', the LED, once lit, will remain lit until reset by a command from the faceplate RESET pushbutton, from a remote device via a communications channel, or from any programmed operand, even if the LED operand state de-asserts.

a) FACTORY PRESET LED PANEL SETTINGS

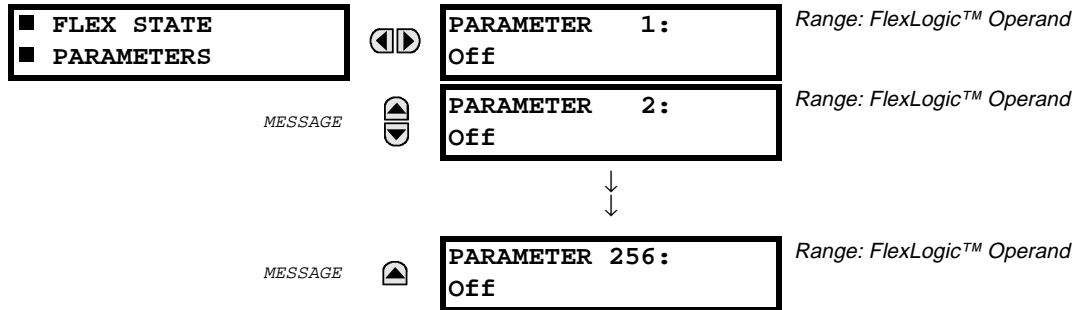
Table 5–2: FACTORY PRESET LED PANEL SETTINGS

SETTING	PARAMETER	SETTING	PARAMETER
LED 1 Operand	SETTING GROUP ACT 1	LED 25 Operand	Virt Op 6 On
LED 2 Operand	SETTING GROUP ACT 2	LED 26 Operand	Off
LED 3 Operand	SETTING GROUP ACT 3	LED 27 Operand	Off
LED 4 Operand	SETTING GROUP ACT 4	LED 28 Operand	Off
LED 5 Operand	SETTING GROUP ACT 5	LED 29 Operand	Off
LED 6 Operand	SETTING GROUP ACT 6	LED 30 Operand	Off
LED 7 Operand	SETTING GROUP ACT 7	LED 31 Operand	Virt Op 1 On
LED 8 Operand	SETTING GROUP ACT 8	LED 32 Operand	Virt Op 2 On
LED 9 Operand	BREAKER 1 OPEN	LED 33 Operand	Virt Op 3 On
LED 10 Operand	BREAKER 1 CLOSED	LED 34 Operand	Virt Op 4 On
LED 11 Operand	BREAKER 1 TROUBLE	LED 35 Operand	Virt Op 5 On
LED 12 Operand	Off	LED 36 Operand	Off
LED 13 Operand	Off	LED 37 Operand	Off
LED 14 Operand	BREAKER 2 OPEN	LED 38 Operand	Off
LED 15 Operand	BREAKER 2 CLOSED	LED 39 Operand	Off
LED 16 Operand	BREAKER 2 TROUBLE	LED 40 Operand	Off
LED 17 Operand	SYNC 1 SYNC OP	LED 41 Operands	Off
LED 18 Operand	SYNC 2 SYNC OP	LED 42 Operand	Off
LED 19 Operand	Off	LED 43 Operand	Off
LED 20 Operand	Off	LED 44 Operand	Off
LED 21 Operand	AR 1 ENABLED	LED 45 Operand	Off
LED 22 Operand	AR 1 DISABLED	LED 46 Operand	Off
LED 23 Operand	AR 1 RIP	LED 47 Operand	Off
LED 24 Operand	AR 1 LO	LED 48 Operand	Off

Refer to the FLEXLOGIC™ EQUATION EDITOR section for the FlexLogic™ equations that define these “Virt Op” (Virtual Output) parameters.

5.2.10 FLEX STATE PARAMETERS

PATH: SETTINGS ↓ PRODUCT SETUP ⇒ ↓ FLEX STATE PARAMETERS



This feature provides a mechanism where any of 256 selected FlexLogic™ operand states can be used for efficient monitoring. The feature allows user-customized access to the FlexLogic™ operand states in the relay. The state bits are packed so that 16 states may be read out in a single Modbus register. The state bits can be configured so that all of the states which are of interest to the user are available in a minimum number of Modbus registers.

The state bits may be read out in the "Flex States" register array beginning at Modbus address 900 hex. 16 states are packed into each register, with the lowest-numbered state in the lowest-order bit. There are 16 registers in total to accommodate the 256 state bits.

5.2.11 USER-DEFINABLE DISPLAYS

PATH: SETTINGS ↓ PRODUCT SETUP ⇨ USER-DEFINABLE DISPLAYS

■ USER-DEFINABLE ■ DISPLAYS	◀▶	■ USER DISPLAY 1 ■
MESSAGE	▲▼	■ USER DISPLAY 2 ■
MESSAGE	▲▼	■ USER DISPLAY 3 ■
MESSAGE	▲▼	■ USER DISPLAY 4 ■
MESSAGE	▲▼	■ USER DISPLAY 5 ■
MESSAGE	▲▼	■ USER DISPLAY 6 ■
MESSAGE	▲▼	■ USER DISPLAY 7 ■
MESSAGE	▲	■ USER DISPLAY 8 ■

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This menu provides a mechanism for manually creating up to 8 user-defined information displays in a convenient viewing sequence in the USER DISPLAYS menu (between the TARGETS and ACTUAL VALUES top-level menus). The sub-menus facilitate text entry and Modbus Register data pointer options for defining the User Display content.

Also, any existing system display can be automatically copied into an available User Display by selecting the existing display and pressing the **ENTER** key. The display will then prompt “ADD TO USER DISPLAY LIST?”. After selecting ‘Yes’, a message will indicate that the selected display has been added to the user display list. When this type of entry occurs, the sub-menus are automatically configured with the proper content - this content may subsequently be edited.







PATH: SETTINGS ↓ PRODUCT SETUP ⇨ USER-DEFINABLE DISPLAYS ⇨ USER DISPLAY 1(8)


■ USER DISPLAY 1 ■	◀▶	DISP 1 TOP LINE:	Range: up to 20 alphanumeric characters
MESSAGE	▲▼	DISP 1 BOTTOM LINE:	Range: up to 20 alphanumeric characters
MESSAGE	▲▼	DISP 1 ITEM 1: 0	Range: 0 to 65535 in steps of 1
MESSAGE	▲▼	DISP 1 ITEM 2: 0	Range: 0 to 65535 in steps of 1
MESSAGE	▲▼	DISP 1 ITEM 3: 0	Range: 0 to 65535 in steps of 1
MESSAGE	▲▼	DISP 1 ITEM 4: 0	Range: 0 to 65535 in steps of 1
MESSAGE	▲	DISP 1 ITEM 5: 0	Range: 0 to 65535 in steps of 1




This menu is used **to enter** user-defined text and/or user-selected Modbus-registered data fields into the particular User Display. Each User Display consists of two 20-character lines (TOP & BOTTOM). The Tilde (~) character is used to mark the start of a data field - the length of the data field needs to be accounted for. Up to 5 separate data fields (ITEM 1...5) can be entered in a User Display - the nth Tilde (~) refers to the nth ITEM.

A User Display may be entered from the faceplate keypad or the URPC interface (preferred for convenience).

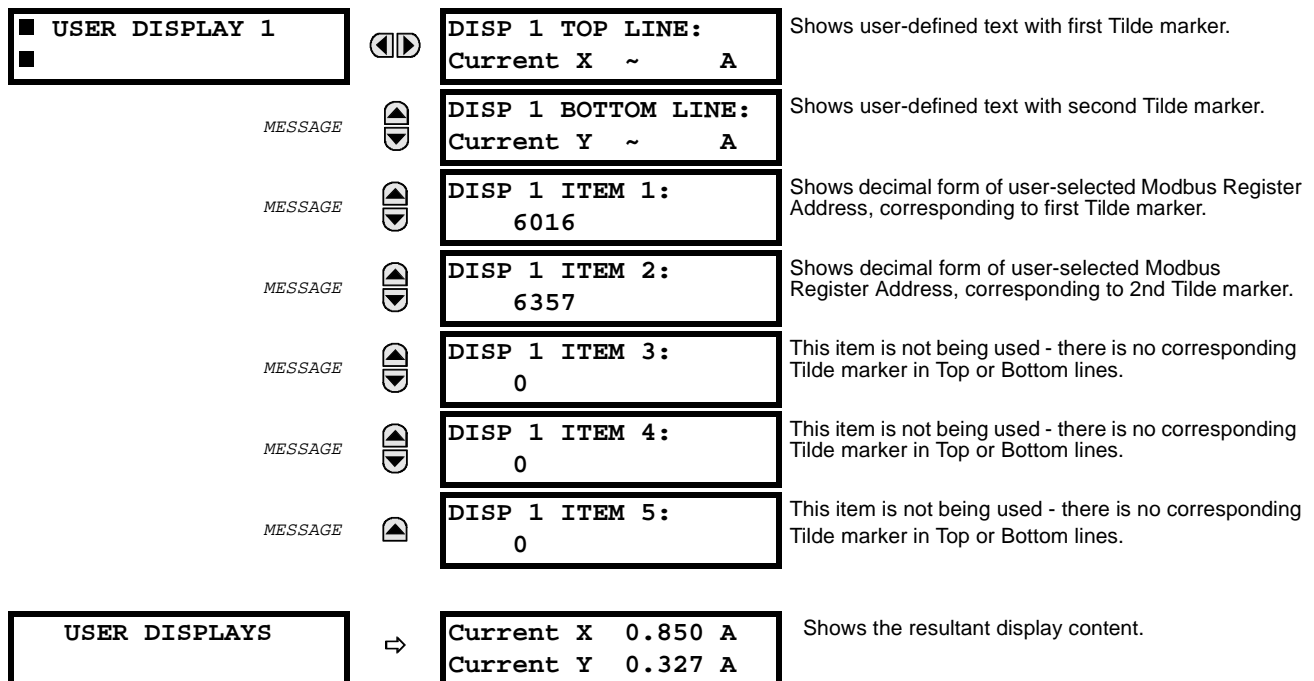
To enter text characters in the TOP LINE and BOTTOM LINE from the faceplate keypad:

1. Select the line to be edited.
2. Press the  key to enter text edit mode.
3. Use either  VALUE  key to scroll through the characters. A space is selected like a character.
4. Press the  key to advance the cursor to the next position.
5. Repeat step 3 and continue entering characters until the desired text is displayed.
6. The  key may be pressed at any time for context sensitive help information.
7. Press the  key to store the new settings.

To enter a numerical value for any of the 5 ITEMS (the decimal form of the selected Modbus Register Address) from the faceplate keypad, use the number keypad. Use the value of '0' for any ITEMS not being used. Use the  key at any selected system display (Setting, Actual Value, or Command) which has a Modbus address, to view the hexadecimal form of the Modbus Register Address, then manually convert it to decimal form before entering it (URPC usage would conveniently facilitate this conversion).

Using the  key, go to the USER DISPLAYS menu **to view** the user-defined content. The current User Displays will show in sequence, changing to the next display every 4 seconds. While viewing a User Display, press the  key and then select the "Yes" option **to remove** the display from the user display list. Use the  key again **to exit** the USER DISPLAYS menu.

a) EXAMPLE USER DISPLAY SETUP & RESULT



5.2.12 INSTALLATION

PATH: SETTINGS ↓ PRODUCT SETUP ⇨ ↓ INSTALLATION

<div>■ INSTALLATION</div> <div>■</div>	<div>◀▶</div> <div>MESSAGE ▲</div>	<div>RELAY SETTINGS:</div> <div>Not Programmed</div>	Range: Not Programmed, Programmed
		<div>RELAY NAME:</div> <div>Relay-1</div>	Range: up to 20 alphanumeric characters

To safeguard against the installation of a relay whose settings have not been entered, the unit will not allow signaling of any output relay until **RELAY SETTINGS** is set to "Programmed". This setting is defaulted to "Not Programmed" when the relay leaves the factory. The UNIT NOT PROGRAMMED self-test error message is displayed automatically until the relay is put into the Programmed state.

The **RELAY NAME** setting allows the user to uniquely identify a relay. This name will appear on generated reports. This name is also used to identify specific devices which are engaged in automatically sending/receiving data over the Ethernet communications channel using the MMS/UCI2 protocol.

5.3.1 AC INPUTS

a) CURRENT BANKS

PATH: SETTINGS ↓ SYSTEM SETUP ⇒ AC INPUTS ⇒ CURRENT BANK X1

<div>■ CURRENT BANK X1</div> <div>■</div>	◀▶	<div>PHASE CT X1</div> <div>PRIMARY: 1 A</div>	Range: 1 to 65000 in steps of 1 A
	MESSAGE ▲▼	<div>PHASE CT X1</div> <div>SECONDARY: 1 A</div>	Range: 1 A, 5 A
	MESSAGE ▲▼	<div>GROUND CT X1</div> <div>PRIMARY: 1 A</div>	Range: 1 to 65000 in steps of 1 A
	MESSAGE ▲▼	<div>GROUND CT X1</div> <div>SECONDARY: 1 A</div>	Range: 1 A, 5 A

'X' = F, L, or S. 'F', 'L', and 'S' are module slot position letters. See also the section INTRODUCTION TO AC SOURCES.

Up to 6 banks of phase/ground CTs can be set.

These settings are critical for all features that have settings dependent on current measurements. When the relay is ordered, the CT module must be specified to include a standard or sensitive ground input. As the phase CTs are connected in Wye (star), the calculated phasor sum of the three phase currents ($I_A + I_B + I_C = \text{Neutral Current} = 3I_o$) is used as the input for the neutral overcurrent elements. In addition, a zero sequence (core balance) CT which senses current in all of the circuit primary conductors, or a CT in a neutral grounding conductor may also be used. For this configuration, the ground CT primary rating must be entered. To detect low level ground fault currents, the sensitive ground input may be used. In this case, the sensitive ground CT primary rating must be entered. For more details on CT connections, refer to the HARDWARE chapter.

Enter the rated CT primary current values. For both 1000:5 and 1000:1 CTs, the entry would be 1000. For correct operation, the CT secondary rating must match the setting (which must also correspond to the specific CT connections used).

If CT inputs (banks of current) are to be summed as one source current, the following rule applies:

EXAMPLE:

$$\text{SRC1} = F1 + F5 + U1$$

Where *F1*, *F5*, and *U1* are banks of CTs with ratios of 500:1, 1000:1 and 800:1 respectively.

1 pu is the highest primary current. In this case, 1000 is entered and the secondary current from the 500:1 and 800:1 ratio CTs will be adjusted to that which would be created by a 1000:1 CT before summation. If a protection element is set up to act on SRC1 currents, then PKP level of 1 pu will operate on 1000 A primary.

The same rule will apply for sums of currents from CTs with different secondary taps (5 A and 1 A).

b) VOLTAGE BANKS

PATH: SETTINGS ↴ SYSTEM SETUP ⇒ AC INPUTS ⇒ VOLTAGE BANK X1

<div>VOLTAGE BANK X5</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div>	<div>PHASE VT X5 CONNECTION: Wye</div>	Range: Wye, Delta
	<div>PHASE VT X5 SECONDARY: 66.4 V</div>	Range: 50.0 to 240.0 in steps of 0.1
	<div>PHASE VT X5 RATIO: 1.00 :1</div>	Range: 1.00 to 24000.00 in steps of 1.00
	<div>AUXILIARY VT X5 CONNECTION: Vag</div>	Range: Vn, Vag, Vbg, Vcg, Vab, Vbc, Vca
	<div>AUXILIARY VT X5 SECONDARY: 66.4 V</div>	Range: 50.0 to 240.0 in steps of 0.1
	<div>AUXILIARY VT X5 RATIO: 1.00 :1</div>	Range: 1.00 to 24000.00 in steps of 1.00

'X' = F, L, or S. 'F', 'L', and 'S' are module slot position letters. See also the section INTRODUCTION TO AC SOURCES.

Up to 3 banks of phase/auxiliary VTs can be set.

5

With VTs installed, the relay can be used to perform voltage measurements as well as power calculations. Enter the VT connection made to the system as 'Wye' or 'Delta'. An open-delta source VT connection would be entered as 'Delta'. See the typical wiring diagram in the HARDWARE chapter for details.



The nominal Phase VT Secondary Voltage setting is the voltage across the relay input terminals when nominal voltage is applied to the VT primary. For example:

NOTE

- On a system with a 13.8 kV nominal primary voltage and with a 14400:120 Volt VT in a Delta connection, the secondary voltage would be 115, i.e. $(13800 / 14400) \times 120$. For a Wye connection, the voltage value entered must be the phase to neutral voltage which would be $115 / \sqrt{3} = 66.4$.
- On a 14.4 kV system with a Delta connection and a VT primary to secondary turns ratio of 14400:120, the voltage value entered would be 120, i.e. $14400 / 120$.

5.3.2 POWER SYSTEM

PATH: SETTINGS ↓ SYSTEM SETUP ⇒ ↓ POWER SYSTEM

<div>■ POWER SYSTEM</div> <div>■</div>	◀▶	NOMINAL FREQUENCY: 60 Hz	Range: 25 to 60 in steps of 1
	MESSAGE ▲▼	PHASE ROTATION: ABC	Range: ABC, ACB
	MESSAGE ▲▼	FREQUENCY AND PHASE REFERENCE: SRC 1	Range: SRC 1,..., SRC 6
	MESSAGE ▲	FREQUENCY TRACKING: Enabled	Range: Disabled, Enabled

The power system **NOMINAL FREQUENCY** value is used as a default to set the digital sampling rate if the system frequency cannot be measured from the IA or VA channels of the CT/VT module. The phase sequence of the power system is required to properly calculate sequence components and power parameters.

The **PHASE ROTATION** setting is used to match the system phase sequence. Note that this setting is used to inform the relay of the actual system phase sequence, either ABC or ACB. CT and VT inputs on the relay, which are labeled as A, B and C must be connected to system phases A, B and C for correct operation.

The **FREQUENCY AND PHASE REFERENCE** setting determines which signal source is used (and hence which AC signal) for frequency tracking and phasor angle reference. The AC signal used is prioritized based on the AC inputs that are configured for the signal source: Phase A voltage takes precedence, followed by auxiliary voltage, then Phase A current, and finally ground current. The phase angle for the reference signal will always display zero degrees and all other phase angles will be relative to this signal.

The reference AC signal is selected based upon the Source configuration, regardless of whether or not a particular signal is actually applied to the relay. If the pre-selected reference signal is not measurable at a given time, the phase angles are not referenced.

The phase angle referencing is done via a phase locked loop which can synchronize independent UR relays if they have the same AC signal reference. This results in very precise correlation of time-tagging in the event recorder between different UR relays provided the relays have an IRIG-B connection.



NOTE

FREQUENCY TRACKING should only be set to '**Disabled**' in very unusual circumstances; consult the factory for special variable-frequency applications.



NOTE

(L60 only): For correct operation of the Phase Comparison Element (87PC), the **FREQUENCY AND PHASE REFERENCE** setting must not be set as '**None**' because deviations in real system frequency may cause improper detection of the zero-crossing of the operating current.

5.3.3 SIGNAL SOURCES

PATH: SETTINGS ↴ SYSTEM SETUP ⇨ ↴ SIGNAL SOURCES ⇨ SOURCE 1(6)

<div>SOURCE 1</div>		<div>◀▶</div>	<div>SOURCE 1 NAME: SRC 1</div>	Range: up to 6 alphanumeric characters
MESSAGE	<div>▲▼</div>		<div>SOURCE 1 PHASE CT: None</div>	Range: None, F1, F5, F1+F5, ..., F1+F5+M1+M5+U1+U5 Note: only phase current inputs will be displayed.
MESSAGE	<div>▲▼</div>		<div>SOURCE 1 GROUND CT: None</div>	Range: None, F1, F5, F1+F5, ..., F1+F5+M1+M5+U1+U5 Note: only ground current inputs will be displayed.
MESSAGE	<div>▲▼</div>		<div>SOURCE 1 PHASE VT: None</div>	Range: None, F1, F5, M1, M5, U1, U5 Note: only phase voltage inputs will be displayed.
MESSAGE	<div>▲</div>		<div>SOURCE 1 AUX VT: None</div>	Range: None, F1, F5, M1, M5, U1, U5 Note: only auxiliary voltage inputs will be displayed.

There are up to 6 identical Source setting menus available, numbered from 1 to 6.

"SRC 1" can be replaced by whatever name is defined by the user for the associated source.

'F', 'U', and 'M' are module slot position letters; the following number represents either the first bank of four channels (1, 2, 3, 4) called '1' or the second bank of four channels (5, 6, 7, 8) called '5' in a particular CT/VT module. See also the section INTRODUCTION TO AC SOURCES.

5

It is possible to select the sum of any combination of CTs. The first channel displayed is the CT to which all others will be referred. For example, the selection "F1+F5" indicates the sum of each phase from channels "F1" and "F5", scaled to whichever CT has the higher ratio.

The selection "None" will result in the hiding of the associated actual values.

The approach used to configure the AC Sources consists of several steps; first step is to specify the information about each CT and VT input. For CT inputs, this is the nominal primary and secondary current. For VTs, this is the connection type, ratio and nominal secondary voltage. Once the inputs have been specified, the configuration for each Source is entered, including specifying which CTs will be summed together.

USER SELECTION OF AC PARAMETERS FOR COMPARATOR ELEMENTS:

CT/VT modules automatically calculate all current and voltage parameters that can be calculated from the inputs available. Users will have to select the specific input parameters that are to be measured by every element, as selected in the element settings. The internal design of the element specifies which type of parameter to use and provides a setting for selection of the Source. In some elements where the parameter may be either fundamental or RMS magnitude, such as phase time overcurrent, two settings are provided. One setting specifies the Source, the second selects between fundamental phasor and RMS.

AC INPUT ACTUAL VALUES:

The calculated parameters associated with the configured voltage and current inputs are displayed in the current and voltage input sections of Actual Values. Only the phasor quantities associated with the actual AC physical input channels will be displayed here. All parameters contained within a configured Source are displayed in the Sources section of Actual Values.

DISTURBANCE DETECTORS (Internal):

The 50DD element is a sensitive current disturbance detector that is used to detect any disturbance on the protected system. 50DD is intended for use in conjunction with measuring elements, blocking of current based elements (to prevent mal-operation as a result of the wrong settings), and starting oscillography data capture. A disturbance detector is provided for every Source, and the resultant output to a measuring element is selected automatically.

The 50DD function responds to the changes in magnitude of the sequence currents.

The disturbance detector scheme logic is as follows:

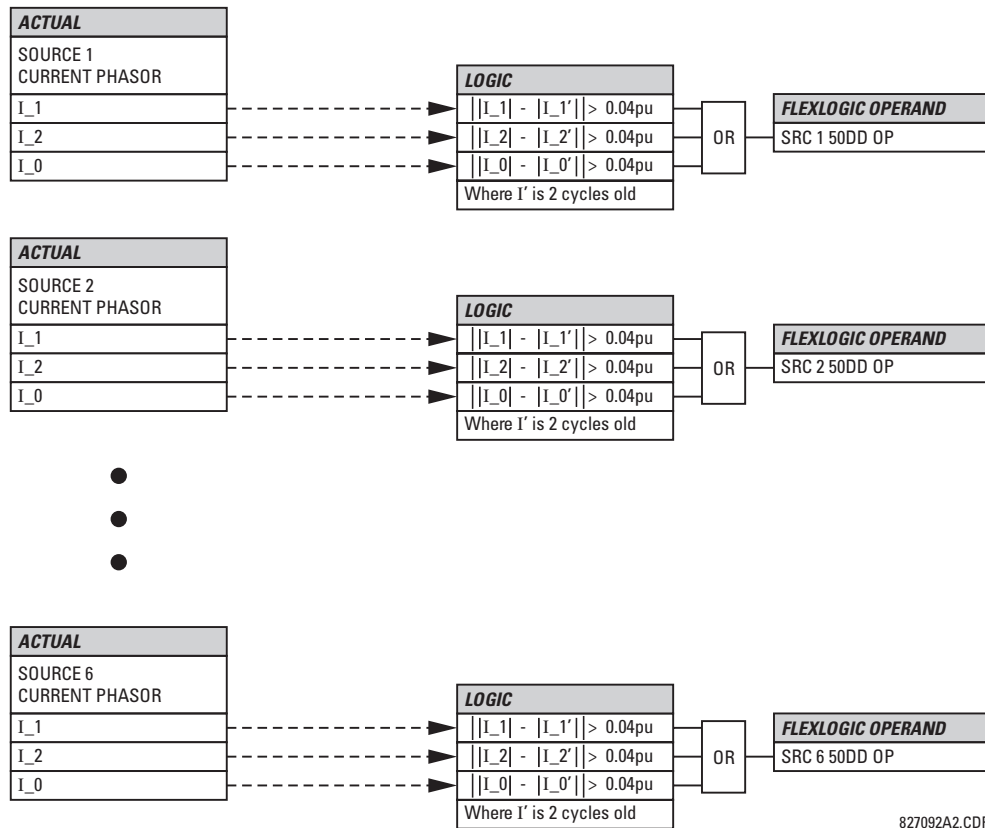


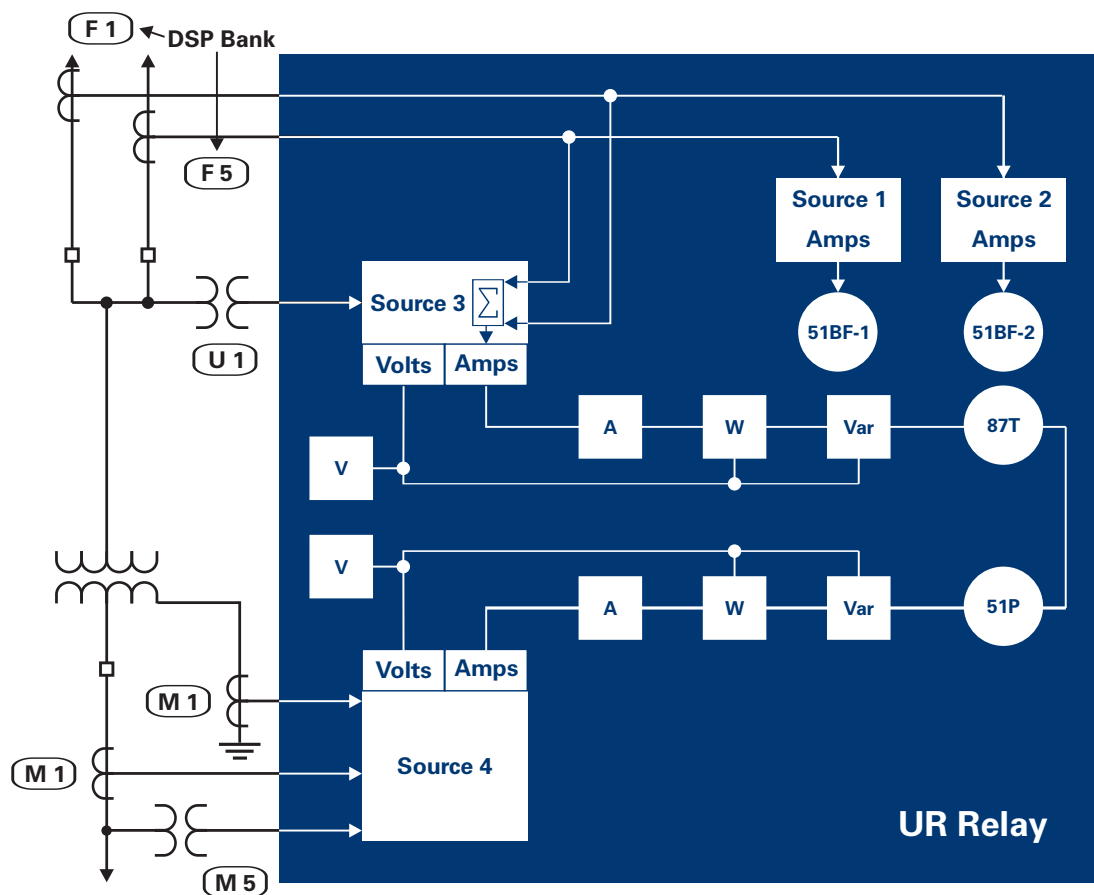
Figure 5–2: DISTURBANCE DETECTOR LOGIC DIAGRAM

a) EXAMPLE USE OF SOURCES:

An example of the use of Sources, with a relay with three CT/VT modules, is shown in the diagram below. A relay could have the following hardware configuration:

Increasing Slot Position Letter -->		
CT/VT Module 1	CT/VT Module 2	CT/VT Module 3
CTs	CTs	VTs
CTs	VTs	---

This configuration could be used on a two winding transformer, with one winding connected into a breaker-and-a-half system. The following figure shows the arrangement of Sources used to provide the functions required in this application, and the CT/VT inputs that are used to provide the data.



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Figure 5–3: EXAMPLE USE OF SOURCES

5.3.4 L60 POWER SYSTEM

PATH: SETTINGS ↓ POWER SYSTEM ⇌ L60 POWER SYSTEM

<div>■ L60 POWER SYSTEM</div> <div>■</div>	◀▶	NUMBER OF TERMINALS: 2	Range: 2, 3
	MESSAGE ▲	NUMBER OF CHANNELS: 1	Range: 1, 2

Models of the relay are available for application on either two or three terminal lines. The model designed for application on three terminal lines may also be applied on two terminal lines by selecting the **NUMBER OF TERMINALS** equal to 2.

The **NUMBER OF CHANNELS** setting should correspond to the type of Communications Card installed. When the model designed for application on three terminal lines is applied on two terminal lines, it may be used with either a single communications channel, or with a second redundant channel for increased dependability. In three terminal line applications, or in two terminal line applications with a redundant channel, the **NUMBER OF CHANNELS** should be selected as 2.

5.3.5 LINE

PATH: SETTINGS ↓ SYSTEM SETUP ⇌ LINE

<div>■ LINE</div> <div>■</div>	◀▶	POS SEQ IMPEDANCE MAGNITUDE: 3.00 Ω	Range: 0.01 to 250.00 in steps of 0.01
	MESSAGE ▲	POS SEQ IMPEDANCE ANGLE: 75°	Range: 25 to 90° in steps of 1°
	MESSAGE ▲	ZERO SEQ IMPEDANCE MAGNITUDE: 9.00 Ω	Range: 0.01 to 650.00 in steps of 0.01
	MESSAGE ▲	ZERO SEQ IMPEDANCE ANGLE: 75°	Range: 25 to 90° in steps of 1°
	MESSAGE ▲	LINE LENGTH UNITS: km	Range: km, miles
	MESSAGE ▲	LINE LENGTH (km) : 100.0	Range: 0.0 to 2000.0 in steps of 0.1

These settings specify the characteristics of the line. The positive sequence and zero sequence values are used in the automatic calculation of the zero compensation for the ground distance measurement.

The line impedance value should be input as Secondary Ohms.

The data is used for fault location calculations.

See the SETTINGS \ PRODUCT SETUP \ FAULT REPORT menu for assigning the Source and Trigger for fault calculations.

5.3.6 BREAKER 1 / BREAKER 2

PATH: SETTINGS ↓ SYSTEM SETUP ⇒ BREAKERS ⇒ BREAKER 1(2)

5	■ BREAKER 1		BREAKER 1	Range: Disabled, Enabled
	■		FUNCTION: Disabled	
	MESSAGE	▲▼	BREAKER1 PUSH BUTTON	Range: Disabled, Enabled
			CONTROL: Disabled	
	MESSAGE	▲▼	BREAKER 1 NAME:	Range: up to 6 alphanumeric characters
			Bkr 1	
	MESSAGE	▲▼	BREAKER 1 MODE:	Range: 3-Pole, 1-Pole
			3-Pole	
	MESSAGE	▲▼	BREAKER 1 OPEN:	Range: FlexLogic™ Operand
			Off	
MESSAGE	▲▼	BREAKER 1 CLOSE:	Range: FlexLogic™ Operand	
		Off		
MESSAGE	▲▼	BREAKER 1 ϕ A / 3-POLE:	Range: FlexLogic™ Operand	
		Off		
MESSAGE	▲▼	BREAKER 1 ϕ B:	Range: FlexLogic™ Operand	
		Off		
MESSAGE	▲▼	BREAKER 1 ϕ C:	Range: FlexLogic™ Operand	
		Off		
MESSAGE	▲▼	BREAKER 1 EXT ALARM:	Range: FlexLogic™ Operand	
		Off		
MESSAGE	▲▼	BREAKER 1 ALARM	Range: 0.000 to 1 000 000.000 sec. in steps of 0.001	
		DELAY: 0.000 s		
MESSAGE	▲	MANUAL CLOSE RECAL1	Range: 0.000 to 1 000 000.000 sec. in steps of 0.001	
		TIME: 0.000 s		

a) BREAKER CONTROL

A description of the operation of the breaker control and status monitoring features is provided in the Human Interfaces chapter. Only information that is involved with programming of the associated settings is covered in this section. These features are provided for two breakers; a user may use only those portions of the design relevant to a single breaker, which must be breaker No. 1.

b) BREAKER CONTROL SETTINGS

BREAKER 1 FUNCTION:

This setting must be selected to 'Enable' to allow the operation of any breaker control feature.

BREAKER1 PUSH BUTTON CONTROL:

This setting must be selected to 'Enable' to allow faceplate PUSH BUTTON operations.

BREAKER 1 NAME:

This setting is used to assign a user-defined name (up to 6 characters) to the breaker, which will be used in flash messages related to breaker No. 1.

BREAKER 1 MODE:

This setting is used to select either 3-pole mode, where all breaker poles are operated simultaneously, or 1-pole mode where all breaker poles are operated either independently or simultaneously.

BREAKER 1 OPEN:

This setting is used to select an operand that will create a signal that can be programmed to operate an output relay to open breaker No. 1.

BREAKER 1 CLOSE:

This setting is used to select an operand that will create a signal that can be programmed to operate an output relay to close breaker No. 1.

BREAKER 1 Φ A/3-POLE:

This setting is used to select an operand, usually a contact input connected to a breaker auxiliary position tracking mechanism. This input can be either a 52/a or 52/b contact which must be programmed to create a logic 0 when the breaker is open. If the mode is selected as 3-pole, this setting selects a single contact input as the operand used to track the breaker open or closed position. If the mode is selected as 1-pole, the input mentioned above is used to track phase A and settings BREAKER 1 Φ B and BREAKER 1 Φ C are provided to select operands to track phases B and C respectively.

BREAKER 1 Φ B:

If the mode is selected as 3-pole, this setting has no function. If the mode is selected as 1-pole, this input is used to track phase B as above for phase A.

BREAKER 1 Φ C:

If the mode is selected as 3-pole, this setting has no function. If the mode is selected as 1-pole, this input is used to track phase C as above for phase A.

BREAKER 1 EXT ALARM:

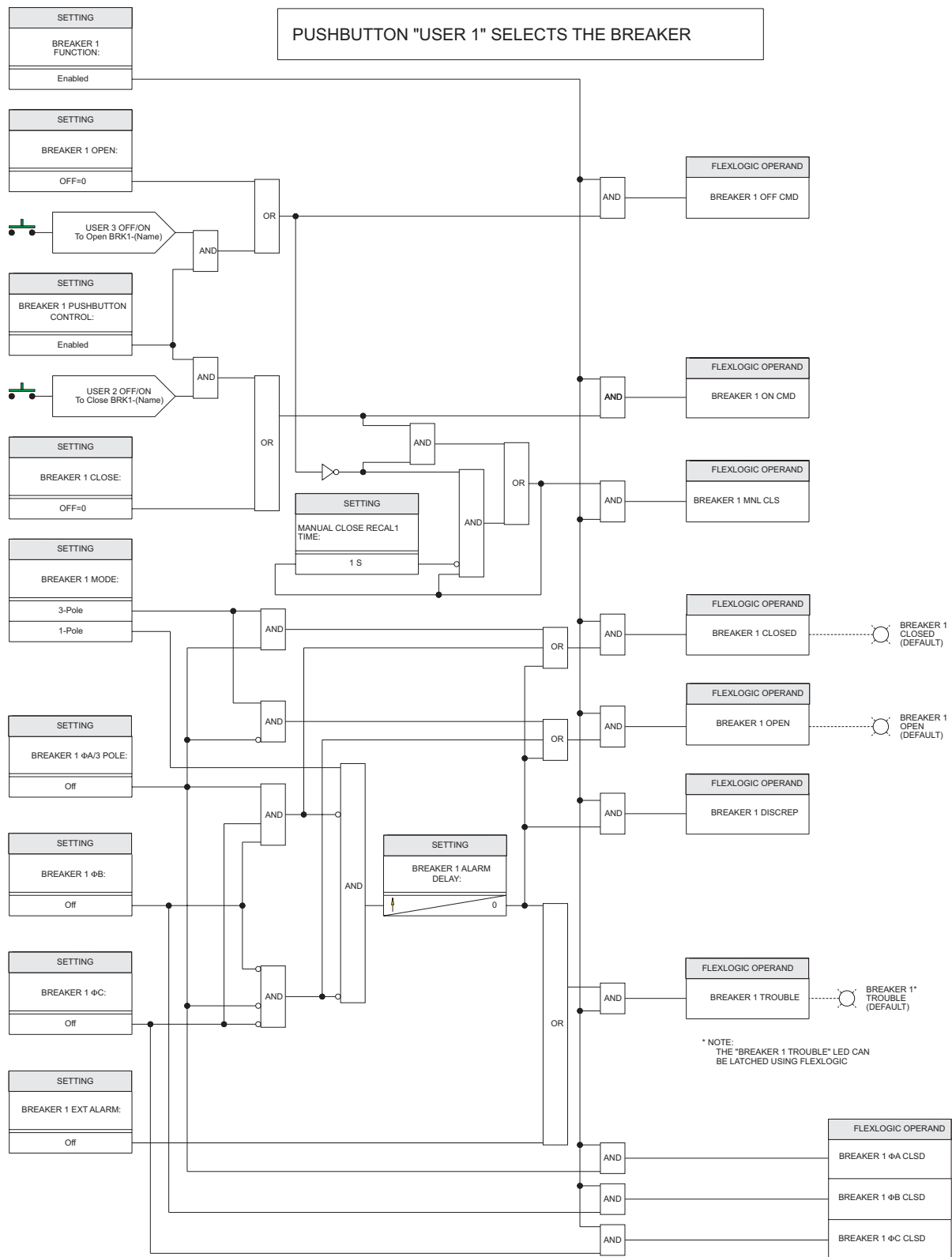
This setting is used to select an operand, usually an external contact input, connected to a breaker alarm reporting contact.

BREAKER 1 ALARM DELAY:

This setting is used to program the delay interval during which a disagreement of status among the three pole position tracking operands will not declare a pole disagreement, to allow for non-simultaneous operation of the poles.

MANUAL CLOSE RECAL1 TIME:

This setting is used to program the interval required to maintain setting changes in effect after an operator has initiated a manual close command to operate a circuit breaker.



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Figure 5-4: DUAL BREAKER CONTROL SCHEME LOGIC

5.3.7 FLEXCURVE™ A / FLEXCURVE™ B

PATH: SETTINGS ↓ SYSTEM SETUP ⇒ FLEXCURVES ⇒ FLEXCURVE A

■ FLEXCURVE A	◀▶	FLEXCURVE A TIME AT	Range: 0 To 65535 ms in steps of 1 ms
■		0.00 xPKP: 0 ms	

Each of FlexCurve™ A and FlexCurve™ B have settings for entering times to Reset/Operate at the following pickup levels: 0.00 to 0.98 / 1.03 to 20.00. This data is converted into 2 continuous curves by linear interpolation between data points. To enter a custom FlexCurve™, enter the Reset/Operate time (using the ▲ VALUE ▼ keys) for each selected pickup point (using the ▲ MESSAGE ▼ keys) for the desired protection curve (A or B).

Table 5–3: FLEXCURVE™ TABLE

RESET	TIME ms	RESET	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms
0.00		0.68		1.03		2.9		4.9		10.5	
0.05		0.70		1.05		3.0		5.0		11.0	
0.10		0.72		1.1		3.1		5.1		11.5	
0.15		0.74		1.2		3.2		5.2		12.0	
0.20		0.76		1.3		3.3		5.3		12.5	
0.25		0.78		1.4		3.4		5.4		13.0	
0.30		0.80		1.5		3.5		5.5		13.5	
0.35		0.82		1.6		3.6		5.6		14.0	
0.40		0.84		1.7		3.7		5.7		14.5	
0.45		0.86		1.8		3.8		5.8		15.0	
0.48		0.88		1.9		3.9		5.9		15.5	
0.50		0.90		2.0		4.0		6.0		16.0	
0.52		0.91		2.1		4.1		6.5		16.5	
0.54		0.92		2.2		4.2		7.0		17.0	
0.56		0.93		2.3		4.3		7.5		17.5	
0.58		0.94		2.4		4.4		8.0		18.0	
0.60		0.95		2.5		4.5		8.5		18.5	
0.62		0.96		2.6		4.6		9.0		19.0	
0.64		0.97		2.7		4.7		9.5		19.5	
0.66		0.98		2.8		4.8		10.0		20.0	

5.4.1 INTRODUCTION TO FLEXLOGIC™

In order to provide maximum flexibility to the user of a UR (Universal Relay) device, the arrangement of internal digital logic combines fixed and user-programmed parameters. Logic upon which individual features are designed is fixed, and all other logic from digital input signals through elements or combinations of elements to digital outputs, is variable. The user has complete control of all variable logic through FlexLogic™. In general, the system receives analog and digital inputs which it uses to produce analog and digital outputs. The major sub-systems of a generic UR relay involved in this process are shown in the following figure.

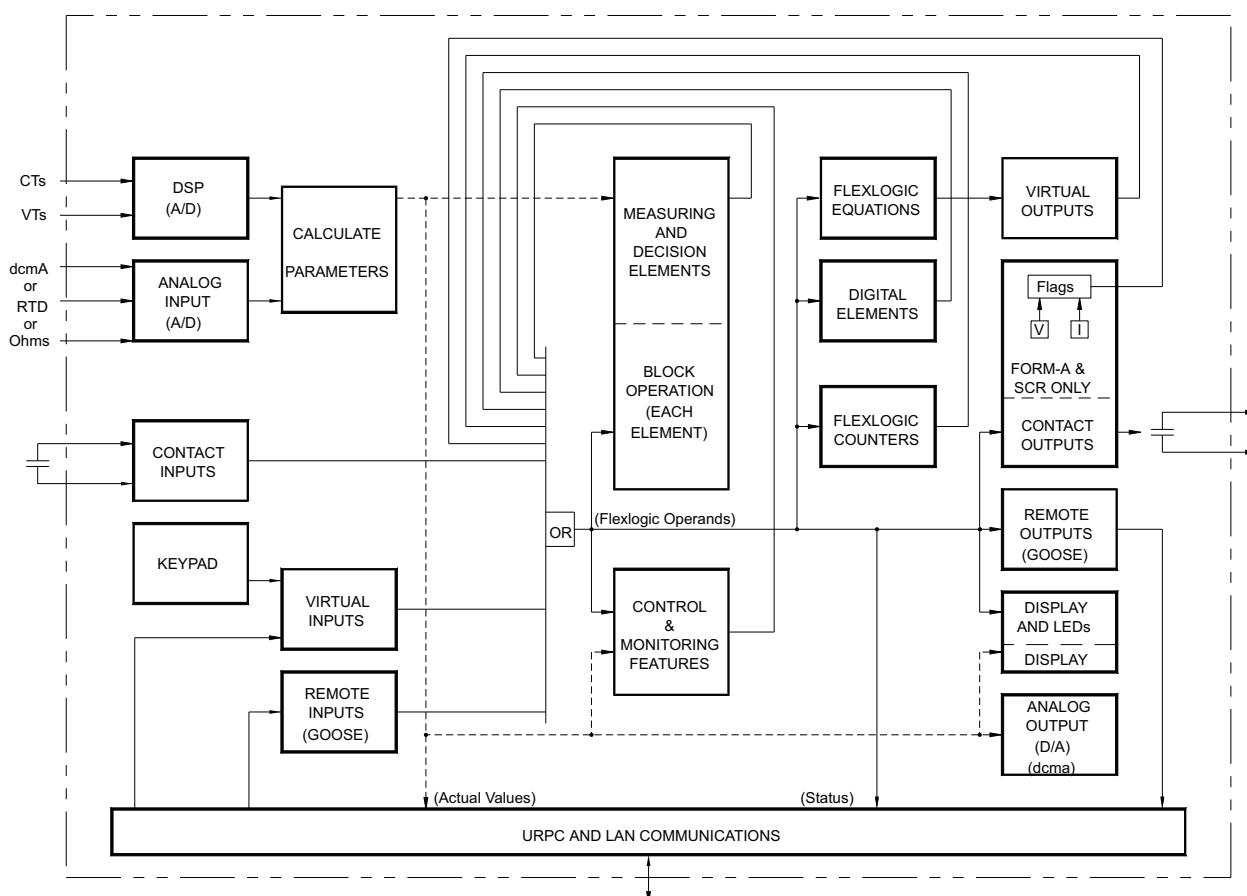


Figure 5-5: UR ARCHITECTURE OVERVIEW

The states of all digital signals used in a UR relay are represented by flags (or FlexLogic™ operands, which are described in a later section). A digital "1" is represented by a 'set' flag. Any external contact change-of-state can be used to block an element from operating, as an input to a control feature in a FlexLogic™ equation, or to operate a contact output. The state of the contact input can be displayed locally or viewed remotely via the communications facilities provided. If it is desired to have a simple scheme where a contact input is used to block an element, this selection is made when programming the element. This capability also applies to the other features that set flags: elements, virtual inputs, remote inputs, schemes, and human operators.

If more logic that is more complex than that presented above is required, it is implemented via FlexLogic™. For example, if it is desired to have the closed state of contact input H7a and the operated state of the phase undervoltage element block the operation of the phase time overcurrent element, the two control input states are programmed in a FlexLogic™ equation. This equation ANDs the two control inputs to produce a "virtual output" which is then selected when programming the phase time overcurrent to be used as a blocking input. Virtual outputs can only be created by FlexLogic™ equations.

Traditionally, protective relay logic has been relatively limited. Any unusual applications involving interlocks, blocking, or supervisory functions had to be hardwired using contact inputs and outputs. FlexLogic™ minimizes the requirement for auxiliary components and wiring while making more complex schemes possible.

The logic that determines the interaction of inputs, elements, schemes and outputs is field programmable through the use of logic equations that are sequentially processed. The use of virtual inputs and outputs in addition to hardware is available internally and on the communication ports for other relays to use (distributed FlexLogic™).

FlexLogic™ allows users to customize the relay through a series of equations that consist of operators and operands. The operands are the states of inputs, elements, schemes and outputs. The operators are logic gates, timers and latches (with set and reset inputs). A system of sequential operations allows any combination of specified operands to be assigned as inputs to specified operators to create an output. The final output of an equation is a numbered register called a virtual output. Virtual outputs can be used as an input operand in any equation, including the equation that generates the output, as a seal-in or other type of feedback.

A FlexLogic™ equation consists of parameters that are either operands or operators. Operands have a logic state of 1 or 0. Operators provide a defined function, such as an AND gate or a Timer. Each equation defines the combinations of parameters to be used to set a VIRTUAL OUTPUT flag. Evaluation of an equation results in either a 1 (= ON, i.e. flag set) or 0 (= OFF, i.e. flag not set). Each equation is evaluated at least 4 times every power system cycle.

Some types of operands are present in the relay in multiple instances; e.g. contact and remote inputs. These types of operands are grouped together (for presentation purposes only) on the faceplate display. The characteristics of the different types of operands are listed in the table: FLEXLOGIC™ OPERAND TYPES.

Table 5–4: FLEXLOGIC™ OPERAND TYPES

OPERAND TYPE	STATE	EXAMPE FORMAT	CHARACTERISTICS [Input Is '1' (= ON) if...]
Element (Analog)	Pickup	PHASE TOC1 PKP	The tested parameter is presently above the pickup setting of an element which responds to rising values or below the pickup setting of an element which responds to falling values.
	Dropout	PHASE TOC1 DPO	This operand is the logical inverse of the above PKP operand.
	Operate	PHASE TOC1 OP	The tested parameter has been above/below the pickup setting of the element for the programmed delay time, or has been at logic 1 and is now at logic 0 but the reset timer has not finished timing.
	Block	PH DIR1 BLK	The output of the comparator is set to the block function.
Element (Digital)	Pickup	Dig Element 1 PKP	The input operand is at logic 1.
	Dropout	Dig Element 1 DPO	This operand is the logical inverse of the above PKP operand.
	Operate	Dig Element 1 OP	The input operand has been at logic 1 for the programmed pickup delay time, or has been at logic 1 for this period and is now at logic 0 but the reset timer has not finished timing.
Element (Digital Counter)	Higher than	Counter 1 HI	The number of pulses counted is above the set number.
	Equal to	Counter 1 EQL	The number of pulses counted is equal to the set number.
	Lower than	Counter 1 LO	The number of pulses counted is below the set number.
Contact Input	On	Cont Ip On	Voltage is presently applied to the input (external contact closed).
	Off	Cont Ip Off	Voltage is presently not applied to the input (external contact open).
Virtual Input	On	Virt Ip 1 On	The virtual input is presently in the ON state.
Remote Input	On	REMOTE INPUT 1 On	The remote input is presently in the ON state.
Contact Output (type Form-A contact only)	Voltage On	Cont Op 1 VOn	Voltage exists across the contact.
	Voltage Off	Cont Op 1 VOff	Voltage does not exists across the contact.
	Current On	Cont Op 1 IOn	Current is flowing through the contact.
	Current Off	Cont Op 1 IOff	Current is not flowing through the contact.
Virtual Output	On	Virt Op 1 On	The virtual output is presently in the set state (i.e. evaluation of the equation which produces this virtual output results in a "1").
Fixed	On	On	Logic 1
	Off	Off	Logic 0

The operands available for this relay are listed in the following table: FLEXLOGIC™ OPERANDS.

Table 5–5: FLEXLOGIC™ OPERANDS (Sheet 1 of 4)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT (Line Pickup)	LINE PICKUP OP LINE PICKUP PKP LINE PICKUP DPO LINE PICKUP UV PKP LINE PICKUP LEO PKP	Line Pickup is operated Line Pickup is picked up Line Pickup is dropped out Line Pickup Undervoltage is picked up Line Pickup Line End Open is picked up
ELEMENT (Power Swing Detect)	POWER SWING OUTER POWER SWING MIDDLE POWER SWING INNER POWER SWING BLOCK POWER SWING TMRX PKP POWER SWING TRIP	Positive Sequence impedance in outer characteristic Positive Sequence impedance in middle characteristic Positive Sequence impedance in inner characteristic Power Swing Blocking element operated Power Swing Timer X picked up Out-of-step Tripping operated
ELEMENT (Phase TOC)	PHASE TOC1 PKP PHASE TOC1 OP PHASE TOC1 DPO PHASE TOC1 PKP A PHASE TOC1 PKP B PHASE TOC1 PKP C PHASE TOC1 OP A PHASE TOC1 OP B PHASE TOC1 OP C PHASE TOC1 DPO A PHASE TOC1 DPO B PHASE TOC1 DPO C	At least one phase of TOC1 is picked up At least one phase of TOC1 is operated At least one phase of TOC1 is dropped out Phase A of TOC1 is picked up Phase B of TOC1 is picked up Phase C of TOC1 is picked up Phase A of TOC1 is operated Phase B of TOC1 is operated Phase C of TOC1 is operated Phase A of TOC1 is dropped out Phase B of TOC1 is dropped out Phase C of TOC1 is dropped out
	PHASE TOC2...	Same set of operands as shown for PHASE TOC1
ELEMENT (Phase IOC)	PHASE IOC1 . . .	Same set of operands as shown for PHASE TOC1
	PHASE IOC2 . . .	Same set of operands as shown for PHASE TOC1
ELEMENT (Neutral TOC)	NEUTRAL TOC1 PKP NEUTRAL TOC1 OP NEUTRAL TOC1 DPO	Neutral TOC1 is picked up Neutral TOC1 is operated Neutral TOC1 is dropped out
	NEUTRAL TOC2...	Same set of operands as shown for NEUTRAL TOC1
ELEMENT (Neutral IOC)	NEUTRAL IOC1 . . .	Same set of operands as shown for NEUTRAL TOC1
	NEUTRAL IOC2...	Same set of operands as shown for NEUTRAL TOC1
ELEMENT (Ground TOC)	GROUND TOC1...	Same set of operands as shown for NEUTRAL TOC1
	GROUND TOC2...	Same set of operands as shown for NEUTRAL TOC1
ELEMENT (Ground IOC)	GROUND IOC1...	Same set of operands as shown for NEUTRAL TOC1
	GROUND IOC2...	Same set of operands as shown for NEUTRAL TOC1
ELEMENT (Neg. Seq. TOC)	NEG SEQ TOC1...	Same set of operands as shown for NEUTRAL TOC1
	NEG SEQ TOC2...	Same set of operands as shown for NEUTRAL TOC1
ELEMENT (Neg. Seq. IOC)	NEG SEQ IOC1...	Same set of operands as shown for NEUTRAL TOC1
	NEG SEQ IOC2...	Same set of operands as shown for NEUTRAL TOC1
ELEMENT (Breaker Failure)	BKR FAIL 1 RETRIPA BKR FAIL 1 RETRIPB BKR FAIL 1 RETRIPC BKR FAIL 1 RETRIP BKR FAIL 1 T1 OP BKR FAIL 1 T2 OP BKR FAIL 1 T3 OP BKR FAIL 1 TRIP OP	Breaker Failure 1 re-trip phase A (only for 1-pole schemes) Breaker Failure 1 re-trip phase B (only for 1-pole schemes) Breaker Failure 1 re-trip phase C (only for 1-pole schemes) Breaker Failure 1 re-trip 3-phase Breaker Failure 1 Timer 1 is operated Breaker Failure 1 Timer 2 is operated Breaker Failure 1 Timer 3 is operated Breaker Failure 1 trip is operated
	BKR FAIL 2...	Same set of operands as shown for BKR FAIL 1

Table 5–5: FLEXLOGIC™ OPERANDS (Sheet 2 of 4)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT (Phase UV)	PHASE UV1 PKP PHASE UV1 OP PHASE UV1 DPO PHASE UV1 PKP A PHASE UV1 PKP B PHASE UV1 PKP C PHASE UV1 OP A PHASE UV1 OP B PHASE UV1 OP C PHASE UV1 DPO A PHASE UV1 DPO B PHASE UV1 DPO C	At least one phase of UV1 is picked up At least one phase of UV1 is operated At least one phase of UV1 is dropped out Phase A of UV1 is picked up Phase B of UV1 is picked up Phase C of UV1 is picked up Phase A of UV1 is operated Phase B of UV1 is operated Phase C of UV1 is operated Phase A of UV1 is dropped out Phase B of UV1 is dropped out Phase C of UV1 is dropped out
	PHASE UV2...	Same set of operands as shown for PHASE UV1
ELEMENT (Phase OV)	PHASE OV1...	Same set of operands as shown for PHASE UV1
ELEMENT (50DD Supv.)	50DD SV	Disturbance Detector is supervising
ELEMENT (Setting Group)	SETTING GROUP ACT 1 ↓ SETTING GROUP ACT 8	Setting group 1 is active ↓ Setting group 8 is active
ELEMENT (Synchrocheck)	SYNC 1 DEAD S OP SYNC 1 DEAD S DPO SYNC 1 SYNC OP SYNC 1 SYNC DPO SYNC 1 CLS OP SYNC 1 CLS DPO	Synchrocheck 1 dead source is operated Synchrocheck 1 dead source is dropped out Synchrocheck 1 in synchronization is operated Synchrocheck 1 in synchronization is dropped out Synchrocheck 1 close is operated Synchrocheck 1 close is dropped out
	SYNC 2...	Same set of operands as shown for SYNC 1
ELEMENT (Autoreclose)	AR 1 ENABLED AR 1 RIP AR 1 LO AR 1 BLK FROM MAN CL AR 1 CLOSE AR 1 SHOT CNT=0 ↓ AR 1 SHOT CNT=4 AR 1 DISABLED	Auto reclose 1 is enabled Auto reclose 1 is in progress Auto reclose 1 is locked out Auto reclose 1 is temporarily disabled Auto reclose 1 close command is issued Auto reclose 1 shot count is 0 ↓ Auto reclose 1 shot count is 4 Auto reclose 1 is disabled
ELEMENT (Digital Element)	Dig Element 1 PKP Dig Element 1 OP Dig Element 1 DPO ↓ Dig Element 16 PKP Dig Element 16 OP Dig Element 16 DPO	Digital Element 1 is picked up Digital Element 1 is operated Digital Element 1 is dropped out ↓ Digital Element 16 is picked up Digital Element 16 is operated Digital Element 16 is dropped out
ELEMENT (Digital Counter)	Counter 1 HI Counter 1 EQL Counter 1 LO ↓ Counter 8 HI Counter 8 EQL Counter 8 LO	Digital Counter 1 output is 'more than' comparison value Digital Counter 1 output is 'equal to' comparison value Digital Counter 1 output is 'less than' comparison value ↓ Digital Counter 8 output is 'more than' comparison value Digital Counter 8 output is 'equal to' comparison value Digital Counter 8 output is 'less than' comparison value
ELEMENT (Breaker Arcing)	BKR ARC 1 OP BKR ARC 2 OP	Breaker Arcing 1 is operated Breaker Arcing 2 is operated
ELEMENT (Continuous Monitor / CT Fail)	CONT MONITOR PKP CONT MONITOR OP	Continuous monitor is picked up Continuous monitor is operated
	CT FAIL...	Same set of operands as shown for CONT MONITOR
ELEMENT (VTFF)	SRCx VT FUSE FAIL OP	Source x VT Fuse Failure detector is operated

Table 5–5: FLEXLOGIC™ OPERANDS (Sheet 3 of 4)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
ELEMENT (Disturbance Detector)	SRCx 50DD OP	Source x Disturbance Detector is operated
ELEMENT (POTT)	POTT OP POTT TX	Permissive over-reaching transfer trip is operated Permissive over-reaching transfer trip is sent
BREAKER	BREAKER 1 OFF CMD BREAKER 1 ON CMD BREAKER 1 ϕ A CLSD BREAKER 1 ϕ B CLSD BREAKER 1 ϕ C CLSD BREAKER 1 CLOSED BREAKER 1 OPEN BREAKER 1 DISCREP BREAKER 1 TROUBLE BREAKER 1 MNL CLS	Breaker 1 OFF command Breaker 1 ON command Breaker 1 phase A is closed Breaker 1 phase B is closed Breaker 1 phase C is closed Breaker 1 is closed Breaker 1 is open Breaker 1 has discrepancy Breaker 1 trouble alarm Breaker 1 manual close
	BREAKER 2...	Same set of operands as shown for BREAKER 1
RESETTING	RESET OP RESET OP (COMMS) RESET OP (OPERAND) RESET OP (PUSHBUTTON)	Reset command is operated (set by all 3 operands below) Communications source of the reset command Operand source of the reset command Reset key (pushbutton) source of the reset command
FIXED	Off	Logic = 0. Does nothing and may be used as a delimiter in an equation list; used as 'Disable' by other features.
	On	Logic = 1. Can be used as a test setting.
CONTACT INPUT	Cont Ip 1 On Cont Ip 2 On ↓ Cont Ip 1 Off Cont Ip 2 Off ↓	(will not appear unless ordered) (will not appear unless ordered) ↓ (will not appear unless ordered) (will not appear unless ordered) ↓
VIRTUAL INPUT	Virt Ip 1 On ↓ Virt Ip 32 On	Flag is set, logic=1 ↓ Flag is set, logic=1
	REMOTE INPUT 1 On ↓ REMOTE INPUT 32 On	Flag is set, logic=1 ↓ Flag is set, logic=1
REMOTE DEVICE	REMOTE DEVICE 1 On ↓ REMOTE DEVICE 16 On	Flag is set, logic=1 ↓ Flag is set, logic=1
	REMOTE DEVICE 1 Off ↓ REMOTE DEVICE 16 Off	Flag is set, logic=1 ↓ Flag is set, logic=1
	Cont Op 1 VOn Cont Op 2 VOn ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
	Cont Op 1 VOff Cont Op 2 VOff ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
CONTACT OUTPUT (voltage) From detector on Form-A output only	Cont Op 1 IOn Cont Op 2 IOn ↓	(will not appear unless ordered) (will not appear unless ordered) ↓
	Cont Op 1 IOff Cont Op 2 IOff ↓	(will not appear unless ordered) (will not appear unless ordered) ↓

Table 5–5: FLEXLOGIC™ OPERANDS (Sheet 4 of 4)

OPERAND TYPE	OPERAND SYNTAX	OPERAND DESCRIPTION
VIRTUAL OUTPUT	Virt Op 1 On ↓ Virt Op 64 On	Flag is set, logic=1 ↓ Flag is set, logic=1
	Direct I/P 1-1 On ↓ Direct I/P 1-8 On	(appears only when L90 Comm card is used) ↓ (appears only when L90 Comm card is used)
DIRECT INPUT	Direct I/P 2-1 On ↓ Direct I/P 2-8 On	(appears only when L90 Comm card is used) ↓ (appears only when L90 Comm card is used)
	ANY MAJOR ERROR ANY MINOR ERROR ANY SELF-TEST LOW ON MEMORY WATCHDOG ERROR PROGRAM ERROR EEPROM DATA ERROR PRI ETHERNET FAIL SEC ETHERNET FAIL BATTERY FAIL SYSTEM EXCEPTION UNIT NOT PROGRAMMED EQUIPMENT MISMATCH FLEXLGC ERROR TOKEN PROTOTYPE FIRMWARE UNIT NOT CALIBRATED NO DSP INTERRUPTS DSP ERROR IRIG-B FAILURE REMOTE DEVICE OFFLINE	Any of the major self-test errors generated (major error) Any of the minor self-test errors generated (minor error) Any self-test errors generated (generic, any error) See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter. See description in the COMMANDS chapter.

Some operands can be re-named by the user. These are the names of the breakers in the breaker control feature, the ID (identification) of contact inputs, the ID of virtual inputs, and the ID of virtual outputs. If the user changes the default name/ID of any of these operands, the assigned name will appear in the relay list of operands. The default names are shown in the FLEXLOGIC™ OPERANDS table above.

The characteristics of the logic gates are tabulated in FLEXLOGIC™ GATE CHARACTERISTICS table, and the operators available in FlexLogic™ are listed in the FLEXLOGIC™ OPERATORS table.

Table 5–6: FLEXLOGIC™ GATE CHARACTERISTICS

GATES	NUMBER OF INPUTS	OUTPUT IS '1' (= ON) IF...
NOT	1	input is '0'
OR	2 to 16	any input is '1'
AND	2 to 16	all inputs are '1'
NOR	2 to 16	all inputs are '0'
NAND	2 to 16	any input is '0'
XOR	2	only one input is '1'

Table 5–7: FLEXLOGIC™ OPERATORS

OPERATOR TYPE	OPERATOR SYNTAX	DESCRIPTION	NOTES
Editor	INSERT	Insert a parameter in an equation list.	
	DELETE	Delete a parameter from an equation list.	
End	END	The first END encountered signifies the last entry in the list of FlexLogic™ parameters that is processed.	
One Shot	POSITIVE ONE SHOT	One shot that responds to a positive going edge.	A 'one shot' refers to a single input gate that generates a pulse in response to an edge on the input. The output from a 'one shot' is True (positive) for only one pass through the FlexLogic™ equation. There is a maximum of 32 'one shots'.
	NEGATIVE ONE SHOT	One shot that responds to a negative going edge.	
	DUAL ONE SHOT	One shot that responds to both the positive and negative going edges.	
Logic Gate	NOT	Logical Not	Operates on the previous parameter.
	OR(2) ↓ OR(16)	2 input OR gate ↓ 16 input OR gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	AND(2) ↓ AND(16)	2 input AND gate ↓ 16 input AND gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	NOR(2) ↓ NOR(16)	2 input NOR gate ↓ 16 input NOR gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	NAND(2) ↓ NAND(16)	2 input NAND gate ↓ 16 input NAND gate	Operates on the 2 previous parameters. ↓ Operates on the 16 previous parameters.
	XOR(2)	2 input Exclusive OR gate	Operates on the 2 previous parameters.
	LATCH (S,R)	Latch (Set, Reset) - reset-dominant	The parameter preceding LATCH(S,R) is the Reset input. The parameter preceding the Reset input is the Set input.
Timer	TIMER 1 ↓ TIMER 32	Timer as configured with FlexLogic™ Timer 1 settings. ↓ Timer as configured with FlexLogic™ Timer 32 settings.	The timer is started by the preceding parameter. The output of the timer is TIMER #.
Assign Virtual Output	= Virt Op 1 ↓ = Virt Op 64	Assigns previous FlexLogic™ parameter to Virtual Output 1. ↓ Assigns previous FlexLogic™ parameter to Virtual Output 64.	The virtual output is set by the preceding parameter

a) FLEXLOGIC™ RULES

When forming a FlexLogic™ equation, the sequence of entries in the linear array of parameters must follow these general rules:

1. Operands must precede the operator which uses the operands as inputs.
2. Operators have only one output. The output of an operator must be used to create a virtual output if it is to be used as an input to two or more operators.
3. Assigning the output of an operator to a Virtual Output terminates the equation.
4. A timer operator (e.g. "TIMER 1") or virtual output assignment (e.g. " = Virt Op 1") may only be used once. If this rule is broken, a syntax error will be declared.

b) FLEXLOGIC™ EVALUATION

Each equation is evaluated in the order in which the parameters have been entered.



FLEXLOGIC™ PROVIDES LATCHES WHICH BY DEFINITION HAVE A MEMORY ACTION, REMAINING IN THE SET STATE AFTER THE SET INPUT HAS BEEN ASSERTED. HOWEVER, THEY ARE VOLATILE; I.E. THEY RESET ON THE RE-APPLICATION OF CONTROL POWER.

WHEN MAKING CHANGES TO PROGRAMMING, ALL FLEXLOGIC™ EQUATIONS ARE RE-COMPILED WHEN ANY NEW SETTING IS ENTERED, SO ALL LATCHES ARE AUTOMATICALLY RESET. IF IT IS REQUIRED TO RE-INITIALIZE FLEXLOGIC™ DURING TESTING, FOR EXAMPLE, IT IS SUGGESTED TO POWER THE UNIT DOWN AND THEN BACK UP.

c) FLEXLOGIC™ PROCEDURE EXAMPLE

An example of the process used to implement a particular set of logic required in an application follows. The sequence of the steps outlined is quite important, as it should minimize the work necessary to develop the settings to be applied to the relay. Note that the example presented below in the figure: EXAMPLE LOGIC SCHEME, is intended to demonstrate the procedure, not to solve a specific application situation.

In the logic example, it is assumed that some logic has already been programmed to produce Virtual Output 1 and Virtual Output 2, and is only a part of the full set of equations used. When using FlexLogic™, it is important to make a note when each Virtual Output is used - a Virtual Output designation (1 to 64) can only be properly assigned once.

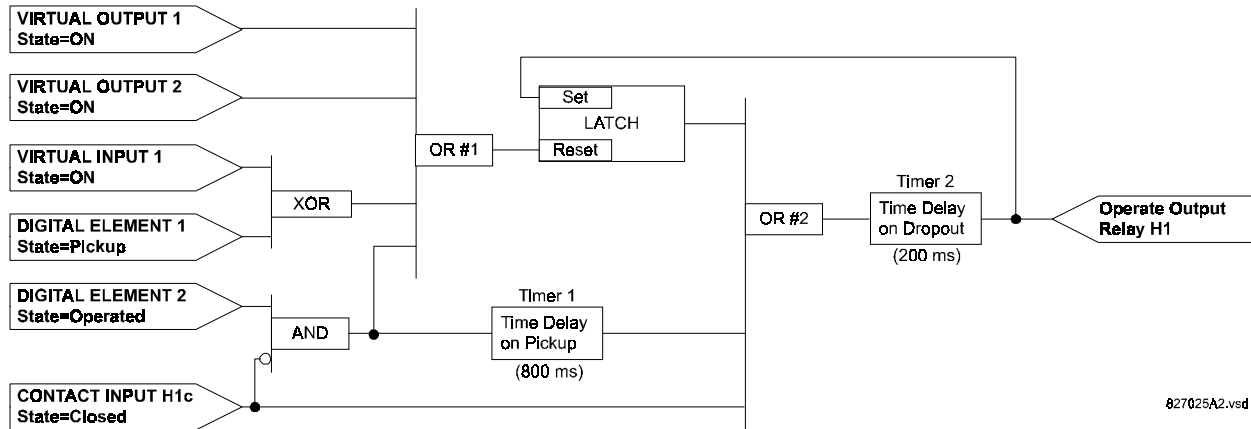


Figure 5-6: EXAMPLE LOGIC SCHEME

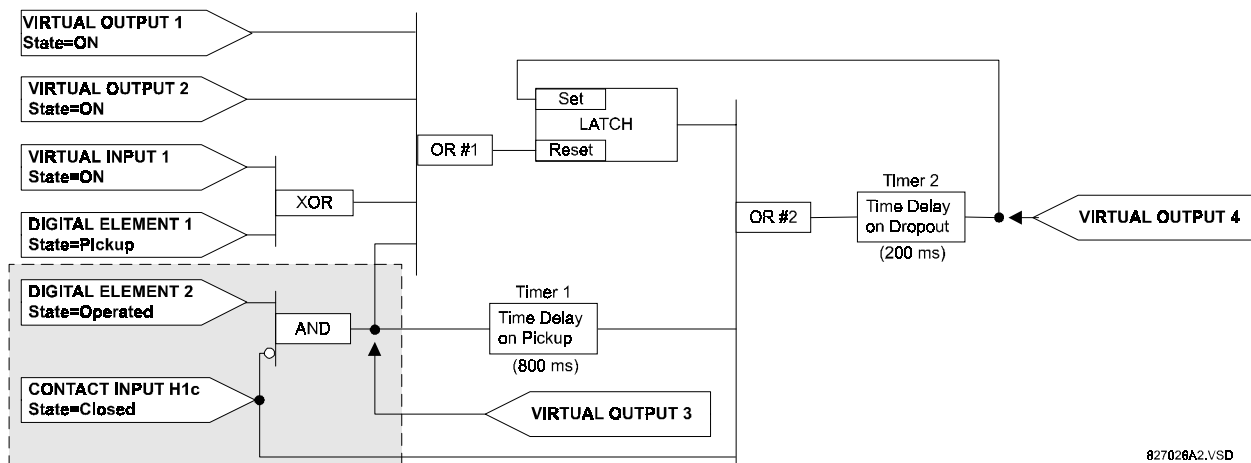
STEP 1:

The initial step in the process is to inspect the example logic diagram to determine that the required logic can be implemented with the types of operators provided by FlexLogic™. If this is not possible, the logic will have to be altered until this condition is satisfied. Once this is done, count the inputs to each gate to check that the number of inputs does not exceed the limits available in FlexLogic™, which is unlikely but possible. If the number of inputs is too high, subdivide the inputs into multiple gates to produce an equivalent. For example, if it is required to have 25 inputs to an AND gate, connect inputs 1 through 16 to one AND(16), 17 through 25 to another AND(9), and the outputs from these two gates to an AND(2).

Inspect each operator between the initial operands and final virtual outputs to determine if the output from the operator is used as an input to more than one following operator. If so, the output of this operator must be assigned as a Virtual Output.

In the example shown in the figure: EXAMPLE LOGIC SCHEME, the output of the AND gate is used as an input to both OR #1 and Timer 1, and must therefore be made a Virtual Output and be assigned the next available number (i.e. Virtual Output 3). The final output must also be assigned to a Virtual Output as Virtual Output 4, which will be programmed in the contact output section to operate relay H1 (i.e. Output Contact H1).

It is now determined that the required logic can be implemented in FlexLogic™ with two FlexLogic™ equations, with outputs of Virtual Output 3 and Virtual Output 4 as shown in the figure: LOGIC EXAMPLE WITH VIRTUAL OUTPUTS.



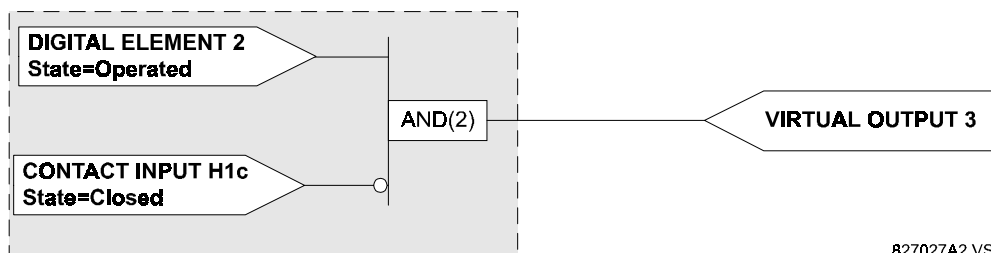
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Figure 5-7: LOGIC EXAMPLE WITH VIRTUAL OUTPUTS

STEP 2:

The next step is to prepare a logic diagram for the equation to produce Virtual Output 3, as this output will be used later as an operand in the equation for Virtual Output 4. (Create the equation for every output which will be used as an operand first, so that when these operands are required they will already have been evaluated and assigned to a specific Virtual Output.) The logic for Virtual Output 3 is shown in the figure: LOGIC FOR VIRTUAL OUTPUT 3, with the final output assigned.

5

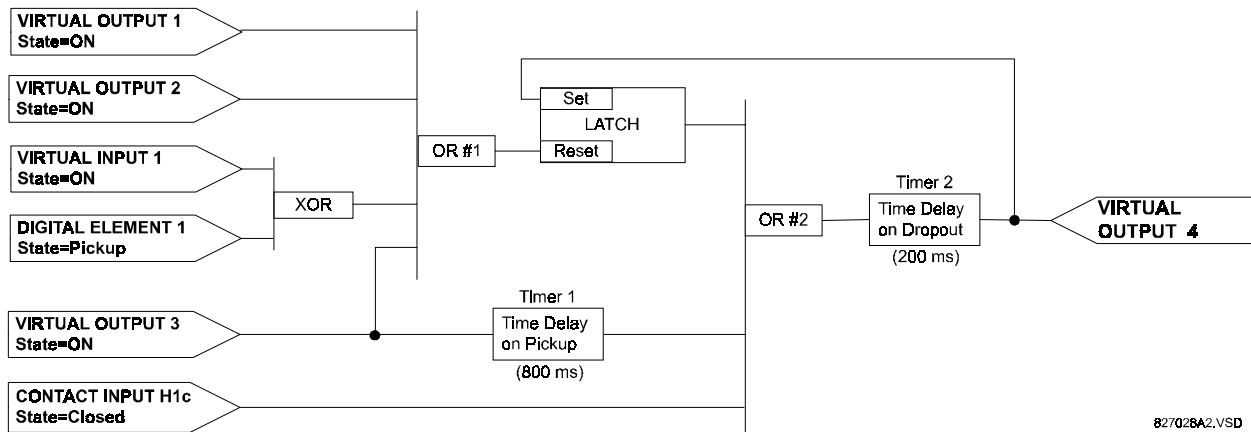


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Figure 5-8: LOGIC FOR VIRTUAL OUTPUT 3

STEP 3:

Next, prepare a logic diagram for Virtual Output 4, while replacing the logic ahead of Virtual Output 3 with a symbol identified as Virtual Output 3, as shown in the figure: LOGIC FOR VIRTUAL OUTPUT 4.



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Figure 5–9: LOGIC FOR VIRTUAL OUTPUT 4

STEP 4:

Now program the FlexLogic™ equation for Virtual Output 3 by translating the logic into the available Flex-Logic™ parameters. The equation is formed one parameter at a time, until the required logic is complete. It is generally easier to start at the output end of the equation and work back towards the input in this process, as shown in the following steps. It is also recommended to list operator inputs from bottom to top. For demonstration, the final output will be arbitrarily identified as parameter 99, and each preceding parameter decremented by one in turn. Until one is accustomed to using FlexLogic™, it is suggested that a worksheet with a series of cells marked with the arbitrary parameter numbers be prepared, as shown in the figure: FLEXLOGIC™ WORKSHEET.

01	
02	
03	
04	
05	
.....	
97	
98	
99	

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Figure 5–10: FLEXLOGIC™ WORKSHEET

STEP 5:

Following the procedure outlined, start with parameter 99, as follows:

99: The final output of the equation is Virtual Output 3, which is created by the operator "= Virt Op n". This parameter is therefore "= Virt Op 3."

98: The gate preceding the output is an AND, which in this case requires two inputs. The operator for this gate is a 2-input AND so the parameter is "AND(2)". Note that FlexLogic™ rules require that the number of inputs to most types of operators must be specified to identify the operands for the gate. As the 2-input AND will operate on the two operands preceding it, these inputs must be specified, starting with the lower.

97: This lower input to the AND gate must be passed through an inverter (the NOT operator) so the next parameter is "NOT". The NOT operator will act upon the operand immediately preceding it, so next specify the input to the inverter.

96: The input to the NOT gate is to be contact input H1c. The ON state of a contact input can be programmed to be set when the contact is either open or closed. Assume for this example the state is to be ON for a closed contact. The operand is therefore "Cont Ip H1c On".

95: The last step in the procedure is to specify the upper input to the AND gate, the operated state of digital element 2. This operand is "DIG ELEM 2 OP".

Writing the parameters in numerical order can now form the equation for VIRTUAL OUTPUT 3:

- [95] DIG ELEM 2 OP
- [96] Cont Ip H1c On
- [97] NOT
- [98] AND(2)
- [99] = Virt Op 3

It is now possible to check that this selection of parameters will produce the required logic by converting the set of parameters into a logic diagram. The result of this process is shown in figure FLEXLOGIC™ EQUATION & LOGIC FOR VIRTUAL OUTPUT 3, which is compared to figure: LOGIC FOR VIRTUAL OUTPUT 3 as a check.

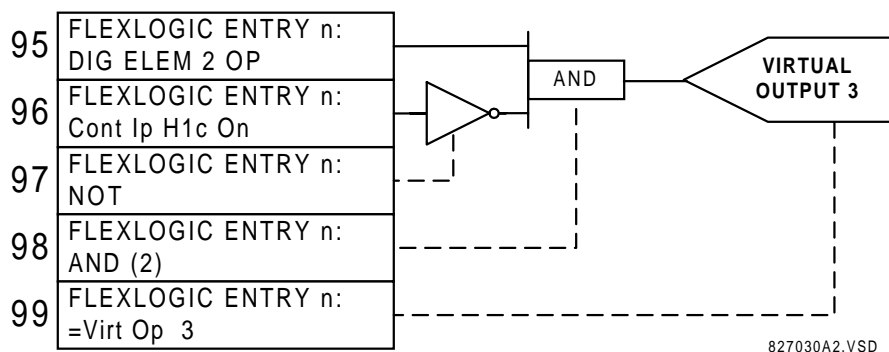


Figure 5–11: FLEXLOGIC™ EQUATION & LOGIC FOR VIRTUAL OUTPUT 3

STEP 6:

Repeating the process described for VIRTUAL OUTPUT 3, select the FlexLogic™ parameters for VIRTUAL OUTPUT 4.

99: The final output of the equation is VIRTUAL OUTPUT 4 which is parameter “= Virt Op 4”.

98: The operator preceding the output is Timer 2, which is operand “TIMER 2”. Note that the settings required for the timer are established in the timer programming section.

97: The operator preceding Timer 2 is OR #2, a 3-input OR, which is parameter “OR(3)”.

96: The lowest input to OR #2 is operand “Cont Ip H1c On”.

95: The center input to OR #2 is operand “TIMER 1”.

94: The input to Timer 1 is operand “Virt Op 3 On”.

93: The upper input to OR #2 is operand “LATCH (S,R)”.

92: There are two inputs to a latch, and the input immediately preceding the latch reset is OR #1, a 4-input OR, which is parameter “OR(4)”.

91: The lowest input to OR #1 is operand “Virt Op 3 On”.

90: The input just above the lowest input to OR #1 is operand “XOR(2)”.

89: The lower input to the XOR is operand “DIG ELEM 1 PKP”.

88: The upper input to the XOR is operand “Virt Ip 1 On”.

87: The input just below the upper input to OR #1 is operand “Virt Op 2 On”.

86: The upper input to OR #1 is operand “Virt Op 1 On”.

85: The last parameter is used to set the latch, and is operand “Virt Op 4 On”.

The equation for VIRTUAL OUTPUT 4 is:

- [85] Virt Op 4 On
- [86] Virt Op 1 On
- [87] Virt Op 2 On
- [88] Virt Ip 1 On
- [89] DIG ELEM 1 PKP
- [90] XOR(2)
- [91] Virt Op 3 On
- [92] OR(4)
- [93] LATCH (S,R)
- [94] Virt Op 3 On
- [95] TIMER 1
- [96] Cont Ip H1c On
- [97] OR(3)
- [98] TIMER 2
- [99] = Virt Op 4

It is now possible to check that the selection of parameters will produce the required logic by converting the set of parameters into a logic diagram. The result of this process is shown in figure: FLEXLOGIC™ EQUATION & LOGIC FOR VIRTUAL OUTPUT 4, which is compared to figure: LOGIC FOR VIRTUAL OUTPUT 4, as a check.

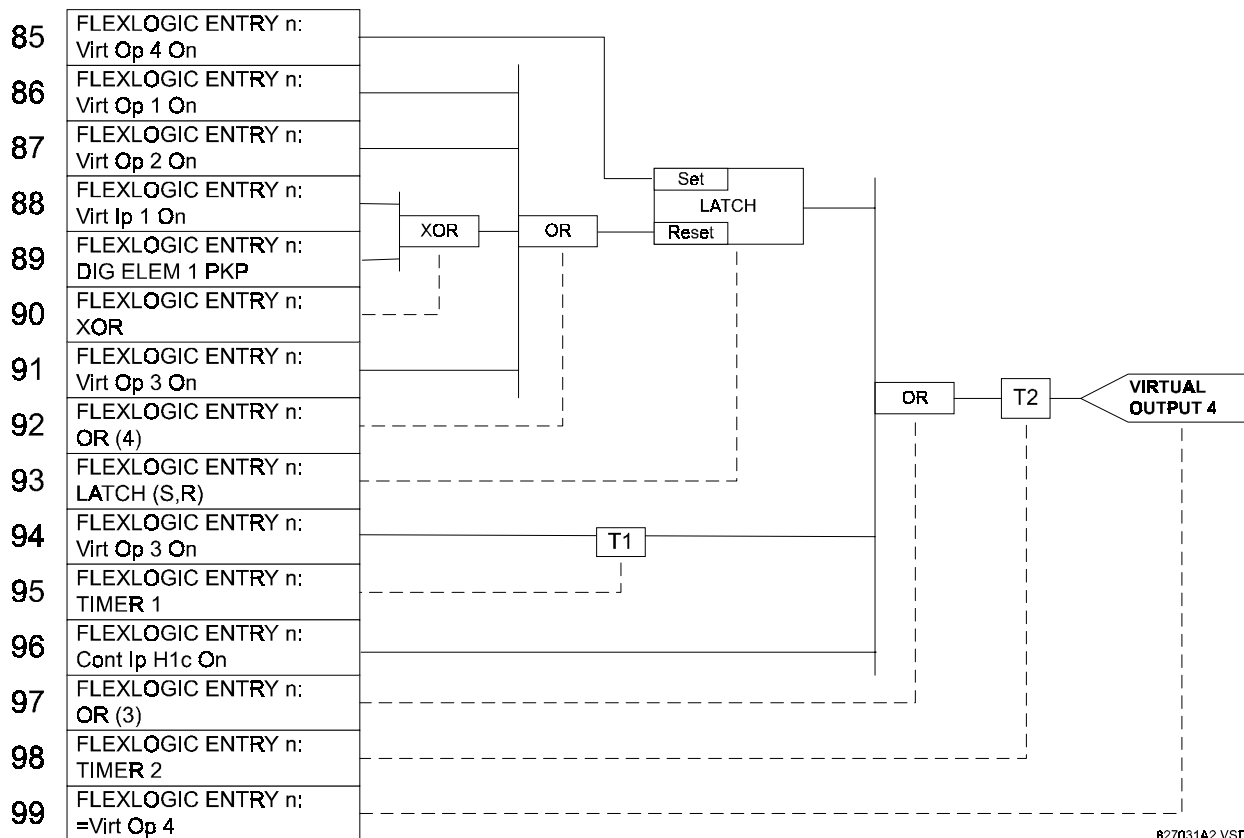


Figure 5-12: FLEXLOGIC™ EQUATION & LOGIC FOR VIRTUAL OUTPUT 4

STEP 7:

Now write the complete FlexLogic™ expression required to implement the required logic, making an effort to assemble the equation in an order where Virtual Outputs that will be used as inputs to operators are created before needed. In cases where a lot of processing is required to perform considerable logic, this may be difficult to achieve, but in most cases will not cause problems because all of the logic is calculated at least 4 times per power frequency cycle. The possibility of a problem caused by sequential processing emphasizes the necessity to test the performance of FlexLogic™ before it is placed in service.

In the following equation, VIRTUAL OUTPUT 3 is used as an input to both Latch 1 and Timer 1 as arranged in the order shown below:

- DIG ELEM 2 OP
- Cont Ip H1c On
- NOT
- AND(2)
- = Virt Op 3
- Virt Op 4 On
- Virt Op 1 On
- Virt Op 2 On
- Virt Ip 1 On
- DIG ELEM 1 PKP
- XOR(2)
- Virt Op 3 On
- OR(4)
- LATCH (S,R)
- Virt Op 3 On
- TIMER 1
- Cont Ip H1c On
- OR(3)
- TIMER 2
- = Virt Op 4
- END

In the expression above, the VIRTUAL OUTPUT 4 input to the 4-input OR is listed before it is created. This is typical of a form of feedback, in this case, used to create a seal-in effect with the latch, and is correct.

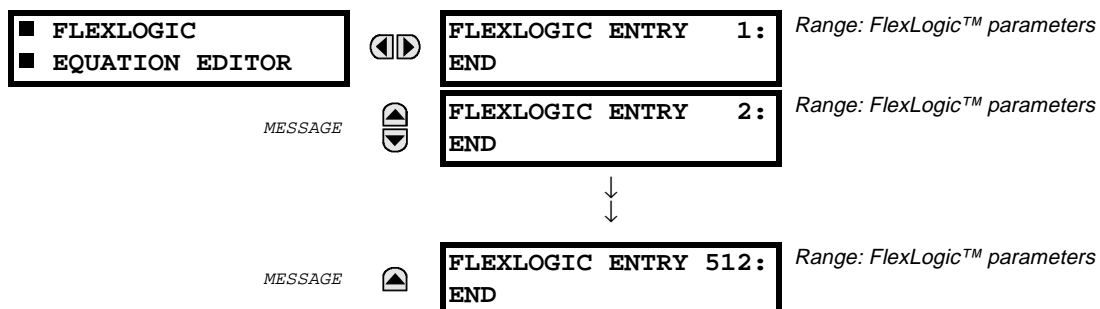
STEP 8:

The logic should always be tested after it is loaded into the relay, in the same fashion as has been used in the past. Testing can be simplified by placing an "END" operator within the overall set of FlexLogic™ equations. The equations will then only be evaluated up to the first "END" operator.

The "On" and "Off" operands can be placed in an equation to establish a known set of conditions for test purposes, and the "INSERT" and "DELETE" commands can be used to modify equations.

5.4.2 FLEXLOGIC™ EQUATION EDITOR

PATH: SETTINGS ↓ FLEXLOGIC ⇌ FLEXLOGIC EQUATION EDITOR



There are 512 FlexLogic™ entries available, numbered from 1 to 512, with default 'END' entry settings.

If a 'disabled' Element is selected as a FlexLogic™ entry, the associated state flag will never be set to '1'.

The '+/-' key may be used when editing FlexLogic™ equations from the keypad to quickly scan through the major parameter types.

a) FLEXLOGIC™ EQUATION FOR FACEPLATE LEDS

The following FlexLogic™ equations have been programmed at the factory for the default operation of faceplate LEDs (see Chapter 4 - FACEPLATE INTERFACE).

Table 5-8: REQUIRED LED PROGRAMMING IN FLEXLOGIC

SETTING	PARAMETER	SETTING	PARAMETER
FLEXLOGIC ENTRY 1:	NEUTRAL IOC1 OP	FLEXLOGIC ENTRY 14:	RESET OP
FLEXLOGIC ENTRY 2:	RESET OP	FLEXLOGIC ENTRY 15:	LATCH (S,R)
FLEXLOGIC ENTRY 3:	LATCH (S,R)	FLEXLOGIC ENTRY 16:	= Virt Op 4
FLEXLOGIC ENTRY 4:	= Virt Op 1	FLEXLOGIC ENTRY 17:	PHASE TOC1 OP
FLEXLOGIC ENTRY 5:	PHASE IOC1 OP	FLEXLOGIC ENTRY 18:	RESET OP
FLEXLOGIC ENTRY 6:	RESET OP	FLEXLOGIC ENTRY 19:	LATCH (S,R)
FLEXLOGIC ENTRY 7:	LATCH (S,R)	FLEXLOGIC ENTRY 20:	= Virt Op 5
FLEXLOGIC ENTRY 8:	= Virt Op 2	FLEXLOGIC ENTRY 21:	87PC OP
FLEXLOGIC ENTRY 9:	NEG SEQ TOC1 OP	FLEXLOGIC ENTRY 22:	RESET OP
FLEXLOGIC ENTRY 10:	RESET OP	FLEXLOGIC ENTRY 23:	LATCH (S,R)
FLEXLOGIC ENTRY 11:	LATCH (S,R)	FLEXLOGIC ENTRY 24:	= Virt Op 6
FLEXLOGIC ENTRY 12:	= Virt Op 3	FLEXLOGIC ENTRY 25:	END
FLEXLOGIC ENTRY 13:	NEUTRAL TOC1 OP		

5.4.3 FLEXLOGIC™ TIMERS

PATH: SETTING ↓ FLEXLOGIC ⇨ ↓ FLEXLOGIC TIMERS ⇨ FLEXLOGIC TIMER 1(32)

<div> <div>■ FLEXLOGIC</div> <div>■ TIMER 1</div> </div>	<div>◀▶</div>	<div>TIMER 1</div> <div>TYPE: millisecond</div>	Range: millisecond, second, minute
		<div>TIMER 1 PICKUP</div> <div>DELAY: 0</div>	Range: 0 to 60000 in steps of 1
		<div>TIMER 1 DROPOUT</div> <div>DELAY: 0</div>	Range: 0 to 60000 in steps of 1

There are 32 identical FlexLogic™ timers available, numbered from 1 to 32.

These timers can be used as operators for FlexLogic™ equations.

TIMER 1 TYPE:

This setting is used to select the time measuring unit.

TIMER 1 PICKUP DELAY:

This setting is used to set the time delay to pickup. If a pickup delay is not required, set this function to '0'.

TIMER 1 DROPOUT DELAY:

This setting is used to set the time delay to dropout. If a dropout delay is not required, set this function to '0'.

5.5.1 OVERVIEW

Each protection element can be assigned up to 8 different sets of settings according to SETTING GROUP designations from 1 to 8. The performance of any of these elements is defined by the SETTING GROUP that is active at a given time. Multiple setting groups provide the capability to conveniently change protection settings for different operating situations (e.g. altered power system configuration, another season of the year). The active setting group can be pre-set or selected via the SETTING GROUPS menu (see the section CONTROL ELEMENTS). See also the section INTRODUCTION TO ELEMENTS at the front of this chapter.

5.5.2 SETTING GROUP 1(8)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8)

5	■ SETTING GROUP 1 ■	◀▶	■ LINE PICKUP ■	See page 5-55.
	MESSAGE	▲▼	■ DISTANCE ■	See page 5-57.
	MESSAGE	▲▼	■ POWER SWING DETECT ■	See page 5-65.
	MESSAGE	▲▼	■ PHASE CURRENT ■	See page 5-79.
	MESSAGE	▲▼	■ NEUTRAL CURRENT ■	See page 5-82.
	MESSAGE	▲▼	■ GROUND CURRENT ■	See page 5-85.
	MESSAGE	▲▼	■ NEGATIVE SEQUENCE ■ CURRENT	See page 5-88.
	MESSAGE	▲▼	■ BREAKER FAILURE ■	See page 5-91.
	MESSAGE	▲	■ VOLTAGE ELEMENTS ■	See page 5-103.

Each of the 8 SETTING GROUP menus is identical. SETTING GROUP 1 (the default active group) automatically becomes active if no other group is active (see section SETTINGS \ CONTROL ELEMENTS \ SETTING GROUPS).

5.5.3 LINE PICKUP

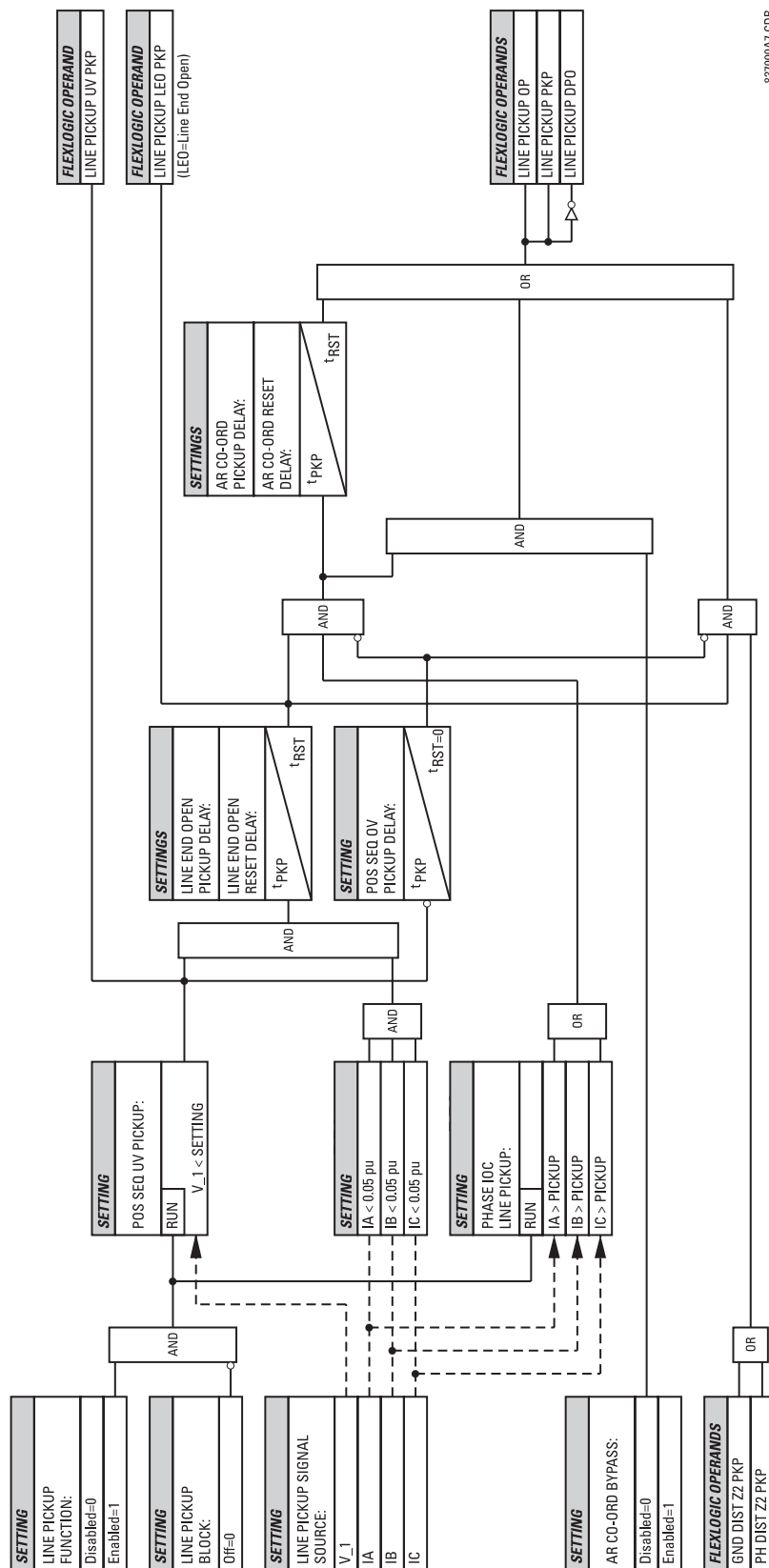
PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ LINE PICKUP

■ LINE PICKUP	◀▶	LINE PICKUP FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	LINE PICKUP SIGNAL SOURCE: SRC 1	Range: SRC 1, ..., SRC 6
MESSAGE	▲▼	PHASE IOC LINE PICKUP: 1.000 pu	Range: 0.000 to 30.000 in steps of 0.001 pu
MESSAGE	▲▼	POS SEQ UV PICKUP: 0.700 pu	Range: 0.000 to 3.000 in steps of 0.001 pu
MESSAGE	▲▼	LINE END OPEN PICKUP DELAY: 0.150 s	Range: 0.000 to 65.535 in steps of 0.001 s
MESSAGE	▲▼	LINE END OPEN RESET DELAY: 0.090 s	Range: 0.000 to 65.535 in steps of 0.001 s
MESSAGE	▲▼	POS SEQ OV PICKUP DELAY: 0.040 s	Range: 0.000 to 65.535 in steps of 0.001 s
MESSAGE	▲▼	AR CO-ORD BYPASS: Enabled	Range: Disabled, Enabled
MESSAGE	▲▼	AR CO-ORD PICKUP DELAY: 0.045 s	Range: 0.000 to 65.535 in steps of 0.001 s
MESSAGE	▲▼	AR CO-ORD RESET DELAY: 0.005 s	Range: 0.000 to 65.535 in steps of 0.001 s
MESSAGE	▲▼	LINE PICKUP BLOCK: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	LINE PICKUP TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲	LINE PICKUP EVENTS: Disabled	Range: Disabled, Enabled

The line pickup feature uses a combination of undercurrent and undervoltage to identify a line that has been de-energized (line end open). Three instantaneous overcurrent elements are used to identify a previously de-energized line that has been closed onto a fault which could be due to maintenance grounds that have not been removed. Faults other than close-in faults can be identified satisfactorily by the distance elements which initially will be self or faulted phase polarized and then become memory polarized when a satisfactory memory signal is available.

Co-ordination features are included to ensure satisfactory operation when high speed 'automatic reclosure (AR)' is employed. The AR CO-ORD DELAY setting allows the overcurrent setting to be below the expected load current seen after reclose. Co-ordination is achieved by the POS SEQ OV element picking up and blocking the trip path, before the AR CO-ORD DELAY times out. The AR CO-ORD BYPASS setting is normally enabled. It is disabled if high speed AR is implemented.

The positive sequence undervoltage pickup setting is based on phase to neutral quantities. If Delta VTs are used, then this per unit pickup is based on the $(VT \text{ secondary setting}) / \sqrt{3}$.

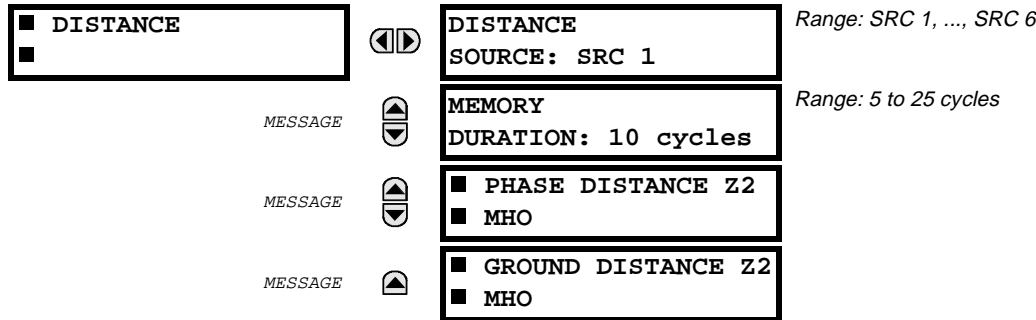


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Figure 5-13: LINE PICKUP SCHEME LOGIC

5.5.4 DISTANCE BACKUP

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ DISTANCE



Two common distance settings and two menus for one zone of phase and ground distance protection specify the distance backup feature.

COMMON DISTANCE SETTINGS:**DISTANCE SOURCE:**

The source setting identifies the Signal Source for the distance backup function.

MEMORY DURATION:

Both phase and ground distance functions use a dynamic mho characteristic: the positive-sequence voltage – either memorized or actual – is used as a polarizing signal.

This setting specifies the length of time a memorized positive-sequence voltage should be used in the distance calculations. After this interval expires, the relay checks the magnitude of the actual positive-sequence voltage. If it is higher than 10% of the nominal, the actual voltage is used, if lower - the memory voltage continues to be used.

The memory is established when the positive-sequence voltage stays above 80% of its nominal value for five power system cycles. For this reason it is important to ensure that the nominal secondary voltage of the VT is entered correctly under the **SETTINGS / SYSTEM SETUP / AC INPUTS / VOLTAGE BANK** menu.

The **MEMORY DURATION** should be set long enough to ensure stability on close-in reverse three-phase faults. For this purpose, the maximum fault clearing time (breaker fail time) in the substation should be considered.

On the other hand, the **MEMORY DURATION** cannot be too long as the power system may experience power swing conditions rotating the voltage and current phasors slowly while the memory voltage is static, as frozen at the beginning of the fault. Keeping the memory in effect for too long may eventually cause maloperation of the distance functions.

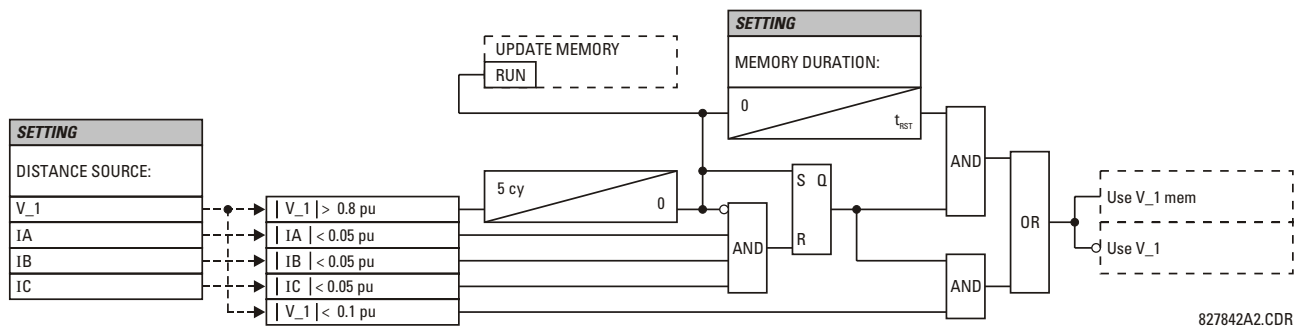


Figure 5-14: MEMORY VOLTAGE LOGIC

a) PHASE DISTANCE Z2

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ DISTANCE ⇒ ↓ PHASE DISTANCE Z2 MHO

<div> <div>■ PHASE DISTANCE Z2</div> <div>■ MHO</div> </div>		<div> <div>◀▶</div> <div>PHS DIST Z2 MHO</div> <div>FUNCTION: Disabled</div> </div>	Range: Disabled, Enabled
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO</div> <div>SUPV: 0.200 pu</div> </div>	Range: 0.050 to 30.000 pu in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO</div> <div>REACH: 2.00 Ω</div> </div>	Range: 0.10 to 250.00 ohms in steps of 0.01 (1 A CT) 0.02 to 250.00 ohms in steps of 0.01 (5 A CT)
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO</div> <div>DIRECTION: Forward</div> </div>	Range: Forward, Reverse
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO</div> <div>COMP LIMIT: 90°</div> </div>	Range: 60 to 90° in steps of 1
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO</div> <div>DELAY: 0.000 s</div> </div>	Range: 0.000 to 65.535 in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO BLK:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>PHS DIST Z2 MHO</div> <div>TARGET: Self-reset</div> </div>	Range: Self-reset, Latched, Disabled
	MESSAGE	<div> <div>▲</div> <div>PHS DIST Z2 MHO</div> <div>EVENTS: Disabled</div> </div>	Range: Disabled, Enabled

The phase distance elements use a dynamic mho characteristic with additional reactance, directional, and current supervision functions.

This setting menu configures the basic distance settings except:

- Signal Source (common for both phase and ground elements as entered under the SETTINGS / GROUPED ELEMENTS / SETTING GROUP 1(8) / DISTANCE).
- Memory duration (common for both phase and ground elements as entered under the SETTINGS / GROUPED ELEMENTS / SETTING GROUP 1(8) / DISTANCE).
- Characteristic angle of the distance function (common for both phase and ground elements; the angle used is the positive-sequence impedance angle of the line as entered under the SETTINGS / SYSTEM SETUP / LINE menu).

The above common distance settings must be properly chosen for correct operation of the phase distance element.



Ensure that the Phase VT Secondary Voltage setting (see Settings \ System Setup \ AC Inputs \ Voltage Bank menu) is set correctly to prevent improper operation of associated memory action.

SETTINGS:**PHS DIST Z2 MHO SUPV:**

The phase distance elements are supervised by the magnitude of the line-to-line current (fault loop current used for the distance calculations). For convenience, $\sqrt{3}$ is accommodated by the pickup (i.e., before being used, the entered value of the threshold setting is multiplied by $\sqrt{3}$).

If the minimum fault current level is sufficient, the current supervision pickup should be set above maximum full load current preventing maloperation under VT fuse fail conditions. This requirement may be difficult to meet if the long distance reach is intended. If this is the case, the current supervision pickup would be set below the full load current, but this may result in maloperation during fuse fail conditions.

PHS DIST Z2 MHO REACH:

This setting defines the reach of the zone. The characteristic angle (similar to the “maximum torque angle” in previous technologies) is not adjustable and equals the angle of the positive-sequence impedance of the line. The same characteristic angle applies to the mho, reactance and directional comparators of the distance elements.

The reach impedance is entered in secondary ohms.

PHS DIST Z2 MHO DIRECTION:

The zone is reversible. The forward direction is defined by the angle of the positive-sequence impedance of the line, whereas the reverse direction is shifted by 180°.

PHS DIST Z2 MHO COMP LIMIT:

This setting enables the user to shape the operating characteristic. In particular, it produces the lens-type characteristic, which increases loadability of the protected line. The same limit angle applies to the mho, reactance and directional comparators of the distance element.

PHS DIST Z2 MHO DELAY:

This setting enables the user to delay operation of the distance element and implement a stepped distance backup protection.

The distance element timer applies a short drop out delay to cope with faults located close to the boundary of the zone when small oscillations in the voltages and/or currents could inadvertently reset the timer.

PHS DIST Z2 MHO BLK:

This setting enables the user to select a FlexLogic™ operand to block the distance element. VT fuse fail detection is one of the applications for this setting.

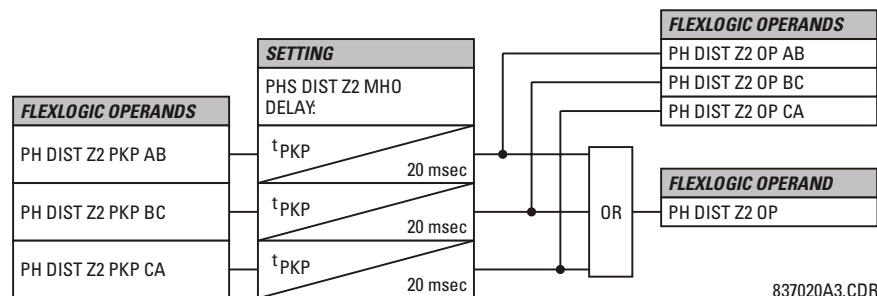


Figure 5-15: PHASE DISTANCE Z2 MHO OP SCHEME

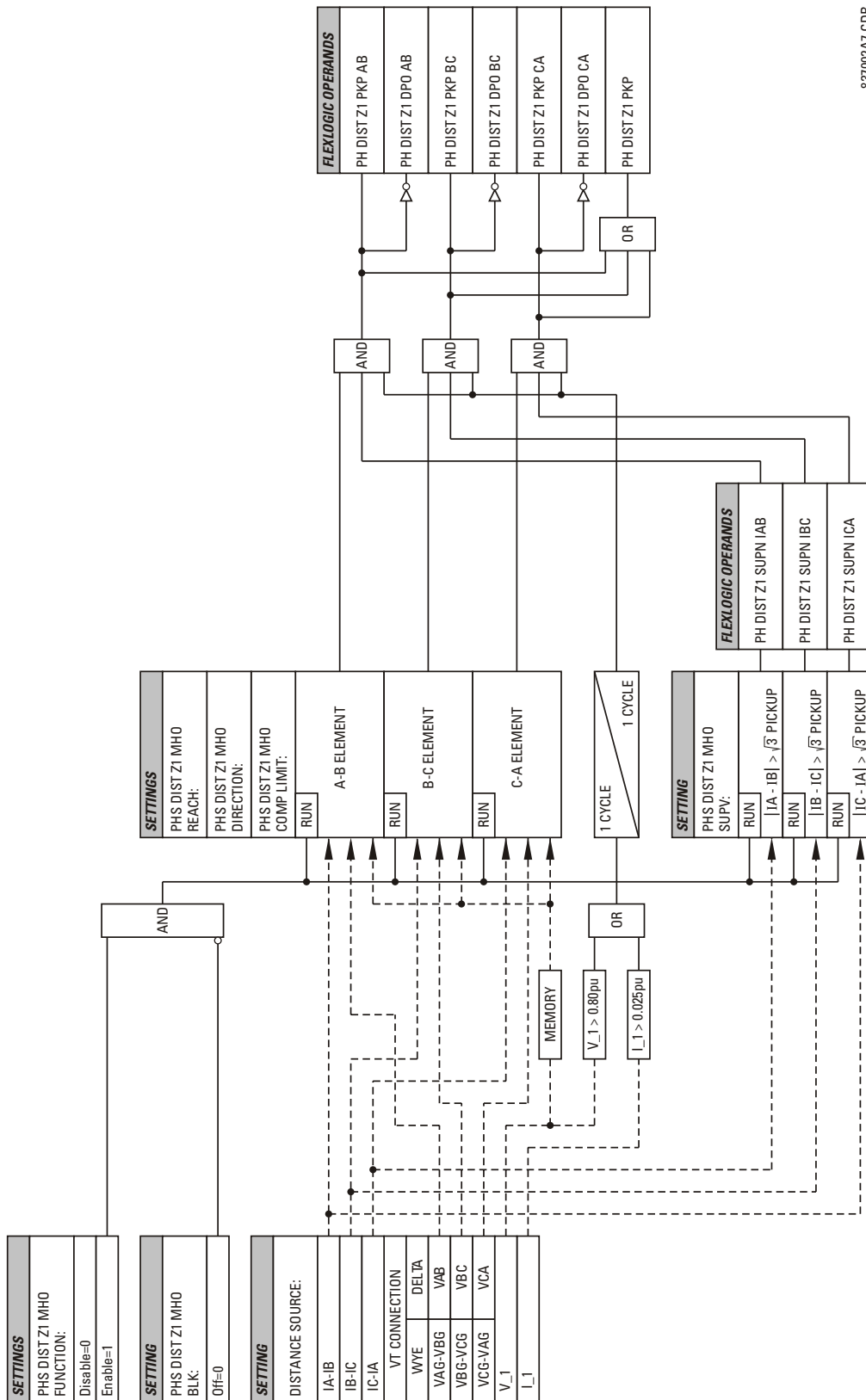


Figure 5-16: PHASE DISTANCE Z2 MHO SCHEME LOGIC

b) GROUND DISTANCE Z2

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ DISTANCE ⇒ ↓ GROUND DISTANCE Z2 MHO

■ GROUND DISTANCE Z2 ■ MHO		GND DIST Z2 MHO FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE		GND DIST Z2 MHO SUPV: 0.200 pu	Range: 0.050 to 30.000 pu in steps of 0.001
MESSAGE		GND DIST Z2 MHO REACH: 2.00 Ω	Range: 0.10 to 250.00 ohms in steps of 0.01 (1 A CT) 0.02 to 250.00 ohms in steps of 0.01 (5 A CT)
MESSAGE		GND DIST Z2 MHO DIRECTION: Forward	Range: Forward, Reverse
MESSAGE		GND DIST Z2 MHO COMP LIMIT: 90°	Range: 60 to 90° in steps of 1°
MESSAGE		GND DIST Z2 MHO DELAY: 0.000 s	Range: 0.000 to 65.535 in steps of 0.001
MESSAGE		GND DIST Z2 MHO BLK: Off	Range: FlexLogic™ Operand
MESSAGE		GND DIST Z2 MHO TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE		GND DIST Z2 MHO EVENTS: Disabled	Range: Disabled, Enabled

The ground distance element uses a dynamic mho characteristic with additional reactance, directional, current, and phase selection supervision functions.

The reactance supervision uses zero-sequence current as a polarizing quantity making the characteristic adaptable to the pre-fault power flow. The directional supervision uses memory voltage as polarizing quantity and both zero- and negative-sequence currents as operating quantities. The phase selection supervision restrains the ground elements during double-line-to-ground faults as they – by principle of distance relaying – may be inaccurate in such conditions.

The ground distance element applies additional zero-sequence directional supervision. This setting menu configures the basic distance settings except:

- Signal Source (common for both phase and ground elements as entered under the SETTINGS / GROUPED ELEMENTS / SETTING GROUP 1(8) / DISTANCE).
- Memory duration (common for both phase and ground elements as entered under the SETTINGS / GROUPED ELEMENTS / SETTING GROUP 1(8) / DISTANCE).
- Characteristic angle of the distance function (Common for both phase and ground elements. The angle used is the positive-sequence impedance angle of the line as entered under the SETTINGS / SYSTEM SETUP / LINE menu).
- Zero-sequence compensating factor (Calculated from the zero- and positive-sequence impedances of the line as entered under the SETTINGS / SYSTEM SETUP / LINE menu).

The common distance settings above must be properly chosen for correct operation of the ground distance elements.



Ensure that the Phase VT Secondary Voltage setting (see Settings \ System Setup \ AC Inputs \ Voltage Bank menu) is set correctly to prevent improper operation of associated memory action.

SETTINGS:

GND DIST Z2 MHO SUPV:

The ground distance elements are supervised by the magnitude of the neutral (3I₀) current.

The current supervision pickup should be set above the maximum unbalance current under maximum load conditions preventing maloperation due to VT fuse failure.

GND DIST Z2 MHO REACH:

Defines the reach of the zone. The characteristic angle (similar to the “maximum torque angle” in previous technologies) is not adjustable and equals the angle of the positive-sequence impedance of the line. The same characteristic angle applies to the mho, reactance and directional comparators of the distance elements.

The reach impedance is entered in secondary ohms.

GND DIST Z2 MHO DIRECTION:

The zone is reversible. The forward direction is defined by the angle of the positive-sequence impedance of the line, whereas the reverse direction is shifted by 180°.

GND DIST Z2 MHO COMP LIMIT:

This setting enables the user to shape the operating characteristic. In particular, it produces the lens-type characteristic, which increases loadability of the protected line. The same limit angle applies to the mho, reactance and directional comparators of the distance elements.

Unavoidably, the fault resistance coverage gets reduced when the limit angle is set below the default of 90°.

GND DIST Z2 MHO DELAY:

This setting enables the user to delay operation of the distance elements and implement a stepped distance backup protection. The distance element timer applies a short drop out delay to cope with faults located close to the boundary of the zone when small oscillations in the voltages and/or currents could inadvertently reset the timer.

GND DIST Z2 MHO BLK:

This setting enables the user to select a FlexLogic™ operand to block the given distance element. VT fuse fail detection is one of the applications for this setting.

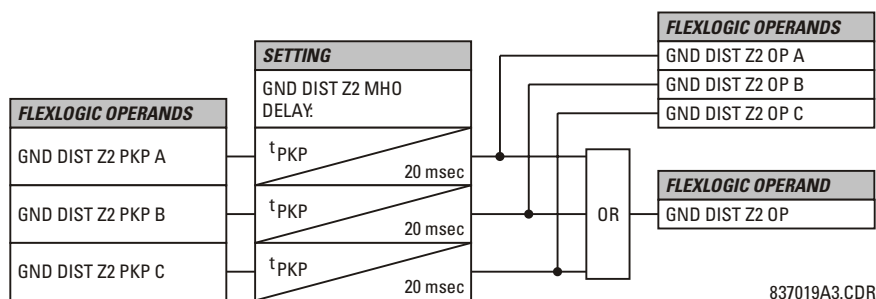


Figure 5-17: GROUND DISTANCE Z2 MHO OP SCHEME

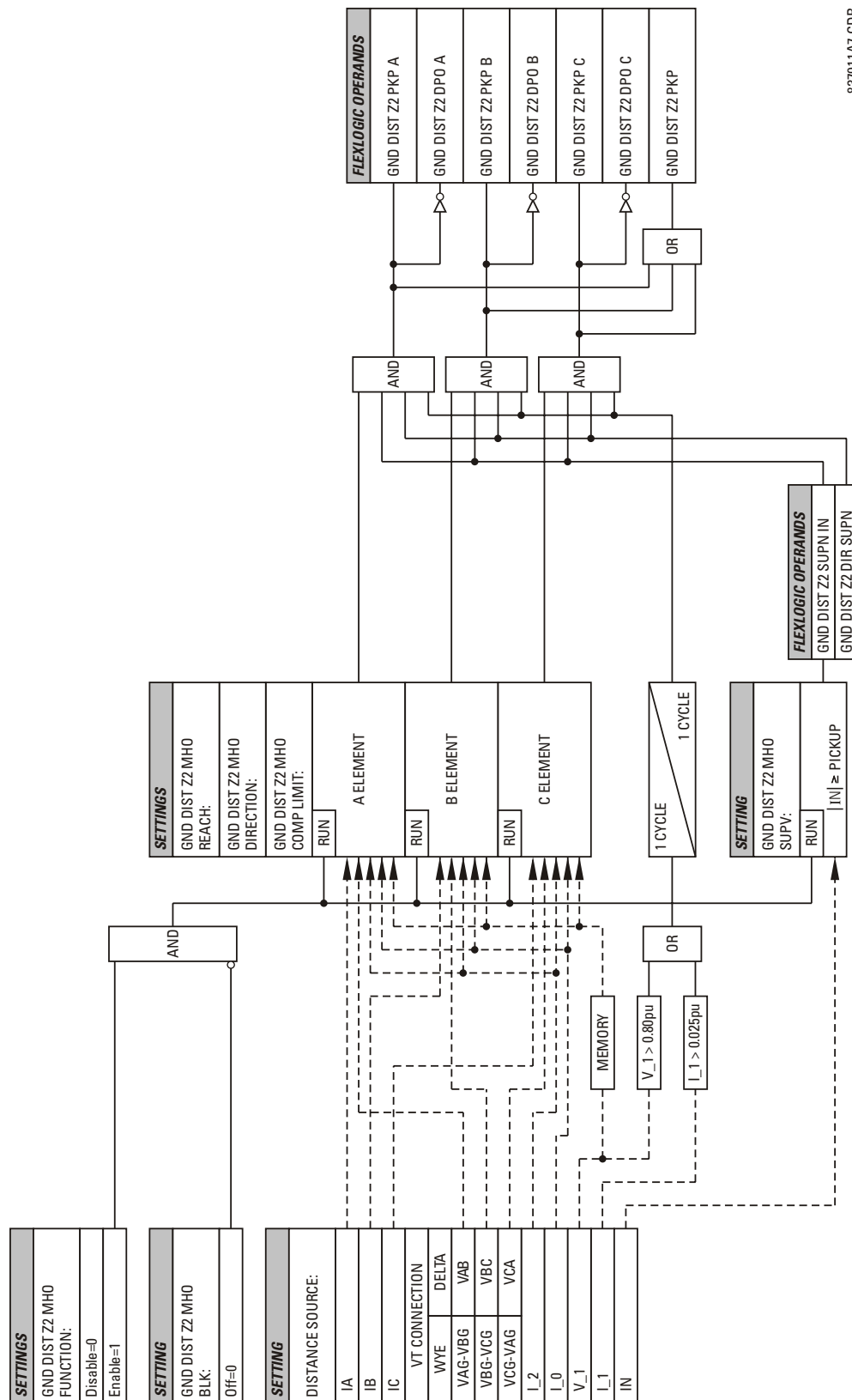


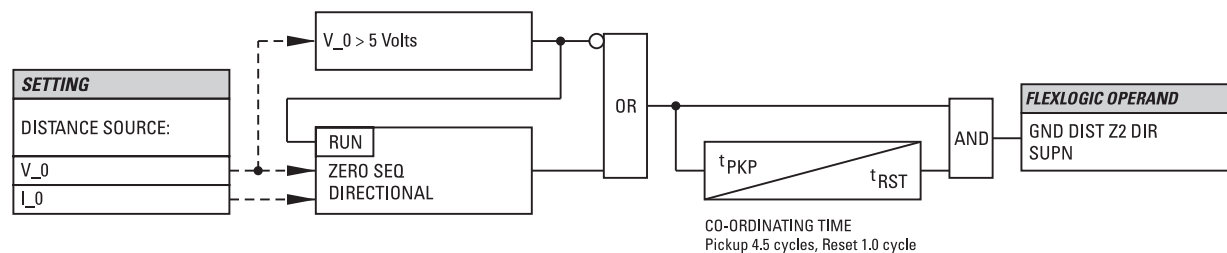
Figure 5–18: GROUND DISTANCE Z2 MHO SCHEME LOGIC

GROUND DIRECTIONAL SUPERVISION

A dual (zero- and negative-sequence) memory-polarized directional supervision applied to the ground distance protection elements has been shown to give good directional integrity. However, a reverse double-line-to-ground fault can lead to a maloperation of the ground element in a sound phase if the zone reach setting is increased to cover high resistance faults.

Ground distance Zone 2 uses additional ground directional supervision to enhance directional integrity. The angle of the positive-sequence impedance of the line as entered under SETTINGS / SYSTEM SETUP / LINE is used as the characteristic angle ("maximum torque angle") together with a 90° limit angle.

The supervision is biased toward operation in order to avoid compromising the sensitivity of ground distance elements at low signal levels. Otherwise, the reverse fault condition that generates concern will have high polarizing levels so that a correct reverse fault decision can be reliably made.



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Figure 5–19: GROUND DIRECTIONAL SUPERVISION

5.5.5 POWER SWING DETECT

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ POWER SWING DETECT

■ POWER SWING DETECT ■	◀▶	POWER SWING FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	POWER SWING SOURCE: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	POWER SWING MODE: 2-step	Range: 2-step, 3-step
MESSAGE	▲▼	POWER SWING SUPV: 0.600 pu	Range: 0.050 to 30.000 pu in steps of 0.001 pu
MESSAGE	▲▼	POWER SWING FWD REACH: 50.00 ohms	Range: 0.50 to 500.00 ohms in steps of 0.05 (1 A CT) 0.10 to 100.00 ohms in steps of 0.01 (5 A CT)
MESSAGE	▲▼	POWER SWING FWD RCA: 75°	Range: 40 to 90° in steps of 1°
MESSAGE	▲▼	POWER SWING REV REACH: 50.00 ohms	Range: 0.50 to 500.00 ohms in steps of 0.05 (1 A CT) 0.10 to 100.00 ohms in steps of 0.01 (5 A CT)
MESSAGE	▲▼	POWER SWING OUTER LIMIT ANGLE: 120°	Range: 40 to 140° in steps of 1°
MESSAGE	▲▼	POWER SWING MIDDLE LIMIT ANGLE: 90°	Range: 40 to 140° in steps of 1°
MESSAGE	▲▼	POWER SWING INNER LIMIT ANGLE: 60°	Range: 40 to 140° in steps of 1°
MESSAGE	▲▼	POWER SWING PICKUP DELAY 1: 0.030 s	Range: 0.000 to 65.535 sec. in steps of 0.001
MESSAGE	▲▼	POWER SWING RESET DELAY 1: 0.050 s	Range: 0.000 to 65.535 sec. in steps of 0.001
MESSAGE	▲▼	POWER SWING PICKUP DELAY 2: 0.017 s	Range: 0.000 to 65.535 sec. in steps of 0.001
MESSAGE	▲▼	POWER SWING PICKUP DELAY 3: 0.009 s	Range: 0.000 to 65.535 sec. in steps of 0.001
MESSAGE	▲▼	POWER SWING PICKUP DELAY 4: 0.017 s	Range: 0.000 to 65.535 sec. in steps of 0.001
MESSAGE	▲▼	POWER SWING SEAL-IN DELAY 1: 0.400 s	Range: 0.000 to 65.535 sec. in steps of 0.001
MESSAGE	▲▼	POWER SWING TRIP MODE: Delayed	Range: Early, Delayed
MESSAGE	▲▼	POWER SWING BLK: Off	Range: Flexlogic™ Operand
MESSAGE	▲▼	POWER SWING TARGET: Self-Reset	Range: Self-Reset, Latched, Disabled
MESSAGE	▲	POWER SWING EVENTS: Disabled	Range: Disabled, Enabled

The POWER SWING DETECT protection element provides both power swing blocking and out-of-step tripping functions. The element measures the positive-sequence apparent impedance and traces its locus with respect to either two or three operating characteristic boundaries as per user choice. Upon detecting appropriate timing relations the blocking and/or tripping indication is given through FlexLogic™ operands. The POWER SWING OPERATING CHARACTERISTICS and POWER SWING LOGIC figures should be viewed along with the following discussion to develop an understanding of the operation of the element.

a) POWER SWING BLOCKING

Three-step operation:

The power swing blocking sequence essentially times the passage of the locus of the positive-sequence impedance between the outer and the middle characteristic boundaries. If the locus enters the outer characteristic (as indicated by setting of the POWER SWING OUTER FlexLogic™ operand) but stays outside the middle characteristic (as indicated by setting of the POWER SWING MIDDLE FlexLogic™ operand) for an interval longer than POWER SWING PICKUP DELAY 1 the power swing blocking signal (POWER SWING BLOCK FlexLogic™ operand) is established and sealed-in. The blocking signal resets when the locus leaves the outer characteristic, but not sooner than after POWER SWING RESET DELAY 1 time.

Two-step operation:

If the 2-step mode is selected, the sequence is identical, but it is the outer and inner characteristics that are used to time the power swing locus.

b) OUT-OF-STEP TRIPPING

Three-step operation:

The out-of-step trip sequence identifies unstable power swings by determining if the impedance locus spends a finite time between the outer and middle characteristics and then a finite time between the middle and inner characteristics.

The first step is similar to the power swing blocking sequence. After timer POWER SWING PICKUP DELAY 1 times out, Latch 1 is set as long as the impedance stays within the outer characteristic.

If afterwards, at any time (given the impedance stays within the outer characteristic), the locus enters the middle characteristic but stays outside the inner characteristic for a period of time defined as POWER SWING PICKUP DELAY 2, Latch 2 is set as long as the impedance stays inside the outer characteristic.

If afterwards, at any time (given the impedance stays within the outer characteristic), the locus enters the inner characteristic and stays there for a period of time defined as POWER SWING PICKUP DELAY 3, Latch 2 is set as long as the impedance stays inside the outer characteristic - the element is now ready to trip.

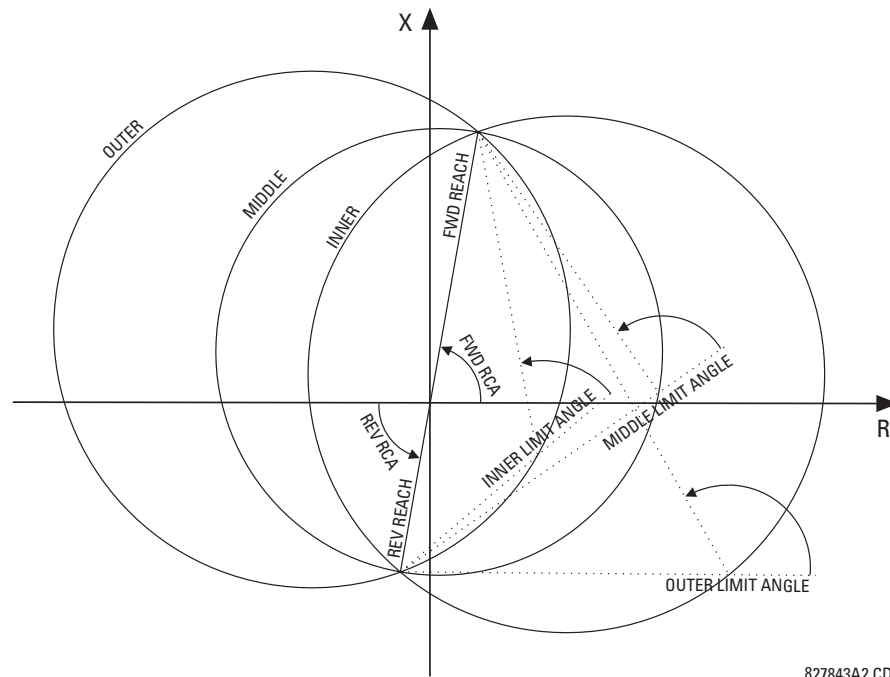
If the "Early" trip mode is selected, operand POWER SWING TRIP is set immediately and is sealed-in for the interval established by setting POWER SWING SEAL-IN DELAY.

If the "Delayed" trip mode is selected, the element waits until the impedance locus leaves the inner characteristic, then times out the POWER SWING PICKUP DELAY 2 delay, and sets Latch 4 - the element is now ready to trip. The trip operand will be set later, when the impedance locus leaves the outer characteristic.

Two-step operation:

The 2-step mode of operation is similar to the 3-step mode with two exceptions. First, the initial stage monitors the time spent by the impedance locus between the outer and inner characteristics. Second, the stage involving timer POWER SWING PICKUP DELAY 2 is bypassed.

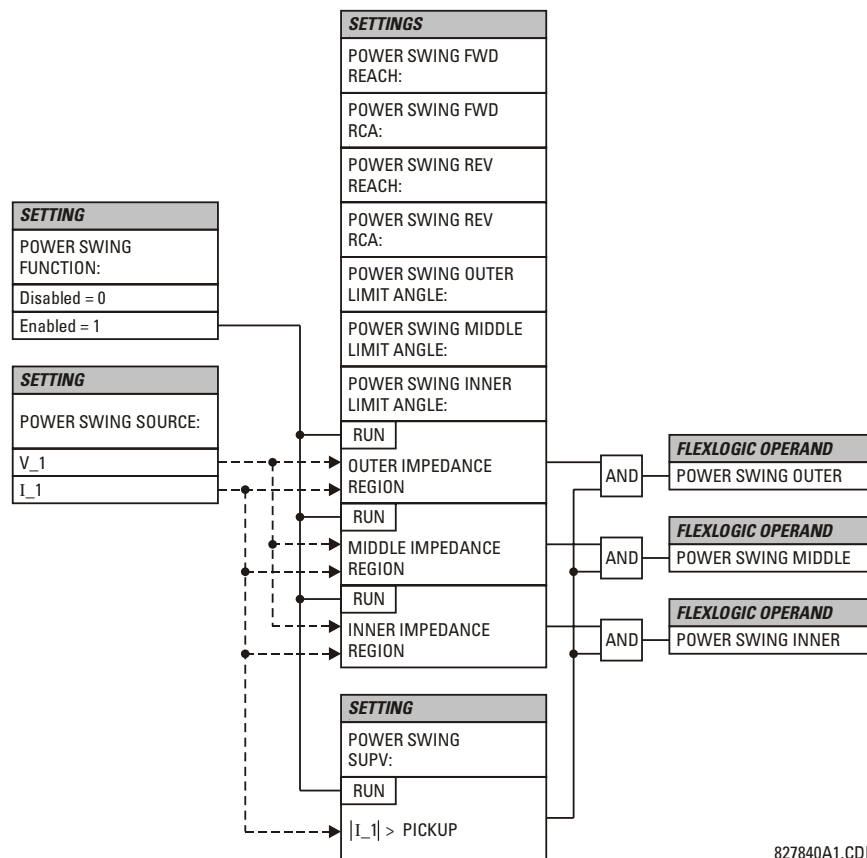
It is up to the user to integrate the blocking (POWER SWING BLOCK) and tripping (POWER SWING TRIP) FlexLogic™ operands with other protection functions and output contacts in order to make this element fully operational.



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Figure 5-20: POWER SWING DETECT ELEMENT OPERATING CHARACTERISTICS

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Figure 5-21: POWER SWING DETECT LOGIC (1 of 2)

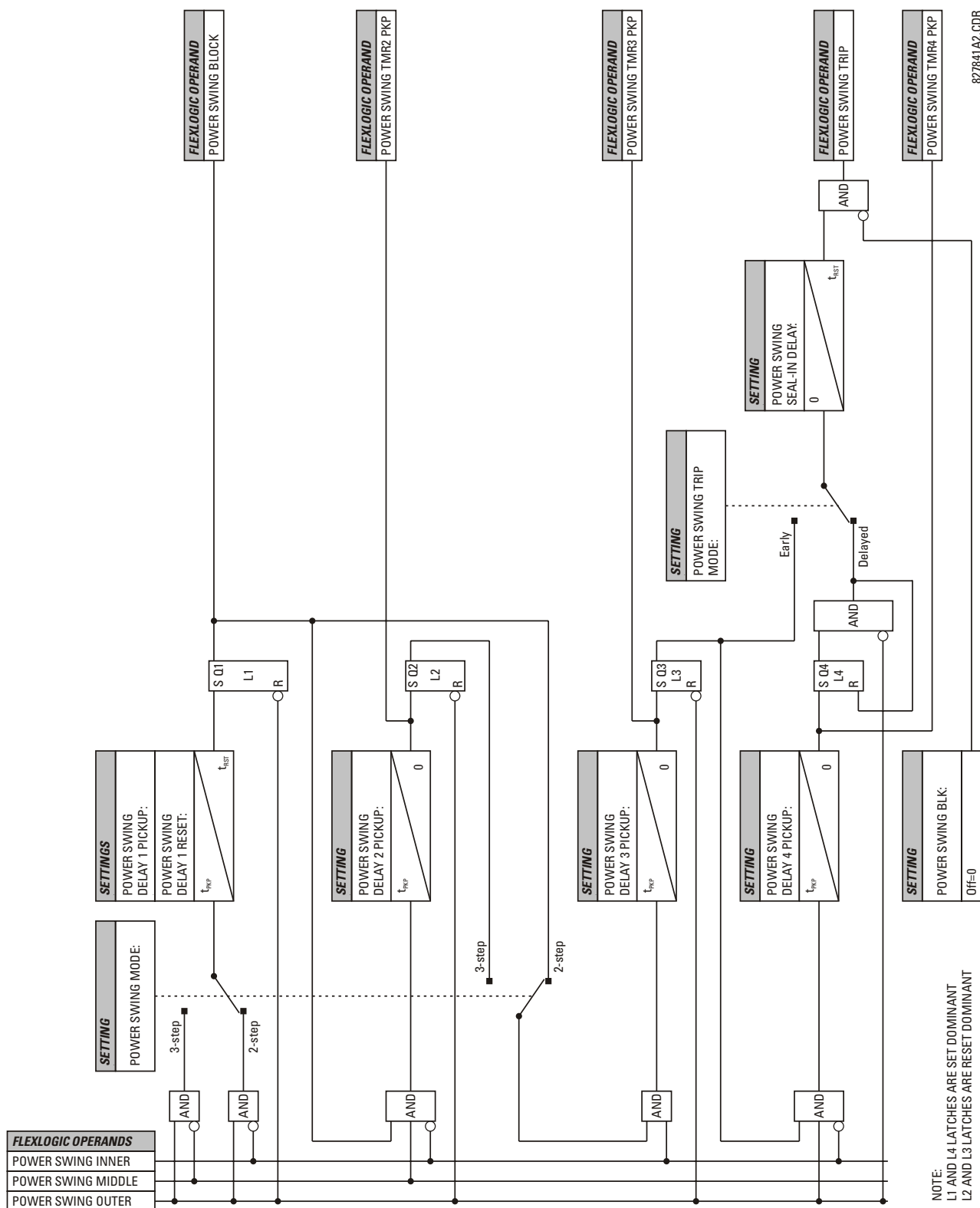


Figure 5-22: POWER SWING DETECT LOGIC (2 of 2)

c) SETTINGS**POWER SWING FUNCTION:**

This setting enables/disables the entire POWER SWING DETECT protection element. The setting applies to both power swing blocking and out-of-step tripping functions.

POWER SWING SOURCE:

The source setting identifies the Signal Source for both blocking and tripping functions.

POWER SWING MODE:

This setting selects between the 2-step and 3-step operating modes and applies to both power swing blocking and out-of-step tripping functions.

The 3-step mode is applicable if there is enough space between the maximum load impedances and distance characteristics of the relay so that all three (outer, middle and inner) characteristics can be placed between the load and the distance characteristics. Whether or not the spans between the outer and middle as well as between the middle and inner characteristics are sufficient should be determined by analysis of the fastest power swings expected in correlation with settings of the power swing timers.

The 2-step mode uses only the outer and inner characteristics for both blocking and tripping functions. This leaves more space in heavily loaded systems to place two power swing characteristics between the distance characteristics and the maximum load, but allows for only one determination of the impedance trajectory.

POWER SWING SUPV:

A common overcurrent pickup level supervises all three power swing characteristics. The supervision responds to the positive sequence current.

POWER SWING FWD REACH:

This setting specifies the forward reach of all three characteristics. For a simple system consisting of a line and two equivalent sources, this reach should be higher than the sum of the line and remote source positive-sequence impedances. Detailed transient stability studies may be needed for complex systems in order to determine this setting.

POWER SWING FWD RCA:

This setting specifies the angle of the forward reach impedance. The angle is measured as shown in the POWER SWING DETECT ELEMENT OPERATING CHARACTERISTICS diagram.

POWER SWING REV REACH:

This setting specifies the reverse reach of all three power detect characteristics. For a simple system consisting of a line and two equivalent sources, this reach should be higher than the positive-sequence impedance of the local source. Detailed transient stability studies may be needed for complex systems in order to determine this setting.

POWER SWING REV RCA:

This setting specifies the angle of the reverse reach impedance. The angle is measured as shown in the POWER SWING DETECT ELEMENT OPERATING CHARACTERISTICS diagram.

POWER SWING OUTER LIMIT ANGLE:

This setting defines the outer power swing detect characteristic. The convention depicted in the POWER SWING DETECT ELEMENT OPERATING CHARACTERISTICS diagram should be observed: values greater than 90° result in an "apple" shaped characteristic, values lower than 90° result in a lens shaped characteristic.

This angle must be selected in consideration of to the maximum expected load. If the "maximum load angle" is known, the outer limit angle should be coordinated with some 20° security margin. Detailed studies may be needed for complex systems in order to determine this setting.

POWER SWING MIDDLE LIMIT ANGLE:

This setting defines the middle power swing detect characteristic.

This setting is relevant only if the 3-step mode is selected. A typical value would be close to the average of the outer and inner limit angles.

POWER SWING INNER LIMIT ANGLE:

This setting defines the inner power swing detect characteristic.

The inner characteristic is used by the out-of-step tripping function: beyond the inner characteristic out-of-step trip action is definite (the actual trip may be delayed as per the TRIP MODE setting). Therefore, this angle must be selected in consideration to the power swing angle beyond which the system becomes unstable and cannot recover.

The inner characteristic is also used by the power swing blocking function in the 2-step mode. Therefore, this angle must be set large enough so that the characteristics of the distance elements are safely enclosed by the inner characteristic.

POWER SWING PICKUP DELAY 1:

All the coordinating timers are related to each other and should be set to detect the fastest expected power swing and produce out-of-step tripping in a secure manner. The timers should be set in consideration to the power swing detect characteristics, mode of power swing detect operation and mode of out-of-step tripping.

This timer defines the interval that the impedance locus must spend between the outer and inner characteristics (2-step operating mode), or between the outer and middle characteristics (3-step operating mode) before the power swing blocking signal is established. This time delay must be set shorter than the time required for the impedance locus to travel between the two selected characteristics during the fastest expected power swing.

This setting is relevant for both power swing blocking and out-of-step tripping.

POWER SWING RESET DELAY 1:

This setting defines the dropout delay for the power swing blocking signal. Detection of a condition requiring a Block output sets Latch 1 after PICKUP DELAY 1 time. When the impedance locus leaves the outer characteristic, timer POWER SWING RESET DELAY 1 is started. When the timer times-out the latch is reset.

This setting should be selected to give extra security for the power swing blocking action.

POWER SWING PICKUP DELAY 2:

This setting controls the out-of-step tripping function in the 3-step mode only. This timer defines the interval the impedance locus must spend between the middle and inner characteristics before the second step of the out-of-step tripping sequence is completed. This time delay must be set shorter than the time required for the impedance locus to travel between the two characteristics during the fastest expected power swing.

POWER SWING PICKUP DELAY 3:

This setting controls the out-of-step tripping function only. This timer defines the interval the impedance locus must spend within the inner characteristic before the last step of the out-of-step tripping sequence is completed and the element is armed to trip. The actual moment of tripping is controlled by the TRIP MODE setting.

This time delay is provided for extra security before the out-of-step trip action is executed.

POWER SWING PICKUP DELAY 4:

This setting controls the out-of-step tripping function in the Delayed trip mode only. This timer defines the interval the impedance locus must spend outside the inner characteristic but within the outer characteristic before the element gets armed for the Delayed trip. The delayed trip will take place when the impedance leaves the outer characteristic.

This time delay is provided for extra security and should be set considering the fastest expected power swing.

POWER SWING SEAL-IN DELAY:

The out-of-step trip FlexLogic™ operand (POWER SWING TRIP) is sealed-in for the specified period of time. The sealing-in is crucial in the delayed trip mode, as the original trip signal is a very short pulse occurring when the impedance locus leaves the outer characteristic after the out-of-step sequence is completed.

POWER SWING TRIP MODE:

Selection of the "Early" trip mode results in an instantaneous trip after the last step in the out-of-step tripping sequence is completed. The Early trip mode will stress the circuit breakers as the currents at that moment are high (the electromotive forces of the two equivalent systems are approximately 180° apart).

Selection of the "Delayed" trip mode results in a trip at the moment when the impedance locus leaves the outer characteristic. Delayed trip mode will relax the operating conditions for the breakers as the currents at that moment are low.

The selection should be made considering the capability of the breakers in the system.

POWER SWING BLK:

This setting specifies the FlexLogic™ operand used for blocking the out-of-step function only. The power swing blocking function is operational all the time as long as the element is enabled.

The blocking signal resets the output POWER SWING TRIP operand but does not stop the out-of-step tripping sequence.

5.5.6 CURRENT ELEMENTS MENU

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒

■ PHASE CURRENT	◀▶	■ PHASE TOC1
■		■
MESSAGE	▲▼	■ PHASE TOC2
		■
MESSAGE	▲▼	■ PHASE IOC1
		■
MESSAGE	▲▼	■ PHASE IOC2
		■
■ NEUTRAL CURRENT	◀▶	■ NEUTRAL TOC1
■		■
MESSAGE	▲▼	■ NEUTRAL TOC2
		■
MESSAGE	▲▼	■ NEUTRAL IOC1
		■
MESSAGE	▲▼	■ NEUTRAL IOC2
		■
■ GROUND CURRENT	◀▶	■ GROUND TOC1
■		■
MESSAGE	▲▼	■ GROUND TOC2
		■
MESSAGE	▲▼	■ GROUND IOC1
		■
MESSAGE	▲▼	■ GROUND IOC2
		■
■ NEGATIVE SEQUENCE	◀▶	■ NEG SEQ TOC1
■ CURRENT		■
MESSAGE	▲▼	■ NEG SEQ TOC2
		■
MESSAGE	▲▼	■ NEG SEQ IOC1
		■
MESSAGE	▲	■ NEG SEQ IOC2
		■

The relay current elements menu consists of two time overcurrent element for each of phase, neutral, and ground currents; two instantaneous overcurrent elements for each of phase, neutral, and ground currents; and two time overcurrent and two instantaneous elements for negative sequence currents. These elements can be used for tripping, alarming, or other functions.

a) INVERSE TIME OVERCURRENT CURVE CHARACTERISTICS

The inverse time overcurrent curves used by the TOC (time overcurrent) Current Elements are the IEEE, IEC, GE Type IAC, and I^2t standard curve shapes. This allows for simplified coordination with downstream devices. If however, none of these curve shapes is adequate, the FlexCurve™ may be used to customize the inverse time curve characteristics. The Definite Time curve is also an option that may be appropriate if only simple protection is required.

Table 5–9: OVERCURRENT CURVE TYPES

IEEE	IEC	GE TYPE IAC	OTHER
IEEE Extremely Inv.	IEC Curve A (BS142)	IAC Extremely Inv.	I^2t
IEEE Very Inverse	IEC Curve B (BS142)	IAC Very Inverse	FlexCurve A
IEEE Moderately Inv.	IEC Curve C (BS142)	IAC Inverse	FlexCurve B
	IEC Short Inverse	IAC Short Inverse	Definite Time

A time dial multiplier setting allows selection of a multiple of the base curve shape (where the time dial multiplier = 1) that is selected with the curve shape setting. Unlike the electromechanical time dial equivalent, operate times are directly proportional to the time multiplier setting value. For example, all times for a multiplier of 10 are 10 times the multiplier 1 or base curve values. Setting the multiplier to zero results in an instantaneous response to all current levels above pickup.

Time overcurrent time calculations are made with an internal “energy capacity” memory variable. When this variable indicates that the energy capacity has reached 100%, a time overcurrent element will operate. If less than 100% energy capacity is accumulated in this variable and the current falls below the dropout threshold of 97–98% of the pickup value, the variable must be reduced. Two methods of this resetting operation are available, “Instantaneous” and “Timed”. The Instantaneous selection is intended for applications with other relays, such as most static relays, which set the energy capacity directly to zero when the current falls below the reset threshold. The Timed selection can be used where the relay must coordinate with electromechanical relays. With this setting, the energy capacity variable is decremented according to the equation provided.

**NOTE**

Graphs of standard time-current curves on 11" × 17" log-log graph paper are available upon request from the GE Power Management literature department. The original files are also available in PDF format on the UR Software Installation CD and the GE Power Management Web Page.

IEEE CURVES:

The IEEE time overcurrent curve shapes conform to industry standards and the IEEE C37.112-1996 curve classifications for extremely, very, and moderately inverse. The IEEE curves are derived from the formulae:

$$T = TDM \times \left[\frac{A}{\left(\frac{I}{I_{pickup}} \right)^p - 1} + B \right] \quad T_{RESET} = TDM \times \left[\frac{t_r}{\left(\frac{I}{I_{pickup}} \right)^2 - 1} \right]$$

where: T = Operate Time (sec)

TDM = Multiplier Setting

I = Input Current

I_{pickup} = Pickup Current Setting

A, B, p = Constants

T_{RESET} = reset time in sec. (assuming energy capacity is 100% and RESET:Timed)

t_r = characteristic constant

Table 5-10: IEEE INVERSE TIME CURVE CONSTANTS

IEEE CURVE SHAPE	A	B	p	t_r
IEEE EXTREMELY INVERSE	28.2	0.1217	2.0000	29.1
IEEE VERY INVERSE	19.61	0.491	2.0000	21.6
IEEE MODERATELY INVERSE	0.0515	0.1140	0.02000	4.85

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MULTIPLIER	CURRENT (I / I _{pickup})									
(TDM)	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
IEEE EXTREMELY INVERSE										
0.5	11.341	4.761	1.823	1.001	0.648	0.464	0.355	0.285	0.237	0.203
1.0	22.682	9.522	3.647	2.002	1.297	0.927	0.709	0.569	0.474	0.407
2.0	45.363	19.043	7.293	4.003	2.593	1.855	1.418	1.139	0.948	0.813
4.0	90.727	38.087	14.587	8.007	5.187	3.710	2.837	2.277	1.897	1.626
6.0	136.090	57.130	21.880	12.010	7.780	5.564	4.255	3.416	2.845	2.439
8.0	181.454	76.174	29.174	16.014	10.374	7.419	5.674	4.555	3.794	3.252
10.0	226.817	95.217	36.467	20.017	12.967	9.274	7.092	5.693	4.742	4.065
IEEE VERY INVERSE										
0.5	8.090	3.514	1.471	0.899	0.654	0.526	0.450	0.401	0.368	0.345
1.0	16.179	7.028	2.942	1.798	1.308	1.051	0.900	0.802	0.736	0.689
2.0	32.358	14.055	5.885	3.597	2.616	2.103	1.799	1.605	1.472	1.378
4.0	64.716	28.111	11.769	7.193	5.232	4.205	3.598	3.209	2.945	2.756
6.0	97.074	42.166	17.654	10.790	7.849	6.308	5.397	4.814	4.417	4.134
8.0	129.432	56.221	23.538	14.387	10.465	8.410	7.196	6.418	5.889	5.513
10.0	161.790	70.277	29.423	17.983	13.081	10.513	8.995	8.023	7.361	6.891
IEEE MODERATELY INVERSE										
0.5	3.220	1.902	1.216	0.973	0.844	0.763	0.706	0.663	0.630	0.603
1.0	6.439	3.803	2.432	1.946	1.688	1.526	1.412	1.327	1.260	1.207
2.0	12.878	7.606	4.864	3.892	3.377	3.051	2.823	2.653	2.521	2.414
4.0	25.756	15.213	9.729	7.783	6.753	6.102	5.647	5.307	5.041	4.827
6.0	38.634	22.819	14.593	11.675	10.130	9.153	8.470	7.960	7.562	7.241
8.0	51.512	30.426	19.458	15.567	13.507	12.204	11.294	10.614	10.083	9.654
10.0	64.390	38.032	24.322	19.458	16.883	15.255	14.117	13.267	12.604	12.068

IEC CURVES

For European applications, the relay offers three standard curves defined in IEC 255-4 and British standard BS142. These are defined as IEC Curve A, IEC Curve B, and IEC Curve C. The formulae for these curves are:

$$T = TDM \times \left[\frac{K}{\left(\frac{I}{I_{pickup}} \right)^E} - 1 \right] \quad T_{RESET} = TDM \times \left[\frac{t_r}{\left(\frac{I}{I_{pickup}} \right)^2} - 1 \right]$$

where: T = Operate Time (sec) TDM = Multiplier Setting
 I = Input Current I_{pickup} = Pickup Current Setting
 K, E = Constants t_r = Characteristic Constant
 T_{RESET} = Reset Time in sec. (assuming energy capacity is 100% and RESET: Timed)

Table 5-11: IEC (BS) INVERSE TIME CURVE CONSTANTS

IEC (BS) CURVE SHAPE	K	E	t_r
IEC CURVE A (BS142)	0.140	0.020	9.7
IEC CURVE B (BS142)	13.500	1.000	43.2
IEC CURVE C (BS142)	80.000	2.000	58.2
IEC SHORT INVERSE	0.050	0.040	0.500

Table 5-12: IEC CURVE TRIP TIMES (in seconds)

Multiplier (TDM)	Current (I / Ipu)									
	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
IEC CURVE A										
0.05	0.860	0.501	0.315	0.249	0.214	0.192	0.176	0.165	0.156	0.149
0.10	1.719	1.003	0.630	0.498	0.428	0.384	0.353	0.330	0.312	0.297
0.20	3.439	2.006	1.260	0.996	0.856	0.767	0.706	0.659	0.623	0.594
0.40	6.878	4.012	2.521	1.992	1.712	1.535	1.411	1.319	1.247	1.188
0.60	10.317	6.017	3.781	2.988	2.568	2.302	2.117	1.978	1.870	1.782
0.80	13.755	8.023	5.042	3.984	3.424	3.070	2.822	2.637	2.493	2.376
1.00	17.194	10.029	6.302	4.980	4.280	3.837	3.528	3.297	3.116	2.971
IEC CURVE B										
0.05	1.350	0.675	0.338	0.225	0.169	0.135	0.113	0.096	0.084	0.075
0.10	2.700	1.350	0.675	0.450	0.338	0.270	0.225	0.193	0.169	0.150
0.20	5.400	2.700	1.350	0.900	0.675	0.540	0.450	0.386	0.338	0.300
0.40	10.800	5.400	2.700	1.800	1.350	1.080	0.900	0.771	0.675	0.600
0.60	16.200	8.100	4.050	2.700	2.025	1.620	1.350	1.157	1.013	0.900
0.80	21.600	10.800	5.400	3.600	2.700	2.160	1.800	1.543	1.350	1.200
1.00	27.000	13.500	6.750	4.500	3.375	2.700	2.250	1.929	1.688	1.500
IEC CURVE C										
0.05	3.200	1.333	0.500	0.267	0.167	0.114	0.083	0.063	0.050	0.040
0.10	6.400	2.667	1.000	0.533	0.333	0.229	0.167	0.127	0.100	0.081
0.20	12.800	5.333	2.000	1.067	0.667	0.457	0.333	0.254	0.200	0.162
0.40	25.600	10.667	4.000	2.133	1.333	0.914	0.667	0.508	0.400	0.323
0.60	38.400	16.000	6.000	3.200	2.000	1.371	1.000	0.762	0.600	0.485
0.80	51.200	21.333	8.000	4.267	2.667	1.829	1.333	1.016	0.800	0.646
1.00	64.000	26.667	10.000	5.333	3.333	2.286	1.667	1.270	1.000	0.808
IEC SHORT TIME										
0.05	0.153	0.089	0.056	0.044	0.038	0.034	0.031	0.029	0.027	0.026
0.10	0.306	0.178	0.111	0.088	0.075	0.067	0.062	0.058	0.054	0.052
0.20	0.612	0.356	0.223	0.175	0.150	0.135	0.124	0.115	0.109	0.104
0.40	1.223	0.711	0.445	0.351	0.301	0.269	0.247	0.231	0.218	0.207
0.60	1.835	1.067	0.668	0.526	0.451	0.404	0.371	0.346	0.327	0.311
0.80	2.446	1.423	0.890	0.702	0.602	0.538	0.494	0.461	0.435	0.415
1.00	3.058	1.778	1.113	0.877	0.752	0.673	0.618	0.576	0.544	0.518

IAC CURVES

The curves for the General Electric type IAC relay family are derived from the formulae:

$$T = TDM \times \left[A + \frac{B}{\left(\frac{I}{I_{pickup}} - C\right)} + \frac{D}{\left(\frac{I}{I_{pickup}} - C\right)^2} + \frac{E}{\left(\frac{I}{I_{pickup}} - C\right)^3} \right] \quad T_{RESET} = TDM \times \left[\frac{t_r}{\left(\frac{I}{I_{pickup}}\right)^2 - 1} \right]$$

where: T = Operate Time (sec) TDM = Multiplier Setting
 I = Input Current I_{pickup} = Pickup Current Setting
 A to E = Constants t_r = Characteristic Constant
 T_{RESET} = Reset Time in sec. (assuming energy capacity is 100% and RESET: Timed)

Table 5-13: GE TYPE IAC INVERSE TIME CURVE CONSTANTS

IAC Curve Shape	A	B	C	D	E	t_r
IAC EXTREME INVERSE	0.0040	0.6379	0.6200	1.7872	0.2461	6.008
IAC VERY INVERSE	0.0900	0.7955	0.1000	-1.2885	7.9586	4.678
IAC INVERSE	0.2078	0.8630	0.8000	-0.4180	0.1947	0.990
IAC SHORT INVERSE	0.0428	0.0609	0.6200	-0.0010	0.0221	0.222

Table 5-14: IAC CURVE TRIP TIMES

Multiplier (TDM)	Current (I / Ipu)									
	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
IAC EXTREMELY INVERSE										
0.5	1.699	0.749	0.303	0.178	0.123	0.093	0.074	0.062	0.053	0.046
1.0	3.398	1.498	0.606	0.356	0.246	0.186	0.149	0.124	0.106	0.093
2.0	6.796	2.997	1.212	0.711	0.491	0.372	0.298	0.248	0.212	0.185
4.0	13.591	5.993	2.423	1.422	0.983	0.744	0.595	0.495	0.424	0.370
6.0	20.387	8.990	3.635	2.133	1.474	1.115	0.893	0.743	0.636	0.556
8.0	27.183	11.987	4.846	2.844	1.966	1.487	1.191	0.991	0.848	0.741
10.0	33.979	14.983	6.058	3.555	2.457	1.859	1.488	1.239	1.060	0.926
IAC VERY INVERSE										
0.5	1.451	0.656	0.269	0.172	0.133	0.113	0.101	0.093	0.087	0.083
1.0	2.901	1.312	0.537	0.343	0.266	0.227	0.202	0.186	0.174	0.165
2.0	5.802	2.624	1.075	0.687	0.533	0.453	0.405	0.372	0.349	0.331
4.0	11.605	5.248	2.150	1.374	1.065	0.906	0.810	0.745	0.698	0.662
6.0	17.407	7.872	3.225	2.061	1.598	1.359	1.215	1.117	1.046	0.992
8.0	23.209	10.497	4.299	2.747	2.131	1.813	1.620	1.490	1.395	1.323
10.0	29.012	13.121	5.374	3.434	2.663	2.266	2.025	1.862	1.744	1.654
IAC INVERSE										
0.5	0.578	0.375	0.266	0.221	0.196	0.180	0.168	0.160	0.154	0.148
1.0	1.155	0.749	0.532	0.443	0.392	0.360	0.337	0.320	0.307	0.297
2.0	2.310	1.499	1.064	0.885	0.784	0.719	0.674	0.640	0.614	0.594
4.0	4.621	2.997	2.128	1.770	1.569	1.439	1.348	1.280	1.229	1.188
6.0	6.931	4.496	3.192	2.656	2.353	2.158	2.022	1.921	1.843	1.781
8.0	9.242	5.995	4.256	3.541	3.138	2.878	2.695	2.561	2.457	2.375
10.0	11.552	7.494	5.320	4.426	3.922	3.597	3.369	3.201	3.072	2.969
IAC SHORT INVERSE										
0.5	0.072	0.047	0.035	0.031	0.028	0.027	0.026	0.026	0.025	0.025
1.0	0.143	0.095	0.070	0.061	0.057	0.054	0.052	0.051	0.050	0.049
2.0	0.286	0.190	0.140	0.123	0.114	0.108	0.105	0.102	0.100	0.099
4.0	0.573	0.379	0.279	0.245	0.228	0.217	0.210	0.204	0.200	0.197
6.0	0.859	0.569	0.419	0.368	0.341	0.325	0.314	0.307	0.301	0.296
8.0	1.145	0.759	0.559	0.490	0.455	0.434	0.419	0.409	0.401	0.394
10.0	1.431	0.948	0.699	0.613	0.569	0.542	0.524	0.511	0.501	0.493

I²t CURVES

The curves for the I²t are derived from the formulae:

$$T = \text{TDM} \times \left[\frac{100}{\left(\frac{I}{I_{\text{pickup}}} \right)^2} \right] \quad T_{\text{RESET}} = \text{TDM} \times \left[\frac{100}{\left(\frac{I}{I_{\text{pickup}}} \right)^{-2}} \right]$$

where:

- T = Operate Time (sec)
- TDM = Multiplier Setting
- I = Input Current
- I_{pickup} = Pickup Current Setting
- T_{RESET} = Reset Time in sec. (assuming energy capacity is 100% and RESET:Timed)

Table 5–15: I²t CURVE TRIP TIMES

MULTIPLIER	CURRENT (I/I _{pu})									
(TDM)	1.5	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
0.01	0.44	0.25	0.11	0.06	0.04	0.03	0.02	0.02	0.01	0.01
0.10	4.44	2.50	1.11	0.63	0.40	0.28	0.20	0.16	0.12	0.10
1.00	44.44	25.00	11.11	6.25	4.00	2.78	2.04	1.56	1.23	1.00
10.00	444.44	250.00	111.11	62.50	40.00	27.78	20.41	15.63	12.35	10.00
100.00	4444.4	2500.0	1111.1	625.00	400.00	277.78	204.08	156.25	123.46	100.00
600.00	26666.7	15000.0	6666.7	3750.0	2400.0	1666.7	1224.5	937.50	740.74	600.00

FLEXCURVE™

The custom FlexCurve™ is described in detail in the sub-section FLEXCURVE™ A / FLEXCURVE™ B of section SETTINGS \ SYSTEM SETUP. The curve shapes for the FlexCurves™ are derived from the formulae:

$$T = \text{TDM} \times \left[\text{FlexcurveTime} @ \left(\frac{I}{I_{pickup}} \right) \right] \quad \text{When } \left(\frac{I}{I_{pickup}} \right) \geq 1.00$$

$$T_{RESET} = \text{TDM} \times \left[\text{FlexcurveTime} @ \left(\frac{I}{I_{pickup}} \right) \right] \quad \text{When } \left(\frac{I}{I_{pickup}} \right) \leq 0.98$$

where:

- T = Operate Time (sec)
- TDM = Multiplier Setting
- I = Input Current
- I_{pickup} = Pickup Current Setting
- T_{RESET} = Reset Time in seconds (assuming energy capacity is 100% and RESET:Timed)

DEFINITE TIME CURVE

The Definite Time curve shape operates as soon as the pickup level is exceeded for a specified period of time. The base definite time curve delay is in seconds. The curve multiplier of 0.00 to 600.00 makes this delay adjustable from instantaneous to 600.00 seconds in steps of 10 ms.

$$T = \text{TDM in seconds, when } I > I_{pickup}$$

$$T_{RESET} = -\text{TDM in seconds}$$

where:

- T = Operate Time (sec)
- TDM = Multiplier Setting
- I = Input Current
- I_{pickup} = Pickup Current Setting
- T_{RESET} = Reset Time in seconds (assuming energy capacity is 100% and RESET: Timed)

b) PHASE TOC1 / TOC2 (PHASE TIME OVERCURRENT - ANSI 51P)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ PHASE CURRENT ⇒ PHASE TOC1

■ PHASE TOC1		◀▶	PHASE TOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	▲▼	PHASE TOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	▲▼	PHASE TOC1 INPUT: Phasor	Range: Phasor, RMS
MESSAGE	▲▼	▲▼	PHASE TOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 in steps of 0.001 pu
MESSAGE	▲▼	▲▼	PHASE TOC1 CURVE: IEEE Mod Inv	See OVERCURRENT CURVE TYPES table
MESSAGE	▲▼	▲▼	PHASE TOC1 TD MULTIPLIER: 1.00	Range: 0.00 to 600.00 in steps of 0.01
MESSAGE	▲▼	▲▼	PHASE TOC1 RESET: Instantaneous	Range: Instantaneous, Timed
MESSAGE	▲▼	▲▼	PHASE TOC1 VOLTAGE RESTRAINT: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	▲▼	PHASE TOC1 BLOCK A: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	▲▼	PHASE TOC1 BLOCK B: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	▲▼	PHASE TOC1 BLOCK C: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	▲▼	PHASE TOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲	▲▼	PHASE TOC1 EVENTS: Disabled	Range: Disabled, Enabled

The phase time overcurrent element may be used to give a desired time-delay operating characteristic versus the applied current, or as a simple Definite Time element. The phase current input quantities may be programmed as Fundamental phasor magnitude or total waveform RMS magnitude as required by the application.

Two methods of resetting operation are available; "Timed" and "Instantaneous" (refer to section INVERSE TIME OVERCURRENT CURVE CHARACTERISTICS for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to "Instantaneous" and the element is blocked, the time accumulator will be cleared immediately.

The PICKUP setting of the element can be dynamically reduced by a VOLTAGE RESTRAINT feature (when enabled). This is accomplished via the multipliers (Mvr) corresponding to the phase-phase voltages of the voltage restraint characteristic curve (see VOLTAGE RESTRAINT CHARACTERISTIC FOR PHASE TOC figure below); the pickup level is calculated as 'Mvr' times the 'Pickup' setting. If the voltage restraint feature is disabled, the pickup level always remains at the setting value.



Figure 5-23: VOLTAGE RESTRAINT CHARACTERISTIC FOR PHASE TOC



Figure 5–24: PHASE TOC1 SCHEME LOGIC

c) PHASE IOC1 / IOC2 (PHASE INSTANTANEOUS OVERCURRENT - ANSI 50P)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ PHASE CURRENT ⇒ PHASE IOC 1

■ PHASE IOC1	◀▶	PHASE IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	PHASE IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1, ..., SRC 6
MESSAGE	▲▼	PHASE IOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 in steps of 0.001 pu
MESSAGE	▲▼	PHASE IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 to 600.00 in steps of 0.01
MESSAGE	▲▼	PHASE IOC1 RESET DELAY: 0.00 s	Range: 0.00 to 600.00 in steps of 0.01
MESSAGE	▲▼	PHASE IOC1 BLOCK A: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	PHASE IOC1 BLOCK B: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	PHASE IOC1 BLOCK C: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	PHASE IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲	PHASE IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The phase instantaneous overcurrent element may be used as an instantaneous element with no intentional delay or as a Definite Time element. The input current is the fundamental phasor magnitude.

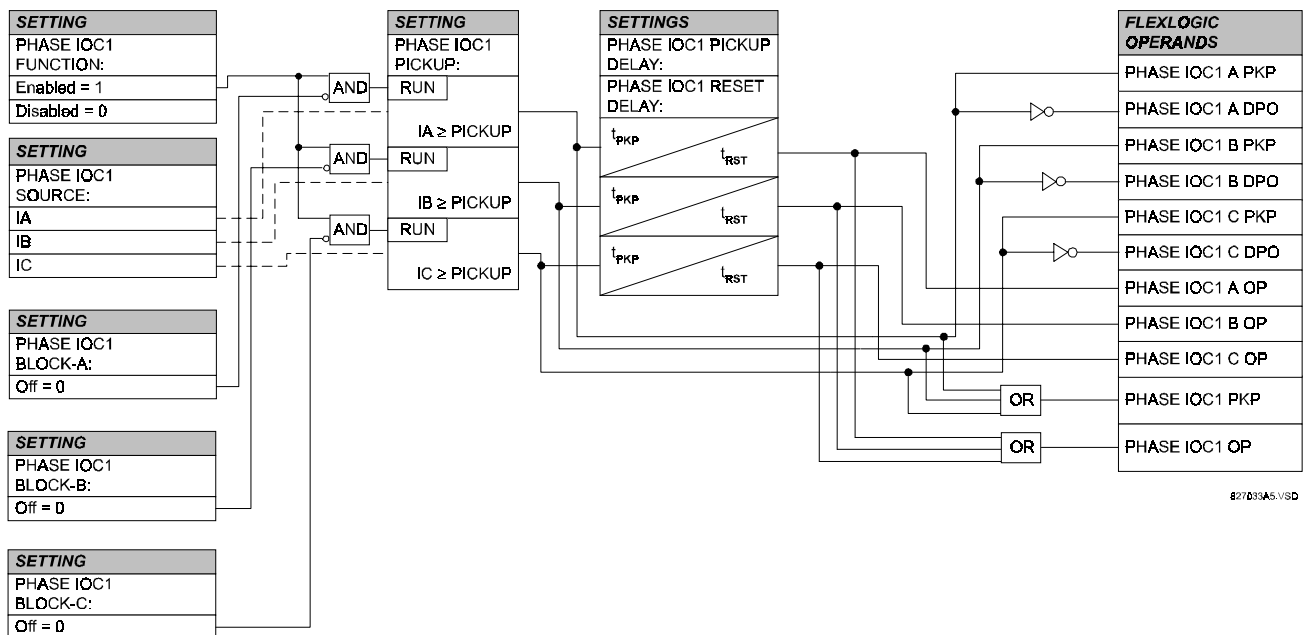


Figure 5-25: PHASE IOC1 SCHEME LOGIC

d) NEUTRAL TOC1 / TOC2 (NEUTRAL TIME OVERCURRENT - ANSI 51N)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ NEUTRAL CURRENT ⇒ NEUTRAL TOC1

<div> <div>■ NEUTRAL TOC1</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> </div>	<div> <div>⏮</div> <div>⏭</div> <div>⏮</div> <div>⏭</div> <div>⏮</div> <div>⏭</div> <div>⏮</div> <div>⏭</div> <div>⏮</div> </div>	<div>NEUTRAL TOC1</div> <div>FUNCTION: Disabled</div>	Range: Disabled, Enabled
		<div>NEUTRAL TOC1 SIGNAL</div> <div>SOURCE: SRC 1</div>	Range: SRC 1,..., SRC 6
		<div>NEUTRAL TOC1</div> <div>INPUT: Phasor</div>	Range: Phasor, RMS
		<div>NEUTRAL TOC1</div> <div>PICKUP: 1.000 pu</div>	Range: 0.000 to 30.000 pu in steps of 0.001
		<div>NEUTRAL TOC1</div> <div>CURVE: IEEE Mod Inv</div>	See Overcurrent Curve Types table
		<div>NEUTRAL TOC1</div> <div>TD MULTIPLIER: 1.00</div>	Range: 0.00 To 600.00 in steps of 0.01
		<div>NEUTRAL TOC1</div> <div>RESET: Instantaneous</div>	Range: Instantaneous, Timed
		<div>NEUTRAL TOC1 BLOCK:</div> <div>Off</div>	Range: FlexLogic™ Operand
		<div>NEUTRAL TOC1</div> <div>TARGET: Self-reset</div>	Range: Self-reset, Latched, Disabled
		<div>NEUTRAL TOC1</div> <div>EVENTS: Disabled</div>	Range: Disabled, Enabled

The neutral time overcurrent element may be used to give a desired time-delay operating characteristic versus the applied current or as a simple Definite Time element. The neutral current input value is a quantity calculated as $3I_0$ from the phase currents and may be programmed as fundamental phasor magnitude or total waveform RMS magnitude as required by the application.

Two methods of resetting operation are available; "Timed" and "Instantaneous" (refer to section INVERSE TIME OVERCURRENT CURVE CHARACTERISTICS for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to "Instantaneous" and the element is blocked, the time accumulator will be cleared immediately.

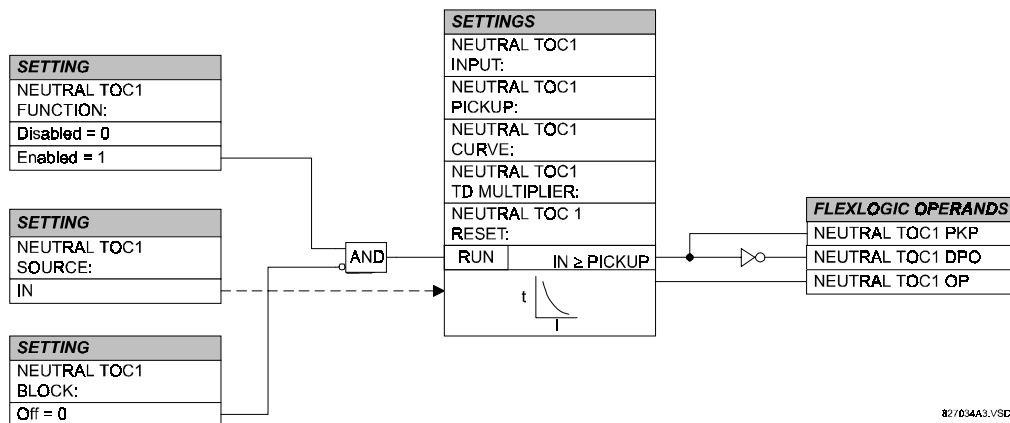


Figure 5-26: NEUTRAL TOC1 SCHEME LOGIC

e) NEUTRAL IOC1 / IOC2 (NEUTRAL INSTANTANEOUS OVERCURRENT - ANSI 50N)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ NEUTRAL CURRENT ⇒ ↓ NEUTRAL IOC1

■ NEUTRAL IOC1		NEUTRAL IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	NEUTRAL IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	NEUTRAL IOC1 PICKUP: 1.05 A	Range: 0.000 to 30.000 pu in steps of 0.001
MESSAGE	▲▼	NEUTRAL IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 To 600.00 in steps of 0.01
MESSAGE	▲▼	NEUTRAL IOC1 RESET DELAY: 0.00 s	Range: 0.00 To 600.00 in steps of 0.01
MESSAGE	▲▼	NEUTRAL IOC1 BLOCK: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	NEUTRAL IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲▼	NEUTRAL IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The Neutral Instantaneous Overcurrent protection element may be used as an instantaneous function with no intentional delay or as a Definite Time function.

The element essentially responds to the magnitude of a neutral current fundamental frequency phasor calculated from the phase currents.

The element applies a “positive-sequence restraint” for better performance. A small portion (6.25%) of the positive-sequence current magnitude is subtracted from the zero-sequence current magnitude when forming the operating quantity of the element:

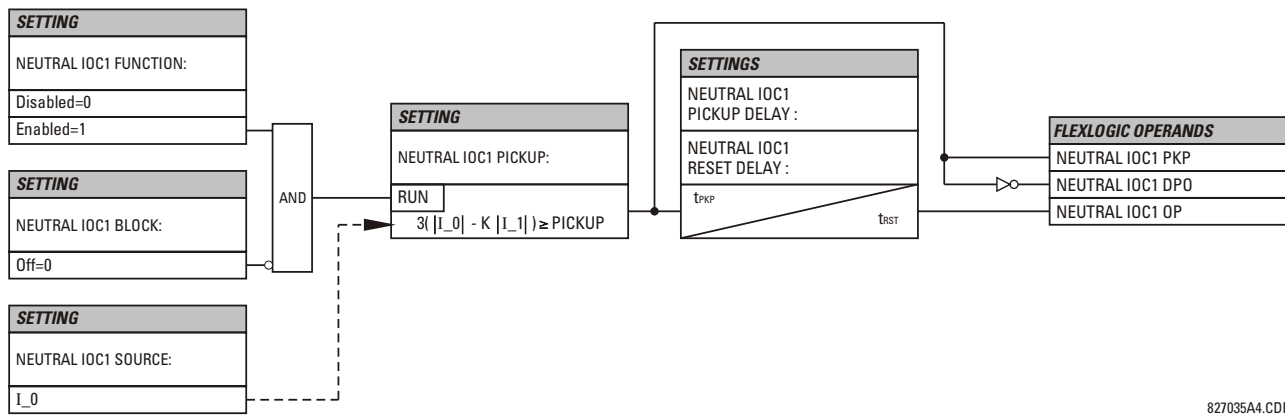
$$I_{op} = 3 \times (|I_0| - K \cdot |I_1|)$$

where $K = 1/16$

The positive-sequence restraint allows for more sensitive settings by counterbalancing spurious zero-sequence currents resulting from:

- system unbalances under heavy load conditions
- transformation errors of current transformers (CTs) during double-line and three-phase faults
- switch-off transients during double-line and three-phase faults

The positive-sequence restraint must be taken into account when testing the element for pickup accuracy and response time (multiple of pickup). The operating quantity depends on how the test currents are injected into the relay (single phase injection: $I_{op} = 0.9375 \cdot I_{injected}$; three-phase pure zero-sequence injection: $I_{op} = 3 \times I_{injected}$).



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Figure 5-27: NEUTRAL IOC1 SCHEME LOGIC

f) GROUND TOC1 / TOC2 (GROUND TIME OVERCURRENT - ANSI 51G)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ GROUND CURRENT ⇒ ↓ GROUND TOC1

<div> <div>■ GROUND TOC1</div> <div>■</div> </div>		<div> <div>GROUND TOC1</div> <div>FUNCTION: Disabled</div> </div>	Range: Disabled, Enabled
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1 SIGNAL</div> <div>SOURCE: SRC 1</div> </div>	Range: SRC 1,..., SRC 6
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1</div> <div>INPUT: Phasor</div> </div>	Range: Phasor, RMS
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1</div> <div>PICKUP: 1.000 pu</div> </div>	Range: 0.000 to 30.000 pu in steps of 0.001
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1</div> <div>CURVE: IEEE Mod Inv</div> </div>	See Overcurrent Curve Types table
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1</div> <div>TD MULTIPLIER: 1.00</div> </div>	Range: 0.00 to 600.00 in steps of 0.01
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1</div> <div>RESET: Instantaneous</div> </div>	Range: Instantaneous, Timed
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1 BLOCK:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
MESSAGE	<div> <div>▲</div> <div>▼</div> </div>	<div> <div>GROUND TOC1</div> <div>TARGET: Self-reset</div> </div>	Range: Self-reset, Latched, Disabled
MESSAGE	<div> <div>▲</div> </div>	<div> <div>GROUND TOC1</div> <div>EVENTS: Disabled</div> </div>	Range: Disabled, Enabled

The ground time overcurrent element may be used to give a desired time-delay operating characteristic versus the applied current or as a simple Definite Time element. The ground current input value is the quantity measured by the ground input CT and is the fundamental phasor or RMS magnitude.

Two methods of resetting operation are available; "Timed" and "Instantaneous" (refer to section INVERSE TIME OVERCURRENT CURVE CHARACTERISTICS for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to "Instantaneous" and the element is blocked, the time accumulator will be cleared immediately.

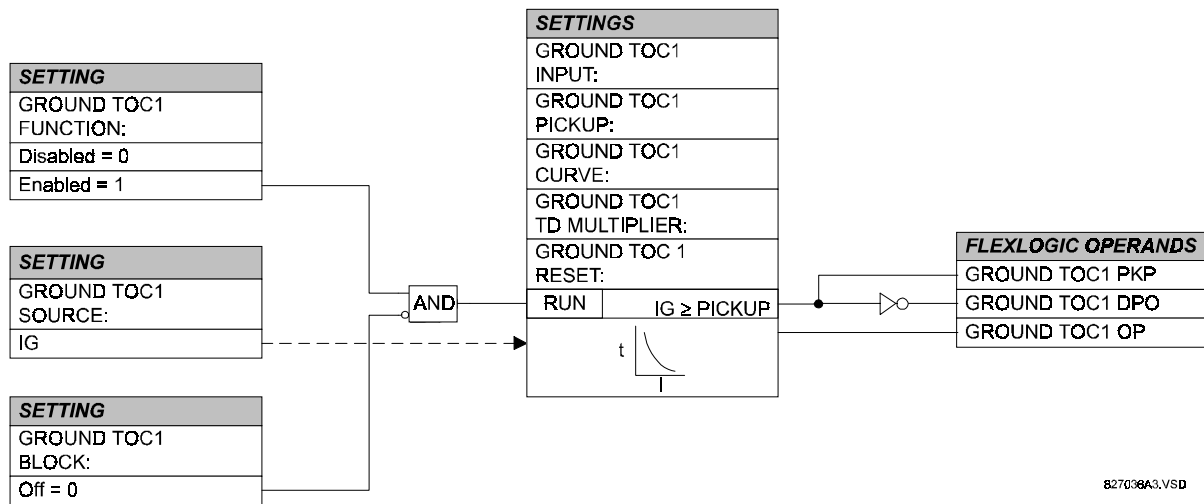


Figure 5-28: GROUND TOC1 SCHEME LOGIC



These elements measure the current that is connected to the ground channel of a CT/VT module. This channel may be equipped with a standard or sensitive input. The conversion range of a standard channel is from 0.02 to 46 times the CT rating. The conversion range of a sensitive channel is from 0.002 to 4.6 times the CT rating.

g) GROUND IOC1 / IOC2 (GROUND INSTANTANEOUS OVERCURRENT - ANSI 50G)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ GROUND CURRENT ⇒ ↓ GROUND IOC1

■ GROUND IOC1	◀▶	GROUND IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	GROUND IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	GROUND IOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 in steps of 0.001 pu
MESSAGE	▲▼	GROUND IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 To 600.00 in Steps of 0.01
MESSAGE	▲▼	GROUND IOC1 RESET DELAY: 0.00 s	Range: 0.00 To 600.00 in Steps of 0.01
MESSAGE	▲▼	GROUND IOC1 BLOCK: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	GROUND IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲	GROUND IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The ground instantaneous overcurrent element may be used as an instantaneous element with no intentional delay or as a Definite Time element. The ground current input value is the quantity measured by the ground input CT and is the fundamental phasor magnitude.

5

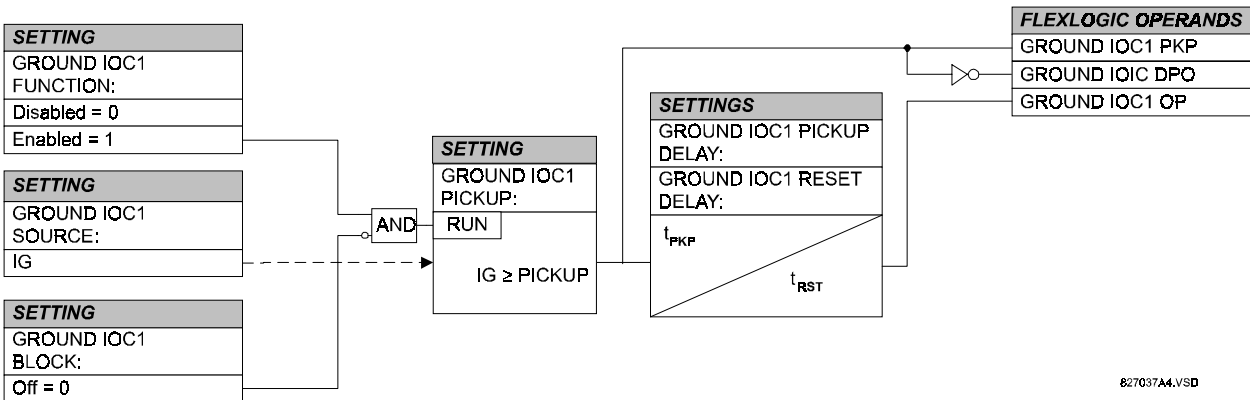


Figure 5–29: GROUND IOC1 SCHEME LOGIC



These elements measure the current that is connected to the ground channel of a CT/VT module. This channel may be equipped with a standard or sensitive input. The conversion range of a standard channel is from 0.02 to 46 times the CT rating. The conversion range of a sensitive channel is from 0.002 to 4.6 times the CT rating.

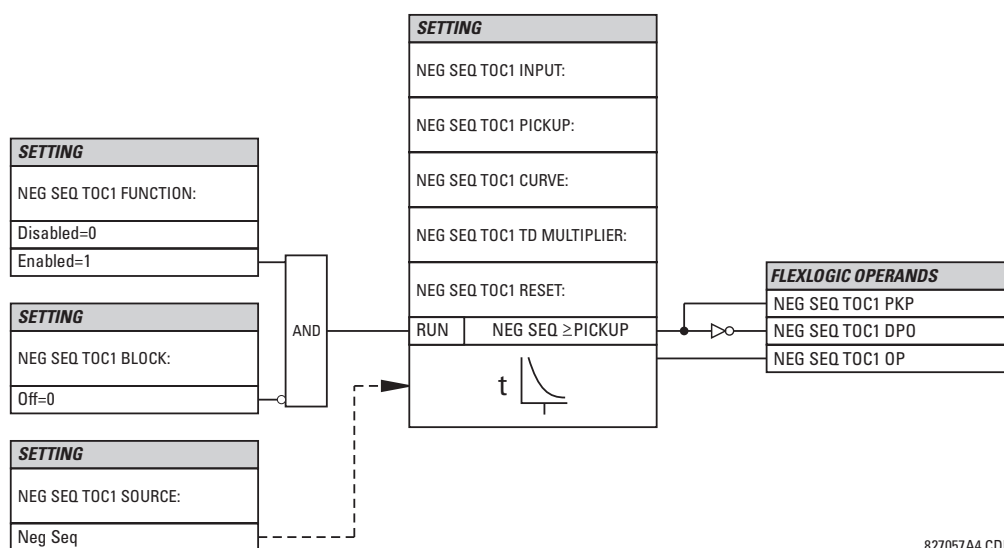
h) **NEGATIVE SEQUENCE TOC1 / TOC2** (NEGATIVE SEQUENCE TIME OVERCURRENT - ANSI 51_2)PATH: SETTINGS ↓ GROUPED ELEMENTS ⇨ SETTING GROUP 1(8) ⇨ **NEGATIVE SEQUENCE CURRENT** ⇨ **NEG SEQ TOC1**

<div> <div>■</div> <div>■</div> </div> <div>NEG SEQ TOC1</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div>		<div> <div>◀▶</div> <div>NEG SEQ TOC1</div> <div>FUNCTION: Disabled</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1 SIGNAL</div> <div>SOURCE: SRC 1</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1</div> <div>PICKUP: 1.000 pu</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1</div> <div>CURVE: IEEE Mod Inv</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1</div> <div>TD MULTIPLIER: 1.00</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1</div> <div>RESET: Instantaneous</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1 BLOCK:</div> <div>Off</div> </div> <div> <div>▲▼</div> <div>NEG SEQ TOC1</div> <div>TARGET: Self-reset</div> </div> <div> <div>▲</div> <div>NEG SEQ TOC1</div> <div>EVENTS: Disabled</div> </div>	<div>Range: Disabled, Enabled</div> <div>Range: SRC 1,..., SRC 6</div> <div>Range: 0.000 to 30.000 pu in steps of 0.001</div> <div>See Overcurrent Curve Types table</div> <div>Range: 0.00 To 600.00 in steps of 0.01</div> <div>Range: Instantaneous, Timed</div> <div>Range: FlexLogic™ Operand</div> <div>Range: Self-reset, Latched, Disabled</div> <div>Range: Disabled, Enabled</div>
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5

The negative sequence time overcurrent element may be used to determine and clear unbalance in the system. The input for calculating negative sequence current is the fundamental phasor value.

Two methods of resetting operation are available; “Timed” and “Instantaneous” (refer to section INVERSE TIME OVERCURRENT CURVE CHARACTERISTICS for details on curve setup, trip times and reset operation). When the element is blocked, the time accumulator will reset according to the reset characteristic. For example, if the element reset characteristic is set to “Instantaneous” and the element is blocked, the time accumulator will be cleared immediately.



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Figure 5–30: NEGATIVE SEQUENCE TOC1 SCHEME LOGIC

i) **NEGATIVE SEQUENCE IOC1 / IOC2** (NEGATIVE SEQUENCE INSTANTANEOUS O/C - ANSI 50_2)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ NEGATIVE SEQUENCE CURRENT ⇒ ↓ NEG SEQ OC1

■ NEG SEQ IOC1		◀▶	NEG SEQ IOC1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	▲▼	NEG SEQ IOC1 SIGNAL SOURCE: SRC 1	Range: SRC 1,..., SRC 6
	MESSAGE	▲▼	NEG SEQ IOC1 PICKUP: 1.000 pu	Range: 0.000 to 30.000 pu n steps of 0.001
	MESSAGE	▲▼	NEG SEQ IOC1 PICKUP DELAY: 0.00 s	Range: 0.00 To 600.00 in steps of 0.01
	MESSAGE	▲▼	NEG SEQ IOC1 RESET DELAY: 0.00 s	Range: 0.00 To 600.00 in steps of 0.01
	MESSAGE	▲▼	NEG SEQ IOC1 BLOCK: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	NEG SEQ IOC1 TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	MESSAGE	▲	NEG SEQ IOC1 EVENTS: Disabled	Range: Disabled, Enabled

The Negative Sequence Instantaneous Overcurrent protection element may be used as an instantaneous function with no intentional delay or as a Definite Time function.

The element essentially responds to the magnitude of the negative-sequence current fundamental frequency phasor calculated from the phase currents. The element applies a “positive-sequence” restraint for better performance: a small portion (12.5%) of the positive-sequence current magnitude is subtracted from the negative-sequence current magnitude when forming the operating quantity of the element:

$$I_{op} = |I_{-2}| - K \cdot |I_{-1}|$$

where $K = 1/8$.

The positive-sequence restraint allows for more sensitive settings by counterbalancing spurious negative-sequence currents resulting from:

- system unbalances under heavy load conditions
- transformation errors of current transformers (CTs) during three-phase faults
- fault inception and switch-off transients during three-phase faults

The positive-sequence restraint must be taken into account when testing the element for pickup accuracy and response time (multiple of pickup). The operating quantity depends on the way the test currents are injected into the relay (single phase injection: $I_{op} = 0.2917 \cdot I_{injected}$; three phase injection, opposite rotation: $I_{op} = I_{injected}$).

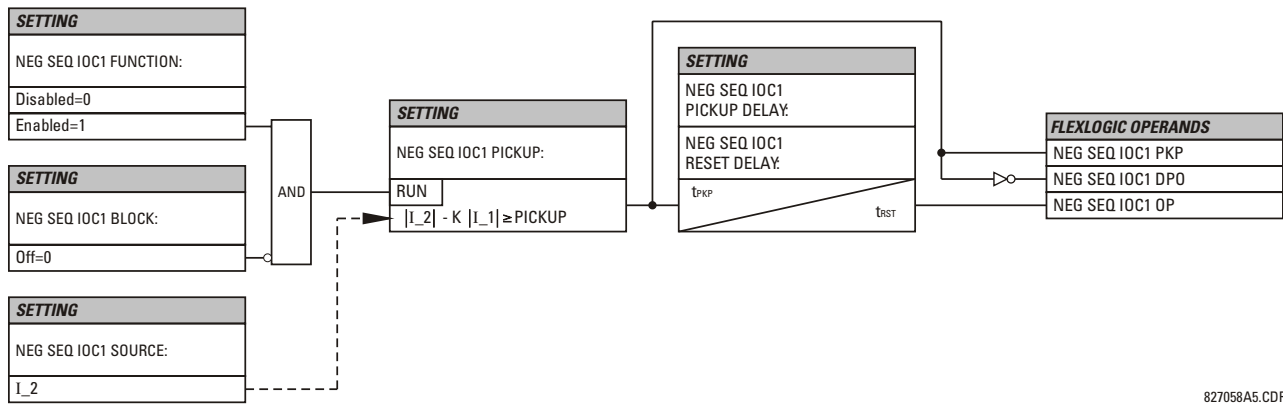


Figure 5–31: NEGATIVE SEQUENCE IOC1 SCHEME LOGIC

5.5.7 BREAKER FAILURE 1(2)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ BREAKER FAILURE ⇒ BREAKER FAILURE 1

■ BREAKER FAILURE 1			BF1 FUNCTION:	Range: Disabled, Enabled
			Disabled	
MESSAGE			BF1 MODE:	Range: 3-Pole, 1-Pole
			3-Pole	
MESSAGE			BF1 SOURCE:	Range: SRC 1, SRC 2,..., SRC 6
			SRC 1	
MESSAGE			BF1 USE AMP SUPV:	Range: Yes, No
			Yes	
MESSAGE			BF1 USE SEAL-IN:	Range: Yes, No
			Yes	
MESSAGE			BF1 3-POLE INITIATE:	Range: FlexLogic™ Operand
			Off	
MESSAGE			BF1 BLOCK:	Range: FlexLogic™ Operand
			Off	
MESSAGE			BF1 PH AMP SUPV PICKUP: 1.050 pu	Range: 0.001 to 30.000 pu in steps of 0.001
MESSAGE			BF1 N AMP SUPV PICKUP: 1.050 pu	Range: 0.001 to 30.000 pu in steps of 0.001
MESSAGE			BF1 USE TIMER 1:	Range: Yes, No
			Yes	
MESSAGE			BF1 TIMER 1 PICKUP DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE			BF1 USE TIMER 2:	Range: Yes, No
			Yes	
MESSAGE			BF1 TIMER 2 PICKUP DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE			BF1 USE TIMER 3:	Range: Yes, No
			Yes	
MESSAGE			BF1 TIMER 3 PICKUP DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE			BF1 BKR POS1 ϕ A/3P:	Range: FlexLogic™ Operand
			Off	
MESSAGE			BF1 BKR POS2 ϕ A/3P:	Range: FlexLogic™ Operand
			Off	
MESSAGE			BF1 BREAKER TEST ON:	Range: FlexLogic™ Operand
			Off	
MESSAGE			BF1 PH AMP HISET PICKUP: 1.050 pu	Range: 0.001 to 30.000 pu in steps of 0.001
MESSAGE			BF1 N AMP HISET PICKUP: 1.050 pu	Range: 0.001 to 30.000 pu in steps of 0.001

MESSAGE		BF1 PH AMP LOSET PICKUP: 1.050 pu	Range: 0.001 to 30.000 pu in steps of 0.001
MESSAGE		BF1 N AMP LOSET PICKUP: 1.050 pu	Range: 0.001 to 30.000 pu in steps of 0.001
MESSAGE		BF1 LOSET TIME DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE		BF1 TRIP DROPOUT DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE		BF1 TARGET Latched	Range: Self-reset, Latched, Disabled
MESSAGE		BF1 EVENTS Enabled	Range: Disabled, Enabled
MESSAGE		BF1 PH A INITIATE: Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.
MESSAGE		BF1 PH B INITIATE: Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.
MESSAGE		BF1 PH C INITIATE: Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.
MESSAGE		BF1 BKR POS1 ϕ B Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.
MESSAGE		BF1 BKR POS1 ϕ C Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.
MESSAGE		BF1 BKR POS2 ϕ B Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.
MESSAGE		BF1 BKR POS2 ϕ C Off	Range: FlexLogic™ Operand Note: valid only for 1-Pole breaker failure schemes.

There are 2 identical Breaker Failure menus available, numbered 1 and 2.

a) BREAKER FAILURE PROTECTION

In general, a breaker failure scheme determines that a breaker signaled to trip has not cleared a fault within a definite time, so further tripping action must be performed. Tripping from the breaker failure scheme should trip all breakers, both local and remote, that can supply current to the faulted zone. Usually operation of a breaker failure element will cause clearing of a larger section of the power system than the initial trip. Because breaker failure can result in tripping a large number of breakers and this affects system safety and stability, a very high level of security is required.

Two schemes are provided, one for use with three-pole only tripping (identified by the name "3BF") and one for use on three pole + single-pole operation (identified by the name "1BF"). The philosophy used in these schemes is identical.

The operation of a breaker failure element includes three stages: initiation, determination of a breaker failure condition, and output; as described below.

INITIATION:

A FlexLogic™ operand that represents the protection trip signal initially sent to the breaker, initiates the scheme. (The protection trip signal does not include other breaker commands that are not indicative of a fault in the protected zone.) The initiating signal should be sealed-in if primary fault detection can reset before the breaker failure timers have finished timing. The seal-in is supervised by current level, so it is reset when the fault is cleared. If desired, an incomplete sequence seal-in reset can be implemented by using the initiating operand to also initiate a FlexLogic™ timer, set longer than any breaker failure timer, whose output operand is selected to block the breaker failure scheme.

Schemes can be initiated either directly or with current level supervision. It is particularly important in any application to decide if a current-supervised initiate is to be used. The use of a current-supervised initiate results in the breaker failure element not being initiated for a breaker that has very little or no current flowing through it, which may be the case for transformer faults. For those situations where it is required to maintain breaker fail coverage for fault levels below the BF1 PH AMP SUPV PICKUP or the BF1 N AMP SUPV PICKUP setting, a current supervised initiate should not be used. This feature should be utilized for those situations where coordinating margins may be reduced when high speed reclosing is used. Thus, if this choice is made, fault levels must always be above the supervision pickup levels for dependable operation of the breaker fail scheme. This can also occur in breaker-and-a-half or ring bus configurations where the first breaker closes into a fault; the protection trips and attempts to initiate breaker failure for the second breaker, which is in the process of closing, but does not yet have current flowing through it.

Immediately when the scheme is initiated, it will send a trip signal to the breaker initially signaled to trip, a feature usually described as Re-Trip. This is intended to reduce the possibility of widespread tripping that results from a declaration of a failed breaker.

DETERMINATION OF A BREAKER FAILURE CONDITION:

The schemes determine a breaker failure condition via three 'paths'. Each of these paths is equipped with a time delay, after which a failed breaker is declared and trip signals are sent to all breakers required to clear the zone. The delayed paths are associated with Breaker Failure Timers 1, 2 and 3, which are intended to have delays increasing with increasing timer numbers. These delayed paths are individually enabled to allow for maximum flexibility.

Timer 1 logic (Early Path) is supervised by a fast-operating breaker auxiliary contact. If the breaker is still closed (as indicated by the auxiliary contact) and fault current is detected after the delay interval, an output is issued. Operation of the breaker auxiliary switch indicates that the breaker has mechanically operated. The continued presence of current indicates that the breaker has failed to interrupt the circuit.

Timer 2 logic (Main Path) is not supervised by a breaker auxiliary contact. If fault current is detected after the delay interval, an output is issued. This path is intended to detect a breaker that opens mechanically but fails to interrupt fault current; the logic therefore does not use a breaker auxiliary contact.

The Timer 1 and 2 paths provide two levels of current supervision, Hiset and Loset, so that the supervision level can be changed from a current which flows before a breaker inserts an opening resistor into the faulted circuit to a lower level after resistor insertion. The Hiset detector is enabled after timeout of Timer 1 or 2, along with a timer that will enable the Loset detector after its delay interval. The delay interval between Hiset and Loset is the expected breaker opening time.

Both current detectors provide a fast operating time for currents at small multiples of the pickup value. The O/C detectors are required to operate after the breaker failure delay interval to eliminate the need for very fast resetting O/C detectors.

Timer 3 logic (Slow Path) is supervised by a breaker auxiliary contact and a control switch contact used to indicate that the breaker is in/out of service, disabling this path when the breaker is out of service for maintenance. There is no current level check in this logic as it is intended to detect low magnitude faults and it is therefore the slowest to operate.

OUTPUT:

The outputs from the schemes are:

- FlexLogic™ operands that report on the operation of portions of the scheme
- FlexLogic™ operand used to re-trip the protected breaker
- FlexLogic™ operands that initiate tripping required to clear the faulted zone. The trip output can be sealed-in for an adjustable period.
- Target message indicating a failed breaker has been declared
- Illumination of the faceplate TRIP LED (and the PHASE A, B or C LED, if applicable)

MAIN PATH SEQUENCE:

A diagram showing trip operating sequences is shown below:

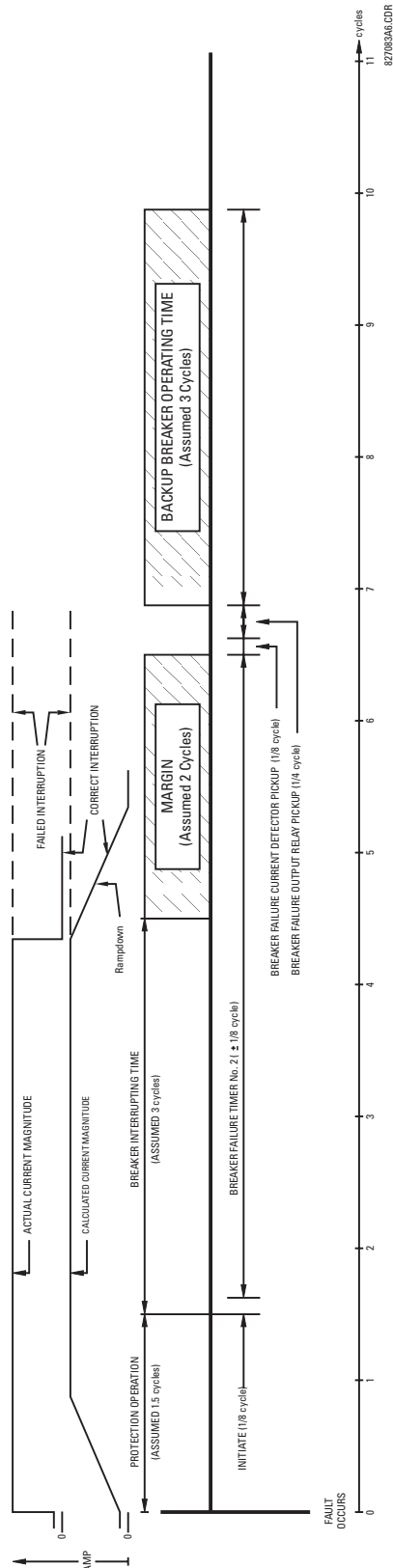


Figure 5-32: BREAKER FAILURE MAIN PATH SEQUENCE

BF1 MODE:

This setting is used to select the breaker failure operating mode: single or three pole.

BF1 USE AMP SUPV:

If set to Yes, the element will only be initiated if current flowing through the breaker is above the supervision pickup level.

BF1 USE SEAL-IN:

If set to Yes, the element will only be sealed-in if current flowing through the breaker is above the supervision pickup level.

BF1 3-POLE INITIATE:

This setting is used to select the Flexlogic™ operand that will initiate 3-pole tripping of the breaker.

BF1 PH AMP SUPV PICKUP:

This setting is used to set the phase current initiation and seal-in supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker. It can be set as low as necessary (lower than breaker resistor current or lower than load current) - Hiset and Loset current supervision will guarantee correct operation.

BF1 N AMP SUPV PICKUP: **

This setting is used to set the neutral current initiate and seal-in supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker. Neutral current supervision is used only in the three phase scheme to provide increased sensitivity.

** This setting is valid only for 3-Pole breaker failure schemes.

BF1 USE TIMER 1:

If set to Yes, the Early Path is operational.

BF1 TIMER 1 PICKUP DELAY:

Timer 1 is set to the shortest time required for breaker auxiliary contact Status-1 to open, from the time the initial trip signal is applied to the breaker trip circuit, plus a safety margin.

BF1 USE TIMER 2:

If set to Yes, the Main Path is operational.

BF1 TIMER 2 PICKUP DELAY:

Timer 2 is set to the expected opening time of the breaker, plus a safety margin. This safety margin was historically intended to allow for measuring and timing errors in the breaker failure scheme equipment. In microprocessor relays this time is not significant. In UR relays, which use a Fourier transform, the calculated current magnitude will ramp-down to zero one power frequency cycle after the current is interrupted, and this lag should be included in the overall margin duration, as it occurs after current interruption. On the figure BREAKER FAILURE MAIN PATH SEQUENCE, a margin of two cycles is presented; this interval is considered the minimum appropriate for most applications.

Note that in bulk oil circuit breakers, the interrupting time for currents less than 25% of the interrupting rating can be significantly longer than the normal interrupting time.

BF1 USE TIMER 3:

If set to Yes, the Slow Path is operational.

BF1 TIMER 3 PICKUP DELAY:

Timer 3 is set to the same interval as Timer 2, plus an increased safety margin. Because this path is intended to operate only for low level faults, the delay can be in the order of 300-500 ms.

BF1 BKR POS1 ϕ A/3P:

This setting is used to select the FlexLogic™ operand that represents the protected breaker early-type auxiliary switch contact (52/a). When using 1-Pole breaker failure scheme, this FlexLogic™ operand represents the protected breaker early-type auxiliary switch contact on pole A. This is normally a non-multiplied Form-A contact. The contact may even be adjusted to have the shortest possible operating time.

BF1 BKR POS2 ϕ A/3P:

This setting is used to select the FlexLogic™ operand that represents the breaker normal-type auxiliary switch contact (52/a). When using 1-Pole breaker failure scheme, this FlexLogic™ operand represents the protected breaker auxiliary switch contact on pole A. This may be a multiplied contact.

BF1 BREAKER TEST ON:

This setting is used to select the FlexLogic™ operand that represents the breaker In-Service/Out-of-Service switch set to the Out-of-Service position.

BF1 PH AMP HISET PICKUP:

This setting is used to set the phase current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, before a breaker opening resistor is inserted.

BF1 N AMP HISET PICKUP: **

This setting is used to set the neutral current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, before a breaker opening resistor is inserted. Neutral current supervision is used only in the three pole scheme to provide increased sensitivity.

** This setting is valid only for 3-Pole breaker failure schemes.

BF1 PH AMP LOSET PICKUP:

This setting is used to set the phase current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, after a breaker opening resistor is inserted (approximately 90% of the resistor current).

BF1 N AMP LOSET PICKUP: **

This setting is used to set the neutral current output supervision level. Generally this setting should detect the lowest expected fault current on the protected breaker, after a breaker opening resistor is inserted (approximately 90% of the resistor current).

** This setting is valid only for 3-Pole breaker failure schemes.

BF1 LOSET TIME DELAY:

This setting is used to set the pickup delay for current detection after opening resistor insertion.

BF1 TRIP DROPOUT DELAY:

This setting is used to set the period of time for which the trip output is sealed-in. This timer must be coordinated with the automatic reclosing scheme of the failed breaker, to which the breaker failure element sends a cancel reclosure signal. Reclosure of a remote breaker can also be prevented by holding a Transfer Trip signal on longer than the "reclaim" time.

The following settings are valid for 1-Pole breaker failure schemes only:

BF1 PH A INITIATE:

This setting is used to select the FlexLogic™ operand that will initiate phase A 1-pole tripping of the breaker and the phase A portion of the scheme.

BF1 PH B INITIATE:

This setting is used to select the FlexLogic™ operand that will initiate phase B 1-pole tripping of the breaker and the phase B portion of the scheme.

BF1 PH C INITIATE:

This setting is used to select the FlexLogic™ operand that will initiate phase C 1-pole tripping of the breaker and the phase C portion of the scheme.

BF1 BKR POS1 ϕ B:

This setting is used to select the FlexLogic™ operand that represents the protected breaker early-type auxiliary switch contact on pole B. This contact is normally a non-multiplied Form-A contact. The contact may even be adjusted to have the shortest possible operating time.

BF1 BKR POS1 ϕ C:

This setting is used to select the FlexLogic™ operand that represents the protected breaker early-type auxiliary switch contact on pole C. This contact is normally a non-multiplied Form-A contact. The contact may even be adjusted to have the shortest possible operating time.

5

BF1 BKR POS2 ϕ B:

This setting is used to select the FlexLogic™ operand that represents the protected breaker normal-type auxiliary switch contact on pole B (52/a). This may be a multiplied contact.

BF1 BKR POS2 ϕ C:

This setting is used to select the FlexLogic™ operand that represents the protected breaker normal-type auxiliary switch contact on pole C (52/a). This may be a multiplied contact.

For single-pole operation, the scheme has the same overall general concept except that it provides re-tripping of each single pole of the protected breaker.

The approach shown in the following single pole tripping figure uses the initiating information to determine which pole is supposed to trip. The logic is segregated on a per-pole basis. The overcurrent detectors have ganged settings.

Upon operation of the breaker failure element for a single pole trip command, a 3-pole trip command should be given via output operand "BF1 TRIP OP".

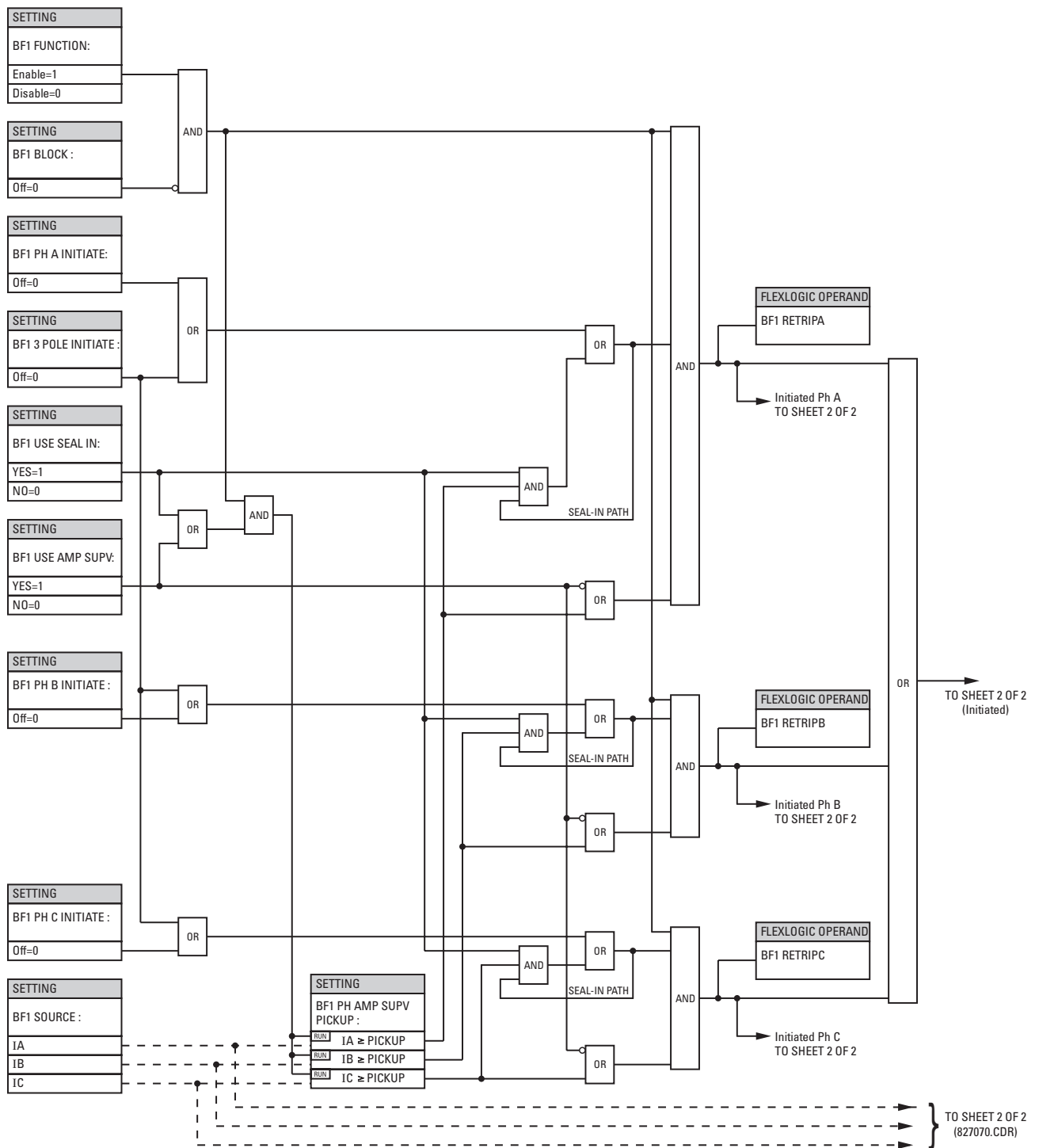


Figure 5-33: BREAKER FAILURE 1-POLE (INITIATE) [Sheet 1 of 2]

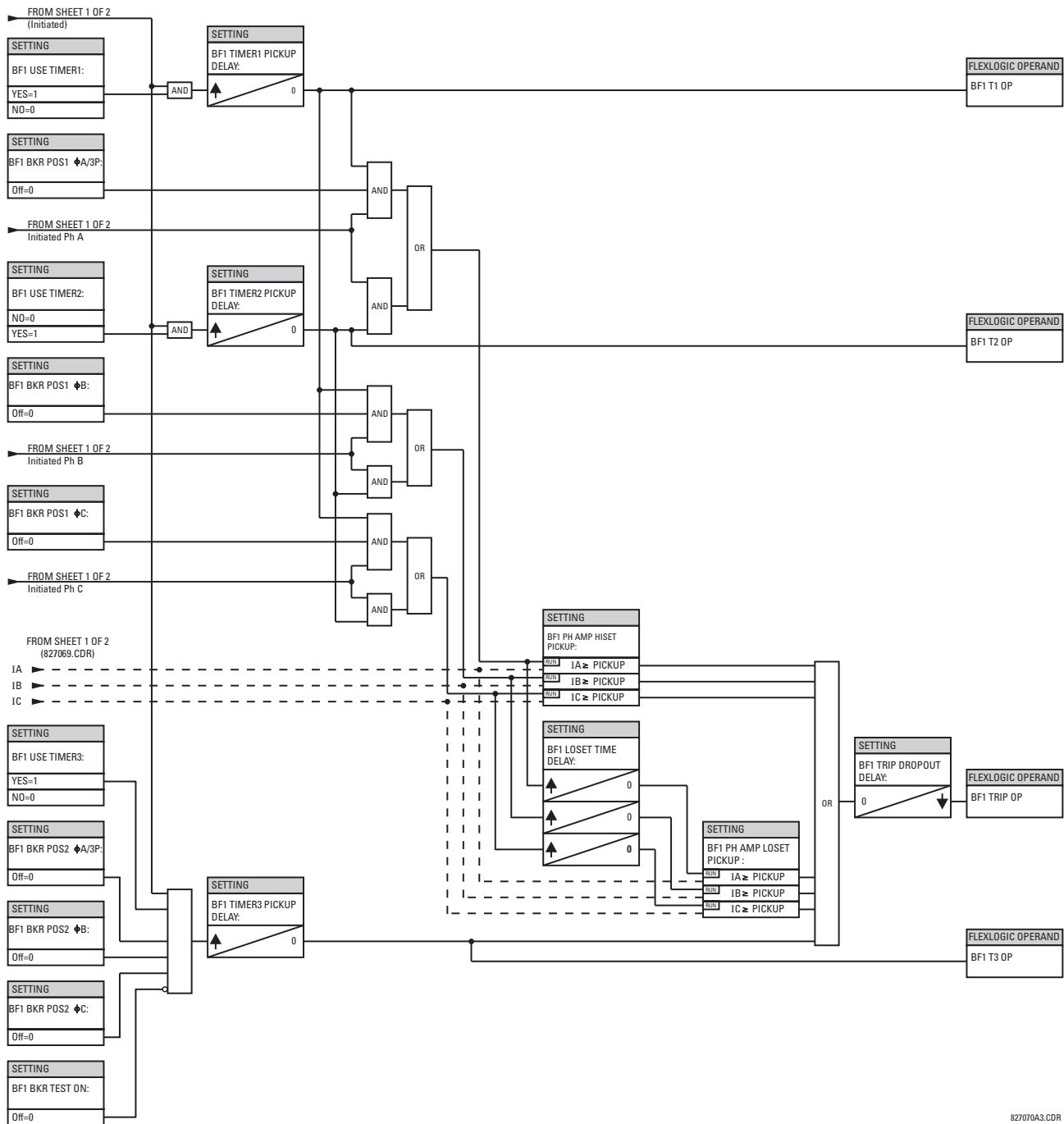


Figure 5–34: BREAKER FAILURE 1-POLE (TIMERS) [Sheet 2 of 2]

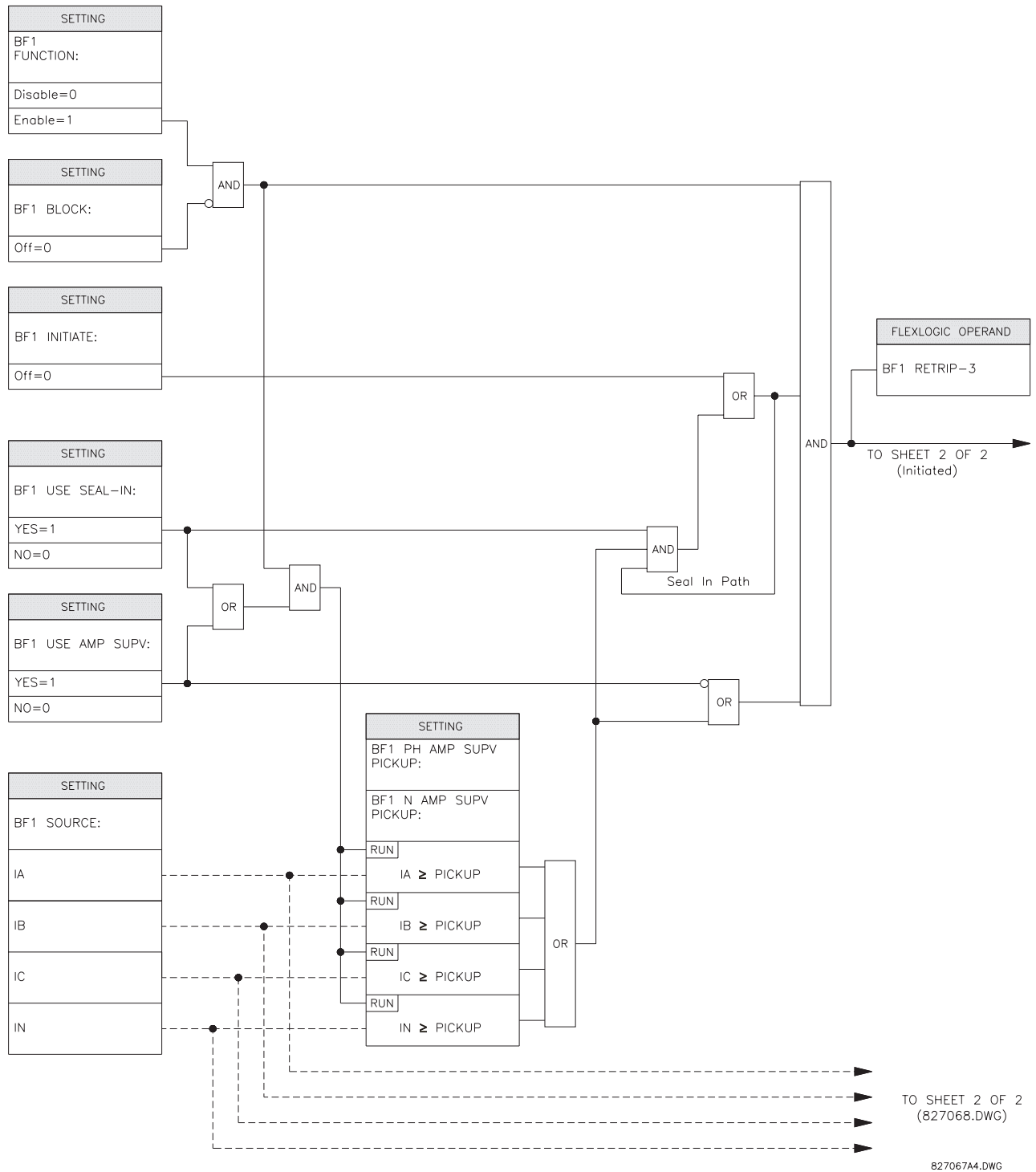


Figure 5–35: BREAKER FAILURE 3-POLE (INITIATE) [Sheet 1 of 2]

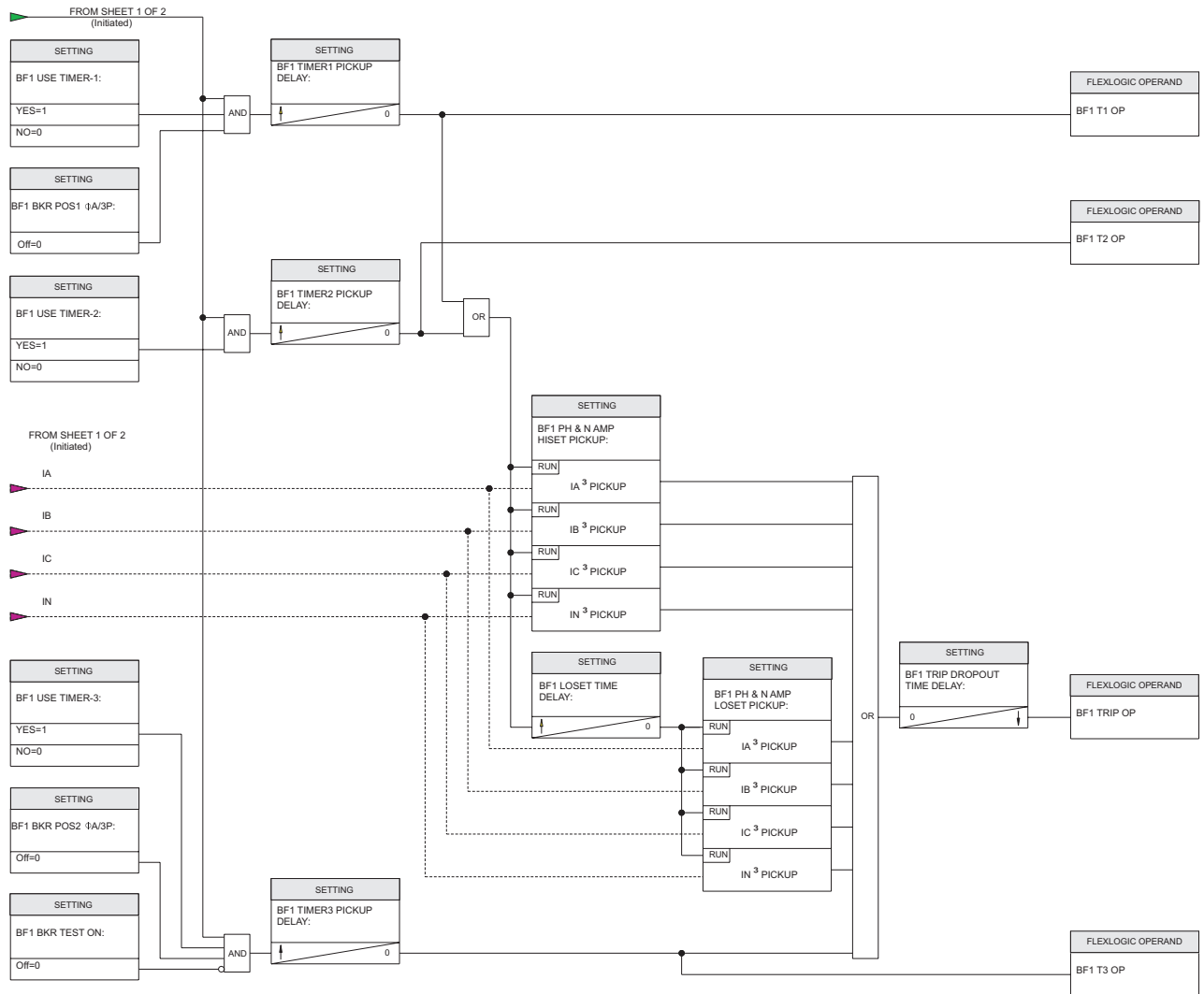
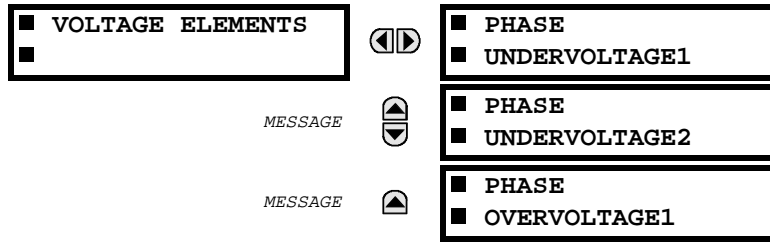


Figure 5–36: BREAKER FAILURE 3-POLE (TIMERS) [Sheet 2 of 2]

5.5.8 VOLTAGE ELEMENTS MENU

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ VOLTAGE ELEMENTS



These protection elements can be used for a variety of applications such as:

Undervoltage Protection: For voltage sensitive loads, such as induction motors, a drop in voltage will result in an increase in the drawn current, which may cause dangerous overheating in the motor. The undervoltage protection feature can be used to either cause a trip or generate an alarm when the voltage drops below a specified voltage setting for a specified time delay.

Permissive Functions: The undervoltage feature may be used to block the functioning of external devices by operating an output relay when the voltage falls below the specified voltage setting. The undervoltage feature may also be used to block the functioning of other elements through the block feature of those elements.

Source Transfer Schemes: In the event of an undervoltage, a transfer signal may be generated to transfer a load from its normal source to a standby or emergency power source.

5

a) UNDERVOLTAGE DEFINITE TIME CHARACTERISTICS

DEFINITE TIME CURVE

The undervoltage elements can be programmed to have a Definite Time delay characteristic. The Definite Time curve operates when the voltage drops below the pickup level for a specified period of time. The time delay is adjustable from 0 to 600.00 seconds in steps of 10 ms.

b) UNDERVOLTAGE INVERSE TIME CHARACTERISTICS

The undervoltage elements can be programmed to have an inverse time delay characteristic. The undervoltage delay setting defines a family of curves as illustrated by the following equation and figure.

$$T = \frac{D}{\left(1 - \frac{V}{V_{pickup}}\right)}$$

where: T = Operating Time
 D = Undervoltage Delay Setting (0.00 gives instantaneous operate)
 V = Secondary Voltage applied to the relay
 V_{pickup} = Pickup Level

Note: at 0% of pickup, the operating time equals the Undervoltage Delay Setting.

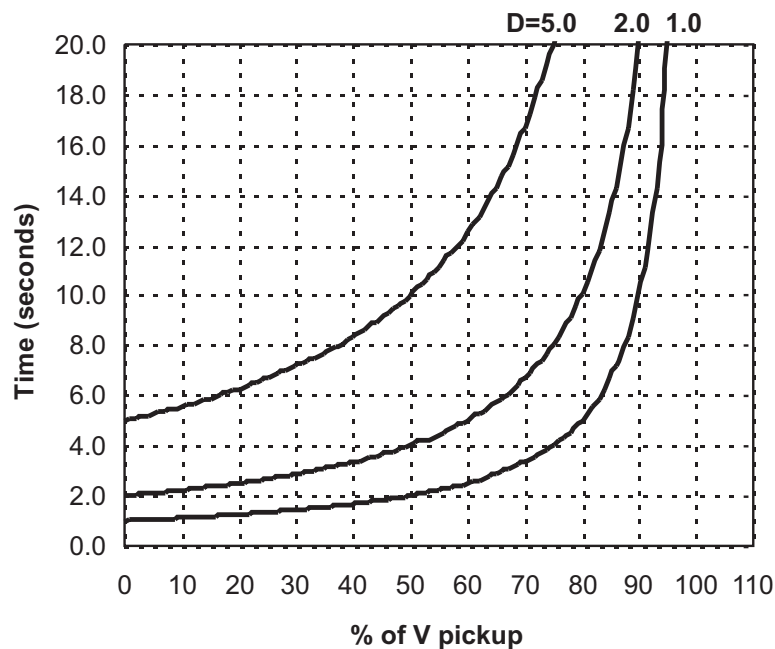


Figure 5–37: INVERSE TIME UNDERVOLTAGE CURVES

c) PHASE UV1 / UV2 (PHASE UNDERVOLTAGE - ANSI 27P)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ VOLTAGE ELEMENTS ⇒ ↓ PHASE UNDERVOLTAGE1

<div> <div>■ PHASE</div> <div>■ UNDERVOLTAGE1</div> </div>		<div> <div>◀▶</div> <div> <div>PHASE UV1</div> <div>FUNCTION: Disabled</div> </div> </div>	Range: Disabled, Enabled
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1 SIGNAL</div> <div>SOURCE: SRC 1</div> </div> </div>	Range: SRC 1,..., SRC 6
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1 MODE:</div> <div>Phase to Ground</div> </div> </div>	Range: Phase to Ground, Phase to Phase
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1</div> <div>PICKUP: 1.000 pu</div> </div> </div>	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1</div> <div>CURVE: Definite Time</div> </div> </div>	Range: Definite Time, Inverse Time
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1</div> <div>DELAY: 1.00 s</div> </div> </div>	Range: 0.00 to 600.00 s in steps of 0.01
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1 MINIMUM</div> <div>VOLTAGE: 0.100 pu</div> </div> </div>	Range: 0.000 to 3.000 pu in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1 BLOCK:</div> <div>Off</div> </div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE UV1</div> <div>TARGET: Self-reset</div> </div> </div>	Range: Self-reset, Latched, Disabled
	MESSAGE	<div> <div>▲</div> <div> <div>PHASE UV1</div> <div>EVENTS: Disabled</div> </div> </div>	Range: Disabled, Enabled

The phase undervoltage element may be used to give a desired time-delay operating characteristic versus the applied fundamental voltage (phase to ground or phase to phase for Wye VT connection, or phase to phase only for Delta VT connection) or as a simple Definite Time element. The element resets instantaneously if the applied voltage exceeds the dropout voltage. The delay setting selects the minimum operating time of the phase undervoltage element. The minimum voltage setting selects the operating voltage below which the element is blocked (a setting of '0' will allow a dead source to be considered a fault condition).

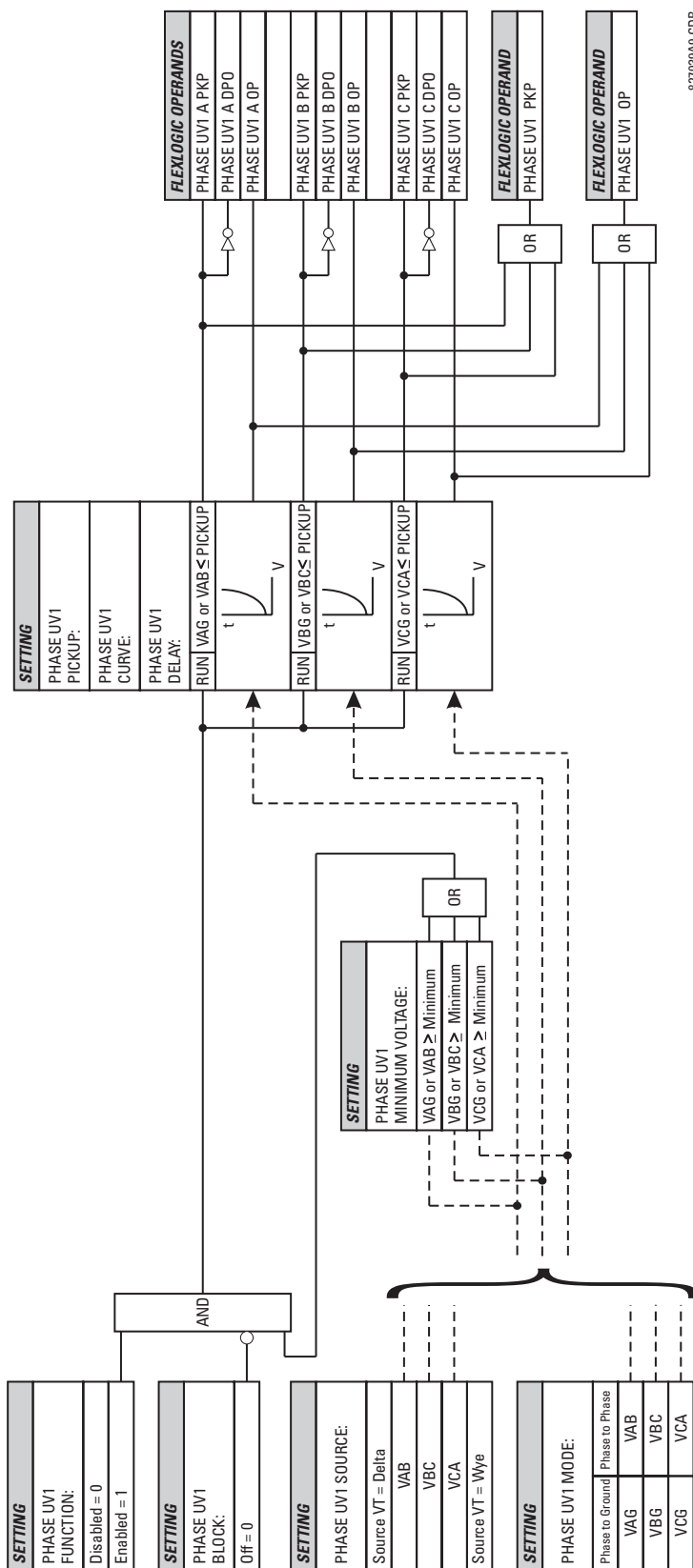


Figure 5-38: PHASE UV1 SCHEME LOGIC

d) PHASE OV1 (PHASE OVERVOLTAGE - ANSI 59P)

PATH: SETTINGS ↓ GROUPED ELEMENTS ⇒ SETTING GROUP 1(8) ⇒ ↓ VOLTAGE ELEMENTS ⇒ ↓ PHASE OVERVOLTAGE1

<div> <div>■ PHASE</div> <div>■ OVERVOLTAGE1</div> </div>		<div> <div>◀▶</div> <div> <div>PHASE OV1</div> <div>FUNCTION: Disabled</div> </div> </div>	Range: Disabled, Enabled
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE OV1 SIGNAL</div> <div>SOURCE: SRC 1</div> </div> </div>	Range: SRC 1,..., SRC 6
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE OV1</div> <div>PICKUP: 1.000 pu</div> </div> </div>	Range: 0.000 to 3.000 pu in steps of 0.001 pu
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE OV1 PICKUP</div> <div>DELAY: 1.00 s</div> </div> </div>	Range: 0.00 to 600.00 s in steps of 0.01 s
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE OV1 RESET</div> <div>DELAY: 1.00 s</div> </div> </div>	Range: 0.00 to 600.00 s in steps of 0.01 s
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE OV1 BLOCK:</div> <div>Off</div> </div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div> <div>PHASE OV1</div> <div>TARGET: Self-reset</div> </div> </div>	Range: Self-reset, Latched, Disabled
	MESSAGE	<div> <div>▲</div> <div> <div>PHASE OV1</div> <div>EVENTS: Disabled</div> </div> </div>	Range: Disabled, Enabled

The phase overvoltage element may be used as an instantaneous element with no intentional time delay or as a Definite Time element. The input voltage is the phase-to-phase voltage, either measured directly from Delta-connected VTs or as calculated from phase-to-ground (Wye) connected VTs. The specific voltages to be used for each phase are shown on the logic diagram.

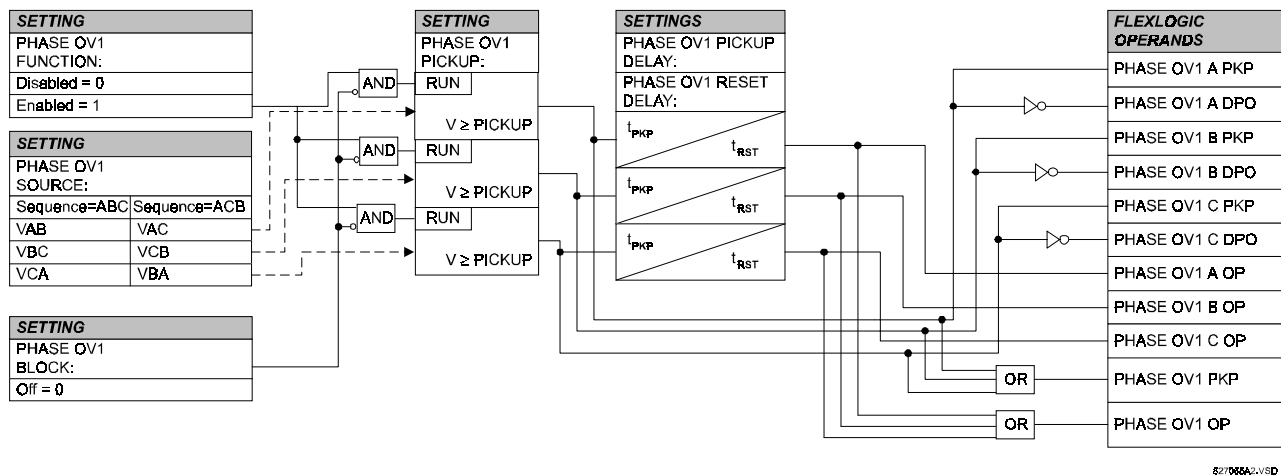


Figure 5-39: PHASE OV1 SCHEME LOGIC

5.6.1 OVERVIEW

CONTROL elements are generally used for control rather than for protection. See the INTRODUCTION TO ELEMENTS section at the front of this chapter for further information.

5.6.2 SETTING GROUPS MENU

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ SETTINGS GROUPS

<div>5</div>	■ SETTING GROUPS	◀▶	SETTING GROUPS FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE	▲▼	SETTING GROUPS BLK: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 2 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 3 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 4 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 5 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 6 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 7 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	GROUP 8 ACTIVATE ON: Off	Range: FlexLogic™ Operand
	MESSAGE	▲	SETTING GROUP EVENTS: Disabled	Range: Disabled, Enabled

This Setting Groups menu controls the activation/de-activation of up to eight possible groups of settings in the GROUPED ELEMENTS settings menu. The faceplate 'SETTINGS IN USE' LEDs indicate which active group (with a non-flashing energized LED) is in service.

The **SETTING GROUPS BLK** block setting prevents the active setting group from changing when the FlexLogic™ parameter is set to 'On'. This can be useful in applications where it is undesirable to change the settings under certain conditions such as the breaker being open.

Each **GROUP ~ ACTIVATE ON** setting selects a FlexLogic™ operand which, when set, will make the particular setting group active for use by any grouped element. A priority scheme ensures that only one group is active at a given time – the highest-numbered group which is activated by its ACTIVATE ON parameter takes priority over the lower-numbered groups. There is no "activate on" setting for group 1 (the default active group), because group 1 automatically becomes active if no other group is active.

The relay can be set up via a FlexLogic™ equation to receive requests to activate or de-activate a particular non-default settings group. The following FlexLogic™ equation (see figure EXAMPLE FLEXLOGIC™ CONTROL OF A SETTINGS GROUP) illustrates requests via remote communications (e.g. VIRTUAL INPUT 1) or from a local contact input (e.g. H7a) to initiate the use of a particular settings group, and requests from several overcurrent pickup measuring elements to inhibit the use of the particular settings group. The assigned VIRTUAL OUTPUT 1 operand is used to control the ON state of a particular settings group.

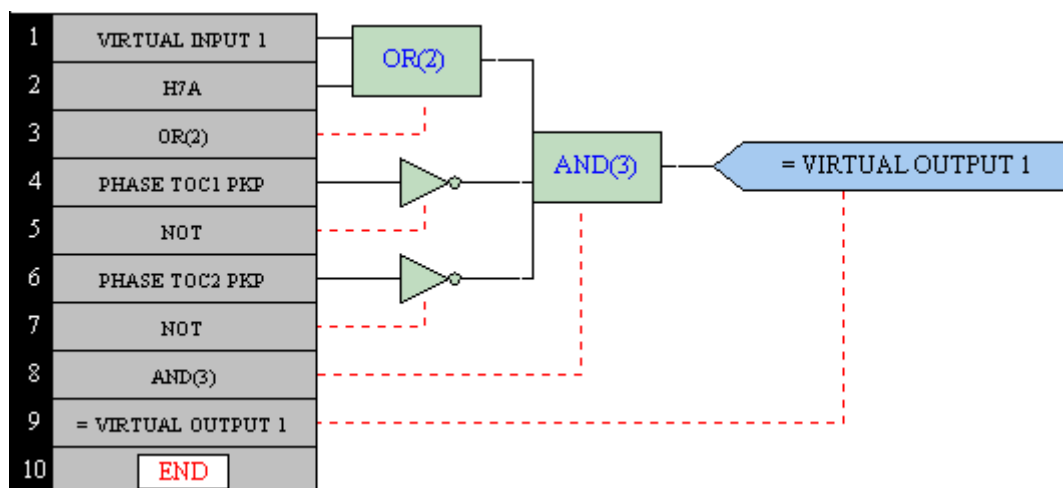


Figure 5-40: EXAMPLE FLEXLOGIC™ CONTROL OF A SETTINGS GROUP

5.6.3 SYNCHROCHECK 1(2)

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ SYNCHROCHECK ⇌ SYNCHROCHECK 1(2)

<div> <div>■ SYNCHROCHECK 1</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> </div>	<div> <div>◀▶</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲</div> </div>	<div> <div>SYNCHK1 FUNCTION:</div> <div>Disabled</div> </div>	Range: Disabled, Enabled
		<div> <div>SYNCHK1 BLOCK:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
		<div> <div>SYNCHK1 V1 SOURCE:</div> <div>SRC 1</div> </div>	Range: SRC 1, ..., SRC 6
		<div> <div>SYNCHK1 V2 SOURCE:</div> <div>SRC 2</div> </div>	Range: SRC 1, ..., SRC 6
		<div> <div>SYNCHK1 MAX VOLT</div> <div>DIFF: 10000 V</div> </div>	Range: 0 to 100,000 V in steps of 1
		<div> <div>SYNCHK1 MAX ANGLE</div> <div>DIFF: 30°</div> </div>	Range: 0 to 100° in steps of 1
		<div> <div>SYNCHK1 MAX FREQ</div> <div>DIFF: 1.00 Hz</div> </div>	Range: 0.00 to 2.00 Hz in steps of 0.01 Hz
		<div> <div>SYNCHK1 DEAD SOURCE</div> <div>SELECT: LV1 and DV2</div> </div>	Range: None, LV1 and DV2, DV1 and LV2, DV1 or DV2, DV1 Xor DV2, DV1 and DV2
		<div> <div>SYNCHK1 DEAD V1</div> <div>MAX VOLT: 0.30 pu</div> </div>	Range: 0.00 to 1.25 pu in steps of 0.01
		<div> <div>SYNCHK1 DEAD V2</div> <div>MAX VOLT: 0.30 pu</div> </div>	Range: 0.00 to 1.25 pu in steps of 0.01
		<div> <div>SYNCHK1 LIVE V1</div> <div>MIN VOLT: 0.70 pu</div> </div>	Range: 0.00 to 1.25 pu in steps of 0.01
		<div> <div>SYNCHK1 LIVE V2</div> <div>MIN VOLT: 0.70 pu</div> </div>	Range: 0.00 to 1.25 pu in steps of 0.01
		<div> <div>SYNCHK1 TARGET:</div> <div>Self-reset</div> </div>	Range: Self-reset, Latched, Disabled
		<div> <div>SYNCHK1 EVENTS:</div> <div>Disabled</div> </div>	Range: Disabled, Enabled

There are two identical synchrocheck elements available, numbered 1 and 2.

The synchronism check function is intended for supervising the paralleling of two parts of a system which are to be joined by the closure of a circuit breaker. The synchrocheck elements are typically used at locations where the two parts of the system are interconnected through at least one other point in the system.

Synchrocheck verifies that the voltages (V1 and V2) on the two sides of the supervised circuit breaker are within set limits of magnitude, angle and frequency differences.

The time while the two voltages remain within the admissible angle difference is determined by the setting of the phase angle difference $\Delta\Phi$ and the frequency difference ΔF (slip frequency). It can be defined as the time it would take the voltage phasor V1 or V2 to traverse an angle equal to $2 \times \Delta\Phi$ at a frequency equal to the frequency difference ΔF . This time can be calculated by:

$$T = \frac{1}{\frac{360^\circ}{2 \times \Delta\Phi} \times \Delta F}$$

where: $\Delta\Phi$ = phase angle difference in degrees; ΔF = frequency difference in Hz.

As an example; for the default values ($\Delta\Phi = 30^\circ$, $\Delta F = 0.1$ Hz), the time while the angle between the two voltages will be less than the set value is:

$$T = \frac{1}{\frac{360^\circ}{2 \times \Delta\Phi} \times \Delta F} = \frac{1}{\frac{360^\circ}{2 \times 30^\circ} \times 0.1 \text{ Hz}} = 1.66 \text{ sec.}$$

If one or both sources are de-energized, the synchrocheck programming can allow for closing of the circuit breaker using undervoltage control to by-pass the synchrocheck measurements (Dead Source function).

SETTINGS:

SYNCHK1 V1 SOURCE:

This setting selects the source for voltage V1 (see **NOTES** below).

SYNCHK1 V2 SOURCE:

This setting selects the source for voltage V2, which must not be the same as used for the V1 (see **NOTES** below).

SYNCHK1 MAX VOLT DIFF:

This setting selects the maximum voltage difference in 'kV' between the two sources. A voltage magnitude difference between the two input voltages below this value is within the permissible limit for synchronism.

SYNCHK1 MAX ANGLE DIFF:

This setting selects the maximum angular difference in degrees between the two sources. An angular difference between the two input voltage phasors below this value is within the permissible limit for synchronism.

SYNCHK1 MAX FREQ DIFF:

This setting selects the maximum frequency difference in 'Hz' between the two sources. A frequency difference between the two input voltage systems below this value is within the permissible limit for synchronism.

SYNCHK1 DEAD SOURCE SELECT:

This setting selects the combination of dead and live sources that will by-pass synchronism check function and permit the breaker to be closed when one or both of the two voltages (V1 or/and V2) are below the maximum voltage threshold. A dead or live source is declared by monitoring the voltage level.

Six options are available:

- | | |
|--------------|---|
| None: | Dead Source function is disabled |
| LV1 and DV2: | Live V1 and Dead V2 |
| DV1 and LV2: | Dead V1 and Live V2 |
| DV1 or DV2: | Dead V1 or Dead V2 |
| DV1 Xor DV2: | Dead V1 exclusive-or Dead V2 (one source is Dead and the other is Live) |
| DV1 and DV2: | Dead V1 and Dead V2 |

SYNCHK1 DEAD V1 MAX VOLT:

This setting establishes a maximum voltage magnitude for V1 in 'pu'. Below this magnitude, the V1 voltage input used for synchrocheck will be considered "Dead" or de-energized.

SYNCHK1 DEAD V2 MAX VOLT:

This setting establishes a maximum voltage magnitude for V2 in 'pu'. Below this magnitude, the V2 voltage input used for synchrocheck will be considered "Dead" or de-energized.

SYNCHK1 LIVE V1 MIN VOLT:

This setting establishes a minimum voltage magnitude for V1 in 'pu'. Above this magnitude, the V1 voltage input used for synchrocheck will be considered "Live" or energized.

SYNCHK1 LIVE V2 MIN VOLT:

This setting establishes a minimum voltage magnitude for V2 in 'pu'. Above this magnitude, the V2 voltage input used for synchrocheck will be considered "Live" or energized.

NOTES:

1. The selected Sources for synchrocheck inputs V1 and V2 (which must not be the same Source) may include both a three-phase and an auxiliary voltage. The relay will automatically select the specific voltages to be used by the synchrocheck element in accordance with the following table.

NO.	V1 or V2 (SOURCE y)	V2 or V1 (SOURCE z)	AUTO-SELECTED COMBINATION		AUTO-SELECTED VOLTAGE
			SOURCE y	SOURCE z	
1	Phase VTs and Auxiliary VT	Phase VTs and Auxiliary VT	Phase	Phase	VAB
2	Phase VTs and Auxiliary VT	Phase VT	Phase	Phase	VAB
3	Phase VT	Phase VT	Phase	Phase	VAB
4	Phase VT and Auxiliary VT	Auxiliary VT	Phase	Auxiliary	V auxiliary (as set for Source z)
5	Auxiliary VT	Auxiliary VT	Auxiliary	Auxiliary	V auxiliary (as set for selected sources)

The voltages V1 and V2 will be matched automatically so that the corresponding voltages from the two Sources will be used to measure conditions. A phase to phase voltage will be used if available in both sources; if one or both of the Sources have only an auxiliary voltage, this voltage will be used. For example, if an auxiliary voltage is programmed to VAG, the synchrocheck element will automatically select VAG from the other Source. If the comparison is required on a specific voltage, the user can externally connect that specific voltage to auxiliary voltage terminals and then use this "Auxiliary Voltage" to check the synchronism conditions.

If using a single CT/VT module with both phase voltages and an auxiliary voltage, ensure that only the auxiliary voltage is programmed in one of the Sources to be used for synchrocheck.

Exception: Synchronism cannot be checked between Delta connected phase VTs and a Wye connected auxiliary voltage.

2. The relay measures frequency and Volts/Hz from an input on a given Source with priorities as established by the configuration of input channels to the Source. The relay will use the phase channel of a three-phase set of voltages if programmed as part of that Source. The relay will use the auxiliary voltage channel only if that channel is programmed as part of the Source and a three-phase set is not.

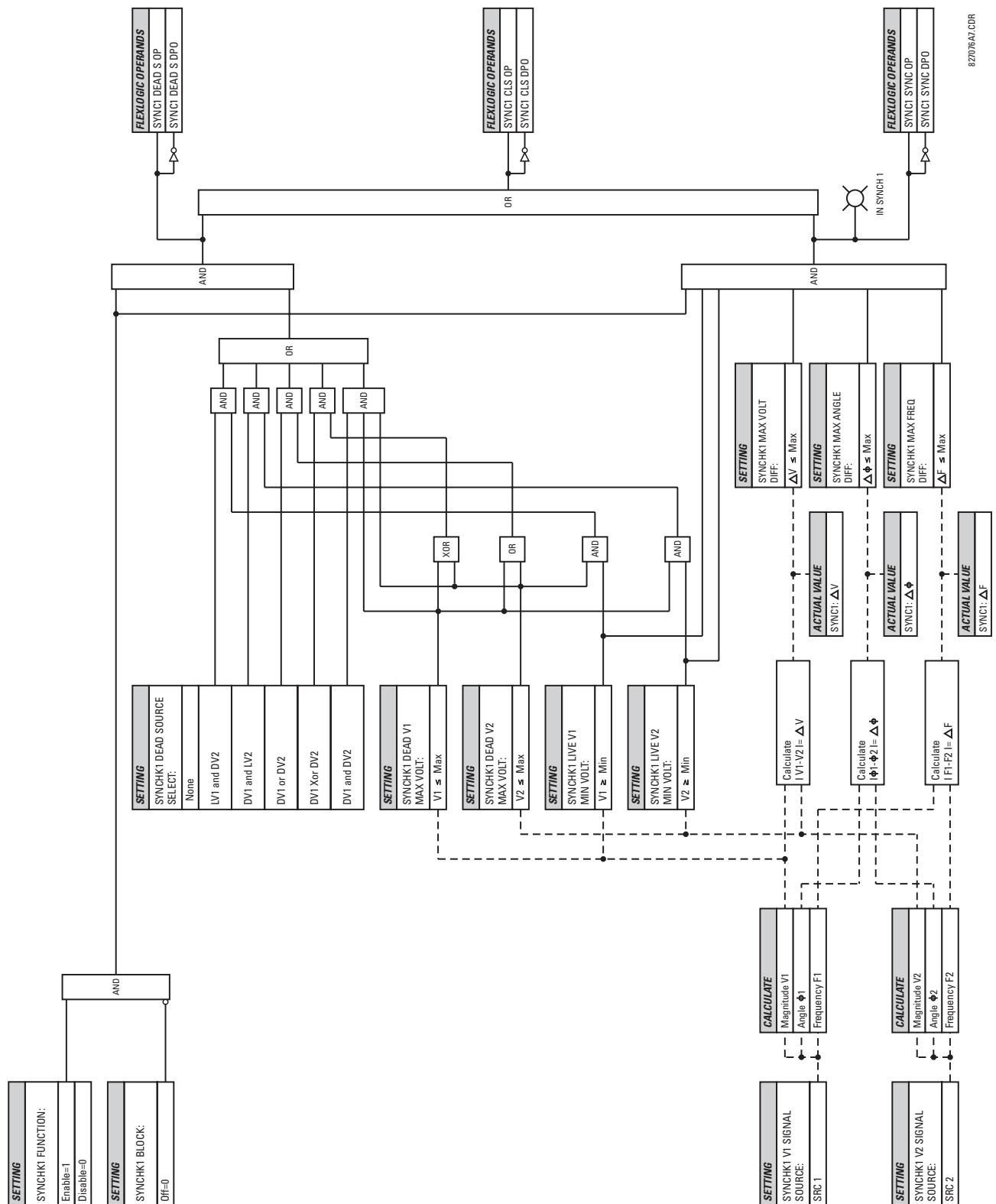


Figure 5–41: SYNCHROCHECK SCHEME LOGIC

5.6.4 AUTORECLOSE

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇨ AUTORECLOSE ⇨ AUTORECLOSE 1

<div> <div>■ AUTORECLOSE 1</div> <div>■</div> </div>		<div> <div>◀▶</div> <div>AR1 FUNCTION:</div> <div>Disabled</div> </div>	Range: Disabled, Enabled
	MESSAGE	<div> <div>▲▼</div> <div>AR1 INITIATE:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 BLOCK:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 MAX NUMBER OF SHOTS:</div> <div>1</div> </div>	Range: 1, 2, 3, 4
	MESSAGE	<div> <div>▲▼</div> <div>AR1 REDUCE MAX TO 1:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 REDUCE MAX TO 2:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 REDUCE MAX TO 3:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 MANUAL CLOSE:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 MNL RST FRM LO:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 RESET LOCKOUT IF BREAKER CLOSED:</div> <div>Off</div> </div>	Range: Off, On
	MESSAGE	<div> <div>▲▼</div> <div>AR1 RESET LOCKOUT ON MANUAL CLOSE:</div> <div>Off</div> </div>	Range: Off, On
	MESSAGE	<div> <div>▲▼</div> <div>AR1 BKR CLOSED:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 BKR OPEN:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 BLK TIME UPON MNL CLS:</div> <div>10.000 s</div> </div>	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>AR1 DEAD TIME 1:</div> <div>1.000 s</div> </div>	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>AR1 DEAD TIME 2:</div> <div>2.000 s</div> </div>	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>AR1 DEAD TIME 3:</div> <div>3.000 s</div> </div>	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>AR1 DEAD TIME 4:</div> <div>4.000 s</div> </div>	Range: 0.000 to 65.535 s in steps of 0.001
	MESSAGE	<div> <div>▲▼</div> <div>AR1 ADD DELAY 1:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
	MESSAGE	<div> <div>▲▼</div> <div>AR1 DELAY 1:</div> <div>0.000 s</div> </div>	Range: 0.000 to 65.535 s in steps of 0.001

MESSAGE		AR1 ADD DELAY 2: Off	Range: FlexLogic™ Operand
MESSAGE		AR1 DELAY 2: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE		AR1 RESET LOCKOUT DELAY: 60.000	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE		AR1 RESET TIME: 60.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE		AR1 INCOMPLETE SEQ TIME: 5.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE		AR1 EVENTS: Disabled	Range: Disabled, Enabled

AUTOMATIC RECLOSURE (AR):

The autoreclosure feature is intended for use with transmission and distribution lines, in three pole tripping schemes for single breaker applications. Up to four selectable reclosures "shots" are possible prior to locking out. Each shot has an independently settable dead time. The protection settings can be changed between shots if so desired, using FlexLogic™. Logic inputs are available for disabling or blocking the scheme.

Faceplate panel LEDs indicate the state of the autoreclose scheme as follows:

- **RECLOSE ENABLED:** The scheme is enabled and may reclose if initiated.
- **RECLOSE DISABLED:** The scheme is disabled.
- **RECLOSE IN PROGRESS:** An autoreclosure has been initiated but the breaker has not yet been signaled to close.
- **RECLOSE LOCKED OUT:** The scheme has generated the maximum number of breaker closures allowed and, as the fault persists, will not close the breaker again; known as "Lockout". The scheme may also be sent in "Lockout" when the incomplete sequence timer times out or when a block signal occurs while in "Reclose in Progress". The scheme must be reset from Lockout in order to perform reclose for further faults.

RECLOSE ENABLED:

The reclosure scheme is considered enabled when all of the following conditions are true:

- The "AR Function" is set to Enabled.
- The scheme is not in the "Lockout" state.
- The "Block" input is not asserted.
- The "AR Block Time Upon Manual Close" timer is not active.

RECLOSE INITIATION:

The autoreclose scheme is initiated by a trip signal from any selected protection feature operand. The scheme is initiated provided the circuit breaker is in the closed state before protection operation.

RECLOSE IN PROGRESS (RIP):

RIP is set when a reclosing cycle begins following a reclose initiate signal. Once the cycle is successfully initiated, the RIP signal will seal-in and the scheme will continue through its sequence until one of the following conditions is satisfied:

- The close signal is issued when the dead timer times out.
- The scheme goes to lockout.

While RIP is active, the scheme checks that the breaker is open and the shot number is below the limit, and then begins measuring the dead time.

DEAD TIME:

Each of the four possible shots has an independently settable dead time. Two additional timers are provided that can be used to increase the initial set dead times 1 to 4 by a delay equal to "AR1 DELAY 1" or "AR1 DELAY 2" or the sum of these two delays depending on the selected settings. This offers enhanced setting flexibility using FlexLogic™ operands to turn the two additional timers "on" and "off". These operands may possibly include "AR x SHOT CNT=n", "SETTING GROUP ACT x", etc.

The autoreclose provides up to maximum 4 selectable shots. Maximum number of shots can be dynamically modified through the settings "AR1 REDUCE MAX TO 1(2,3)", using the appropriate Flexlogic™ operand.

LOCKOUT:

Scheme lockout will block all phases of the reclosing cycle, preventing automatic reclosure, if any of the following conditions occurs:

- The maximum shot number was reached.
- A "Block" input is in effect (for instance; Breaker Failure, bus differential protection operated, etc.).
- The "Incomplete Sequence" timer times out.

The recloser will be latched in the Lockout state until a "Reset from lockout" signal is asserted, either from a manual close of the breaker or from a manual reset command (local or remote).

The reset from lockout can be accomplished:

- by operator command
- by manually closing the breaker
- whenever the breaker has been closed and stays closed for a preset time.

CLOSE:

After the dead time elapses, the scheme issues the close signal. The close signal is latched until the breaker closes or the scheme goes to Lockout.

RESET TIME:

A reset timer output resets the recloser following a successful reclosure sequence. The reset time is based on the breaker "reclaim time" which is the minimum time required between successive reclose sequences.

SETTINGS:

AR1 INITIATE:

Selects the FlexLogic™ Operand that initiates the scheme, typically the trip signal from protection.

AR1 BLOCK:

Selects the FlexLogic™ Operand that blocks the Autoreclosure initiate (it could be from the Breaker Failure, Bus differential protection, etc.).

AR1 MAX NUMBER OF SHOTS:

Specifies the number of reclosures that can be attempted before reclosure goes to "Lockout" because the fault is permanent.

AR1 REDUCE MAX TO 1:

Selects the FlexLogic™ operand that changes the maximum number of shots from the initial setting to 1.

AR1 REDUCE MAX TO 2:

Selects the FlexLogic™ operand that changes the maximum number of shots from the initial setting to 2.

AR1 REDUCE MAX TO 3:

Selects the FlexLogic™ operand that changes the maximum number of shots from the initial setting to 3.

AR1 MANUAL CLOSE:

Selects the logic input set when the breaker is manually closed.

AR1 MNL RST FRM LO:

Selects the FlexLogic™ Operand that resets the autoreclosure from Lockout condition. Typically this is a manual reset from lockout, local or remote.

AR1 RESET LOCKOUT IF BREAKER CLOSED:

This setting allows the autoreclose scheme to reset from Lockout if the breaker has been manually closed and stays closed for a preset time. In order for this setting to be effective, the next setting (AR1 RESET LOCKOUT ON MANUAL CLOSE) should be disabled.

AR 1 RESET LOCKOUT ON MANUAL CLOSE:

This setting allows the autoreclose scheme to reset from Lockout when the breaker is manually closed regardless if the breaker remains closed or not. This setting overrides the previous setting (AR1 RESET LOCKOUT IF BREAKER CLOSED).

AR1 BLK TIME UPON MNL CLS:

The autoreclose scheme can be disabled for a programmable time delay after the associated circuit breaker is manually closed. This prevents reclosing onto a fault after a manual close. This delay must be longer than the slowest expected trip from any protection not blocked after manual closing. If no overcurrent trips occur after a manual close and this time expires, the autoreclose scheme is enabled.

AR1 DEAD TIME 1:

This is the intentional delay before first breaker automatic reclosure (1st shot) and should be set longer than the estimated deionizing time following a three pole trip.

AR1 DEAD TIME 2:

This is the intentional delay before second breaker automatic reclosure (2nd shot) and should be set longer than the estimated deionizing time following a three pole trip.

AR1 DEAD TIME 3:

This is the intentional delay before third breaker automatic reclosure (3rd shot) and should be set longer than the estimated deionizing time following a three pole trip.

AR1 DEAD TIME 4:

This is the intentional delay before fourth breaker automatic reclosure (4th shot) and should be set longer than the estimated deionizing time following a three pole trip.

AR1 ADD DELAY 1:

This setting selects the FlexLogic™ operand that introduces an additional delay (DELAY 1) to the initial set Dead Time (1 to 4). When this setting is "Off", DELAY 1 is by-passed.

AR1 DELAY 1:

This setting establishes the extent of the additional dead time DELAY 1.

AR1 ADD DELAY 2:

This setting selects the FlexLogic™ operand that introduces an additional delay (DELAY 2) to the initial set Dead Time (1 to 4). When this setting is "Off", DELAY 2 is by-passed.

AR1 DELAY 2:

This setting establishes the extent of the additional dead time DELAY 2.

AR1 RESET LOCKOUT DELAY:

This setting establishes how long the breaker should stay closed after a manual close command, in order for the autorecloser to reset from Lockout.

AR1 RESET TIME:

A reset timer output resets the recloser following a successful reclosure sequence. The setting is based on the breaker "reclaim time" which is the minimum time required between successive reclose sequences.

AR1 INCOMPLETE SEQ TIME:

This timer is used to set the maximum time interval allowed for a single reclose shot. It is started whenever a reclosure is initiated and is active when the scheme is in the "RECLOSE IN PROGRESS" state. If all conditions allowing a breaker closure are not satisfied when this time expires, the scheme goes to "Lockout".

5

This timer must be set to a delay less than the reset timer.

NOTE

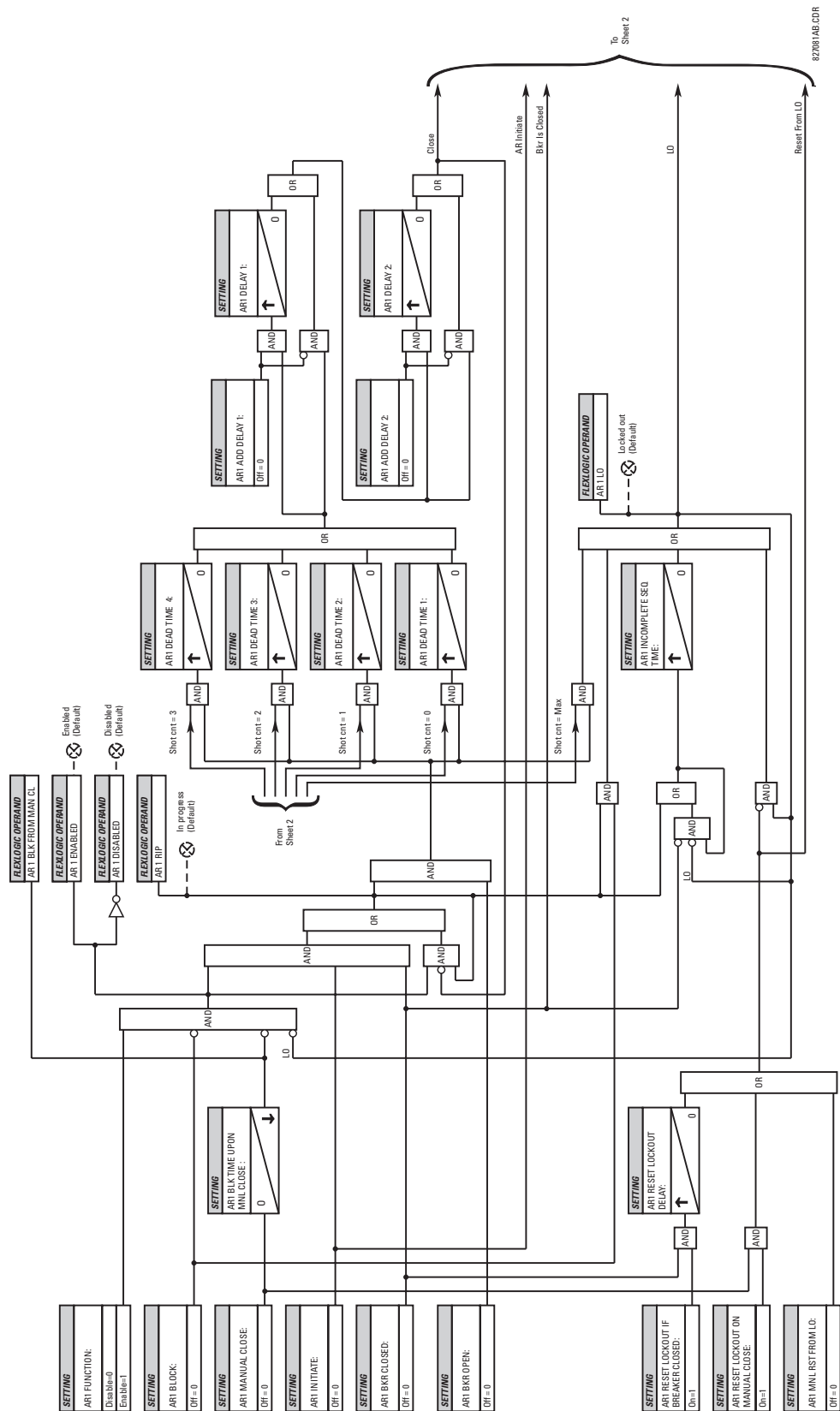


Figure 5-42: AUTORECLOSURE SCHEME LOGIC (Sheet 1 of 2)



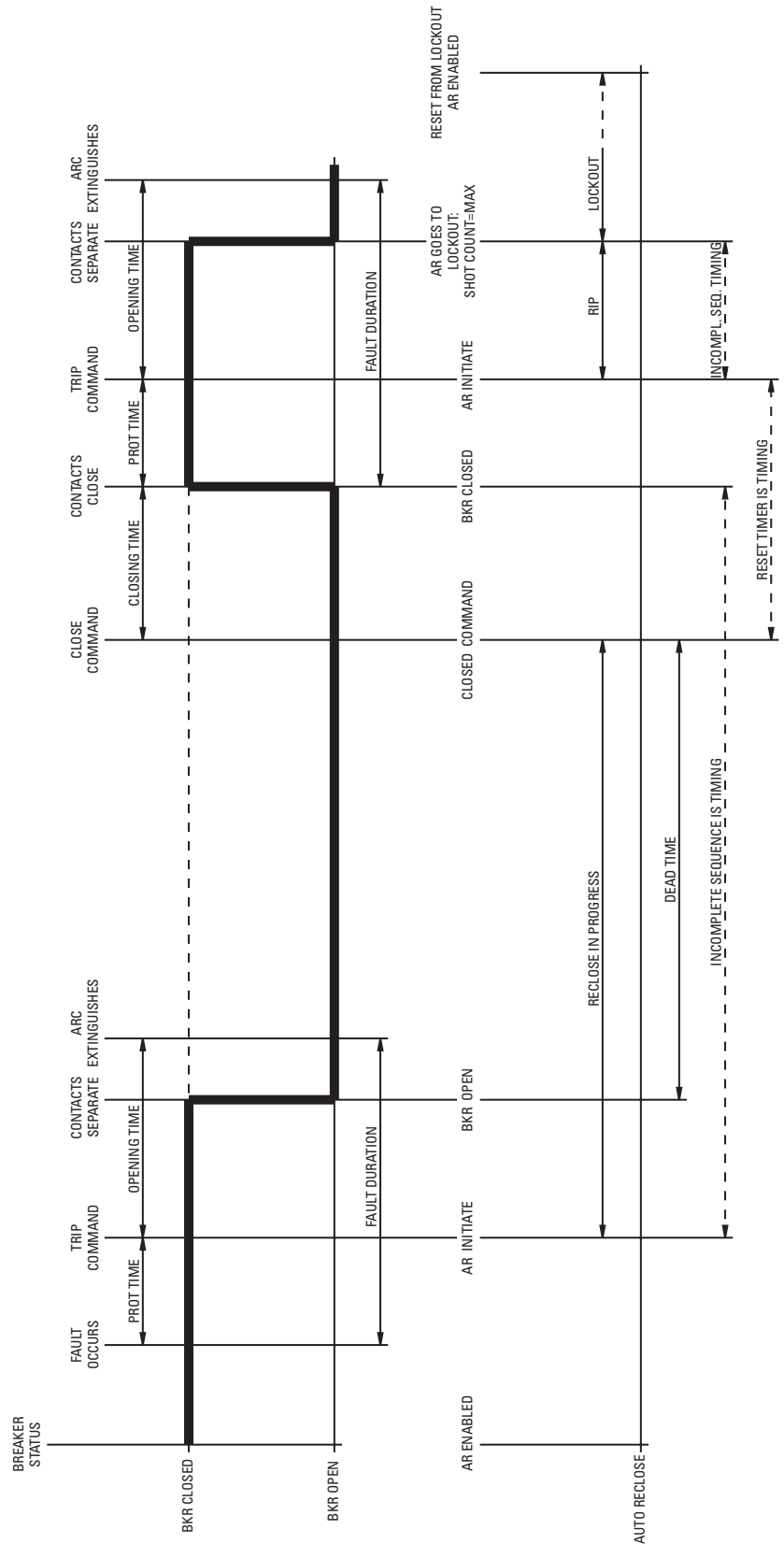
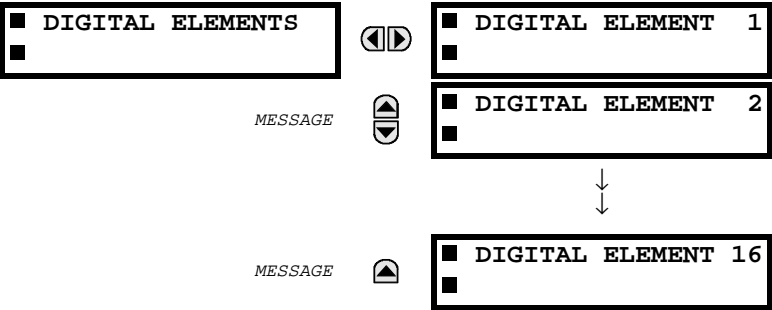


Figure 5-44: SINGLE SHOT AUTORECLOSING SEQUENCE - PERMANENT FAULT

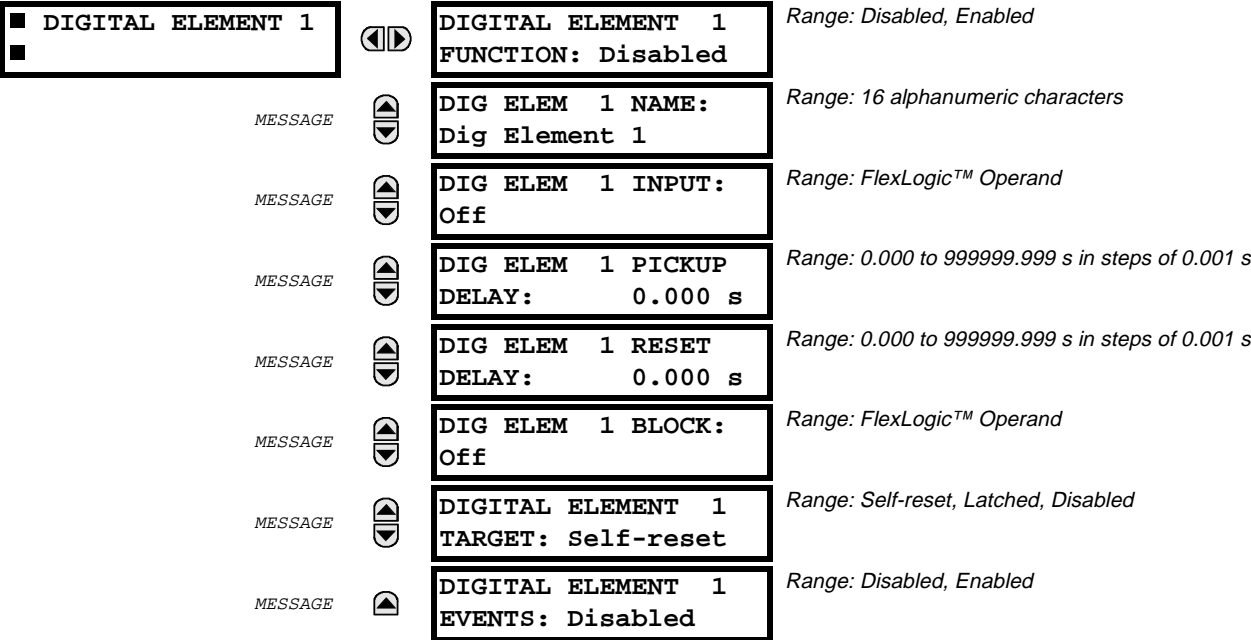
5.6.5 DIGITAL ELEMENTS MENU

PATH: SETTINGS ↴ CONTROL ELEMENTS ⇌ ↴ DIGITAL ELEMENTS



a) DIGITAL ELEMENT 1

PATH: SETTINGS ↴ CONTROL ⇌ ↴ DIGITAL ELEMENTS ⇌ DIGITAL ELEMENT 1(16)



There are 16 identical Digital Elements available, numbered from 1 to 16.

A Digital Element can be used to monitor any FlexLogic™ operand, and to present a target message and/or enable events recording depending on the output operand state. The digital element settings include a ‘name’ which will be referenced in any target message, a blocking input from any selected FlexLogic™ operand, and a timer for pickup and reset delays for the output operand.

DIGITAL ELEMENT 1 INPUT:

This setting is used to select a FlexLogic™ operand to be monitored by the Digital Element.

DIGITAL ELEMENT 1 PICKUP DELAY:

This setting is used to set the time delay to pickup. If a pickup delay is not required, set this function to ‘0’.

DIGITAL ELEMENT 1 RESET DELAY:

This setting is used to set the time delay to reset. If a reset delay is not required, set this function to ‘0’.

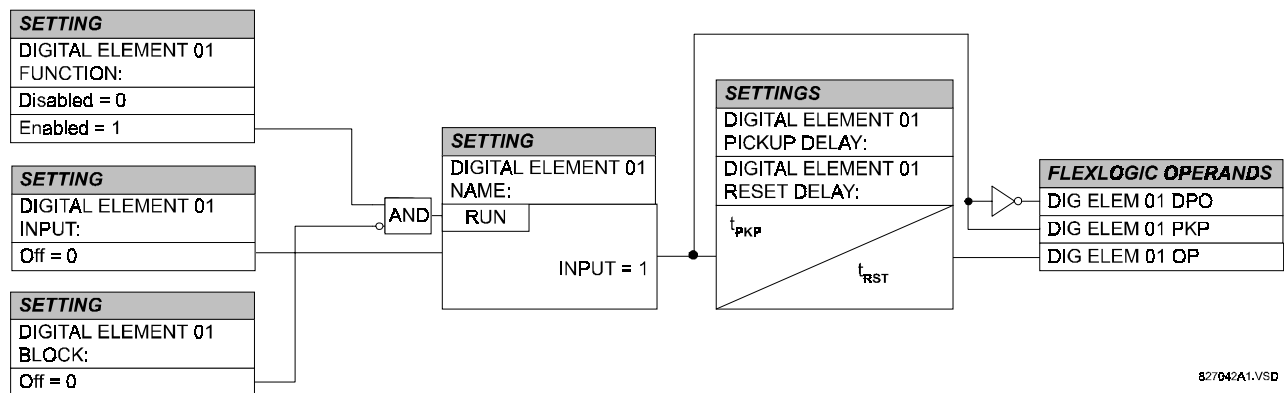


Figure 5-45: DIGITAL ELEMENT SCHEME LOGIC

b) CIRCUIT MONITORING APPLICATIONS

Some versions of the digital input modules include an active Voltage Monitor circuit connected across Form-A contacts. The Voltage Monitor circuit limits the trickle current through the output circuit (see Technical Specifications for Form-A).

As long as the current through the Voltage Monitor is above a threshold (see Technical Specifications for Form-A), the FlexLogic™ operand "Cont Op # VOn" will be set. (# represents the output contact number).

If the output circuit has a high resistance or the DC current is interrupted, the trickle current will drop below the threshold and the FlexLogic™ operand "Cont Op # VOff" will be set.

Consequently, the state of these operands can be used as indicators of the integrity of the circuits in which Form-A contacts are inserted.

BREAKER TRIP CIRCUIT INTEGRITY MONITORING:

In many applications it is desired to monitor the breaker trip circuit integrity so problems can be detected before a trip operation is required. The circuit is considered to be healthy when the Voltage Monitor connected across the trip output contact detects a low level of current, well below the operating current of the breaker trip coil. If the circuit presents a high resistance, the trickle current will fall below the monitor threshold and an alarm would be declared.

Example 1:

In most breaker control circuits, the trip coil is connected in series with a breaker auxiliary contact which is open when the breaker is open (see TRIP CIRCUIT EXAMPLE 1 diagram). To prevent unwanted alarms in this situation, the trip circuit monitoring logic must include the breaker position.

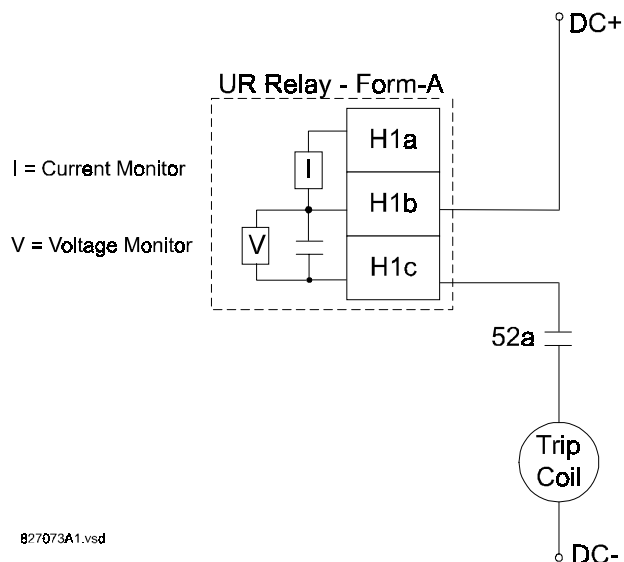


Figure 5-46: TRIP CIRCUIT EXAMPLE 1

Assume the output contact H1 is a trip contact. Using the contact output settings, this output will be given an ID name, e.g. "Cont Op 1".

Assume a 52a breaker auxiliary contact is connected to contact input H7a to monitor breaker status. Using the contact input settings, this input will be given an ID name, e.g. "Cont Ip 1" and will be set "ON" when the breaker is closed. Using Digital Element 1 to monitor the breaker trip circuit, the settings will be:

DIGITAL ELEMENT 1	DIGITAL ELEMENT 1
FUNCTION: Enabled	DIG ELEM 1 NAME:
Bkr Trip Cct Out	DIG ELEM 1 INPUT:
Cont Op 1 VOff	DIG ELEM 1 PICKUP
DELAY: 0.200 s	DIG ELEM 1 RESET
DELAY: 0.100 s	DIG ELEM 1 BLOCK:
Cont Ip 1	DIGITAL ELEMENT 1
TARGET: Self-reset	DIGITAL ELEMENT 1
EVENTS: Enabled	



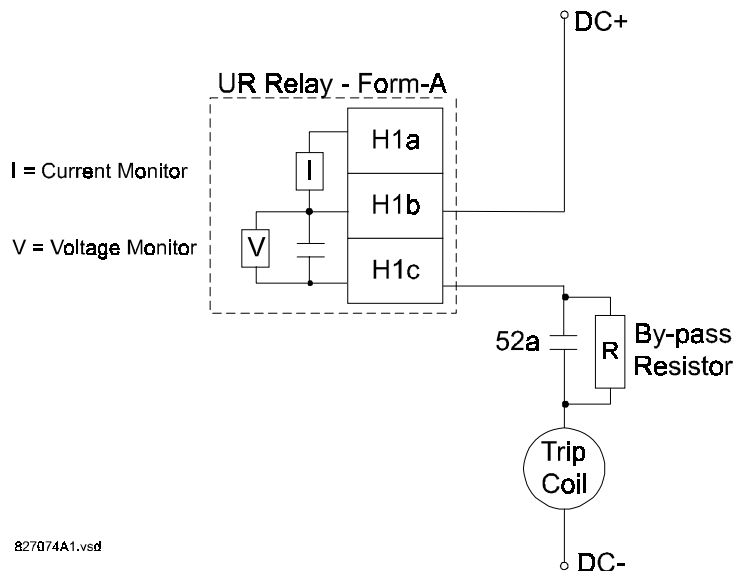
The PICKUP DELAY setting should be greater than the operating time of the breaker to avoid nuisance alarms.

NOTE

Example 2:

If it is required to monitor the trip circuit continuously, independent of the breaker position (open or closed), a method to maintain the monitoring current flow through the trip circuit when the breaker is open must be provided (as shown in Figure: TRIP CIRCUIT - EXAMPLE 2). This can be achieved by connecting a suitable resistor (as listed in the VALUES OF RESISTOR 'R' table) across the auxiliary contact in the trip circuit. In this case, it is not required to supervise the monitoring circuit with the breaker position - the BLOCK setting is selected to Off. In this case, the settings will be:

■ DIGITAL ELEMENT 1	◀▶	DIGITAL ELEMENT 1 FUNCTION: Enabled
MESSAGE	▲▼	DIG ELEM 1 NAME: Bkr Trip Cct Out
MESSAGE	▲▼	DIG ELEM 1 INPUT: Cont Op 1 VOff
MESSAGE	▲▼	DIG ELEM 1 PICKUP DELAY: 0.200 s
MESSAGE	▲▼	DIG ELEM 1 RESET DELAY: 0.100 s
MESSAGE	▲▼	DIG ELEM 1 BLOCK: Off
MESSAGE	▲▼	DIGITAL ELEMENT 1 TARGET: Self-reset
MESSAGE	▲	DIGITAL ELEMENT 1 EVENTS: Enabled

**Table 5-16: VALUES OF RESISTOR 'R'**

POWER SUPPLY (V DC)	RESISTANCE (Ohms)	POWER (Watts)
24	1000	2
30	5000	2
48	10000	2
110	25000	5
125	25000	5
250	50000	5

Figure 5-47: TRIP CIRCUIT - EXAMPLE 2

5.6.6 DIGITAL COUNTERS

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇒ ↓ DIGITAL COUNTERS ⇒ COUNTER 1(8)

<div> <div>COUNTER 1</div> <div></div> </div>	<div> <div>COUNTER 1</div> <div>FUNCTION: Disabled</div> </div>	Range: Disabled, Enabled
<div>MESSAGE</div>	<div> <div>COUNTER 1 NAME:</div> <div>Counter 1</div> </div>	Range: 12 alphanumeric characters
<div>MESSAGE</div>	<div> <div>COUNTER 1 UNITS:</div> <div></div> </div>	Range: 6 alphanumeric characters
<div>MESSAGE</div>	<div> <div>COUNTER 1 PRESET:</div> <div>0</div> </div>	Range: -2,147,483,647 to +2,147,483,647
<div>MESSAGE</div>	<div> <div>COUNTER 1 COMPARE:</div> <div>0</div> </div>	Range: -2,147,483,647 to +2,147,483,647
<div>MESSAGE</div>	<div> <div>COUNTER 1 UP:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
<div>MESSAGE</div>	<div> <div>COUNTER 1 DOWN:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
<div>MESSAGE</div>	<div> <div>COUNTER 1 BLOCK:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
<div>MESSAGE</div>	<div> <div>CNT1 SET TO PRESET:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
<div>MESSAGE</div>	<div> <div>COUNTER 1 RESET:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
<div>MESSAGE</div>	<div> <div>COUNT1 FREEZE/RESET:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand
<div>MESSAGE</div>	<div> <div>COUNT1 FREEZE/COUNT:</div> <div>Off</div> </div>	Range: FlexLogic™ Operand

There are 8 identical digital counters available, numbered from 1 to 8.

A digital counter counts the number of state transitions from Logic 0 to Logic 1. The counter can be used to count operations such as the pickups of an element, the changes of state of an external contact such as a breaker auxiliary switch, or pulses from a watt-hour meter, etc.

COUNTER 1 UNITS:

This setting is used to assign a label to identify the unit of measure pertaining to the digital transitions to be counted. The units label will appear in the corresponding Actual Values status.

COUNTER 1 PRESET:

This setting is used to set the count to a required preset value before counting operations begin, as in the case where a substitute relay is to be installed in place of an in-service relay, or while the counter is running.

COUNTER 1 COMPARE:

This setting is used to set the value to which the accumulated count value is compared. Three FlexLogic™ output operands are provided to indicate if the present value is "more than (HI)", "equal to (EQL)", or "less than (LO)" the set value.

COUNTER 1 UP:

This setting is used to select the FlexLogic™ operand for incrementing the counter. If an enabled UP input is received when the accumulated value is at the limit of +2,147,483,647 counts, the counter will rollover to -2,147,483,647.

COUNTER 1 DOWN:

This setting is used to select the FlexLogic™ operand for decrementing the counter. If an enabled DOWN input is received when the accumulated value is at the limit of -2,147,483,647 counts, the counter will rollover to +2,147,483,647.

COUNTER 1 BLOCK:

This setting is used to select the FlexLogic™ operand for blocking the counting operation.

CNT1 SET TO PRESET:

This setting is used to select the FlexLogic™ operand used to set the count to the preset value. The counter will be set to the preset value in the following situations:

1. When the counter is enabled and the "CNT1 SET TO PRESET" operand has the value 1. (When the counter is enabled and the "CNT1 SET TO PRESET" operand has the value 0, the counter will be set to 0.)
2. When the counter is running and the "CNT1 SET TO PRESET" operand changes the state from 0 to 1. (The change of state of the "CNT1 SET TO PRESET" operand from 1 to 0 while the counter is running has no effect on the count.)
3. When a reset or reset/freeze command is sent to the counter and the "CNT1 SET TO PRESET" operand has the value 1. (When a reset or reset/freeze command is sent to the counter and the "CNT1 SET TO PRESET" operand has the value 0, the counter will be set to 0.)

COUNTER 1 RESET:

This setting is used to select the FlexLogic™ operand for setting the count to either '0' or the preset value depending on the state of the "CNT1 SET TO PRESET" operand.

COUNTER 1 FREEZE/RESET:

This setting is used to select the FlexLogic™ operand for capturing (freezing) the accumulated count value into a separate register with the date and time of the operation, and resetting the count to '0' or the preset value.

COUNTER 1 FREEZE/COUNT:

This setting is used to select the FlexLogic™ operand for capturing (freezing) the accumulated count value into a separate register with the date and time of the operation, and continuing counting.

The present accumulated value and captured frozen value with the associated date/time stamp are available as Actual Values. If control power to the relay is interrupted, the accumulated and frozen values will be saved into non-volatile memory during the powerdown operation.

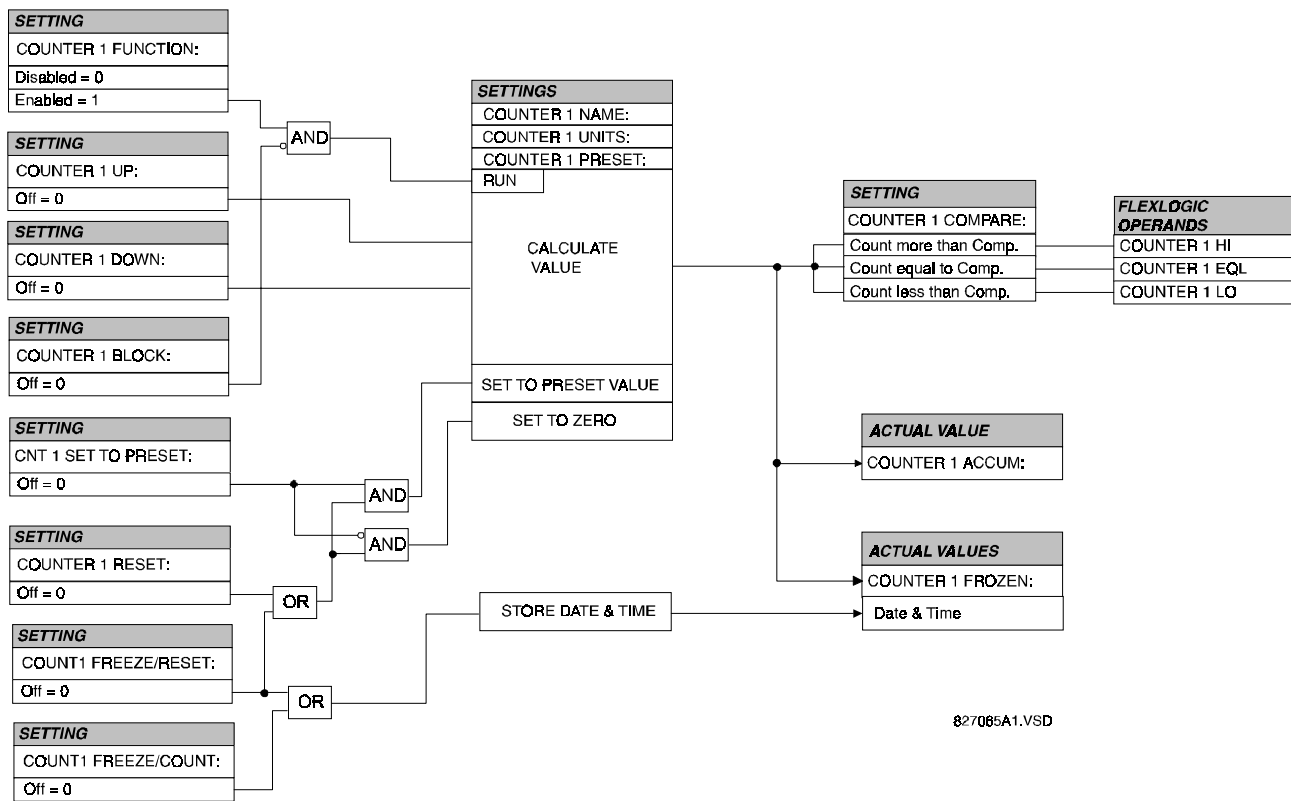


Figure 5-48: DIGITAL COUNTER SCHEME LOGIC

5.6.7 MONITORING ELEMENTS MENU

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ ↓ MONITORING ELEMENTS

■ MONITORING ■ ELEMENTS	◀▶	■ BREAKER 1 ■ ARCING CURRENT
MESSAGE	▲▼	■ BREAKER 2 ■ ARCING CURRENT
MESSAGE	▲▼	■ CONTINUOUS MONITOR ■
MESSAGE	▲▼	■ CT FAILURE ■ DETECTOR
MESSAGE	▲	■ VT FUSE FAILURE ■

a) BREAKER 1(2) ARCING CURRENT

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ ↓ MONITORING ELEMENTS ⇌ ↓ BREAKER 1 ARCING CURRENT

■ BREAKER 1 ■ ARCING CURRENT	◀▶	BKR 1 ARC AMP FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	BKR 1 ARC AMP SOURCE: SRC 1	Range: SRC 1, ..., SRC 6
MESSAGE	▲▼	BKR 1 ARC AMP INIT: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	BKR 1 ARC AMP DELAY: 0.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE	▲▼	BKR 1 ARC AMP LIMIT: 1000 kA ² -cyc	Range: 0 to 50000 in steps of 1 kA ² -cycle
MESSAGE	▲▼	BKR 1 ARC AMP BLOCK: Off	Range: FlexLogic™ Operand
MESSAGE	▲▼	BKR 1 ARC AMP TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲	BKR 1 ARC AMP EVENTS: Disabled	Range: Disabled, Enabled

There are 2 identical Breaker Arcing Current features available for Breakers 1 and 2.

This element calculates an estimate of the per-phase wear on the breaker contacts by measuring and integrating the current squared passing through the breaker contacts as an arc. These per-phase values are added to accumulated totals for each phase and compared to a programmed threshold value. When the threshold is exceeded in any phase, the relay can set an output operand to "1". The accumulated value for each phase can be displayed as an actual value.

The operation of the scheme is shown in the BREAKER ARCING CURRENT SCHEME LOGIC diagram. The same output operand that is selected to operate the output relay used to trip the breaker, indicating a tripping sequence has begun, is used to initiate this feature. A time delay is introduced between initiation and the starting of integration to prevent integration of current flow through the breaker before the contacts have parted. This interval includes the operating time of the output relay, any other auxiliary relays and the breaker mecha-

nism. For maximum measurement accuracy, the interval between change-of-state of the operand (from 0 to 1) and contact separation should be measured for the specific installation. Integration of the measured current continues for 100 milliseconds, which is expected to include the total arcing period.

SETTINGS:

BKR 1 ARC AMP INIT:

Selects the same output operand that is selected to operate the output relay used to trip the breaker.

BKR 1 ARC AMP DELAY:

This setting is used to program the delay interval between the time the tripping sequence is initiated and the time the breaker contacts are expected to part, starting the integration of the measured current.

BKR 1 ARC AMP LIMIT:

Selects the threshold value above which the output operand is set.

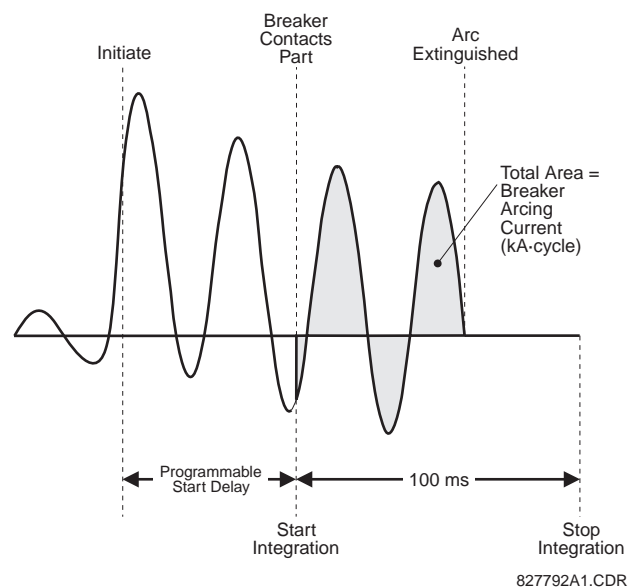
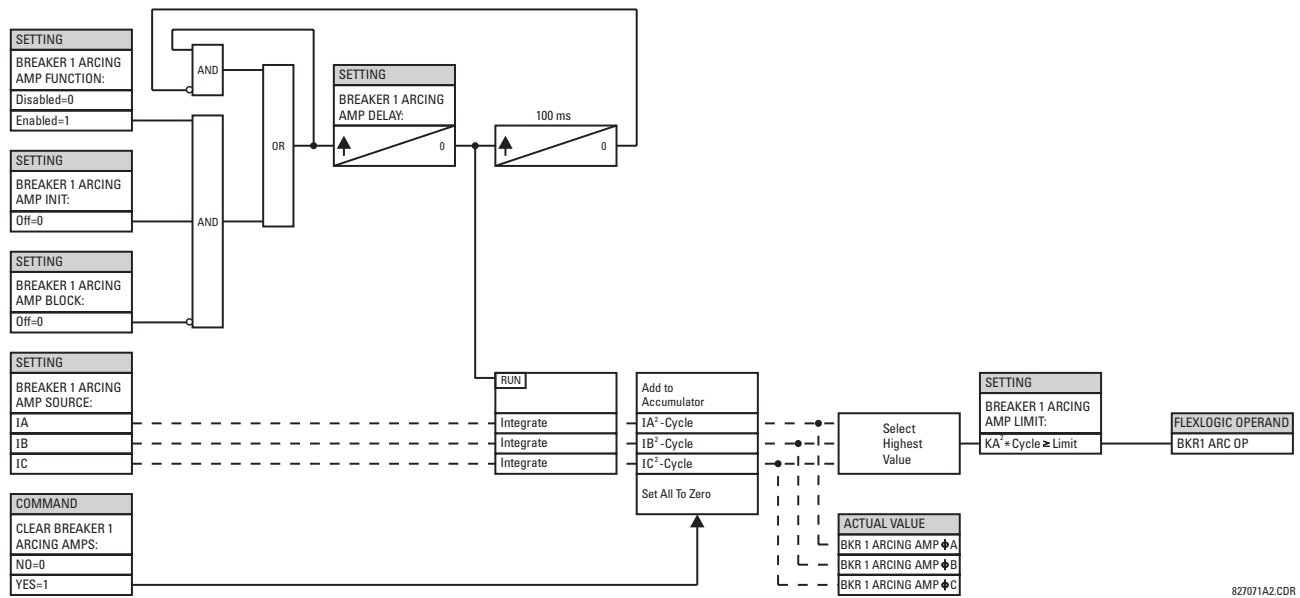


Figure 5-49: ARcing Current Measurement



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Figure 5-50: BREAKER ARCING CURRENT SCHEME LOGIC

b) CONTINUOUS MONITOR

PATH: SETTINGS ⇩ CONTROL ELEMENTS ⇨ ⇩ MONITORING ELEMENTS ⇨ ⇩ CONTINUOUS MONITOR

<div>■ CONTINUOUS MONITOR</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div>	CONT MONITOR FUNCTION: Disabled	Range: Disabled, Enabled
	CONT MONITOR I-OP: Off	Range: FlexLogic™ Operand Note: any Current Element(s) OP
	CONT MONITOR I-SUPV: Off	Range: FlexLogic™ Operand Note: to supervise current logic, use 50DD OP
	CONT MONITOR V-OP: Off	Range: FlexLogic™ Operand Note: any Voltage Element(s) OP
	CONT MONITOR V-SUPV: Off	Range: FlexLogic™ Operand To supervise voltage logic, use VT FUSE FAIL OP
	CONT MONITOR TARGET: Self-reset	Range: Self-reset, Latched, Disabled
	CONT MONITOR EVENTS: Disabled	Range: Disabled, Enabled

The Continuous Monitor logic is intended to detect the operation of any tripping element that has operated under normal load conditions; that is, when the DD disturbance detector has not operated. Because all tripping is supervised by the DD function, no trip will be issued under these conditions. This could occur when an element is incorrectly set so that it may misoperate under load. The Continuous Monitor can detect this state and issue an alarm and/or block the tripping of the relay.

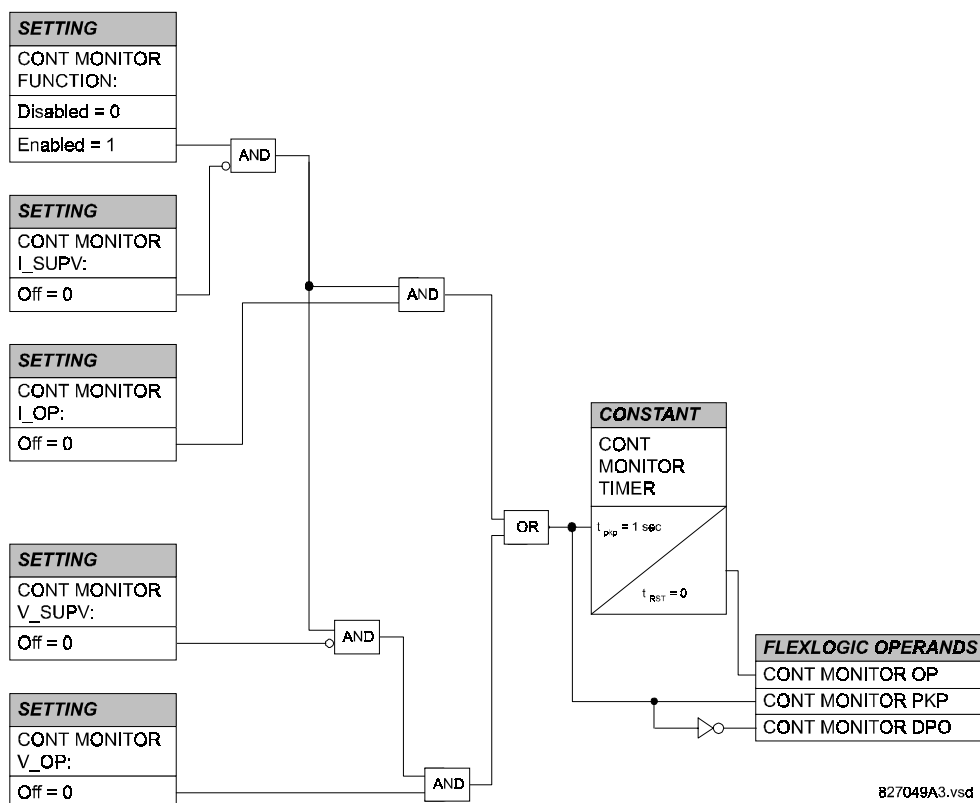


Figure 5-51: CONTINUOUS MONITOR SCHEME LOGIC

c) CT FAILURE DETECTOR

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ ↓ MONITORING ELEMENTS ⇌ ↓ CT FAILURE DETECTOR

<input checked="" type="checkbox"/> CT FAILURE <input checked="" type="checkbox"/> DETECTOR	<div>◀▶</div>	CT FAIL FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲▼	CT FAIL BLOCK: Off	Range: FlexLogic™ Operand,
MESSAGE	▲▼	CT FAIL 3I0 INPUT 1: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	CT FAIL 3I0 INPUT 1 PKP: 0.2 pu	Range: 0.0 to 2.0 pu in steps of 0.1
MESSAGE	▲▼	CT FAIL 3I0 INPUT 2: SRC 2	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	CT FAIL 3I0 INPUT 2 PKP: 0.2 pu	Range: 0.0 to 2.0 pu in steps of 0.1
MESSAGE	▲▼	CT FAIL 3V0 INPUT: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲▼	CT FAIL 3V0 INPUT PKP: 0.2 pu	Range: 0.0 to 2.0 pu in steps of 0.1
MESSAGE	▲▼	CT FAIL PICKUP DELAY: 1.000 s	Range: 0.000 to 65.535 s in steps of 0.001
MESSAGE	▲▼	CT FAIL TARGET: Self-reset	Range: Self-reset, Latched, Disabled
MESSAGE	▲	CT FAIL EVENTS: Disabled	Range: Disabled, Enabled

The CT FAIL logic is designed to detect problems with the system current transformers used to supply current to the relay. This logic detects the presence of a zero sequence current at the supervised source of current without a simultaneous zero sequence current at another source, zero sequence voltage or some protection element condition.

CT FAIL logic (see figure below) is based on the presence of the zero sequence current in the supervised CT source and absence of one of three or all three conditions as follows:

- zero sequence current at different source current (may be different set of CTs or different CT core of the same CT)
- zero sequence voltage at the assigned source
- appropriate protection element or remote signal

SETTINGS:**CT FAIL FUNCTION:**

This setting is used to Enable/Disable operation of the element.

CT FAIL BLOCK:

This setting is used to select a FlexLogic™ Operand that blocks operation of the element during some conditions (i.e. open pole in process of the single pole tripping-reclosing) when CT Fail should be blocked. Remote signals representing operation of some remote current protection elements via communication channel or local ones can be chosen as well.

CT FAIL 3I0 INPUT 1:

This setting is used to select the source for the current for input 1. Most important protection element of the relay should be assigned to the same source.

CT FAIL 3I0 INPUT 1 PICKUP:

This setting is used to select the pickup value for 3I_0 for the input 1 (main supervised CT source) of the relay.

CT FAIL 3I0 INPUT 2:

This setting is used to select the source for the current for input 2. Input 2 should use different set of CTs or different CT core of the same CT. Against absence at input 2 CT source (if exists), 3I_0 current logic is built.

CT FAIL 3I0 INPUT 2 PICKUP:

This setting is used to select the pickup value for 3I_0 for the input 2 (different CT input) of the relay.

CT FAIL 3V0 INPUT:

This setting is used to select the source for the voltage.

CT FAIL 3V0 INPUT PICKUP:

This setting is used to select the pickup value for 3V_0 source.

CT FAIL PICKUP DELAY:

This setting is used to select the pickup delay of the element.

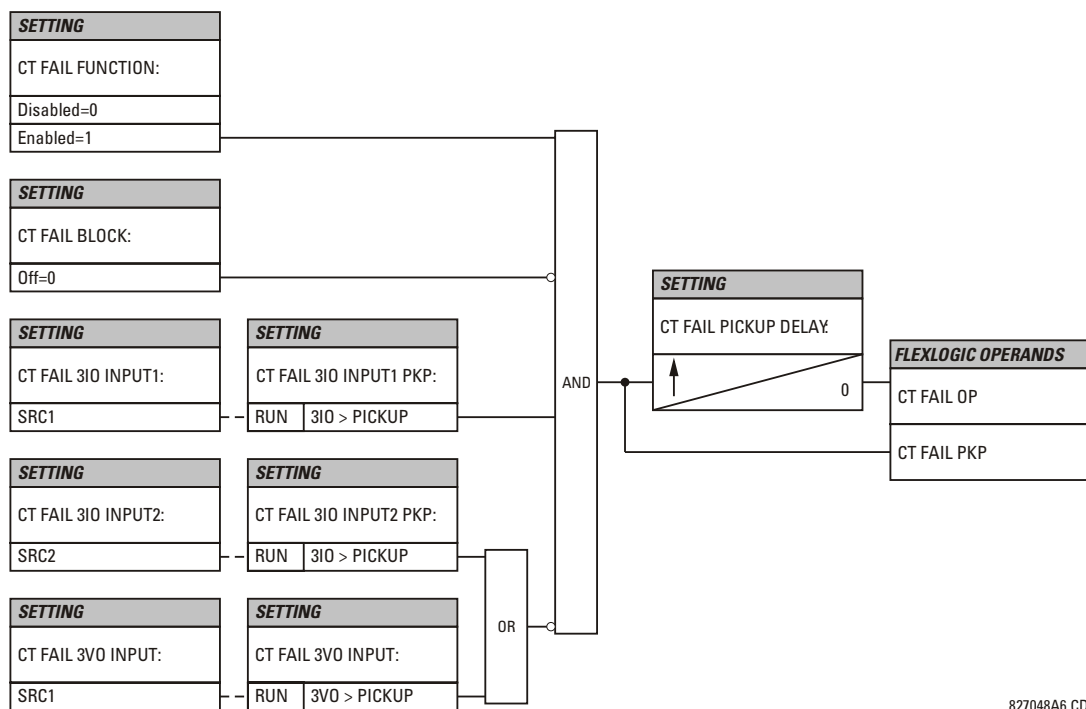
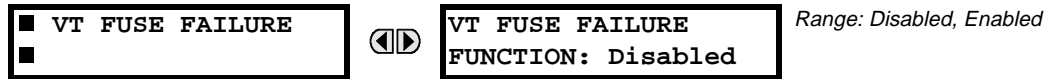


Figure 5-52: CT FAILURE DETECTOR SCHEME LOGIC

d) VT FUSE FAILURE

PATH: SETTINGS ⇩ CONTROL ELEMENTS ⇨ ⇩ MONITORING ELEMENTS ⇨ ⇩ VT FUSE FAILURE



Every signal source includes a fuse failure scheme.

The VT fuse failure detector can be used to raise an alarm and/or block elements that may operate incorrectly for a full or partial loss of AC potential caused by one or more blown fuses. Some elements that might be blocked (via the BLOCK input) are distance, voltage restrained overcurrent, and directional current.

There are two classes of fuse failure that may occur: (A) loss of one or two phases, and (B) loss of all three phases. A different means of detection is required for each class. An indication of class A failures is a significant level of negative sequence voltage, whereas an indication of class B failures is when positive sequence current is present and there is an insignificant amount of positive sequence voltage. These noted indications of fuse failure could also be present when faults are present on the system, so a means of detecting faults and inhibiting fuse failure declarations during these events is provided. Once the fuse failure condition is declared, it will be sealed-in until the cause that generated it disappears.

An additional condition is introduced to inhibit a fuse failure declaration when the monitored circuit is de-energized; positive sequence voltage and current are both below threshold levels.

The common FUNCTION setting will Enable/Disable the fuse failure feature for all 6 sources.

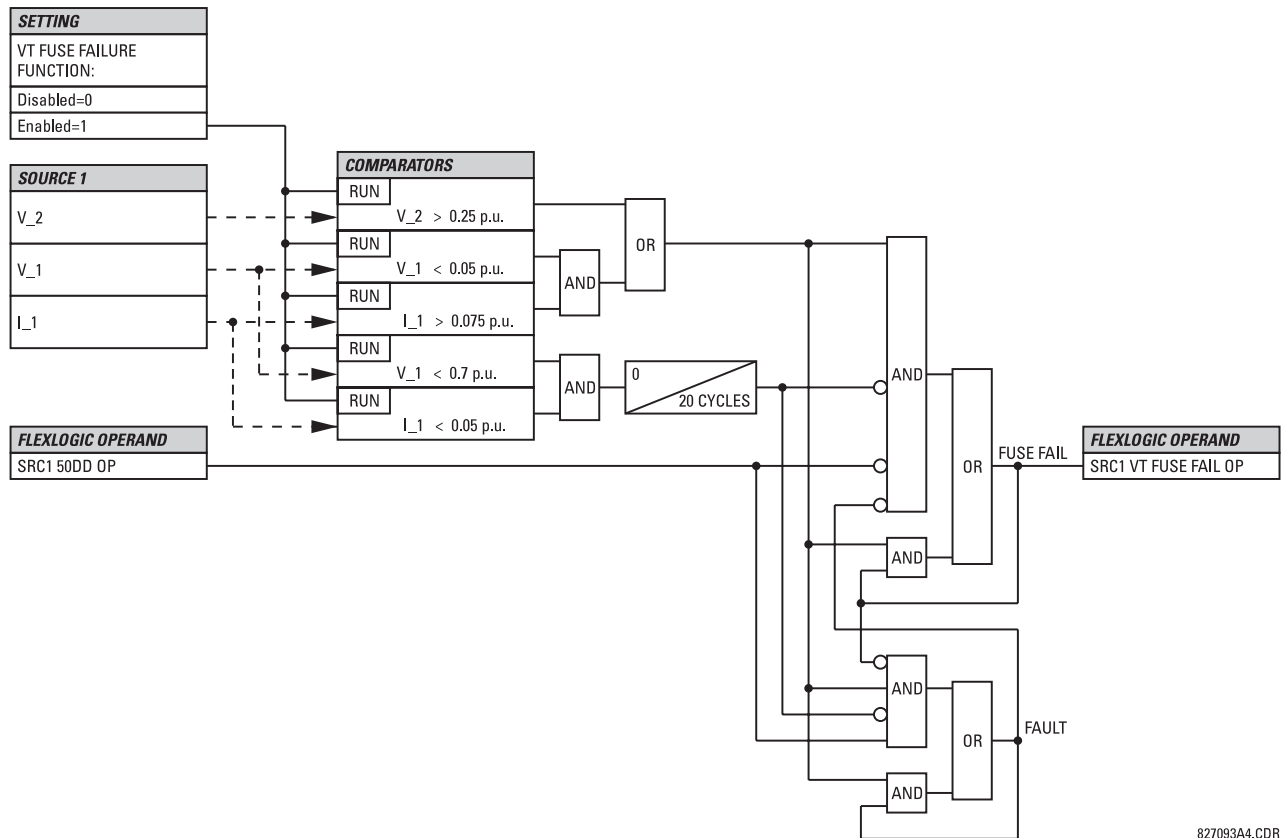


Figure 5-53: VT FUSE FAIL SCHEME LOGIC

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5.6.8 PILOT SCHEMES

a) PERMISSIVE OVER-REACHING TRANSFER TRIP (POTT)

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ PILOT SCHEMES ⇌ POTT SCHEME

<div> <div>■ POTT SCHEME</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> <div>MESSAGE</div> </div>	<div> <div>◀▶</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲▼</div> <div>▲</div> </div>	<div>POTT SCHEME</div> <div>FUNCTION: Disabled</div>	Range: Disabled, Enabled
		<div>POTT PERMISSIVE</div> <div>ECHO: Disabled</div>	Range: Disabled, Enabled
		<div>POTT RX PICKUP</div> <div>DELAY: 0.000 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>TRANS BLOCK PICKUP</div> <div>DELAY: 0.020 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>TRANS BLOCK RESET</div> <div>DELAY: 0.090 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>ECHO DURATION:</div> <div>0.100 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>ECHO LOCKOUT:</div> <div>0.250 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>LINE END OPEN PICKUP</div> <div>DELAY: 0.050 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>POTT SEAL-IN</div> <div>DELAY: 0.400 s</div>	Range: 0.000 to 65.535 sec. in steps of 0.001
		<div>GND DIR O/C FWD:</div> <div>Off</div>	Range: FlexLogic™ Operand
		<div>POTT RX:</div> <div>Off</div>	Range: FlexLogic™ Operand

This scheme is intended for two-terminal line applications only.

This scheme uses an over-reaching zone 2 distance element to essentially compare the direction to a fault at both the ends of the line.

Ground directional overcurrent functions available in the relay can be used in conjunction with the zone 2 distance element to key the scheme and initiate its operation. This provides increased coverage for high-resistance faults.

For proper operation of the scheme the zone 2 phase and ground distance elements must be enabled, configured and set per rules of distance relaying. The LINE PICKUP element should be enabled, configured and set properly to detect line-end-open/weak-infeed conditions.

If used by this scheme, the selected ground directional overcurrent function (-s) must be enabled, configured and set accordingly.

SETTINGS**POTT PERMISSIVE ECHO:**

If set to "Enabled" this setting will result in sending a permissive echo signal to the remote end. The permissive signal is echoed back upon receiving a reliable POTT RX signal from the remote end while the line-end-open condition is identified by the LINE PICKUP logic. The Permissive Echo is programmed as a one-shot logic. The

echo is sent only once and then the echo logic locks out for a settable period of time (ECHO LOCKOUT setting). The duration of the echo pulse does not depend on the duration or shape of the received POTT RX signal but is settable as ECHO DURATION.

POTT RX PICKUP DELAY:

This setting enables the relay to cope with spurious receive signals. The delay should be set longer than the longest spurious TX signal that can occur simultaneously with the zone 2 pickup. The selected delay will increase the response time of the scheme.

TRANS BLOCK PICKUP DELAY:

This setting defines a transient blocking mechanism embedded in the POTT scheme for coping with the exposure of a ground directional overcurrent function (if used) to current reversal conditions. The transient blocking mechanism applies to the ground overcurrent path only as the reach settings for the zone 2 distance functions is not expected to be long for two-terminal applications, and the security of the distance functions is not endangered by the current reversal conditions.

Upon receiving the POTT RX signal, the transient blocking mechanism allows the RX signal to be passed and aligned with the GND DIR O/C FWD indication only for a period of time defined as TRANS BLOCK PICKUP DELAY. After that the ground directional overcurrent path will be virtually disabled for a period of time specified as TRANS BLOCK RESET DELAY.

The TRANS BLOCK PICKUP DELAY should be long enough to give the selected ground directional overcurrent function time to operate, but not longer than the fastest possible operation time of the protection system that can create current reversal conditions within the reach of the selected ground directional overcurrent function.

This setting should take into account the POTT RX PICKUP DELAY. The POTT RX signal is shaped for aligning with the ground directional indication as follows: The original RX signal is delayed by the POTT RX PICKUP DELAY, then terminated at TRANS BLOCK PICKUP DELAY after the pickup of the original POTT TX signal, and eventually, locked-out for TRANS BLOCK RESET DELAY.

TRANS BLOCK RESET DELAY:

This setting defines a transient blocking mechanism embedded in the POTT scheme for coping with the exposure of a ground directional overcurrent function (if used) to current reversal conditions (see also the TRANS BLOCK PICKUP DELAY).

This delay should be selected long enough to cope with transient conditions including not only current reversals but also spurious negative- and zero-sequence currents occurring during breaker operations. The breaker failure time of the surrounding protection systems within the reach of the ground directional function used by the POTT scheme may be considered to make sure that the ground directional function is not jeopardized during delayed breaker operations.

ECHO DURATION:

This setting defines the guaranteed and exact duration of the echo pulse. The duration does not depend on the duration and shape of the received POTT RX signal. This setting enables the relay to avoid a permanent lock-up of the transmit/receive loop.

ECHO LOCKOUT:

This setting defines the lockout period for the echo logic after sending the echo pulse.

LINE END OPEN PICKUP DELAY:

This setting defines the pickup setting for validation of the line end open conditions as detected by the LINE PICKUP logic through the LINE PICKUP LEO PKP FlexLogic™ operand.

The validated line end open condition is a requirement for the POTT scheme to return a received echo signal (if the ECHO feature is enabled).

The value of this setting should take into account the principle of operation and settings of the LINE PICKUP element.

POTT SEAL-IN DELAY:

The output FlexLogic™ operand (POTT OP) is produced according to the POTT scheme logic. A seal-in time delay is applied to this operand for coping with noisy communication channels. The POTT SEAL-IN DELAY defines a minimum guaranteed duration of the POTT OP pulse.

GND DIR O/C FWD:

This setting defines the FlexLogic™ operand (if any) of a protection element that is used in addition to the zone 2 for identifying faults on the protected line, and thus, for keying the communication channel and initiating operation of the scheme.

Good directional integrity is the key requirement for an over-reaching forward-looking protection element used as GND DIR O/C FWD.

Even though any FlexLogic™ operand could be used as GND DIR O/C FWD allowing the user to combine responses of various protection elements, or to apply extra conditions through FlexLogic™ equations, this extra signal is primarily meant to be the output operand from either the Negative-Sequence Directional IOC or Neutral Directional IOC. Both of these elements have separate forward (FWD) and reverse (REV) output operands. The forward indication should be used (NEG SEQ DIR OC1 FWD or NEUTRAL DIR OC1 FWD).

POTT RX:

This setting enables the user to select the FlexLogic™ operand that represents the receive signal (RX) for the scheme. Typically an input contact interfacing with a signaling system is used. Other choices include Remote Inputs and FlexLogic™ equations.

The POTT transmit signal (TX) should be appropriately interfaced with the signaling system by assigning the output FlexLogic™ operand (POTT TX) to an output contact. The Remote Output mechanism is another choice.

The output operand from the scheme (POTT OP) must be configured to interface with other relay functions, output contacts in particular, in order to make the scheme fully operational. Typically, the output operand should be programmed to initiate a trip, breaker fail, and autoreclose, and drive a user-programmable LED as per user application.

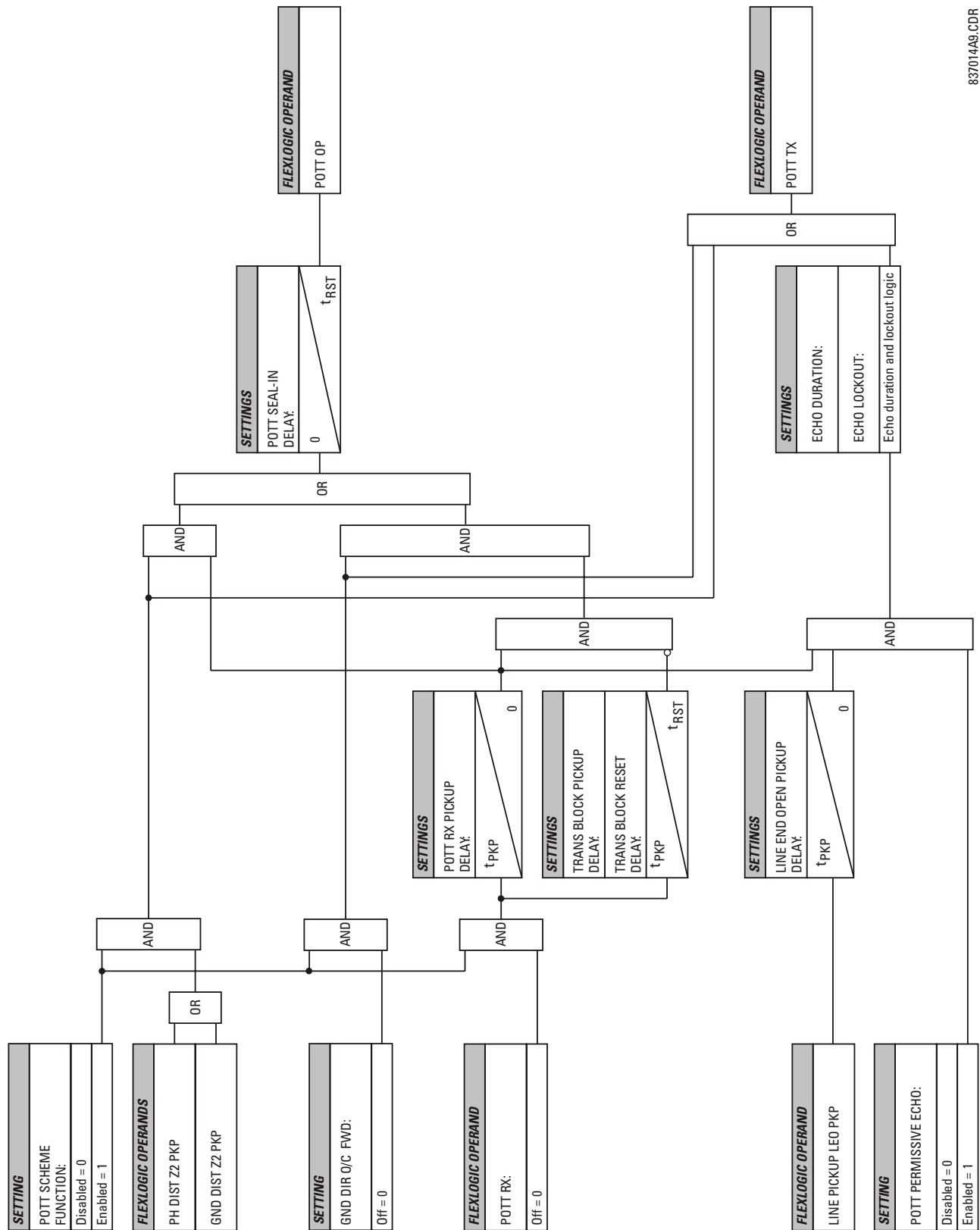


Figure 5-54: POTT SCHEME LOGIC

5.6.9 PHASE COMPARISON ELEMENTS MENU




PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ ↓ PHASE COMPARISON ELEMENTS

■ PHASE COMPARISON ■ ELEMENTS	◀▶	■ 87PC SCHEME ■
MESSAGE	▲	■ OPEN BREAKER ■ ECHO

a) 87PC SCHEME

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ ↓ PHASE COMPARISON ELEMENTS ⇌ 87PC SCHEME

■ 87PC SCHEME ■	◀▶	87PC FUNCTION: Disabled	Range: Disabled, Enabled
MESSAGE	▲	87PC SCHEME SELECT: 2TL-PT-SPC-2FC	Range: 2TL-PT/BL-SPC-2FC, 2TL-PT/BL-DPC-3FC, 2TL-BL-DPC-2FC, etc.
MESSAGE	▲	87PC BLOCK: Off	Range: Flexlogic™ Operand
MESSAGE	▲	87PC SIGNAL SOURCE: SRC 1	Range: SRC 1,..., SRC 6
MESSAGE	▲	87PC SIGNAL: Mixed I ₂ -K*I ₁	Range: Mixed I ₂ -K*I ₁ , 3I ₀
MESSAGE	▲	87PC MIXED SIGNAL K: 0.20	Range: 0.00 to 0.25 in steps of 0.01
MESSAGE	▲	87PC FDL PICKUP: 0.50 pu	Range: 0.01 to 15.00 pu in steps of 0.01
MESSAGE	▲	87PC FDH PICKUP: 0.75 pu	Range: 0.01 to 15.00 pu in steps of 0.01
MESSAGE	▲	87PC FD INPUT: Off	Range: FlexLogic™ Operand
MESSAGE	▲	87PC SYMMETRY CH1: 0.0 ms	Range: -20.0 to 20.0 ms in steps of 0.1
MESSAGE	▲	87PC SYMMETRY CH2: 0.0 ms	Range: -20.0 to 20.0 ms in steps of 0.1
MESSAGE	▲	87PC PHASE DELAY CH1: 0.000 ms	Range: 0.0 to 65.535 ms in steps of 0.001
MESSAGE	▲	87PC PHASE DELAY CH2: 0.000 ms	Range: 0.0 to 65.535 ms in steps of 0.001
MESSAGE	▲	87PC STABILITY ANGLE: 75 deg	Range: 40 to 140° in steps of 10°
MESSAGE	▲	87PC TRANS BLOCK PICKUP: 0.030 s	Range: 0 to 65.535 sec. in steps of 0.001
MESSAGE	▲	87PC TRANS BLOCK RESET: 0.030 s	Range: 0 to 65.535 sec. in steps of 0.001

MESSAGE		87PC CHNL LOSS TRIP WINDOW: 0.000 S	Range: 0 to 65.535 sec. in steps of 0.001
MESSAGE		87PC TARGET: Self-Reset	Range: Self-Reset, Latched, Disabled
MESSAGE		87PC EVENTS: Disabled	Range: Disabled, Enabled2

The phase comparison tripping scheme menu provides the main setup for the phase comparison relay.

SETTINGS

87PC SCHEME SELECT:

Selects the Phase Comparison Element scheme logic as follows:

- 2TL-PT-SPC-2FC: 2 terminal line, permissive tripping, single phase comparison, 2 frequency channel
- 2TL-BL-SPC-2FC: 2 terminal line, blocking, single phase comparison, 2 frequency channel
- 2TL-PT-DPC-3FC: 2 terminal line, permissive tripping, dual phase comparison, 3 frequency channel
- 2TL-BL-DPC-3FC: 2 terminal line, blocking, dual phase comparison, 3 frequency channel
- 2TL-BL-DPC-2FC: 2 terminal line, blocking, dual phase comparison, 2 frequency channel (FSK PLC only)
- 3TL-PT-SPC-3FC: 3 terminal line, permissive tripping, single phase comparison, 3 frequency channel
- 3TL-BL-SPC-3FC: 3 terminal line, blocking, single phase comparison, 3 frequency channel



NOTE

1. A two frequency channel (2FC) can be either On-Off Carrier or a High-Low FSK system
2. More information on phase comparison schemes can be found in the THEORY OF OPERATION chapter.
3. In Blocking schemes, the Open Breaker Echo element must be disabled.

87PC BLOCK:

Selects a Flexlogic™ Operand that blocks operation of the phase comparison scheme (for example, an operand that indicates operation of a communications channel failure detector).

87PC SIGNAL:

A mixed I₂-K*I₁ signal or a single 3I₀ signal can be chosen as the operating signal for the FDH and FDL detectors and squaring amplifier. The constant K in the mixed excitation signal is adjustable.

87PC MIXED SIGNAL K:

Selects the K factor used in the mixed excitation operating signal I₂-K*I₁.

87PC FDL PICKUP:

This setting is used to select the FDL pickup value. FDL is used as a start-keying element.

87PC FDH PICKUP:

This setting is used to select FDH pickup value. FDH is used as a trip-arming element.

87PC FD INPUT:

Selects a FlexLogic™ Operand that indicates the operation of an external Fault Detector (e.g. an impedance element) that forces the coincidence detector of the phase comparison element to start during some power system conditions if FDH cannot pick up.

87PC SYMMETRY CH1(2):

This setting is used to enter the symmetry adjustment to make “positive” and “negative” halves of the power cycle of the received signal from the remote terminal via communication channel noise symmetrical. Refer to the test procedures for more detailed information.

87PC PHASE DELAY CH1(2):

This setting delays the local signal until the remote signal is received. Refer to the test procedures for more detailed information.

87PC STABILITY ANGLE:

This setting is used to select the stability angle for trip security.

87PC TRANS BLOCK PICKUP:

This setting increases sensitivity during and after the clearing of an external fault and prevents false tripping during transient current intervals.

87PC TRANS BLOCK RESET:

Resets transient blocking and allows tripping

87PC CHNL LOSS TRIP WINDOW:

This setting is applicable to the 2TL-BL-DPC-2FC scheme only. If a loss of carrier is detected in the course of the fault, a trip is allowed for the time defined by this setting (default value is 0). The trip is blocked after the expiration of this time window.

Refer to the APPLICATION OF SETTINGS chapter for the calculation of settings for the 87PC element.

SCHEME LOGIC:

The following three figures illustrate logic diagrams for all available schemes. The choice of the scheme must be made by protection and control engineer according to the communication equipment employed, requirements of trip speed, and reliability. These schemes are considered in THEORY OF OPERATION chapter.

In single phase comparison schemes (see SINGLE PHASE COMPARISON LOGIC diagram) coincidence of the local and remote squares is detected during one half the power cycle only, positive or negative. As a result, some delay in operation can be expected under “unfavorable” fault inception.

This weakness of the single phase comparison schemes is eliminated in dual phase comparison schemes (see DUAL PHASE COMPARISON LOGIC diagram) but cost of the communication link is higher.

Some advantages of dual phase comparison and two frequency FSK PLC are incorporated in the scheme shown in the DUAL PHASE COMPARISON LOGIC WITH 2 FREQUENCY FSK PLC logic diagram. Since there is no third or guard frequency available, the PLC low frequency signal serves as the guard frequency for some logic implemented in this scheme. Tripping is permitted if the FDL relay sees the change in received signal from low to high (indicated that communication link is healthy and remote relay detected the fault) within 20 ms after fault is detected. If the PLC low frequency has not been received prior the fault detection, the trip output is blocked as well. Another enhancement of this scheme is the trip window defined by the 87PC CHNL LOSS TRIP WINDOW setting. This logic allows the relay to make a trip decision within this time if the PLC signal was lost in the course of the fault.

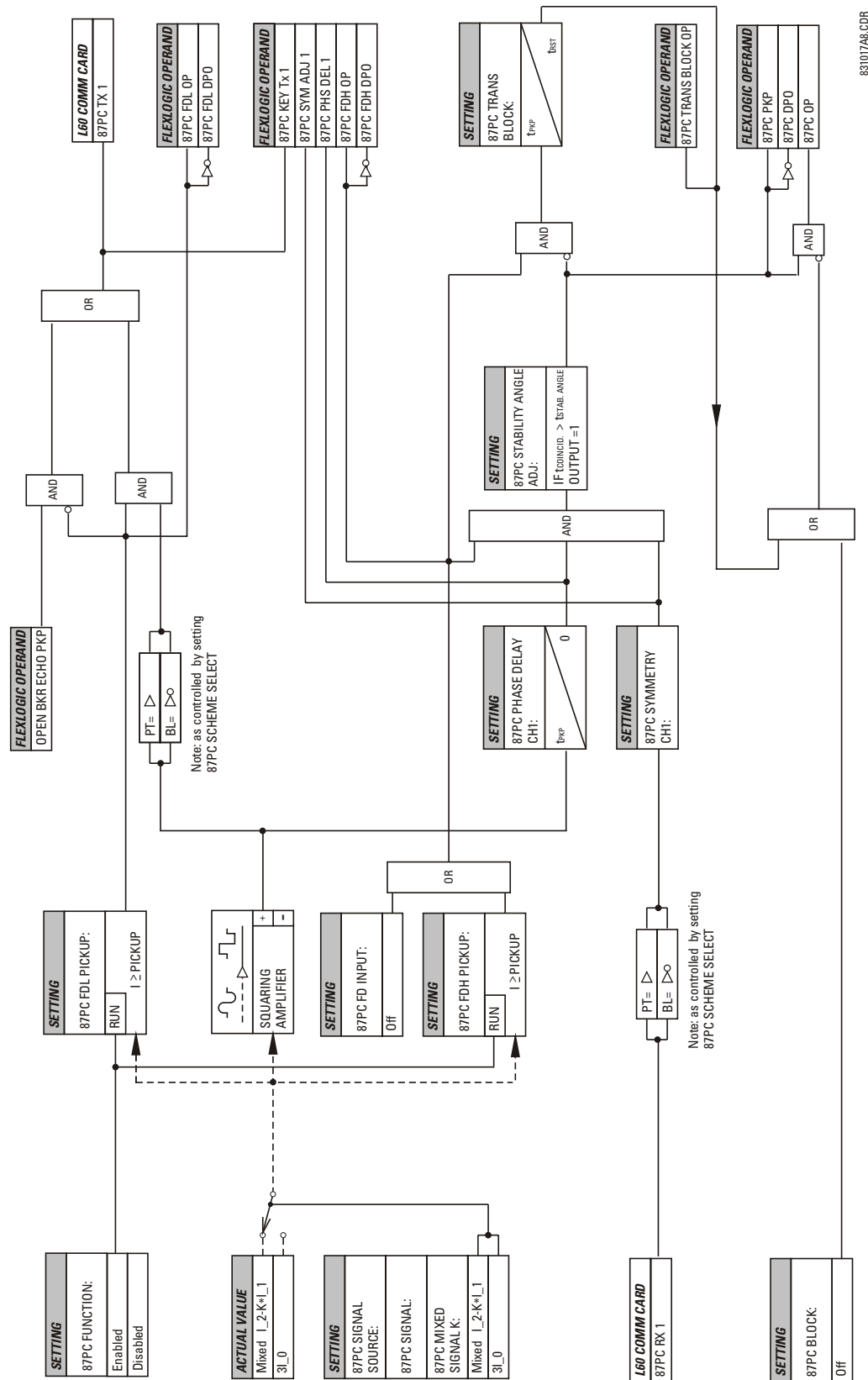
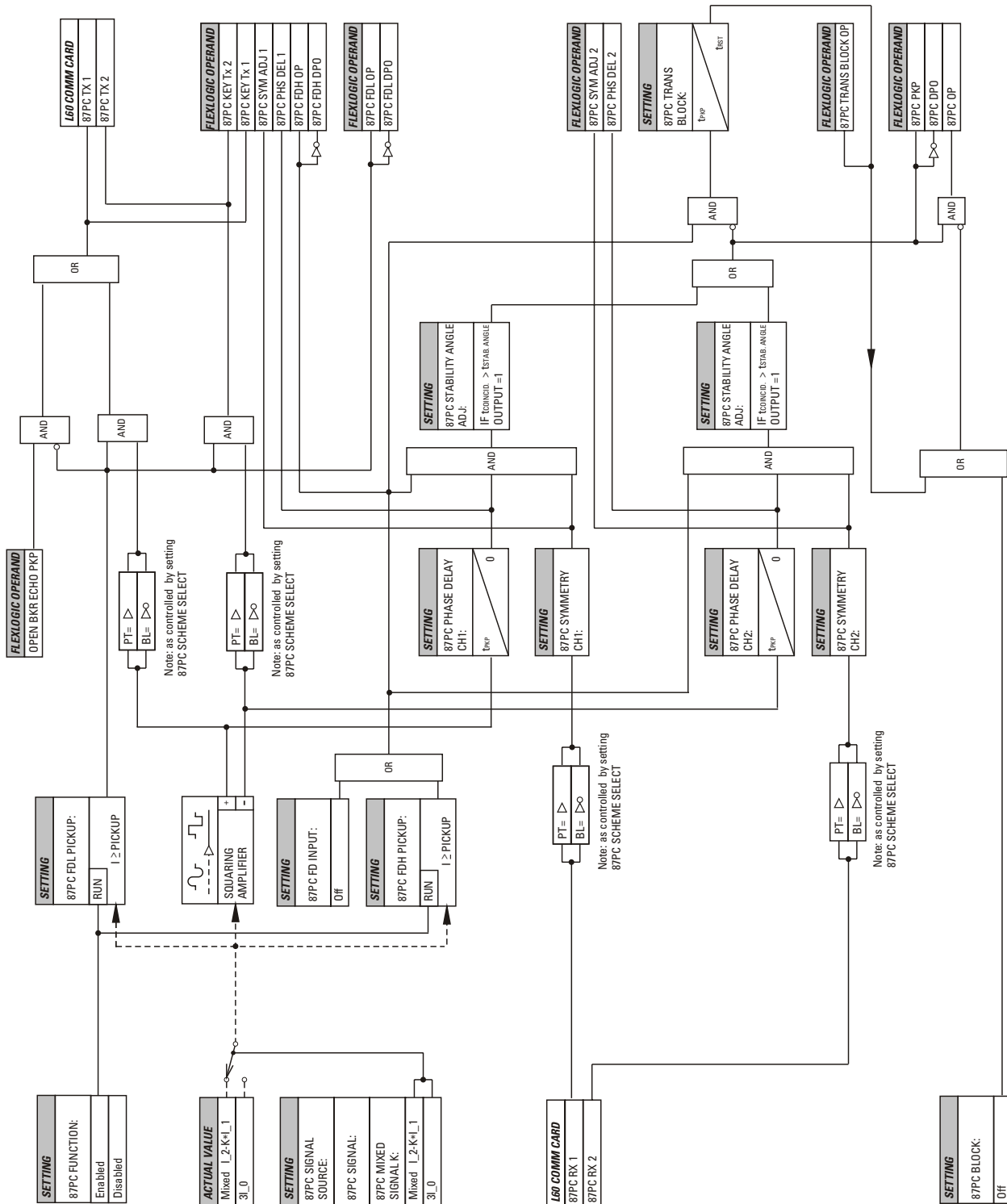
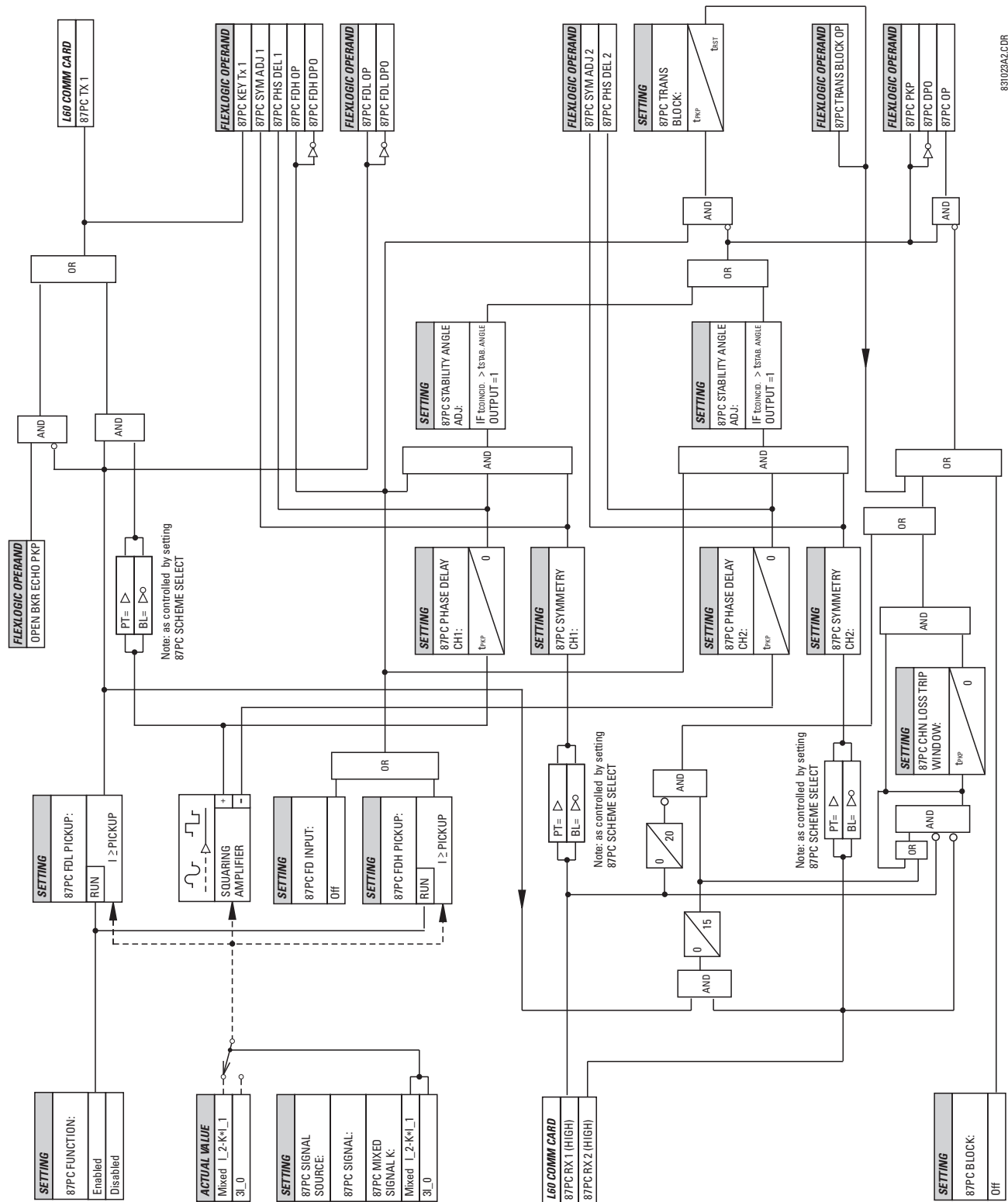


Figure 5-55: SINGLE PHASE COMPARISON LOGIC (schemes 2TL-PT-SPC-2FC & 2TL-BL-SPC-2FC)



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b) OPEN BREAKER ECHO

PATH: SETTINGS ↓ CONTROL ELEMENTS ⇌ PHASE COMPARISON ELEMENTS ⇌ OPEN BREAKER ECHO

<div> <div>■ OPEN BREAKER</div> <div>■ ECHO</div> </div>		◀▶	OPEN BREAKER KEYING: Disabled	Range: Disabled, Enabled
	MESSAGE	▲▼	BRK 1 AUX CONTACT: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	BRK 1 CONT SUPV: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	BRK 2 AUX CONTACT: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	BRK 2 CONT SUPV: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	OPEN BREAKER KEYING PKP DELAY: 0.000 s	Range: 0.000 to 50.000 s in steps of 0.001
	MESSAGE	▲▼	OPEN BREAKER KEYING RST DELAY: 0.000 s	Range: 0.000 to 50.000 s in steps of 0.001
	MESSAGE	▲▼	WEAK-INFEED KEYING: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	WEAK-INFEED SUPV: Off	Range: FlexLogic™ Operand
	MESSAGE	▲▼	WEAK-INFEED PICKUP DELAY: 0.000 s	Range: 0.000 to 50.000 s in steps of 0.001
	MESSAGE	▲	WEAK-INFEED RESET DELAY: 0.035 s	Range: 0.000 to 50.000 s in steps of 0.001

As operation of the Permissive Tripping mode of phase comparison protection and tripping of the line is fundamentally dependent on transmitting the signal to the remote end of the line, some cases of system operating conditions require attention:

1. If a line is open at one end, the phase comparison element is unable to detect an internal fault and give trip permission to the remote terminal relay.
2. A weak-infeed or no fault infeed at one end of the faulted line may prevent phase comparison element trip. Consequently, instant conversion from weak-infeed logic with sending permissive continuous signal to fault logic with sending square waves is required in case of the external fault at the adjacent or internal fault for proper operation of phase comparison relay at the remote line's terminal.

OPEN BREAKER ECHO should be applied to any particular application according to local system conditions.

SETTINGS:**OPEN BREAKER KEYING:**

Disables/Enables Open Breaker Keying feature.

BRK 1 AUX CONTACT:

Setting is used to assign a FlexLogic™ operand to control open/close state of the breaker # 1 with either 52a or 52b type contact to create logic "1" when the breaker is open.

BRK 1 CONT SUPV:

Setting is used to select a supervising element such as Test/Normal Switch usually used in breaker # 1 control schemes or any other elements. If no element is required, the default 'Off' should be used.

BRK 2 AUX CONTACT:

If supervision of two breakers is required, this setting is used to assign a FlexLogic™ operand to control open/close state of the breaker # 2 with either 52a or 52b type contact to create logic "1" when the breaker is open

BRK 2 CONT SUPV:

Setting is used to select a supervising element such as Test/Normal Switch usually used in breaker # 2 control schemes or any other elements. If no element is required, the default 'Off' should be used.

OPEN BREAKER KEYING PKP DELAY:

Setting is used to delay operation of Open Breaker Keying to override disagreement between main and auxiliary contacts of the breaker or any other operating conditions.

OPEN BREAKER KEYING RST DELAY:

Setting is used to delay reset of Open Breaker Keying to override disagreement between main and auxiliary contacts of the breaker or any other operating conditions.

WEAK-INFEED KEYING:

Setting is used to assign a sensitive phase-current element for Weak-Infeed Keying control. It should be normally picked up with a minimum line load current. IOC element is suitable for this purpose or a group of OC elements. Also it can be FDM (mixed signal).

WEAK-INFEED SUPV:

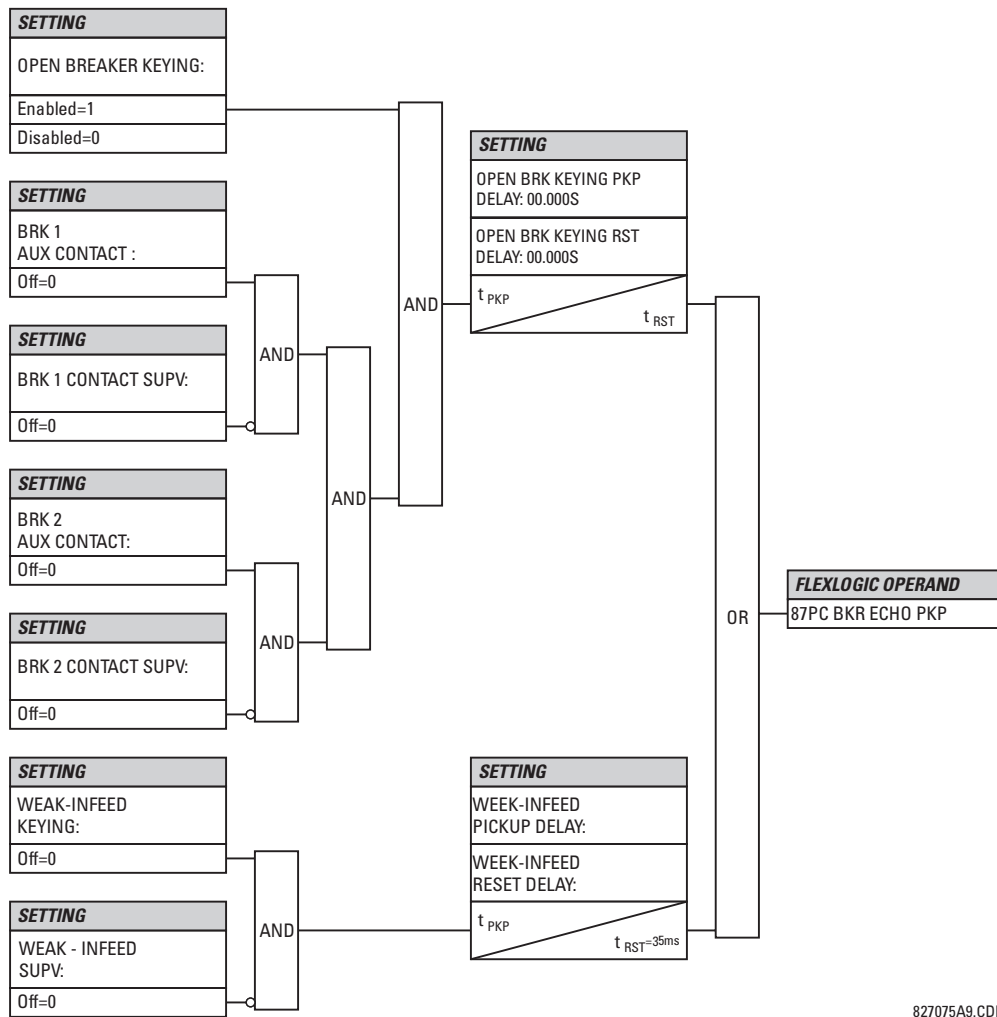
Setting is used to select a weak-infeed supervising element from FlexLogic™ operands. Undervoltage element, auxiliary contacts of breakers indicating close position or other elements can be useful for no-current supervision.

WEAK-INFEED PICKUP DELAY:

Setting is used to delay operation of Weak-Infeed Keying during some transient conditions such as breaker reclosure, etc.

WEAK-INFEED RESET DELAY:

The Weak-Infeed Keying function incorporates default 35 ms reset delay to assure reset coordination with FDH trip-level fault detector at the remote terminal during fault clearing. Default reset time can be changed according to local conditions.

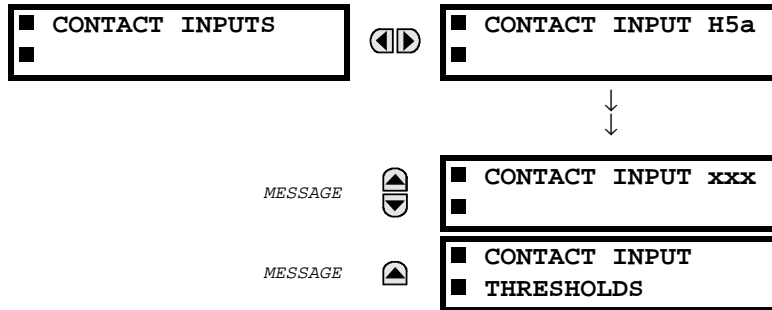


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Figure 5–58: OPEN BREAKER ECHO SCHEME LOGIC

5.7.1 CONTACT INPUTS MENU

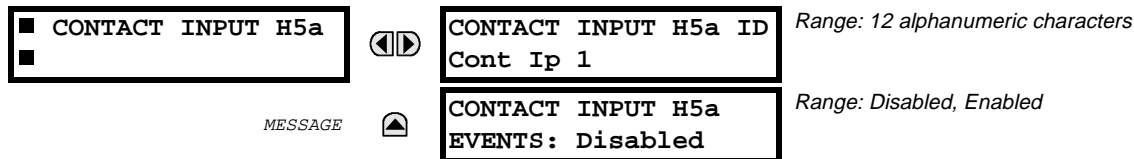
PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ CONTACT INPUTS



The contact inputs menu consists of configuration settings for each individual contact input as well as voltage thresholds for each group of four contact inputs. Upon startup of the relay, the main processor will determine, from an assessment of the modules installed in the chassis, which contact inputs are available and then display settings for only those inputs.

a) CONTACT INPUT EXAMPLE

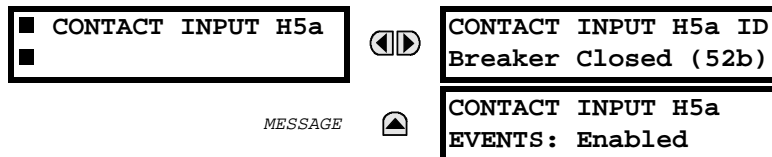
PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ CONTACT INPUTS ⇒ CONTACT INPUT H5a



An alphanumeric ID may be assigned to a contact input, which will be used for diagnostic purposes. The contact input 'ON' (Logic 1) state corresponds to the contact input being closed. If the contact input events is set to Enabled, every change in the contact input state will trigger an event.

APPLICATION EXAMPLE:

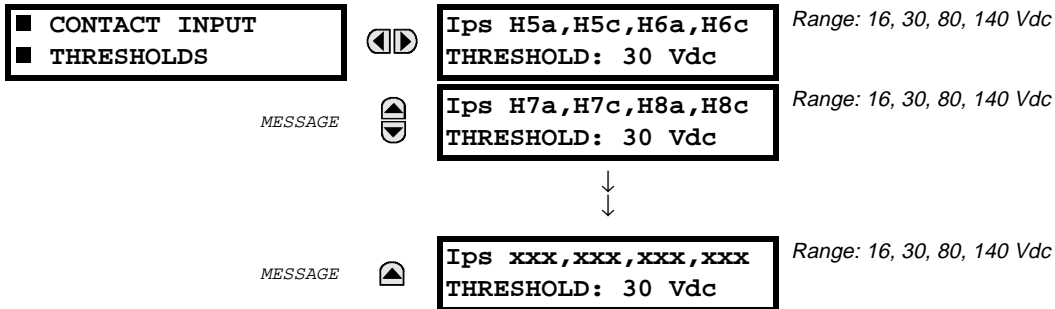
To use contact input H5a as a status input from the breaker 52b contact to seal-in the trip relay and record it in the Event Records menu, program it as follows:



The 52b contact is closed when the breaker is open and open when the breaker is closed.

b) CONTACT INPUT THRESHOLDS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ CONTACT INPUTS ⇒ ↓ CONTACT INPUT THRESHOLDS



Contact inputs are isolated in groups of four to allow connection of wet contacts from different voltage sources for each group. The contact input threshold determines the minimum voltage required to detect a closed contact input. This value should be selected according to the following criteria: 16 for 24 V sources, 30 for 48 V sources, 80 for 110 to 125 V sources and 140 for 250 V sources.

5.7.2 VIRTUAL INPUTS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ ↓ VIRTUAL INPUTS ⇒ VIRTUAL INPUT 1(32)

<div>■ VIRTUAL INPUT 1</div> <div>■</div>	◀▶	VIRTUAL INPUT 1 FUNCTION: Disabled	Range: Disabled, Enabled
	MESSAGE ▲▼	VIRTUAL INPUT 1 ID: Virt Ip 1	Range: Up to 12 alphanumeric characters
	MESSAGE ▲▼	VIRTUAL INPUT 1 TYPE: Latched	Range: Self-Reset, Latched
	MESSAGE ▲	VIRTUAL INPUT 1 EVENTS: Disabled	Range: Disabled, Enabled

There are 32 virtual inputs that can be individually programmed to respond to input signals from the keypad (COMMANDS menu) and non-UCA2 communications protocols only. All virtual input operands are defaulted to OFF = 0 unless the appropriate input signal is received.

Note: virtual input states are preserved through a control power loss.

VIRTUAL INPUT 1 FUNCTION:

If set to Disabled, the input will be forced to 'OFF' (Logic 0) regardless of any attempt to alter the input. If set to Enabled, the input will operate as shown on the scheme logic diagram, and generate output FlexLogic™ operands in response to received input signals and the applied settings.

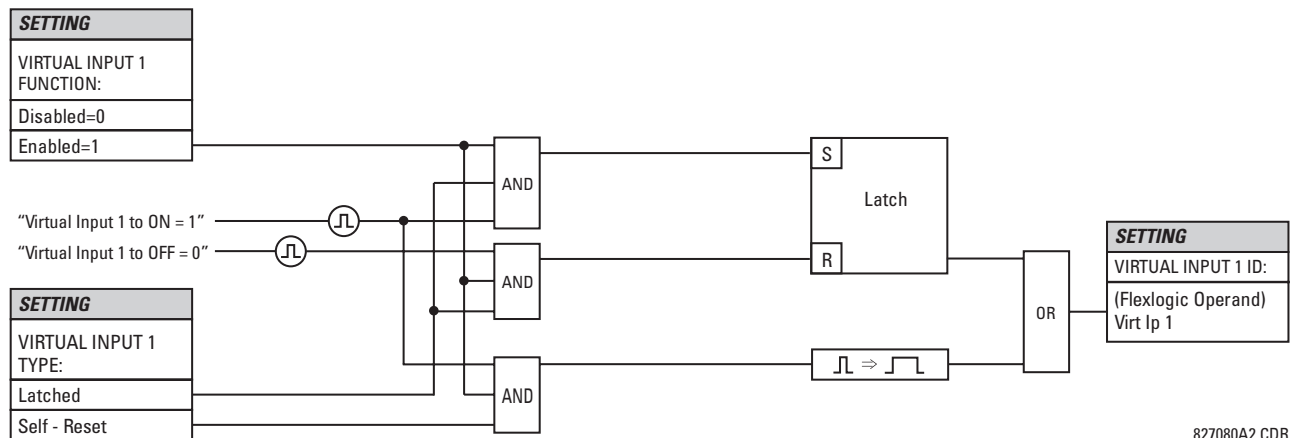
VIRTUAL INPUT 1 TYPE:

There are two types of operation, Self-Reset and Latched. If set to Self-Reset, when the input signal transits from OFF = 0 to ON = 1, the output operand will be set to ON = 1 for only one evaluation of the FlexLogic™ equations and then return to OFF = 0. If set to Latched, the virtual input sets the state of the output operand to the same state as the most recent received input, ON = 1 or OFF = 0.



NOTE

Virtual Input operating mode Self-Reset generates the output operand for a single evaluation of the FlexLogic™ equations. If the operand is to be used anywhere other than internally in a FlexLogic™ equation, it will most probably have to be lengthened in time. A FlexLogic™ Timer with a delayed reset can perform this function.



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Figure 5-59: VIRTUAL INPUTS SCHEME LOGIC

a) UCA SBO TIMER

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ ↓ VIRTUAL INPUTS ⇒ ↓ UCA SBO TIMER

■ UCA SBO TIMER	◀▶	UCA SBO TIMEOUT: 30 s	Range: 1 to 60 s in steps of 1 s
-----------------	----	--------------------------	----------------------------------

The Select-Before-Operate timer sets the interval from the receipt of an Operate signal to the automatic deselection of the virtual input, so that an input does not remain selected indefinitely (this is used only with the UCA Select-Before-Operate feature).

5.7.3 CONTACT OUTPUTS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ ↓ CONTACT OUTPUTS ⇒ CONTACT OUTPUT H1

<div>■ CONTACT OUTPUT H1</div> <div>■</div>		CONTACT OUTPUT H1 ID Cont Op 1	Range: Up to 12 alphanumeric characters	
	MESSAGE	▲▼	OUTPUT H1 OPERATE: Off	Range: Flexlogic™ operand
	MESSAGE	▲▼	OUTPUT H1 SEAL-IN: Off	Range: Flexlogic™ operand
	MESSAGE	▲	CONTACT OUTPUT H1 EVENTS: Enabled	Range: Disabled, Enabled

Upon startup of the relay, the main processor will determine from an assessment of the modules installed in the chassis which contact outputs are available and present the settings for only these outputs.

An ID may be assigned to each contact output. The signal that can OPERATE a contact output may be any FlexLogic™ operand (virtual output, element state, contact input, or virtual input). An additional FlexLogic™ operand may be used to SEAL-IN the relay. Any change of state of a contact output can be logged as an Event if programmed to do so.

EXAMPLE:

The trip circuit current is monitored by providing a current threshold detector in series with some Form-A contacts (see the TRIP CIRCUIT - EXAMPLE figures in the DIGITAL ELEMENTS section). The monitor will set a flag (see Technical Specifications for Form-A). The name of the FlexLogic™ operand set by the monitor, consists of the output relay designation, followed by the name of the flag; e.g. 'Cont Op 1 IOn' or 'Cont Op 1 IOff'.

In most breaker control circuits, the trip coil is connected in series with a breaker auxiliary contact used to interrupt current flow after the breaker has tripped, to prevent damage to the less robust initiating contact. This can be done by monitoring an auxiliary contact on the breaker which opens when the breaker has tripped, but this scheme is subject to incorrect operation caused by differences in timing between breaker auxiliary contact change-of-state and interruption of current in the trip circuit. The most dependable protection of the initiating contact is provided by directly measuring current in the tripping circuit, and using this parameter to control resetting of the initiating relay. This scheme is often called "trip seal-in".

In UR relays, this can be realized using the 'Cont Op 1 IOn' FlexLogic™ operand to seal-in the Contact Output. For example,

<div>■ CONTACT OUTPUT H1</div> <div>■</div>		CONTACT OUTPUT H1 ID Cont Op 1	
	MESSAGE	▲▼	OUTPUT H1 OPERATE: Off
	MESSAGE	▲▼	OUTPUT H1 SEAL-IN: Cont Op 1 IOn
	MESSAGE	▲	CONTACT OUTPUT H1 EVENTS: Enabled

5.7.4 VIRTUAL OUTPUTS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇨ ↓ VIRTUAL OUTPUTS ⇨ VIRTUAL OUTPUT 1

■ VIRTUAL OUTPUT 1	◀▶	VIRTUAL OUTPUT 1 ID Virt Op 1	Range: Up to 12 alphanumeric characters
■	▲	VIRTUAL OUTPUT 1 EVENTS: Disabled	Range: Disabled, Enabled

MESSAGE

There are 64 virtual outputs that may be assigned via FlexLogic™. If not assigned, the output will be forced to 'OFF' (Logic 0). An ID may be assigned to each virtual output. Virtual outputs are resolved in each pass through the evaluation of the FlexLogic™ equations. Any change of state of a virtual output can be logged as an event if programmed to do so.

EXAMPLE:

If Virtual Output 1 is the trip signal from FlexLogic™ and the trip relay is used to signal events, the settings would be programmed as follows:

■ VIRTUAL OUTPUT 1	◀▶	VIRTUAL OUTPUT 1 ID Trip
■	▲	VIRTUAL OUTPUT 1 EVENTS: Disabled

MESSAGE

5.7.5 REMOTE DEVICES

a) REMOTE INPUTS / OUTPUTS - OVERVIEW

Remote inputs and outputs, which are a means of exchanging information regarding the state of digital points between remote devices, are provided in accordance with the Electric Power Research Institute's (EPRI) UCA2 "Generic Object Oriented Substation Event (GOOSE)" specifications.



The UCA2 specification requires that communications between devices be implemented on Ethernet communications facilities. For UR relays, Ethernet communications is provided only on the type 9C and 9D versions of the CPU module.

The sharing of digital point state information between GOOSE equipped relays is essentially an extension to FlexLogic™ to allow distributed FlexLogic™ by making operands available to/from devices on a common communications network. In addition to digital point states, GOOSE messages identify the originator of the message and provide other information required by the communication specification. All devices listen to network messages and capture data from only those messages that have originated in selected devices.

GOOSE messages are designed to be short, high priority and with a high level of reliability. The GOOSE message structure contains space for 128 bit pairs representing digital point state information. The UCA specification provides 32 "DNA" bit pairs, which are status bits representing pre-defined events. All remaining bit pairs are "UserSt" bit pairs, which are status bits representing user-definable events. The UR implementation provides 32 of the 96 available UserSt bit pairs.

The UCA2 specification includes features that are used to cope with the loss of communication between transmitting and receiving devices. Each transmitting device will send a GOOSE message upon a successful power-up, when the state of any included point changes, or after a specified interval (the "default update" time) if a change-of-state has not occurred. The transmitting device also sends a "hold time" which is set to three times the programmed default time, which is required by the receiving device.

Receiving devices are constantly monitoring the communications network for messages they require, as recognized by the identification of the originating device carried in the message. Messages received from remote devices include the message "hold" time for the device. The receiving relay sets a timer assigned to the originating device to the "hold" time interval, and if it has not received another message from this device at time-out, the remote device is declared to be non-communicating, so it will use the programmed default state for all points from that specific remote device. This mechanism allows a receiving device to fail to detect a single transmission from a remote device which is sending messages at the slowest possible rate, as set by its "default update" timer, without reverting to use of the programmed default states. If a message is received from a remote device before the "hold" time expires, all points for that device are updated to the states contained in the message and the hold timer is restarted. The status of a remote device, where 'Offline' indicates 'non-communicating', can be displayed.

b) LOCAL DEVICES - Device ID for Transmitting GOOSE Messages

In a UR relay, the device ID that identifies the originator of the message is programmed in the setting 'RELAY NAME' under the heading 'INSTALLATION' in the 'SETTINGS / PRODUCT SETUP' section.

c) REMOTE DEVICES - Device ID for Receiving GOOSE Messages

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ ↓ REMOTE DEVICES ⇒ REMOTE DEVICE 1(16)

■ REMOTE DEVICE 1	◀▶	REMOTE DEVICE 1 ID:	Range: Up to 20 alphanumeric characters
■		Remote Device 1	

Sixteen Remote Devices, numbered from 1 to 16, can be selected for setting purposes.

A receiving relay must be programmed to capture messages from only those originating remote devices of interest. This setting is used to select specific remote devices by entering (bottom row) the exact identification (ID) assigned to those devices.

5.7.6 REMOTE INPUTS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ ↓ REMOTE INPUTS ⇒ REMOTE INPUT 1(32)

<div style="border: 1px solid black; padding: 5px; width: fit-content;"> ■ REMOTE INPUT 1 ■ </div>		REMOTE IN 1 DEVICE: Remote Device 1	<i>Range: 1 to 16 inclusive</i>
<i>MESSAGE</i>		REMOTE IN 1 BIT PAIR: None	<i>Range: None, DNA-1 to DNA-32, and UserSt-1 to UserSt-32</i>
<i>MESSAGE</i>		REMOTE IN 1 DEFAULT STATE: Off	<i>Range: On, Off</i>
<i>MESSAGE</i>		REMOTE IN 1 EVENTS: Disabled	<i>Range: Disabled, Enabled</i>

Remote Inputs which create FlexLogic™ operands at the receiving relay, are extracted from GOOSE messages originating in remote devices. The relay provides 32 Remote Inputs, each of which can be selected from a list consisting of 64 selections: DNA-1 through DNA-32 and UserSt-1 through UserSt-32. The function of DNA inputs is defined in the UCA2 specifications and is presented in the UCA2 DNA ASSIGNMENTS table in the section on Remote Outputs. The function of UserSt inputs is defined by the user selection of the FlexLogic™ operand whose state is represented in the GOOSE message. A user must program a DNA point from the appropriate operand.

Remote Input 1 must be programmed to replicate the logic state of a specific signal from a specific remote device for local use. This programming is performed via the three settings shown above.

Setting 'REMOTE IN 1 DEVICE' is used to select the number (1-16) of the Remote Device which originates the signal required, as previously assigned to the remote device via the setting 'REMOTE DEVICE nn ID' (see the REMOTE DEVICES section). Setting 'REMOTE IN 1 BIT PAIR' is used to select the specific bits of the GOOSE message required. Setting 'REMOTE IN 1 DEFAULT STATE' is used to select the logic state that will be used for this point if the local relay has just completed startup or the remote device sending this point is declared to be non-communicating.



For more information on GOOSE specifications, see REMOTE INPUTS/OUTPUTS – OVERVIEW in the REMOTE DEVICES section.

NOTE

5.7.7 REMOTE OUTPUTS - DNA BIT PAIRS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇒ REMOTE OUTPUTS DNA BIT PAIRS ⇒ REMOTE OUPUTS DNA- 1 BIT PAIR

■ REMOTE OUTPUTS
 ■ DNA- 1 BIT PAIR

DNA- 1 OPERAND:
 Off

Range: FlexLogic™ Operand

MESSAGE

DNA- 1 EVENTS:
 Disabled

Range: Disabled, Enabled

Remote Outputs (1-32) are FlexLogic™ operands inserted into GOOSE messages that are transmitted to remote devices on a LAN. Each digital point in the message must be programmed to carry the state of a specific FlexLogic™ operand. The above operand setting represents a specific DNA function (as shown in the UCA2 DNA ASSIGNMENTS table) to be transmitted.

Table 5–17: UCA DNA2 ASSIGNMENTS

DNA	DEFINITION	INTENDED FUNCTION	LOGIC 0	LOGIC 1
1	OperDev		Trip	Close
2	Lock Out		LockoutOff	LockoutOn
3	Initiate Reclosing	Initiate remote reclose sequence	InitRecloseOff	InitRecloseOn
4	Block Reclosing	Prevent/cancel remote reclose sequence	BlockOff	BlockOn
5	Breaker Failure Initiate	Initiate remote breaker failure scheme	BFIOff	BFIOOn
6	Send Transfer Trip	Initiate remote trip operation	TxXfrTripOff	TxXfrTripOn
7	Receive Transfer Trip	Report receipt of remote transfer trip command	RxXfrTripOff	RxXfrTripOn
8	Send Perm	Report permissive affirmative	TxPermOff	TxPermOn
9	Receive Perm	Report receipt of permissive affirmative	RxPermOff	RxPermOn
10	Stop Perm	Override permissive affirmative	StopPermOff	StopPermOn
11	Send Block	Report block affirmative	TxBlockOff	TxBlockOn
12	Receive Block	Report receipt of block affirmative	RxBlockOff	RxBlockOn
13	Stop Block	Override block affirmative	StopBlockOff	StopBlockOn
14	BkrDS	Report breaker disconnect 3-phase state	Open	Closed
15	BkrPhsADS	Report breaker disconnect phase A state	Open	Closed
16	BkrPhsBDS	Report breaker disconnect phase B state	Open	Closed
17	BkrPhsCDS	Report breaker disconnect phase C state	Open	Closed
18	DiscSwDS		Open	Closed
19	Interlock DS		DSLockOff	DSLockOn
20	LineEndOpen	Report line open at local end	Open	Closed
21	Status	Report operating status of local GOOSE device	Offline	Available
22	Event		EventOff	EventOn
23	Fault Present		FaultOff	FaultOn
24	Sustained Arc	Report sustained arc	SustArcOff	SustArcOn
25	Downed Conductor	Report downed conductor	DownedOff	DownedOn
26	Sync Closing		SyncClsOff	SyncClsOn
27	Mode	Report mode status of local GOOSE device	Normal	Test
28→32	Reserved			



For more information on GOOSE specifications, see REMOTE INPUTS/OUTPUTS – OVERVIEW in the REMOTE DEVICES section.

NOTE

5.7.8 REMOTE OUTPUTS - UserSt BIT PAIRS

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇨ REMOTE OUTPUTS UserSt BIT PAIRS ⇨ REMOTE OUTPUTS UserSt- 1 BIT PAIR

<div>■ REMOTE OUTPUTS</div> <div>■ UserSt- 1 BIT PAIR</div>	<div>◀▶</div> <div> UserSt- 1 OPERAND: Off </div> <div> UserSt- 1 EVENTS: Disabled </div>	<div>Range: FlexLogic™ Operand</div> <div>Range: Disabled, Enabled</div>
---	---	--

MESSAGE ▲

Remote Outputs 1 to 32 originate as GOOSE messages to be transmitted to remote devices. Each digital point in the message must be programmed to carry the state of a specific FlexLogic™ operand. The setting above is used to select the operand which represents a specific UserSt function (as selected by the user) to be transmitted.

The following setting represents the time between sending GOOSE messages when there has been no change of state of any selected digital point. This setting is located under the menu heading COMMUNICATIONS in the SETTINGS \ PRODUCT SETUP section.

DEFAULT GOOSE UPDATE TIME: 60 s	Range: 1 to 60 in steps of 1 second
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For more information on GOOSE specifications, see REMOTE INPUTS/OUTPUTS – OVERVIEW in the REMOTE DEVICES section.

NOTE

5

5.7.9 RESETTING

PATH: SETTINGS ↓ INPUTS/OUTPUTS ⇨ RESETTING

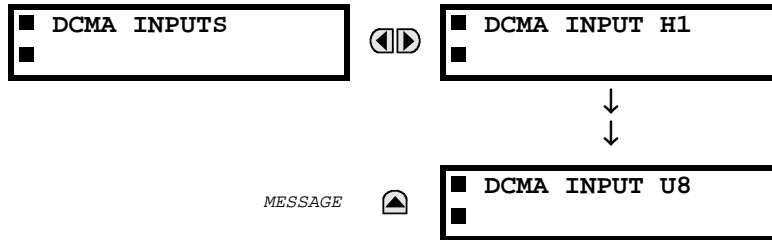
<div>■ RESETTING</div> <div>■</div>	<div>◀▶</div> <div> RESET OPERAND: Off </div>	Range: FlexLogic™ Operand
-------------------------------------	---	---------------------------

Some events can be programmed to latch the faceplate LED event indicators and the target message on the display. Once set, the latching mechanism will hold all of the latched indicators or messages in the set state after the initiating condition has cleared until a RESET command is received to return these latches (not including FlexLogic™ latches) to the reset state. The RESET command can be sent from the faceplate RESET push-button, a remote device via a communications channel, or any programmed operand.

When the RESET command is received by the relay, two FlexLogic™ operands are created. These operands, which are stored as events, reset the latches if the initiating condition has cleared. The three sources of RESET commands each create the FlexLogic™ operand "RESET OP". Each individual source of a RESET command also creates its individual operand "RESET OP (PUSHBUTTON)", RESET OP (COMMS) or RESET OP (OPERAND) to identify the source of the command. The setting shown above selects the operand that will create the RESET OP (OPERAND) operand.

5.8.1 DCMA INPUTS

PATH: SETTINGS ↓ TRANSDUCER I/O ⇒ DCMA INPUTS



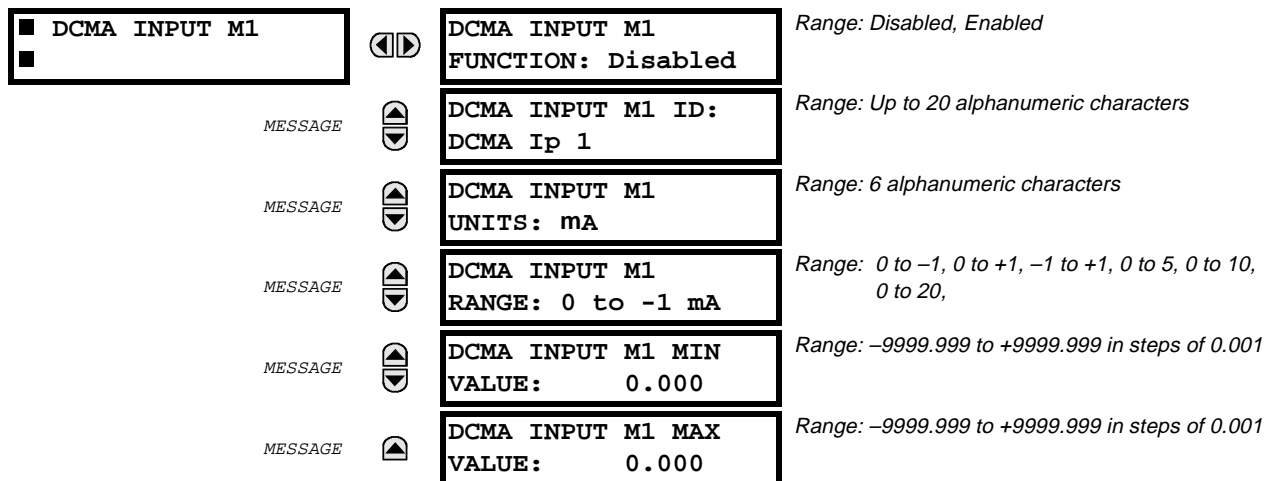
Hardware and software is provided to receive signals from external transducers and convert these signals into a digital format for use as required. The relay will accept inputs in the range of -1 to $+20$ mA DC, suitable for use with most common transducer output ranges; all inputs are assumed to be linear over the complete range. Specific hardware details are contained in the **HARDWARE** chapter.

Before the DCMA input signal can be used, the value of the signal measured by the relay must be converted to the range and quantity of the external transducer primary input parameter, such as DC voltage or temperature. The relay simplifies this process by internally scaling the output from the external transducer and displaying the actual primary parameter.

DCMA input channels are arranged in a manner similar to CT and VT channels. The user configures individual channels with the settings shown here.

The channels are arranged in sub-modules of two channels, numbered from 1 through 8 from top to bottom. On power-up, the relay will automatically generate configuration settings for every channel, based on the order code, in the same general manner that is used for CTs and VTs. Each channel is assigned a slot letter followed by the row number, 1 through 8 inclusive, which is used as the channel number. The relay generates an actual value for each available input channel.

Settings are automatically generated for every channel available in the specific relay as shown below for the first channel of a type 5F transducer module installed in slot M.

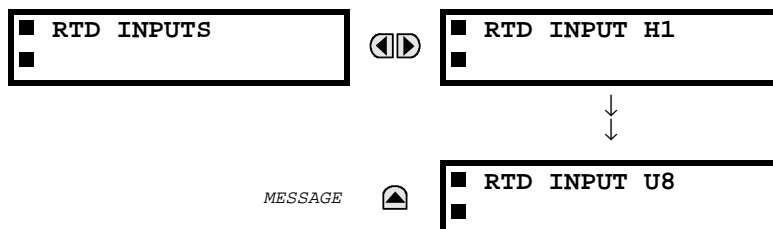


The function of the channel may be either "Enabled" or "Disabled." If Disabled, there will not be an actual value created for the channel. An alphanumeric "ID" is assigned to the channel - this ID will be included in the display of the channel actual value, along with the programmed "UNITS" associated with the parameter measured by the transducer, such as Volt, °C, MegaWatts, etc. This ID is also used to reference the channel as the input parameter to features designed to measure this type of parameter. The RANGE setting is used to select the specific mA DC range of the transducer connected to the input channel.

The MIN VALUE and MAX VALUE settings are used to program the span of the transducer in primary units. For example, a temperature transducer might have a span from 0 to 250°C; in this case the MIN value would be 0 and the MAX value 250. Another example would be a Watt transducer with a span from –20 to +180 MW; in this case the MIN value would be –20 and the MAX value 180. Intermediate values between the MIN and MAX are scaled linearly.

5.8.2 RTD INPUTS

PATH: SETTINGS ↓ TRANSDUCER I/O ⇨ ↓ RTD INPUTS

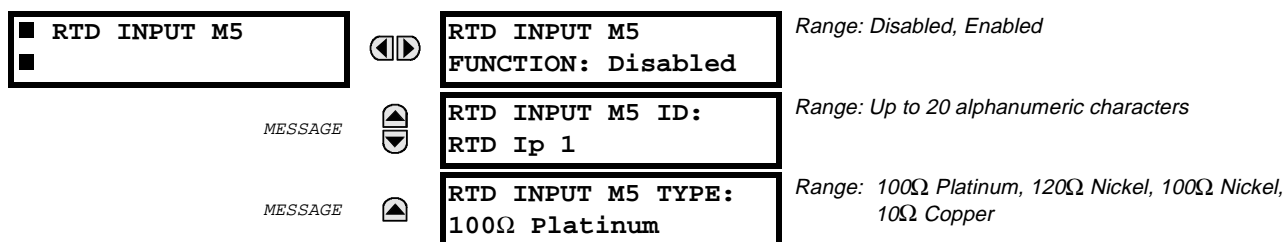


Hardware and software is provided to receive signals from external Resistance Temperature Detectors and convert these signals into a digital format for use as required. These channels are intended to be connected to any of the RTD types in common use. Specific hardware details are contained in the HARDWARE chapter.

RTD input channels are arranged in a manner similar to CT and VT channels. The user configures individual channels with the settings shown here.

The channels are arranged in sub-modules of two channels, numbered from 1 through 8 from top to bottom. On power-up, the relay will automatically generate configuration settings for every channel, based on the order code, in the same general manner that is used for CTs and VTs. Each channel is assigned a slot letter followed by the row number, 1 through 8 inclusive, which is used as the channel number. The relay generates an actual value for each available input channel.

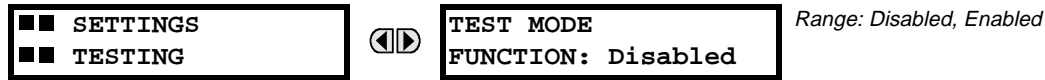
Settings are automatically generated for every channel available in the specific relay as shown below for the first channel of a type 5C transducer module installed in slot M.



The function of the channel may be either "Enabled" or "Disabled." If Disabled, there will not be an actual value created for the channel. An alphanumeric "ID" is assigned to the channel - this ID will be included in the display of the channel actual value. This ID is also used to reference the channel as the input parameter to features designed to measure this type of parameter. Selecting the type of RTD connected to the channel configures the channel.

5.9.1 TEST MODE

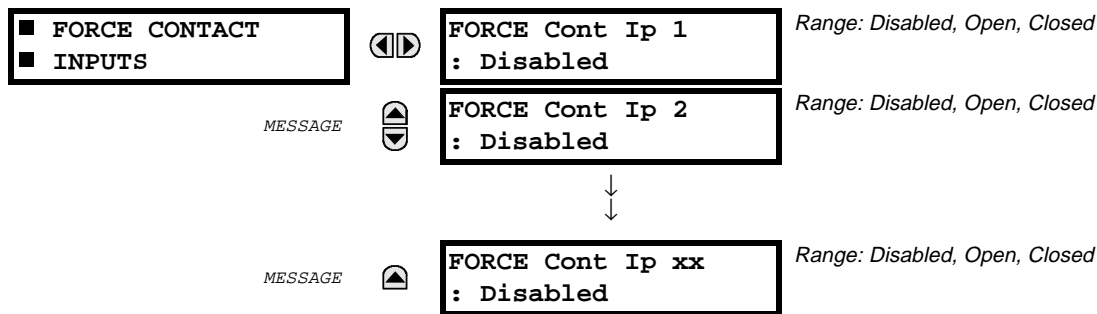
PATH: SETTINGS ↓ TESTING ⇌ TEST MODE



The relay provides test settings to verify that the relay is functional using simulated conditions to test all contact inputs and outputs. While the relay is in **TEST MODE** (FUNCTION Enabled), the feature being tested overrides normal functioning of the relay. During this time the TEST MODE LED will remain on. Once out of TEST MODE (FUNCTION Disabled), the normal functioning of the relay will be restored.

5.9.2 FORCE CONTACT INPUTS

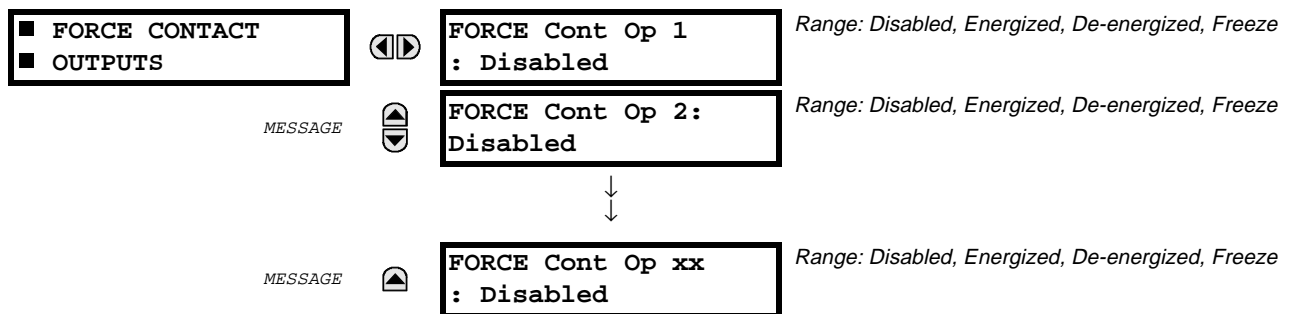
PATH: SETTINGS ↓ TESTING ⇌ FORCE CONTACT INPUTS



The Force Contact Inputs test feature of the relay provides a method of performing checks on the function of all contact inputs. Once enabled, the relay will be placed into Test Mode, allowing this feature to override the normal function of contact inputs. The TEST MODE LED will be ON indicating that the relay is in test mode. The state of each contact input may be programmed as Disabled, Open or Closed. All contact input operations return to normal when all settings for this feature are disabled.

5.9.3 FORCE CONTACT OUTPUTS

PATH: SETTINGS ↓ TESTING ⇌ FORCE CONTACT OUTPUTS



The Force Contact Output test feature of the relay, provides a method of performing checks on all contact outputs. Once enabled, the relay will be placed into a Test Mode, allowing this feature to override the normal function of contact outputs. The TEST MODE LED will be ON. The state of each contact output may be programmed as Disabled, Energized, De-energized or Freeze. The Freeze option maintains the output contact in the state at which it was frozen. All contact output operations return to normal when all the settings for this feature are disabled.

5.9.4 CHANNEL TESTS

PATH: SETTINGS ↓ TESTING ⇌ CHANNEL TESTS ⇌ CHANNEL 1

<div>■ CHANNEL 1</div> <div>■</div>	<div>◀▶</div> <div>▲</div>	CHANNEL 1 LOOPBACK FUNCTION: NO	Range: No, Yes
		CHANNEL 1 ECHOBACK FUNCTION: NO	Range: No, Yes

MESSAGE

Test facilities are provided for both channels 1 and 2.

These tests are used to characterize the communications channels to establish parameters that are used to set up the scheme. Channel testing requires that the channels are working correctly and simultaneous access to both relays. For testing the relay at one end is in the loopback mode and the relay at the other end is in the echoback mode. The relay set to loopback will originate the test signals and the other relay will receive this signal and transmit this signal back to the originator. Measurements of channel delay are made only by the relay in the loopback mode.

A test is run, without AC current or voltage injected into either relay, by:

1. Setting the 87PC FUNCTION to Disabled on both relays.
2. Setting the TEST MODE FUNCTION to Enabled on both relays.
3. Setting the CHANNEL X LOOPBACK FUNCTION to Yes on relay A (the originator).
4. Setting the CHANNEL X ECHOBACK FUNCTION to Yes on relay B (the repeater).
5. In the ACTUAL VALUES / STATUS / CHANNEL TESTS / CHANNEL X / CHANNEL X LOOPBACK STATUS menu at relay A should read "OK" indicating a signal was transmitted and received.
6. In the ACTUAL VALUES / STATUS / CHANNEL TESTS / CHANNEL X / CHANNEL X DELAY at relay A should be read and recorded to be entered on relay A.
7. Repeating tests 3 to 6 with relay A set to the ECHOBACK function (the repeater) and relay B set to the LOOPBACK function (the originator).
8. Setting the TEST MODE FUNCTION to Disabled on both relays.
9. Entering the measured and recorded values in settings CONTROL ELEMENTS / PHASE COMPARISON ELEMENTS / 87PC SCHEME / 87PC PHASE DELAY CH X on both relays.
10. Setting the 87PC FUNCTION to Enabled on both relays.

Initiating the LOOPBACK function or ECHOBACK function starts a 20 minute timer, which will automatically return all these settings to Disabled upon timeout, to prevent accidentally leaving the relays in the test mode.

During channel delay tests one of the relay will send the control message which remote

will loop it back to be read at the sending relay. The sending relay will measure the channel delay and verify channel communications both directions.



NOTE

Asymmetry of the receiving from the remote PLC signal has to be measured using appropriate oscilloscope by injecting pure sinusoidal current into the remote relay above FDL level what subsequently keying the remote PLC. If, for example, the received pulse is shorter than half of the power cycle duration by 0.5 ms, the value "0.5 ms" has to be entered under 87PC SYMMETRY CH X setting. If received pulse is longer by 0.5 ms, the value "-0.5" has to be entered.

Test to be carried out at both channels if applicable.

6.1.1 ACTUAL VALUES MAIN MENU

<div> <div>■ ■ ACTUAL VALUES</div> <div>■ ■ STATUS</div> </div>		<div> <div>■ CONTACT INPUTS</div> <div>■</div> </div>	See page 6-3.
		<div> <div>■ VIRTUAL INPUTS</div> <div>■</div> </div>	See page 6-3.
		<div> <div>■ REMOTE INPUTS</div> <div>■</div> </div>	See page 6-4.
		<div> <div>■ CONTACT OUTPUTS</div> <div>■</div> </div>	See page 6-4.
		<div> <div>■ VIRTUAL OUTPUTS</div> <div>■</div> </div>	See page 6-5.
		<div> <div>■ AUTORECLOSE</div> <div>■</div> </div>	See page 6-5.
		<div> <div>■ REMOTE DEVICES</div> <div>■ STATUS</div> </div>	See page 6-5.
		<div> <div>■ REMOTE DEVICES</div> <div>■ STATISTICS</div> </div>	See page 6-6.
		<div> <div>■ CHANNEL TESTS</div> <div>■</div> </div>	See page 6-6.
		<div> <div>■ DIGITAL COUNTERS</div> <div>■</div> </div>	See page 6-7.
		<div> <div>■ FLEX STATES</div> <div>■</div> </div>	See page 6-7.
		<div> <div>■ ETHERNET</div> <div>■</div> </div>	See page 6-7.
		<div> <div>■ SOURCE SRC 1</div> <div>■</div> </div>	See page 6-12.
		<div> <div>■ SOURCE SRC 2</div> <div>■</div> </div>	
		<div> <div>■ SOURCE SRC 3</div> <div>■</div> </div>	
		<div> <div>■ SOURCE SRC 4</div> <div>■</div> </div>	
		<div> <div>■ SOURCE SRC 5</div> <div>■</div> </div>	
		<div> <div>■ SOURCE SRC 6</div> <div>■</div> </div>	
		<div> <div>■ SYNCHROCHECK</div> <div>■</div> </div>	See page 6-15.
		<div> <div>■ TRACKING FREQUENCY</div> <div>■</div> </div>	See page 6-15.

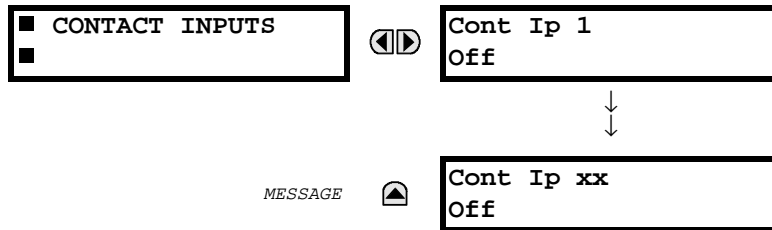
	▲▼	■ TRANSDUCER I/O ■ DCMA INPUTS	See page 6-15.
	▲	■ TRANSDUCER I/O ■ RTD INPUTS	See page 6-15.
▲ ■ ACTUAL VALUES ■ RECORDS	◀▶	■ FAULT REPORTS ■	See page 6-16.
▼	▲▼	■ EVENT RECORDS ■	See page 6-19.
	▲▼	■ OSCILLOGRAPHY ■	See page 6-19.
	▲▼	■ DATA LOGGER ■	See page 6-20.
	▲	■ MAINTENANCE ■	See page 6-20.
▲ ■ ACTUAL VALUES ■ PRODUCT INFO	◀▶	■ MODEL INFORMATION ■	See page 6-21.
	▲	■ FIRMWARE REVISIONS ■	See page 6-21.



For status reporting, 'On' represents Logic 1 and 'Off' represents Logic 0.

6.2.1 CONTACT INPUTS

PATH: ACTUAL VALUES ↓ STATUS ⇨ CONTACT INPUTS



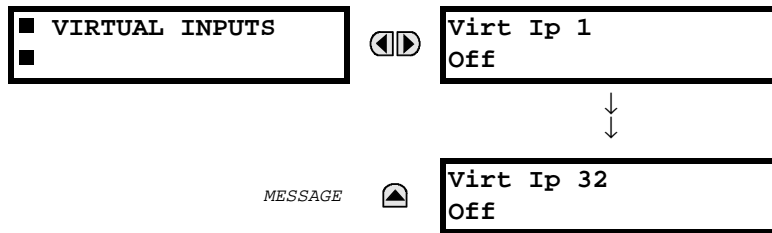
The present status of the contact inputs is shown here.

The first line of a message display indicates the ID of the contact input. For example, 'Cont Ip 1' refers to the contact input in terms of the default name-array index.

The second line of the display indicates the logic state of the contact input.

6.2.2 VIRTUAL INPUTS

PATH: ACTUAL VALUES ↓ STATUS ⇨ ↓ VIRTUAL INPUTS



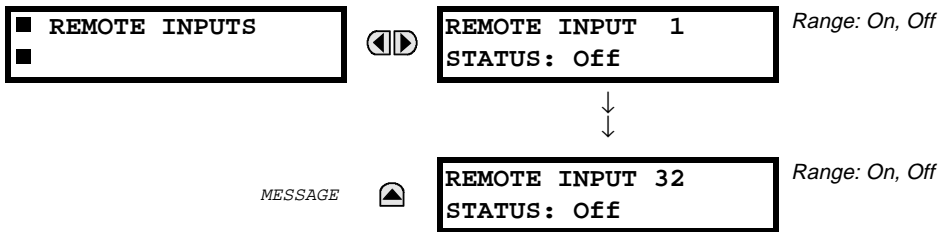
The present status of the 32 virtual inputs is shown here.

The first line of a message display indicates the ID of the virtual input. For example, 'Virt Ip 1' refers to the virtual input in terms of the default name-array index.

The second line of the display indicates the logic state of the virtual input.

6.2.3 REMOTE INPUTS

PATH: ACTUAL VALUES ↓ STATUS ⇌ ↓ REMOTE INPUTS

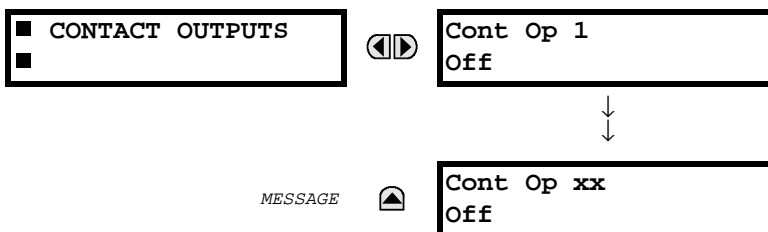


The present state of the 32 remote inputs is shown here.

The state displayed will be that of the remote point unless the remote device has been established to be "Offline" in which case the value shown is the programmed default state for the remote input.

6.2.4 CONTACT OUTPUTS

PATH: ACTUAL VALUES ↓ STATUS ⇌ ↓ CONTACT OUTPUTS



6

The present state of the contact outputs is shown here.

The first line of a message display indicates the ID of the contact output. For example, 'Cont Op 1' refers to the contact output in terms of the default name-array index.

The second line of the display indicates the logic state of the contact output.

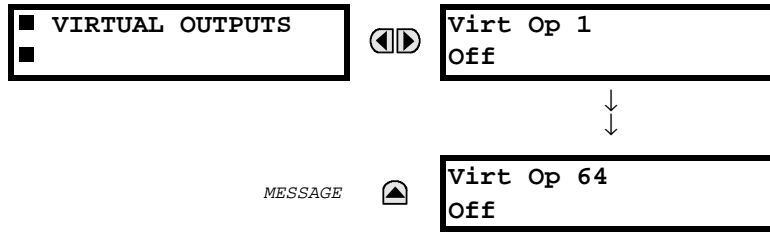


NOTE

For Form-A outputs, the state of the voltage(V) and/or current(I) detectors will show as: Off, VOff, IOff, On, VOn, and/or IOn. For Form-C outputs, the state will show as Off or On.

6.2.5 VIRTUAL OUTPUTS

PATH: ACTUAL VALUES ↓ STATUS ⇌ ↓ VIRTUAL OUTPUTS



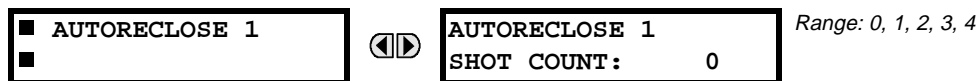
The present state of up to 64 virtual outputs is shown here.

The first line of a message display indicates the ID of the virtual output. For example, 'Virt Op 1' refers to the virtual output in terms of the default name-array index.

The second line of the display indicates the logic state of the virtual output, as calculated by the FlexLogic™ equation for that output.

6.2.6 AUTORECLOSE

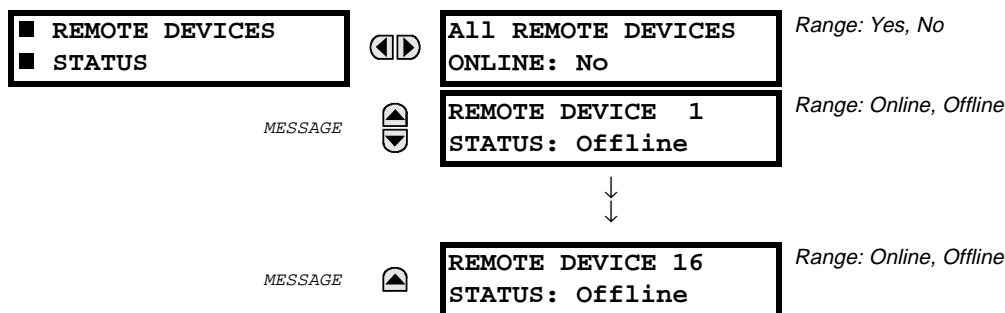
PATH: ACTUAL VALUES ↓ STATUS ⇌ ↓ AUTORECLOSE ⇌ AUTORECLOSE 1



The automatic reclosure shot count is shown here.

6.2.7 REMOTE DEVICES STATUS

PATH: ACTUAL VALUES ↓ STATUS ⇌ ↓ REMOTE DEVICES STATUS



The present state of up to 16 programmed Remote Devices is shown here.

The ALL REMOTE DEVICES ONLINE message indicates whether or not all programmed Remote Devices are online. If the corresponding state is 'No', then at least one required Remote Device is not online.

6.2.8 REMOTE DEVICES STATISTICS

PATH: ACTUAL VALUES ↓ STATUS ⇨ ↓ REMOTE DEVICES STATISTICS ⇨ REMOTE DEVICE 1(16)

REMOTE DEVICE 1

◀▶

REMOTE DEVICE 1

StNum: 0

MESSAGE

▲

REMOTE DEVICE 1

SqNum: 0

Statistical data (2 types) for up to 16 programmed Remote Devices is shown here.

- The ‘StNum’ number is obtained from the indicated Remote Device and is incremented whenever a change of state of at least one DNA or UserSt bit occurs.
- The ‘SqNum’ number is obtained from the indicated Remote Device and is incremented whenever a GOOSE message is sent. This number will rollover to zero when a count of 4,294,967,295 is incremented.

6.2.9 CHANNEL TESTS

PATH: ACTUAL VALUES ↓ STATUS ⇨ ↓ CHANNEL TESTS ⇨ CHANNEL 1(2)

CHANNEL 1

◀▶

CHANNEL 1 LOOPBACK

STATUS: n/a

MESSAGE

▲▼

CHANNEL 1 DELAY

0.000 ms

Range: n/a, OK, Fail

Range: 0.000 to 65.535

There are two identical test channel results menus available, numbered 1 and 2. The status of loopback testing and the results of channel tests are shown here.

The following applies to the messages displayed In the CHANNEL 1 LOOPBACK STATUS actual value:

- n/a** = loopback testing is not active
- OK** = a signal was transmitted and received
- Fail** = a signal was transmitted but not received

The result of the CHANNEL 1(2) DELAY measurement is entered in the 87PC scheme.

6.2.10 DIGITAL COUNTERS

PATH: ACTUAL VALUES ↓ DIGITAL COUNTERS ⇨ ↓ DIGITAL COUNTERS ⇨ DIGITAL COUNTERS Counter 1(8)

■ DIGITAL COUNTERS ■ Counter 1	◀▶	Counter 1 ACCUM: 0
	MESSAGE ▲▼	Counter 1 FROZEN: 0
	MESSAGE ▲▼	Counter 1 FROZEN: YYYY/MM/DD HH:MM:SS
	MESSAGE ▲	Counter 1 MICROS: 0

The present status of the 8 digital counters is shown here.

The status of each counter, with the user-defined counter name, includes the accumulated and frozen counts (the count units label will also appear). Also included, is the date/time stamp for the frozen count. The 'MICROS' value refers to the microsecond portion of the time stamp.

6.2.11 FLEX STATES

PATH: ACTUAL VALUES ↓ STATUS ⇨ ↓ FLEX STATES

■ FLEX STATES ■	◀▶	PARAM 1: Off Off	Range: Off, On
	MESSAGE ▲▼	PARAM 2: Off Off	Range: Off, On
	MESSAGE ▲	PARAM 256: Off Off	Range: Off, On

↓

There are 256 FlexState bits available, numbered from 1 to 256. The second line value indicates the state of the given FlexState bit.

6.2.12 ETHERNET

PATH: ACTUAL VALUES ↓ STATUS ⇨ ↓ ETHERNET

■ ETHERNET ■	◀▶	ETHERNET PRI LINK STATUS: OK	Range: Fail, OK, n/a
	MESSAGE ▲	ETHERNET SEC LINK STATUS: OK	Range: Fail, OK, n/a

6.3.1 METERING CONVENTIONS

a) UR CONVENTION FOR MEASURING POWER AND ENERGY

The following figure illustrates the conventions established for use in UR relays.

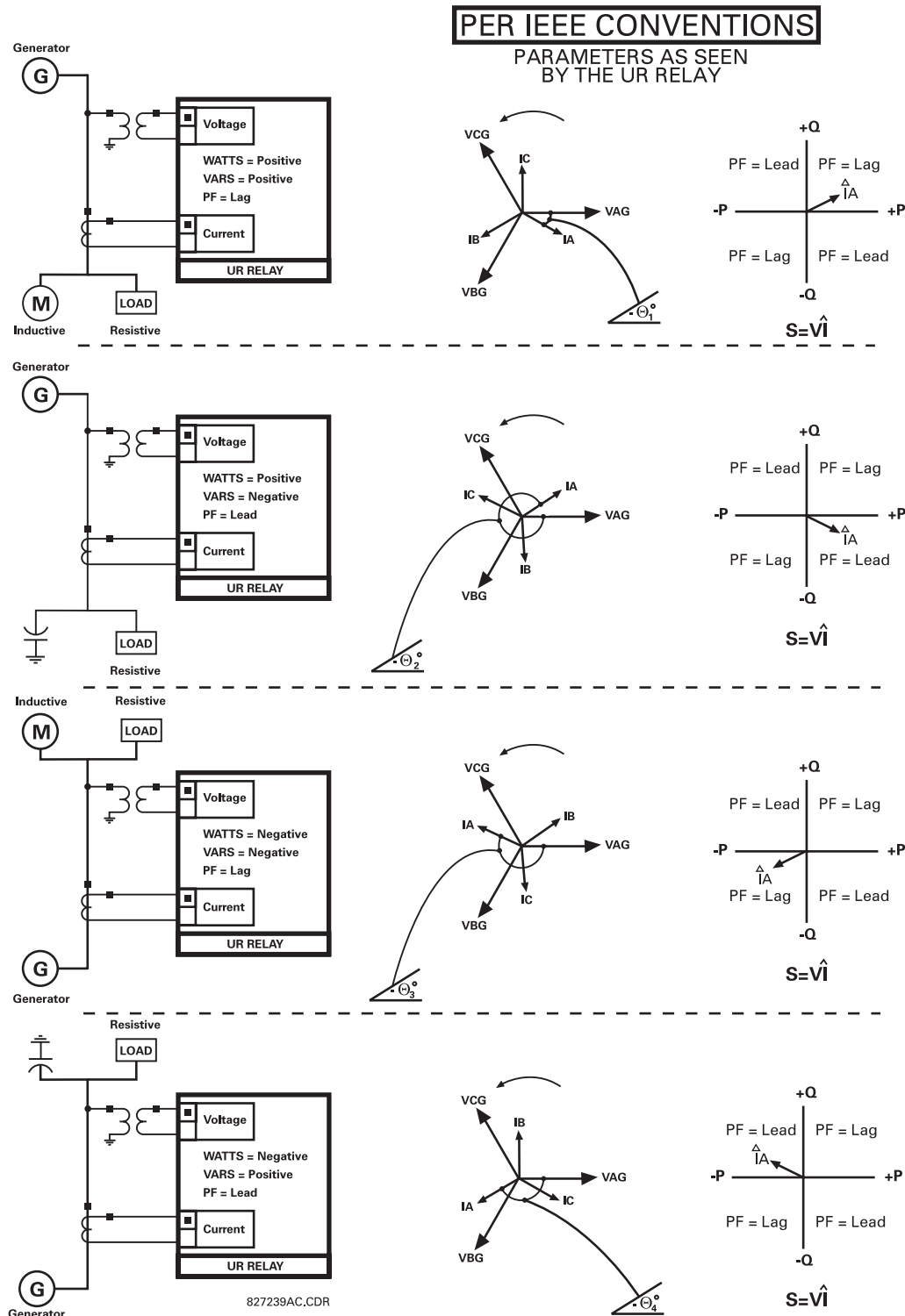


Figure 6-1: FLOW DIRECTION OF SIGNED VALUES FOR WATTS AND VARs

b) UR CONVENTION FOR MEASURING PHASE ANGLES

All phasors calculated by UR relays and used for protection, control and metering functions are rotating phasors that maintain the correct phase angle relationships with each other at all times.

For display and oscillography purposes, all phasor angles in a given relay are referred to an AC input channel which is pre-selected by setting SETTINGS / SYSTEM SETUP / POWER SYSTEM / FREQUENCY AND PHASE REFERENCE. This setting defines a particular Source that is to be used as the reference.

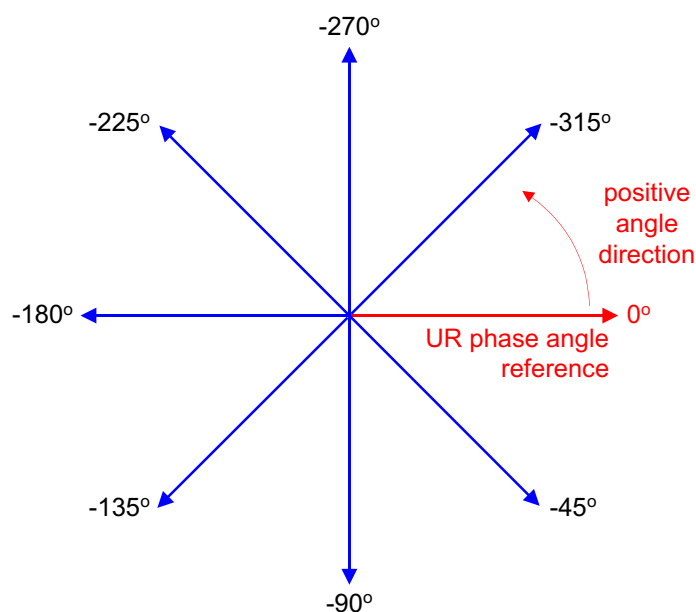
The relay will first determine if any "Phase VT" bank is indicated in the Source - if it is voltage channel VA of that bank is used as the angle reference.

Otherwise, the relay determines if any "Aux VT" bank is indicated - if it is the auxiliary voltage channel of that bank is used as the angle reference.

If neither of the above conditions is satisfied, then two more steps of this hierarchical procedure to determine the reference signal include "Phase CT" bank and "Ground CT" bank.

If the AC signal pre-selected by the relay upon configuration is not measurable, the phase angles are not referenced.

The phase angles are assigned as positive in the leading direction, and are presented as negative in the lagging direction, to more closely align with power system metering conventions. This is illustrated below.



827845A1.CDR

Figure 6-2: UR PHASE ANGLE MEASUREMENT CONVENTION

c) UR CONVENTION FOR MEASURING SYMMETRICAL COMPONENTS

UR relays calculate voltage symmetrical components for the power system phase A line-to-neutral voltage, and symmetrical components of the currents for the power system phase A current.

Owing to the above definition, phase angle relations between the symmetrical currents and voltages stay the same irrespective of the connection of instrument transformers. This is important for setting directional protection elements that use symmetrical voltages.

For display and oscillography purposes the phase angles of symmetrical components are referenced to a common reference as described in the previous sub-section.

WYE-Connected Instrument Transformers:

- ABC phase rotation:

$$V_{-0} = \frac{1}{3}(V_{AG} + V_{BG} + V_{CG})$$

$$V_{-1} = \frac{1}{3}(V_{AG} + aV_{BG} + a^2V_{CG})$$

$$V_{-2} = \frac{1}{3}(V_{AG} + a^2V_{BG} + aV_{CG})$$

- ACB phase rotation:

$$V_{-0} = \frac{1}{3}(V_{AG} + V_{BG} + V_{CG})$$

$$V_{-1} = \frac{1}{3}(V_{AG} + a^2V_{BG} + aV_{CG})$$

$$V_{-2} = \frac{1}{3}(V_{AG} + aV_{BG} + a^2V_{CG})$$

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The above equations apply to currents as well.

DELTA-Connected Instrument Transformers:

- ABC phase rotation:

$$V_{-0} = \text{N/A}$$

$$V_{-1} = \frac{1 \angle 30^\circ}{3\sqrt{3}}(V_{AB} + a^2V_{BC} + aV_{CA})$$

$$V_{-2} = \frac{1 \angle -30^\circ}{3\sqrt{3}}(V_{AB} + aV_{BC} + a^2V_{CA})$$

- ACB phase rotation:

$$V_{-0} = \text{N/A}$$

$$V_{-1} = \frac{1 \angle 30^\circ}{3\sqrt{3}}(V_{AB} + aV_{BC} + a^2V_{CA})$$

$$V_{-2} = \frac{1 \angle -30^\circ}{3\sqrt{3}}(V_{AB} + a^2V_{BC} + aV_{CA})$$

The zero-sequence voltage is not measurable under the DELTA connection of instrument transformers and is defaulted to zero.

The table below shows an example of symmetrical components calculations for the ABC phase rotation.

Table 6–1: CALCULATING VOLTAGE SYMMETRICAL COMPONENTS EXAMPLE

SYSTEM VOLTAGES, sec. V *						VT conn.	UR INPUTS, sec. V			SYMM. COMP, sec. V		
V_{AG}	V_{BG}	V_{CG}	V_{AB}	V_{BC}	V_{CA}		F5ac	F6ac	F7ac	V_0	V_1	V_2
13.9 $\angle 0^\circ$	76.2 $\angle -125^\circ$	79.7 $\angle -250^\circ$	84.9 $\angle -313^\circ$	138.3 $\angle -97^\circ$	85.4 $\angle -241^\circ$	WYE	13.9 $\angle 0^\circ$	76.2 $\angle -125^\circ$	79.7 $\angle -250^\circ$	19.5 $\angle -192^\circ$	56.5 $\angle -7^\circ$	23.3 $\angle -187^\circ$
UNKNOWN (only V_1 and V_2 can be determined)			84.9 $\angle 0^\circ$	138.3 $\angle -144^\circ$	85.4 $\angle -288^\circ$	DELTA	84.9 $\angle 0^\circ$	138.3 $\angle -144^\circ$	85.4 $\angle -288^\circ$	N/A	56.5 $\angle -54^\circ$	23.3 $\angle -234^\circ$

* The power system voltages are phase-referenced – for simplicity – to V_{AG} and V_{AB} , respectively. This, however, is a relative matter. It is important to remember that the UR displays are always referenced as specified under SETTINGS / SYSTEM SETUP / POWER SYSTEM / FREQUENCY AND PHASE REFERENCE.

The example above is illustrated in the following figure.

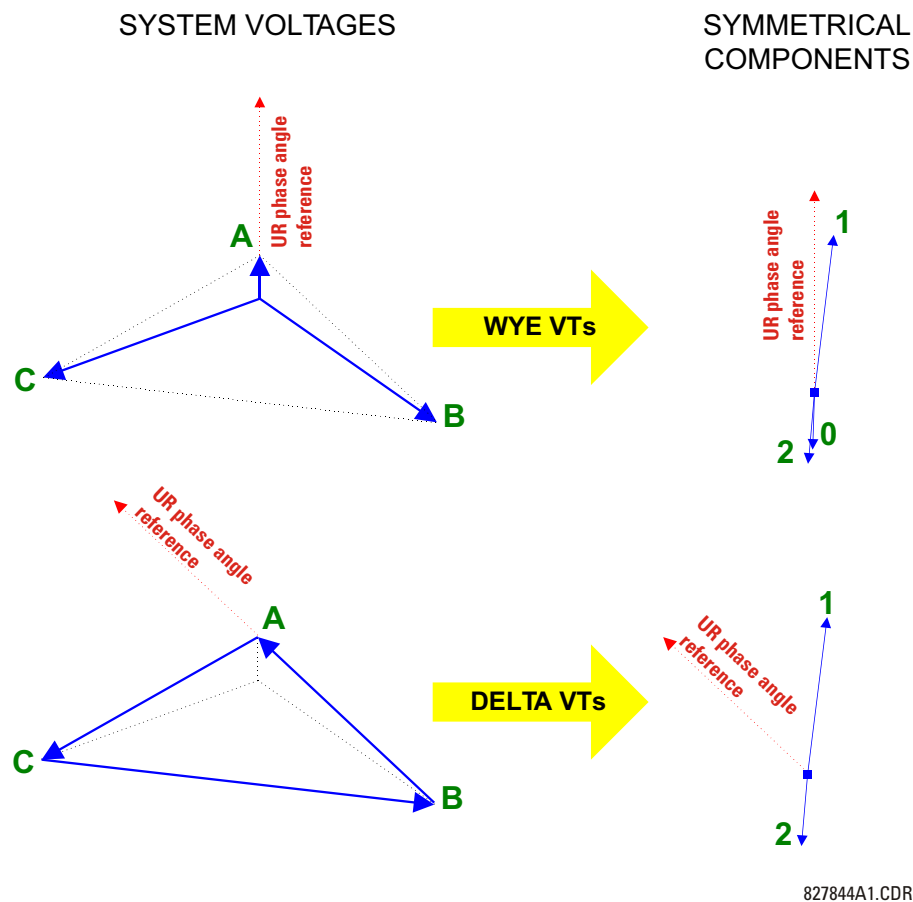


Figure 6–3: ILLUSTRATION OF THE UR CONVENTION FOR SYMMETRICAL COMPONENTS

6.3.2 SOURCES

PATH: ACTUAL VALUES ↓ METERING ⇒ SOURCE SRC 1 ⇒

<div> <div>■ PHASE CURRENT</div> <div>■ SRC 1</div> </div>		◀▶	SRC 1 RMS Ia: 0.000 b: 0.000 c: 0.000 A
	MESSAGE	▲▼	SRC 1 RMS Ia: 0.000 A
	MESSAGE	▲▼	SRC 1 RMS Ib: 0.000 A
	MESSAGE	▲▼	SRC 1 RMS Ic: 0.000 A
	MESSAGE	▲▼	SRC 1 RMS In: 0.000 A
	MESSAGE	▲▼	SRC 1 PHASOR Ia: 0.000 A 0.0°
	MESSAGE	▲▼	SRC 1 PHASOR Ib: 0.000 A 0.0°
	MESSAGE	▲▼	SRC 1 PHASOR Ic: 0.000 A 0.0°
	MESSAGE	▲▼	SRC 1 PHASOR In: 0.000 A 0.0°
	MESSAGE	▲▼	SRC 1 ZERO SEQ I0: 0.000 A 0.0°
	MESSAGE	▲▼	SRC 1 POS SEQ I1: 0.000 A 0.0°
	MESSAGE	▲	SRC 1 NEG SEQ I2: 0.000 A 0.0°
		▲	
<div> <div>■ GROUND CURRENT</div> <div>■ SRC 1</div> </div>		◀▶	SRC 1 RMS Ig: 0.000 A
	MESSAGE	▲▼	SRC 1 PHASOR Ig: 0.000 A 0.0°
	MESSAGE	▲	SRC 1 PHASOR Igd: 0.000 A 0.0°
		▲	
<div> <div>■ PHASE VOLTAGE</div> <div>■ SRC 1</div> </div>		◀▶	SRC 1 RMS Vag: 0.000 V
	MESSAGE	▲▼	SRC 1 RMS Vbg: 0.000 V
	MESSAGE	▲▼	SRC 1 RMS Vcg: 0.000 V
	MESSAGE	▲▼	SRC 1 PHASOR Vag: 0.000 V 0.0°

MESSAGE		SRC 1 PHASOR Vbg: 0.000 V 0.0°
MESSAGE		SRC 1 PHASOR Vcg: 0.000 V 0.0°
MESSAGE		SRC 1 RMS Vab: 0.000 V
MESSAGE		SRC 1 RMS Vbc: 0.000 V
MESSAGE		SRC 1 RMS Vca: 0.000 V
MESSAGE		SRC 1 PHASOR Vab: 0.000 V 0.0°
MESSAGE		SRC 1 PHASOR Vbc: 0.000 V 0.0°
MESSAGE		SRC 1 PHASOR Vca: 0.000 V 0.0°
MESSAGE		SRC 1 ZERO SEQ V0: 0.000 V 0.0°
MESSAGE		SRC 1 POS SEQ V1: 0.000 V 0.0°
MESSAGE		SRC 1 NEG SEQ V2: 0.000 V 0.0°
 		SRC 1 RMS Vx: 0.000 V
MESSAGE		SRC 1 PHASOR Vx: 0.000 V 0.0°
 		SRC 1 REAL POWER 3φ: 0.000 W
MESSAGE		SRC 1 REAL POWER φa: 0.000 W
MESSAGE		SRC 1 REAL POWER φb: 0.000 W
MESSAGE		SRC 1 REAL POWER φc: 0.000 W
MESSAGE		SRC 1 REACTIVE PWR 3φ: 0.000 var
MESSAGE		SRC 1 REACTIVE PWR φa: 0.000 var
MESSAGE		SRC 1 REACTIVE PWR φb: 0.000 var

MESSAGE

▲▼

SRC 1 REACTIVE PWR

ϕc: 0.000 var

MESSAGE

▲▼

SRC 1 APPARENT PWR

3ϕ: 0.000 VA

MESSAGE

▲▼

SRC 1 APPARENT PWR

ϕa: 0.000 VA

MESSAGE

▲▼

SRC 1 APPARENT PWR

ϕb: 0.000 VA

MESSAGE

▲▼

SRC 1 APPARENT PWR

ϕc: 0.000 VA

MESSAGE

▲▼

SRC 1 POWER FACTOR

3ϕ: 1.000

MESSAGE

▲▼

SRC 1 POWER FACTOR

ϕa: 1.000

MESSAGE

▲▼

SRC 1 POWER FACTOR

ϕb: 1.000

MESSAGE

▲▼

SRC 1 POWER FACTOR

ϕc: 1.000

▲

■ FREQUENCY

■ SRC 1

◀▶

SRC 1 FREQUENCY:

0.00 Hz

There are up to 6 identical Source actual value menus available, numbered from SRC 1 to SRC 6.

"SRC 1" will be replaced by whatever name was programmed by the user for the associated source (see SETTINGS \ SYSTEM SETUP \ SIGNAL SOURCES).

SOURCE FREQUENCY is measured via zero-crossings of an AC input signal. The signal is low-pass filtered and passed through a 'rejection' filter that eliminates false readings due to phase reversals and harmonics.

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L60 Line Phase Comparison Relay

GE Power Management

6.3.3 SYNCHROCHECK

PATH: ACTUAL VALUES ↓ METERING ⇨ SYNCHROCHECK ⇨ SYNCHROCHECK 1

■ SYNCHROCHECK1	◀▶	SYNCHROCHECK 1 DELTA VOLT: 0.000 V
■	▲▼	SYNCHROCHECK 1 DELTA PHASE: 0.0°
MESSAGE	▲	SYNCHROCHECK 1 DELTA FREQ: 0.00 Hz

The Actual Values menu for SYNCHROCHECK2 is identical to that of SYNCHROCHECK1.

If a Synchrocheck Function setting is set to Disabled, the corresponding Actual Values menu item will not be displayed.

6.3.4 TRACKING FREQUENCY

PATH: ACTUAL VALUES ↓ METERING ⇨ TRACKING FREQUENCY

■ TRACKING FREQUENCY	◀▶	TRACKING FREQUENCY: 60.00 Hz
■		

The tracking frequency of the reference signal source is displayed here. See also the SETTINGS \ SYSTEM SETUP \ POWER SYSTEM menu section. Frequency is measured from the VAG input for 'Wye', the VAB (ABC rotation) or VAC (ACB rotation) input for 'Delta', or the IA input if voltages are not available.

6.3.5 TRANSDUCER I/O

a) DCMA INPUTS

PATH: ACTUAL VALUES ↓ METERING ⇨ TRANSDUCER I/O DCMA INPUTS ⇨ DCMA INPUT xx

■ DCMA INPUT xx	◀▶	DCMA INPUT xx 0.000 mA
■		

Actual values for each DCMA input channel that is Enabled are displayed with the top line as the programmed channel "ID" and the bottom line as the value followed by the programmed units.

b) RTD INPUTS

PATH: ACTUAL VALUES ↓ METERING ⇨ TRANSDUCER I/O RTD INPUTS ⇨ RTD INPUT xx

■ RTD INPUT xx	◀▶	RTD INPUT xx -50 °C
■		

Actual values for each RTD input channel that is Enabled are displayed with the top line as the programmed channel "ID" and the bottom line as the value.

6.4.1 FAULT REPORTS

PATH: ACTUAL VALUES ↓ RECORDS ⇌ FAULT REPORTS ⇌

NO FAULTS TO REPORT

OR

■ FAULT REPORT #	◀▶	FAULT #	DATE:	(YYYY/MM/DD)
■		2000/08/11		
MESSAGE	▲▼	FAULT #	TIME:	(HH:MM:SS.ssssss)
		00:00:00.000000		
MESSAGE	▲▼	FAULT #	TYPE:	(where applicable)
		ABG		
MESSAGE	▲▼	FAULT #	LOCATION	(where applicable)
		00.0 km		
MESSAGE	▲	FAULT #	RECLOSE	(where applicable)
		SHOT: 0		

Up to the latest 10 fault reports can be stored. The most recent fault location calculation (when applicable) is displayed in this menu, along with the date and time stamp of the event which triggered the calculation.

See the SETTINGS \ PRODUCT SETUP \ FAULT REPORT menu for assigning the Source and Trigger for fault calculations. Refer to the COMMANDS CLEAR RECORDS menu for clearing fault reports.

6

a) FAULT LOCATOR OPERATION

Fault Type determination is required for calculation of Fault Location – the algorithm uses the angle between the negative and positive sequence components of the relay currents.

To improve accuracy and speed of operation, the fault components of the currents are used, i.e., the pre-fault phasors are subtracted from the measured current phasors.

In addition to the angle relationships, certain extra checks are performed on magnitudes of the negative and zero sequence currents.

The single-ended fault location method assumes that the fault components of the currents supplied from the local (A) and remote (B) systems are in phase. The figure below shows an equivalent system for fault location.

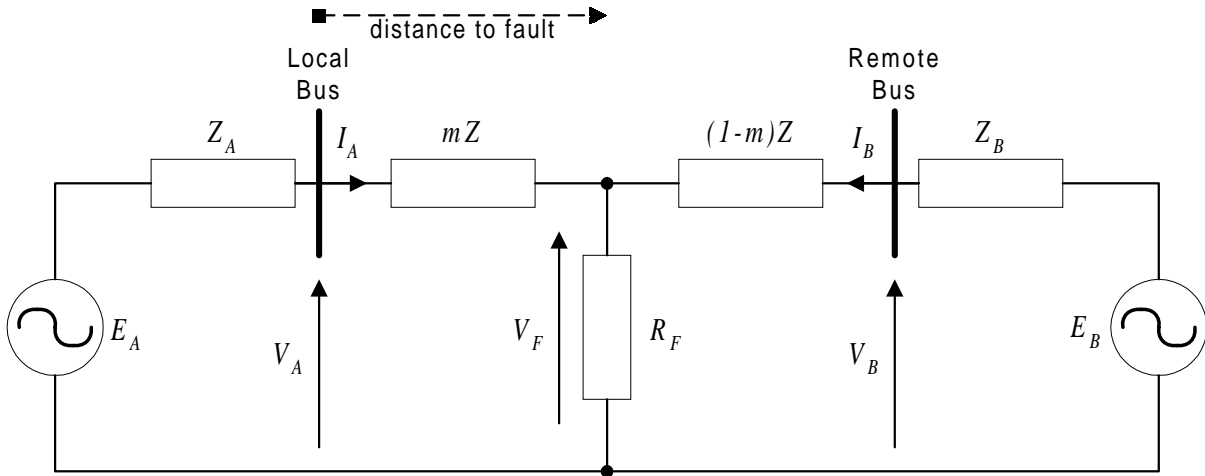


Figure 6-4: EQUIVALENT SYSTEM FOR FAULT LOCATION

The following equations hold true for this equivalent system.

$$V_A = m \cdot Z \cdot I_A + R_F \cdot (I_A + I_B) \quad \text{eqn. 1}$$

where: m = sought pu distance to fault,
 Z = positive sequence impedance of the line.

The currents supplied from the local and remote systems can be parted between their fault (F) and pre-fault load (pre) components:

$$I_A = I_{AF} + I_{Apre} \quad \text{eqn. 2}$$

and neglecting shunt parameters of the line:

$$I_B = I_{BF} - I_{Apre} \quad \text{eqn. 3}$$

Inserting equations 2 and 3 into equation 1 and solving for the fault resistance yields:

$$R_F = \frac{V_A - m \cdot Z \cdot I_A}{I_{AF} \cdot \left(1 + \frac{I_{BF}}{I_{AF}}\right)} \quad \text{eqn. 4}$$

Assuming the fault components of the currents, I_{AF} and I_{BF} are in phase, and observing that the fault resistance, as impedance, does not have any imaginary part gives:

$$\text{Im}\left(\frac{V_A - m \cdot Z \cdot I_A}{I_{AF}}\right) \quad \text{eqn. 5}$$

where: $\text{Im}()$ represents the imaginary part of a complex number.

Equation 5 solved for the unknown m creates the following fault location algorithm:

$$m = \frac{\text{Im}(V_A \cdot I_{AF}^*)}{\text{Im}(Z \cdot I_A \cdot I_{AF}^*)} \quad \text{eqn. 6}$$

where: * denotes the complex conjugate and: $I_{AF} = I_A - I_{Apre}$ eqn. 7

Depending on the fault type, appropriate voltage and current signals are selected from the phase quantities before applying equations 6 and 7 (the superscripts denote phases, the subscripts denote stations):

- For AG faults:

$$V_A = V_A^A, \quad I_A = I_A^A + K_0 \cdot I_{0A} \quad \text{eqn. 8a}$$

- For BG faults:

$$V_A = V_A^B, \quad I_A = I_A^B + K_0 \cdot I_{0A} \quad \text{eqn. 8b}$$

- For CG faults:

$$V_A = V_A^C, \quad I_A = I_A^{BC} + K_0 \cdot I_{0A} \quad \text{eqn. 8c}$$

- For AB and ABG faults:

$$V_A = V_A^A - V_A^B, \quad I_A = I_A^A - I_A^B \quad \text{eqn. 8d}$$

- For BC and BCG faults:

$$V_A = V_A^B - V_A^C, \quad I_A = I_A^B - I_A^C \quad \text{eqn. 8e}$$

- For CA and CAG faults:

$$V_A = V_A^C - V_A^A, \quad I_A = I_A^C - I_A^A \quad \text{eqn. 8f}$$

where K_0 is the zero sequence compensation factor (for equations 8a to 8f)

- For ABC faults, all three AB, BC, and CA loops are analyzed and the final result is selected based upon consistency of the results

The element calculates the distance to the fault (with m in miles or kilometers) and the phases involved in the fault.

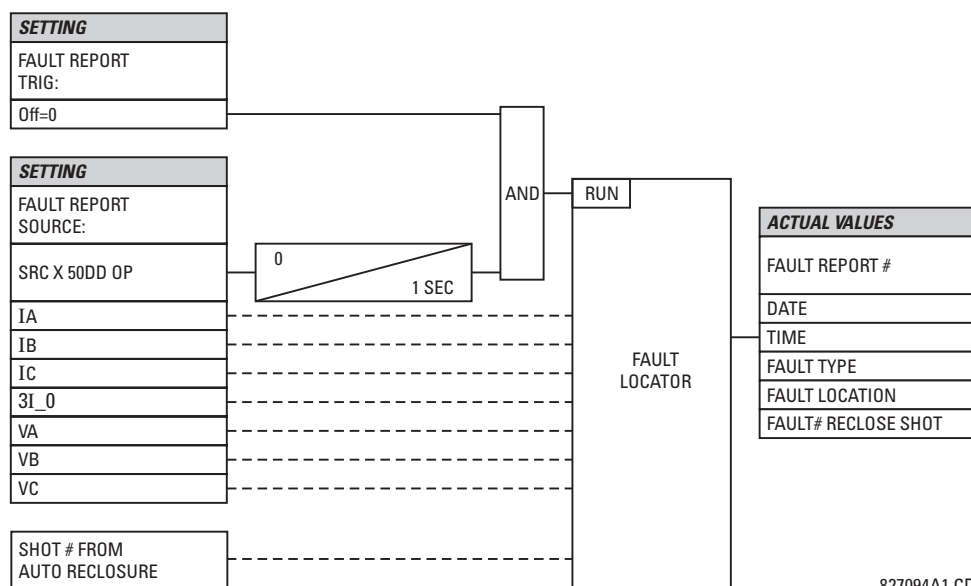
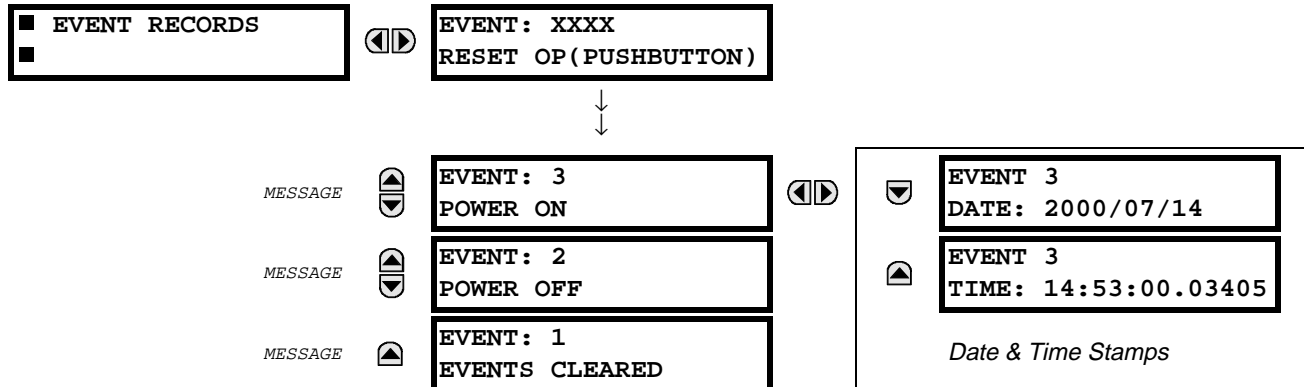


Figure 6-5: FAULT LOCATOR SCHEME

6.4.2 EVENT RECORDS

PATH: ACTUAL VALUES ↓ RECORDS ⇌ ↓ EVENT RECORDS



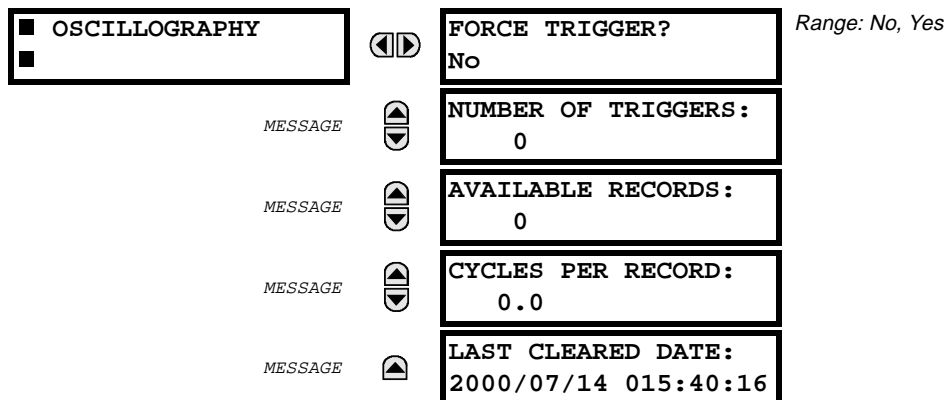
The Event Records menu shows the contextual data associated with up to the last 1024 events, listed in chronological order from most recent to oldest. If all 1024 event records have been filled, the oldest record will be removed as a new record is added.

Each event record will show the event identifier/sequence number, cause, and date/time stamp associated with the event trigger.

Refer to the COMMANDS CLEAR RECORDS menu for clearing event records.

6.4.3 OSCILLOGRAPHY

PATH: ACTUAL VALUES ↓ RECORDS ⇌ ↓ OSCILLOGRAPHY



This menu allows the user to view the number of triggers involved and number of oscillography traces available. The 'cycles per record' value is calculated to account for the fixed amount of data storage for oscillography. See also the SETTINGS \ PRODUCT SETUP \ OSCILLOGRAPHY section.

A trigger can be forced here at any time by setting 'Yes' to the FORCE TRIGGER? command.

Refer to the COMMANDS CLEAR RECORDS menu for clearing the oscillography records.

6.4.4 DATA LOGGER

PATH: ACTUAL VALUES ↓ RECORDS ⇨ ↓ DATA LOGGER

DATA LOGGER

◀▶

OLDEST SAMPLE TIME:

2000/01/14 13:45:51

MESSAGE

▲

NEWEST SAMPLE TIME:

2000/01/14 15:21:19

Oldest Sample Time is the time at which the oldest available samples were taken. It will be static until the log gets full, at which time it will start counting at the defined sampling rate.

Newest Sample Time is the time at which the most recent samples were taken. It counts up at the defined sampling rate.

If no channels are defined for Data Logger, both Times are static.

Refer to the COMMANDS CLEAR RECORDS menu for clearing data logger records.

6.4.5 MAINTENANCE

a) BREAKER 1(2)

PATH: ACTUAL VALUES ↓ RECORDS ⇨ ↓ MAINTENANCE ⇨ BREAKER 1

BREAKER 1

◀▶

BKR 1 ARCING AMP φA:

0.00 kA2-cyc

MESSAGE

▲▼

BKR 1 ARCING AMP φB:

0.00 kA2-cyc

MESSAGE

▲

BKR 1 ARCING AMP φC:

0.00 kA2-cyc

There is an identical Actual Value menu for each of the 2 Breakers. The Arcing AMP values are in units of kA²-cycles.

Refer to the COMMANDS CLEAR RECORDS menu for clearing breaker arcing current records.

6

6-20

L60 Line Phase Comparison Relay

GE Power Management

6.5.1 MODEL INFORMATION

PATH: ACTUAL VALUES ↓ PRODUCT INFO ⇨ MODEL INFORMATION

<div>■ MODEL INFORMATION</div> <div>■</div>		<div>ORDER CODE LINE 1: L60-A00-HCH-F8A-H6A</div>	(example code shown)
	MESSAGE	<div>ORDER CODE LINE 2:</div>	
	MESSAGE	<div>ORDER CODE LINE 3:</div>	
	MESSAGE	<div>ORDER CODE LINE 4:</div>	
	MESSAGE	<div>SERIAL NUMBER:</div>	
	MESSAGE	<div>ETHERNET MAC ADDRESS 000000000000</div>	
	MESSAGE	<div>MANUFACTURING DATE: 0</div>	(YYYY/MM/DD HH:MM:SS)
	MESSAGE	<div>OPERATING TIME: 0:00:00</div>	

The product order code, serial number, Ethernet MAC address, date/time of manufacture, and operating time are shown here.

6.5.2 FIRMWARE REVISIONS

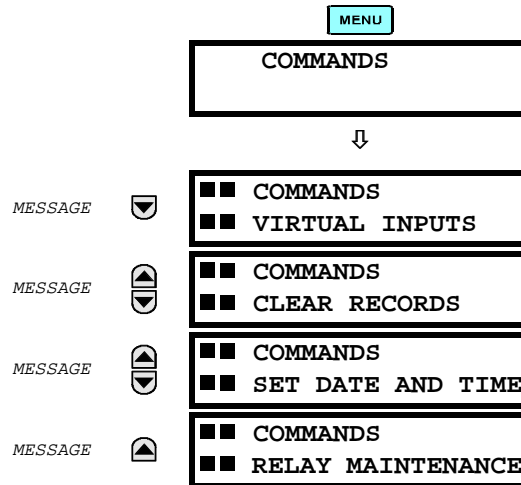
6

PATH: ACTUAL VALUES ↓ PRODUCT INFO ⇨ FIRMWARE REVISIONS

<div>■ FIRMWARE REVISIONS</div> <div>■</div>		<div>L60 Line Relay REVISION: 2.60</div>	Range: 0.00 to 655.35 Revision number of the application firmware.
	MESSAGE	<div>MODIFICATION FILE NUMBER: 0</div>	Range: 0 to 65535 (ID of the MOD FILE.) Value is 0 for each standard firmware release.
	MESSAGE	<div>BOOT PROGRAM REVISION: 1.12</div>	Range: 0.00 to 655.35 Revision number of the boot program firmware.
	MESSAGE	<div>FRONT PANEL PROGRAM REVISION: 0.08</div>	Range: 0.00 to 655.35 Revision number of faceplate program firmware.
	MESSAGE	<div>COMPILE DATE: 2000/09/08 04:55:16</div>	Range: Any valid date & time. Date and time when product firmware was built.
	MESSAGE	<div>BOOT DATE: 2000/05/11 16:41:32</div>	Range: Any valid date & time. Date and time when the boot program was built.

The shown data is illustrative only. A modification file number of 0 indicates that, currently, no modifications have been installed.

7.1.1 COMMANDS MENU



The COMMANDS menu contains directives to the relay intended to be available to operations personnel.

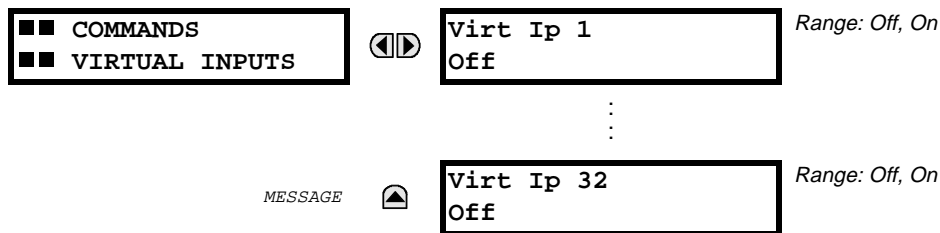
All commands can be protected from unauthorized access via the Command Password; see the Password Security menu description in the Settings \ Product Setup section.

After successfully entering any command, the following flash message will appear:

COMMAND
EXECUTED

7.1.2 VIRTUAL INPUTS

PATH: COMMANDS ↓ VIRTUAL INPUTS



The states of up to 32 virtual inputs may be changed here.

The first line of the display indicates the ID of the virtual input. The second line indicates the current or selected status of the virtual input. This status will be a logical state 'Off' (0) or 'On' (1).

7.1.3 CLEAR RECORDS

PATH: COMMANDS ↓ COMMANDS CLEAR RECORDS

COMMANDS

CLEAR RECORDS

◀▶

CLEAR FAULT REPORTS?

No

Range: No, Yes

▲▼

CLEAR EVENT RECORDS?

No

Range: No, Yes

▲▼

CLEAR OSCILLOGRAPHY?

No

Range: No, Yes

▲▼

CLEAR DATA LOGGER?

No

Range: No, Yes

▲▼

CLEAR BREAKER 1

ARCING AMPS? No

Range: No, Yes

▲

CLEAR BREAKER 2

ARCING AMPS? No

Range: No, Yes

This menu contains commands for clearing historical data such as the Event Records.

Changing a command setting to ‘Yes’ and then clicking the **ENTER** key will clear the corresponding data. The command setting will then automatically revert to ‘No’.

7.1.4 SET DATE AND TIME

PATH: COMMANDS ↓ SET DATE AND TIME

COMMANDS

SET DATE AND TIME

◀▶

SET DATE AND TIME:

2000/01/14 13:47:03

(YYYY/MM/DD HH:MM:SS)

The date and time can be entered here via the faceplate keypad, provided that the IRIG-B signal is not being used. The time setting is based on the 24-hour clock. The complete date, as a minimum, must be entered to allow execution of this command. The new time will take effect at the moment the **ENTER** key is clicked.

7.1.5 RELAY MAINTENANCE

PATH: COMMANDS ↓ RELAY MAINTENANCE

■■ COMMANDS ■■ RELAY MAINTENANCE	◀▶	PERFORM LAMPTEST? No	Range: No, Yes
	▲	UPDATE ORDER CODE? No	Range: No, Yes

This menu contains commands for relay maintenance purposes.

Changing a command setting to 'Yes' and then clicking the **ENTER** key will activate the command. The command setting will then automatically revert to 'No'.

The **PERFORM LAMPTEST** command turns on all faceplate LEDs and display pixels for a short duration.

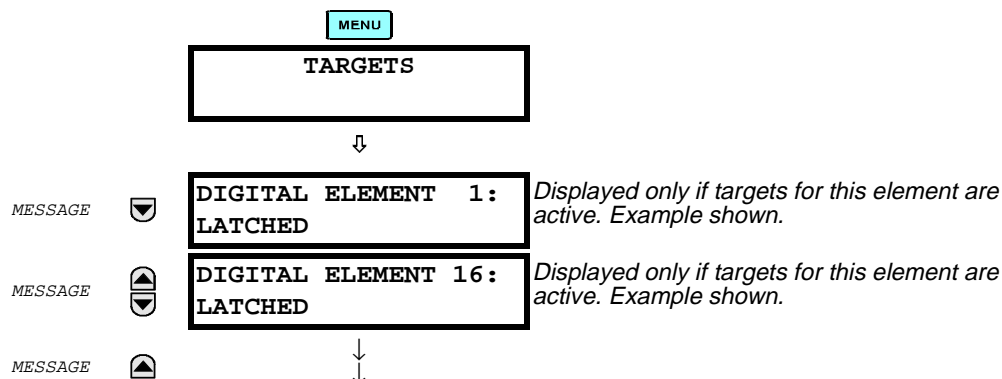
The **UPDATE ORDER CODE** command causes the relay to scan the backplane for the hardware modules and update the order code to match. If an update occurs, the following message will be shown.

UPDATING... PLEASE WAIT

There will be no impact if there have been no changes to the hardware modules. When an update does not occur, the following message will be shown.

ORDER CODE NOT UPDATED

7.2.1 TARGETS MENU



The status of any active targets will be displayed in the TARGETS menu. If no targets are active, the display will be:

No Active
Targets

a) TARGET MESSAGES

When there are no active targets, the first target to become active will cause the display to immediately default to that message. If there are active targets and the user is navigating through other messages, and when the default message timer times out (i.e. the keypad has not been used for a determined period of time), the display will again default back to the target message.

The range of variables for the target messages is described below. Phase information will be included if applicable. If a target message status changes, the status with the highest priority will be displayed.

Table 7–1: TARGET MESSAGE PRIORITY STATUS

PRIORITY	ACTIVE STATUS	DESCRIPTION
1	OP	element operated and still picked up
2	PKP	element picked up and timed out
3	LATCHED	element had operated but has dropped out

If a self test error is detected, a message appears indicating the cause of the error.

For example:

UNIT NOT PROGRAMMED
:Self Test Error

7.2.2 RELAY SELF-TESTS

The relay performs a number of self-test diagnostic checks to ensure device integrity. There are two types of self-tests, major and minor, which are listed in the tables below. When either type of self-test error has occurred the TROUBLE indicator will be on and a target message will be displayed. All errors record an event in the event recorder. Latched errors can be cleared by pressing the RESET key, providing the condition is no longer present.

Major self-test errors also result in the following:

- the critical fail relay on the power supply module is de-energized
- all other output relays are de-energized and are prevented from further operation
- the faceplate IN SERVICE indicator is turned off
- a RELAY OUT OF SERVICE event is recorded

Table 7–2: MAJOR SELF-TEST ERROR MESSAGES

SELF-TEST ERROR MESSAGE	LATCHED TARGET MSG	DESCRIPTION OF PROBLEM	WHAT TO DO
UNIT NOT PROGRAMMED	No	PRODUCT SETUP \ INSTALLATION setting indicates relay is not in a programmed state.	Program all settings (especially those under PRODUCT SETUP \ INSTALLATION).
EQUIPMENT MISMATCH with 2nd-line detail message	No	Configuration of modules does not match the order code stored in the CPU.	Check all module types against the order code; make sure they are inserted properly, and cycle the control power (if problem persists, contact the factory).
UNIT NOT CALIBRATED	No	Settings indicate the unit is not calibrated.	Contact the factory.
FLEXLOGIC ERR TOKEN with 2nd-line detail message	No	FlexLogic equations do not compile properly.	Finish all equation editing and use self test to debug any errors.
DSP ERRORS: A/D RESET FAILURE A/D CAL FAILURE A/D INT. MISSING A/D VOLT REF. FAIL NO DSP INTERRUPTS DSP CHECKSUM FAILED DSP FAILED	Yes	CT/VT module with digital signal processor may have a problem.	Cycle the control power (if the problem recurs, contact the factory).
FLASH PROGRAMMING	No	Firmware is being upgraded into flash memory.	Do not cycle power. Allow the upgrade to complete.
PROGRAM MEMORY Test Failed	Yes	Error was found while checking Flash memory.	Contact the factory.

Table 7–3: MINOR SELF-TEST ERROR MESSAGES

SELF-TEST ERROR MESSAGE	LATCHED TARGET MSG	DESCRIPTION OF PROBLEM	WHAT TO DO
EEPROM CORRUPTED	Yes	The non-volatile memory has been corrupted.	Contact the factory.
IRIG-B FAILURE	No	Bad IRIG-B input signal.	<ul style="list-style-type: none"> • Check to ensure that the IRIG-B cable is connected to the relay. • Check the functionality of the cable (i.e. look for physical damage or perform a continuity test). • Check to ensure the IRIG-B receiver is functioning properly. • Check the input signal level; it may be lower than specification. If none of the above items apply, contact the factory.
PRIM ETHERNET FAIL	No	Primary Ethernet connection failed	Check connections.
SEC ETHERNET FAIL	No	Secondary Ethernet connection failed	Check connections.
BATTERY FAIL	No	Battery is not functioning.	Replace the battery.
PROTOTYPE FIRMWARE	Yes	A prototype version of the firmware is loaded.	Contact the factory.
SYSTEM EXCEPTION	Yes	System discrepancy detected.	Contact the factory.
LOW ON MEMORY	Yes	Memory is close to 100% capacity	Contact the factory.
WATCHDOG ERROR	No	Some tasks are behind schedule	Contact the factory.
REMOTE DEVICE OFFLINE	Yes	One or more GOOSE devices are not responding	Check GOOSE setup

8.1.1 INTRODUCTION

Phase comparison relaying is a kind of differential relaying that compares the phase angles of currents entering one terminal of a transmission line with the phase angles of the currents entering all remote terminals of the same line. For the conditions of a fault within the protected zone (internal fault), the currents entering all the terminals will be in phase. For conditions of a fault outside the zone of protection (external or through fault), or for load flow, the currents entering any one terminal will be 180° out of phase with the currents entering at least one of the remote terminals. The phase comparison relay scheme makes this phase angle comparison and trips the associated breakers for internal faults. Since the terminals of a transmission line are normally many miles apart, some sort of communication channel between the terminals is required to make this comparison.

8.1.2 FUNDAMENTAL PRINCIPLE OF PHASE COMPARISON

The basic operation of a phase comparison scheme requires that the phase angle of two or more currents be compared with each other. In the case of transmission line protection, these currents may originate many miles from each other so, as noted above, some form of communication channel is required as part of the scheme.

If a two-terminal line is considered (see Figure 8–1 below), the relays located at terminal A can measure the current at that terminal directly. The phase angle of the current at the remote terminal (B) must somehow be communicated to terminal A. Since the current sine wave is positive for $\frac{1}{2}$ -cycle and then negative for the next $\frac{1}{2}$ -cycle, it may be used to key a transmitter first to a MARK signal for a half cycle and then to a SPACE signal for the next half cycle for as long as the current is present. Such a signal transmitted at B and received at A can be compared with the current at A to determine whether the two quantities are in phase or out of phase with each other. Conversely, the current at terminal B may be compared with the signal received from terminal A.

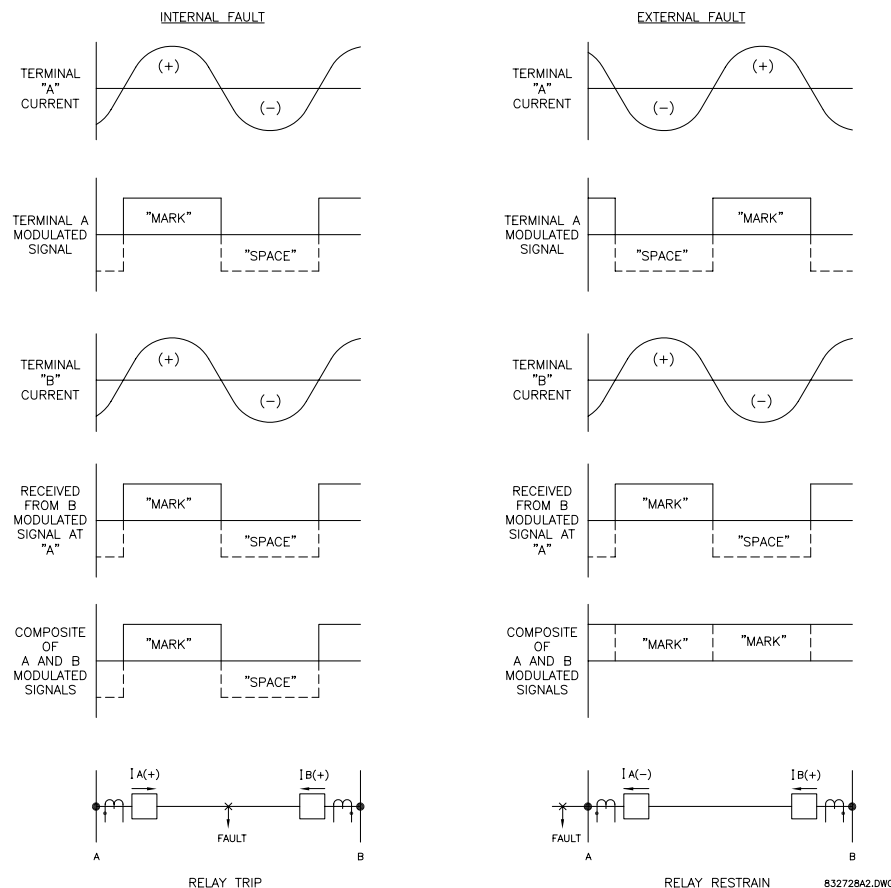


Figure 8–1: PHASE ANGLE COMPARISON

It becomes apparent that a comparison such as that described above must be made on a single phase basis. That is, it would not be possible to compare all three phase currents at terminal A individually with all three at terminal B over one single channel and one single comparing unit. However, to reduce communications channel requirements, all three phase currents are mixed to produce a single phase quantity whose magnitude and phase angle have a definite relation to the magnitude and phase angle of the three original currents. It is this single phase quantity that is phase compared with a similarly obtained quantity at the remote end(s) of the line.

While there are many variations on the basic scheme (these are discussed subsequently), the general method employed to compare the phase angle or phase position of the currents is always the same. The left side of Figure 8–1 illustrates the conditions for a fault internal to the protected zone. The sketches show about 1 cycle of the currents under internal and external faults to represent relay 'A' trip logic.

The MARK-SPACE designations given to the received signal are for identification and have no special significance. If the communication equipment happened to be a simple radio frequency transmitter-receiver, and if the positive half cycle of current keyed the transmitter to ON, then the MARK block corresponds to a received remote signal while the SPACE block corresponds to no signal. Conversely, if the negative portion of the current wave keyed the transmitter to ON, then the SPACE block would represent the received signal.

With a frequency-shift transmitter-receiver as the communication equipment, the MARK block would represent the receipt of the hi-shift frequency and the SPACE block the low-shift frequency if the remote transmitter was keyed to high from a positive current signal. The converse would be true if the transmitter was keyed to high from a negative current signal. In any case the MARK block received at A, whatever it represents, corresponds to positive current at B while the SPACE block corresponds to negative current at B.

If we consider an internal fault (as shown on the left side of Figure 8–1), the relay at A would be comparing modulated quantities illustrated in the sketches. If these two signals at terminal A were to be compared as shown in Figure 8–2A over a frequency-shift equipment, a trip output would occur if positive current and a receiver MARK signal were both concurrently and continuously present for at least one-half cycle (8.33 ms at 60 Hz or 10 ms at 50 Hz). The trip output would be continued for 18 ms to ride over the following half cycle during which the current is negative, and the half cycle after that when the pick-up timing takes place again.

Assuming that the MARK and SPACE signals cannot both be present concurrently then it might be argued that a comparison could be made between the positive half cycle of current and the absence of a receiver SPACE output. Figure 8–2B illustrates this logic.

If the communication equipment happened to be a frequency shift channel so that both the MARK and the SPACE signals were definite outputs, Figure 8–2B would represent a tripping scheme since tripping is predicated on the receipt of a remote MARK or tripping signal. On the other hand, Figure 8–2B would represent a blocking scheme in as much as it will block tripping in the presence of a MARK or blocking signal. It will trip only in the absence of this signal.

The right side of Figure 8–1 illustrates the conditions during an external fault. Referring to Figures 8–2A and 8–2B, neither approach, the blocking or the tripping, will result in a trip output for this condition since the AND circuits will never produce any outputs to the integrator.

The conditions illustrated in Figure 8–1 are ideal. They seldom, if ever, occur in a real power system. Actually, an internal fault would not produce a received signal MARK-SPACE relationship that is exactly in phase with the locally contrived single phase current. This is true for a variety of reasons including the following:

1. Current transformer saturation.
2. Phase angle differences between the currents entering both ends of the line as a result of phase angle differences in the driving system voltages.
3. Load and charging currents of the line.
4. Transit time of the communication signal.
5. Unsymmetrical build-up and tail-off times of the receiver.

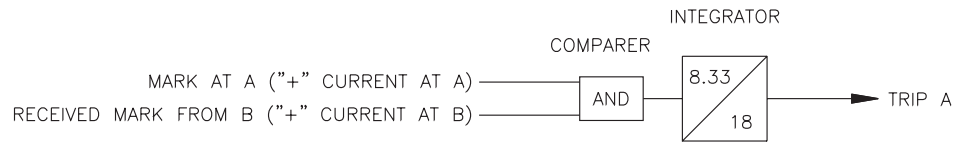


FIGURE 2A

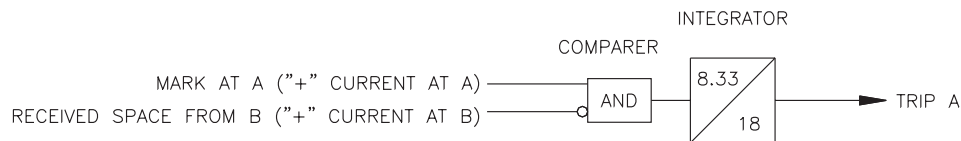


FIGURE 2B

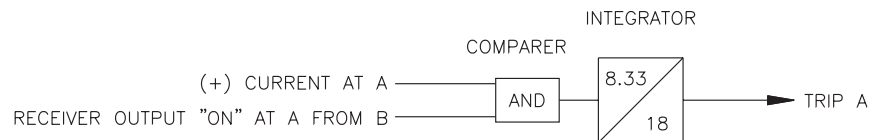


FIGURE 2C

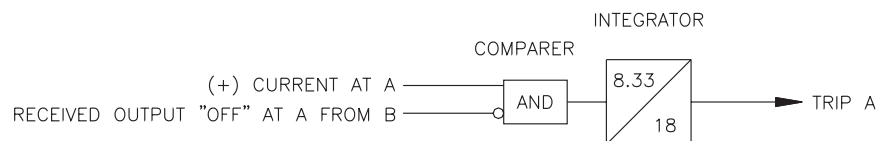


FIGURE 2D

832008A2.DWG

Figure 8–2: 2-TERMINAL LINE PHASE COMPARISON

Thus, the logic shown in Figures 8–2A and 8–2B would rarely, if ever, produce a trip output on an internal fault because the 8.33 ms (which is the time of a half cycle on a 60 Hz base) requires perfect matching. In actual practice a 3 to 4 ms setting is used rather than the 8.33 setting illustrated. This makes it much easier to trip on internal faults. It also makes it much easier to trip undesirably on external faults. However, experience has indicated that with proper settings and adjustments in the relay such a timer setting offers an excellent compromise. This may be better appreciated if it is recognized that item (a) above is generally minimized and item (b) is nonexistent on external faults.

As shown in Figure 8–3: STABILITY ANGLE, a stability angle setting of 3 ms for a 60 Hz system allows for about 65 electrical degrees of blocking zone. This provides sufficient security to prevent tripping in the cases indicated above and provides reliable tripping for all types of internal faults.

In the event that ON-OFF communication equipment were to be employed rather than frequency-shift equipment, the logic would appear as in Figures 8–2C and 8–2D. It will be noted in these two Figures that the reference to MARK and SPACE have been conveniently omitted since the receiver output is either present or not as against the case of the frequency-shift equipment where it could be there in either of two states. Figure 8–2C illustrates a tripping scheme while Figure 8–2D a blocking scheme. Here again, the integrator is, in practice, actually set for 3 to 4 ms.

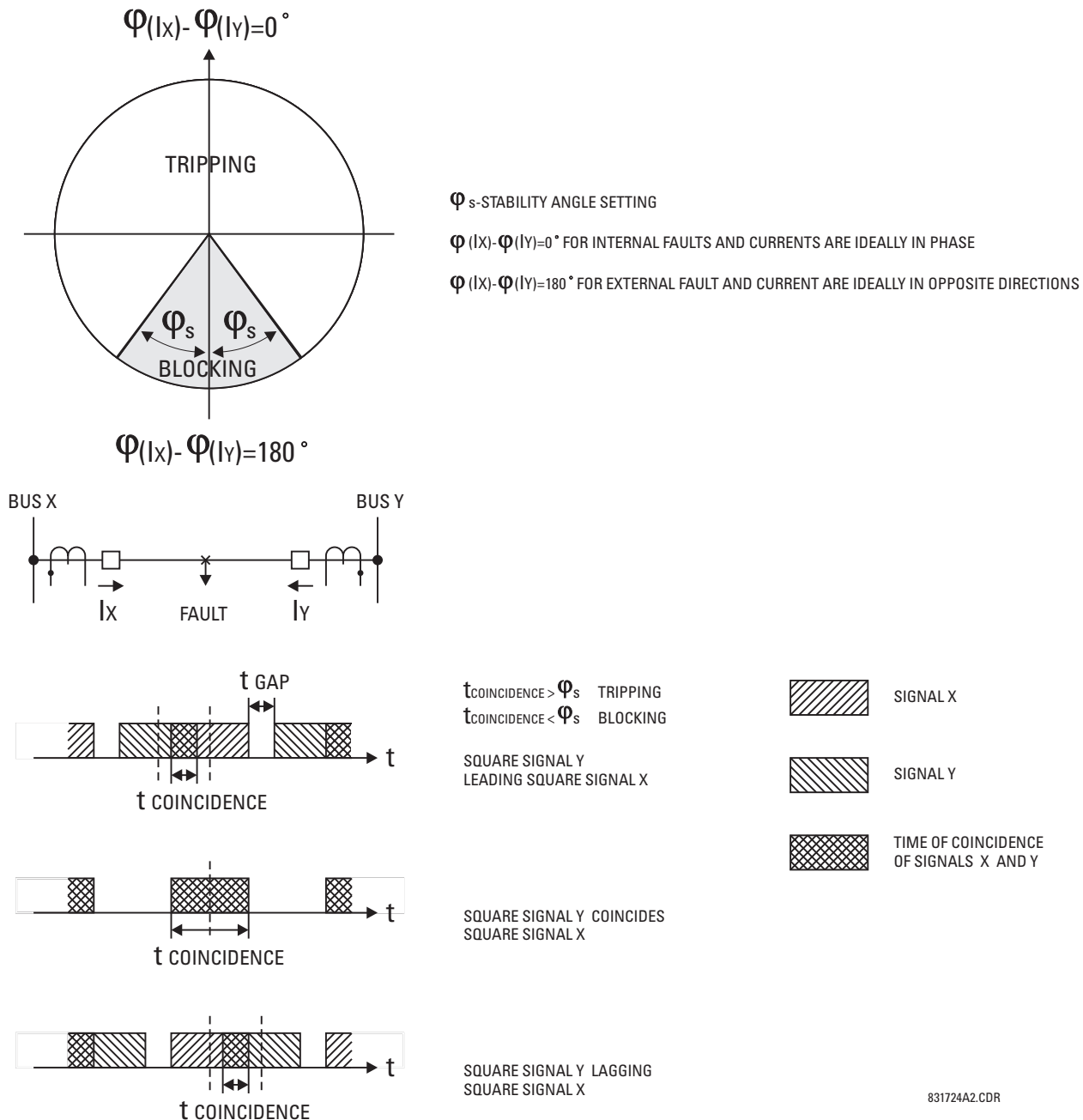


Figure 8-3: STABILITY ANGLE

Figures 8-4A, 8-4B, 8-4C, and 8-4D are for three-terminal lines and they correspond directly to Figures 8-2A, 8-2B, 8-2C, and 8-2D. It will be noted from Figure 8-3 that for a three-terminal line, the relay at A must receive information from both the remote terminals. The same applies to the relays at terminals B and C. As in the case of the two-terminal lines, the integrator illustrated in Figure 8-4 will actually be set for 3 to 4 ms.



FIGURE 3A



FIGURE 3B

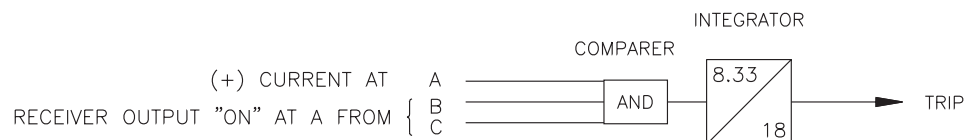


FIGURE 3C

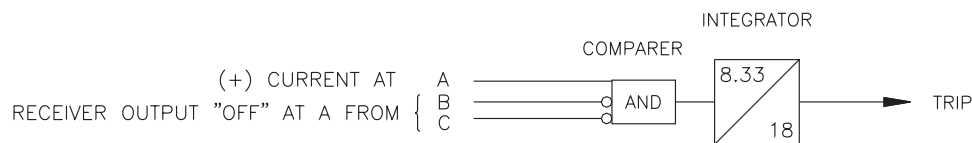


FIGURE 3D

832009A3.DWG

Figure 8–4: 3-TERMINAL LINE PHASE COMPARISON

While all the sketches in Figures 8–2 and 8–4 compare the positive half cycle of current with a receiver output, the negative half cycle might just as well have been selected. However, if this were done, in Figure 8–2A for example, it would have been necessary to compare the presence of negative current with a received SPACE signal rather than a MARK signal.

It should be recognized that the above discussion, as well as Figures 8–1 and 8–2, are rudimentary. The complete phase comparison scheme is considerably more sophisticated and will be discussed in more detail subsequently. However, at this point it would be well to note that phase comparison on a continuous basis is not permitted mainly because it would tend to reduce the security of the scheme. For this reason, fault detectors are provided. They initiate phase comparison only when a fault occurs on, or in the general vicinity of, the protected line. A simplified sketch of the logic of a phase comparison blocking scheme including fault detectors is illustrated in Figure 8–5. This is a somewhat more fully developed version of Figure 8–2D, and the same logic is present at both ends of a two-terminal line.

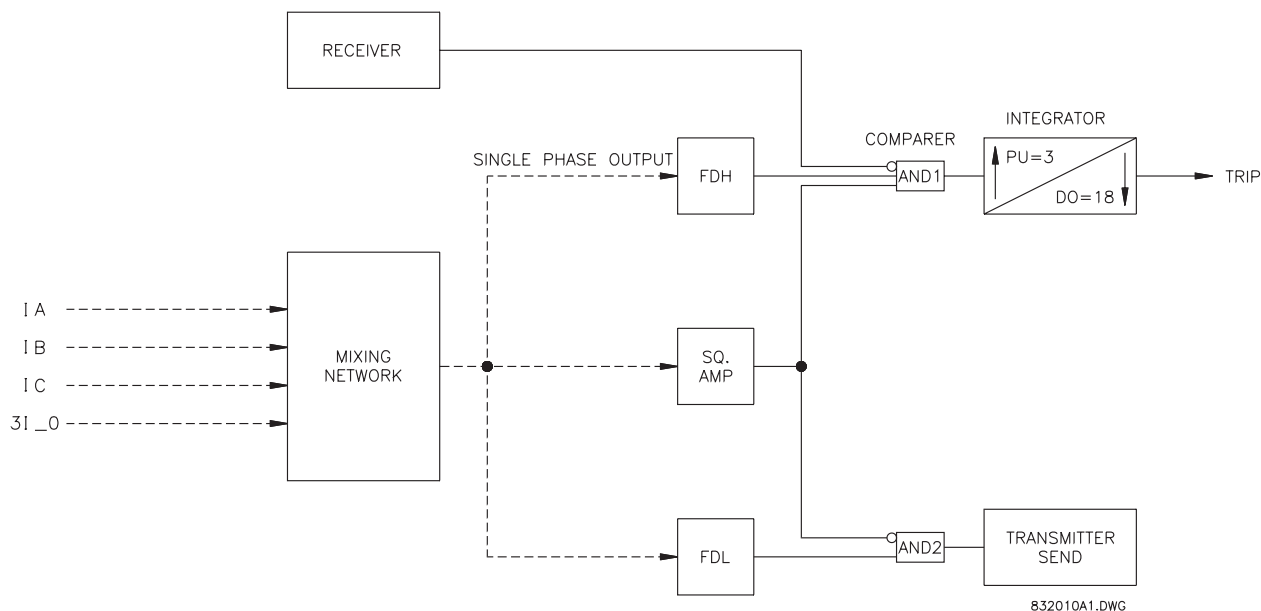


Figure 8–5: SINGLE PHASE COMPARISON BLOCKING SCHEME PRINCIPLE

It will be noted from Figure 8–5 that AND1 (the comparer) at each end of the line compares the coincidence time of the positive half cycle of current with the absence of receiver output. This is initiated only when a fault is present as indicated by an output from FDH (Fault Detector High-set). FDH is set so that it does not pick up on load current but does pick up for all faults on the protected line section. Thus, when a fault occurs, FDH picks up, and if the receiver output is not present for 3 milliseconds during the positive half cycle of current out of the mixing network, a trip output will be obtained.

Of course, the output from the receiver will depend on the keying of the remote transmitter. The transmitters at all line terminals are keyed in the same manner. They are keyed ON by an output from FDL (Fault Detector Low-set) and keyed OFF by the squaring amplifier via AND2 during the positive half cycles of current. The FDL function is required at all terminals in all phase comparison blocking schemes to initiate a blocking signal from the associated transmitter. This is received at the remote receiver and blocks tripping via the comparer during external faults. FDL has a more sensitive setting and therefore operates faster than the remote FDH function. It is obvious from Figure 8–4 that if an external fault occurred, and FDL did not operate at least as fast as the remote FDH, false tripping could occur because of the lack of receiver output. In general FDL is set so as not to pick up on load current but still with a lower pick up than FDH so that it will operate before FDH. For an internal fault, the currents entering both ends of the line are in phase with each other. Thus, during the half cycle that the SQ AMP is providing an input to AND1, the associated receiver is producing no output, and so tripping will take place at both ends of the line.

For an external fault, the current entering one terminal is 180° out of phase with the current entering the other terminal. Under these conditions, during the half cycles when the SQ AMP is producing outputs, the associated receiver is also providing an output thus preventing an AND1 output. No tripping will take place.

8.1.3 VARIATIONS IN PHASE COMPARISON SCHEMES

There are a number of different phase comparison schemes in general use today and while all of these employ the same basic means of comparison described above, significant differences do exist. These differences relate to the following:

- Phase comparison excitation (component or current to be compared).
- Pure phase comparison vs. combined phase and directional comparison.
- Blocking vs. tripping schemes.
- Single vs. dual phase comparison.

8.1.4 PHASE COMPARISON EXCITATION

Before discussing this subject, it is well to consider what takes place in terms of the currents that are available for comparison when a fault occurs on a power system. The table below lists the sequence components of fault current that are present during the various different kinds of faults while Figure 8–6 illustrates the relative phase positions of the sequence components of fault current for the different kinds of faults and the different phases involved.

Table 8–1: FAULT TYPES

TYPE OF FAULT	SEQUENCE COMPONENTS		
	POSITIVE	NEGATIVE	ZERO
Single-Phase-to-Ground	yes	yes	yes
Phase-to-Phase	yes	yes	no
Double-Phase-to-Ground	yes	yes	yes
Three-Phase	yes	no	no

Figure 8–6 shows the relative phase positions of the outputs of a positive sequence network, a negative sequence network, and a zero sequence network all referenced to phase A. The transfer functions of these three networks are given by the following equations.

$$I_1 = \frac{1}{3}(I_a + I_b \angle 120^\circ + I_c \angle -120^\circ)$$

$$I_2 = \frac{1}{3}(I_a + I_b \angle -120^\circ + I_c \angle 120^\circ)$$

$$I_3 = \frac{1}{3}(I_a + I_b + I_c)$$

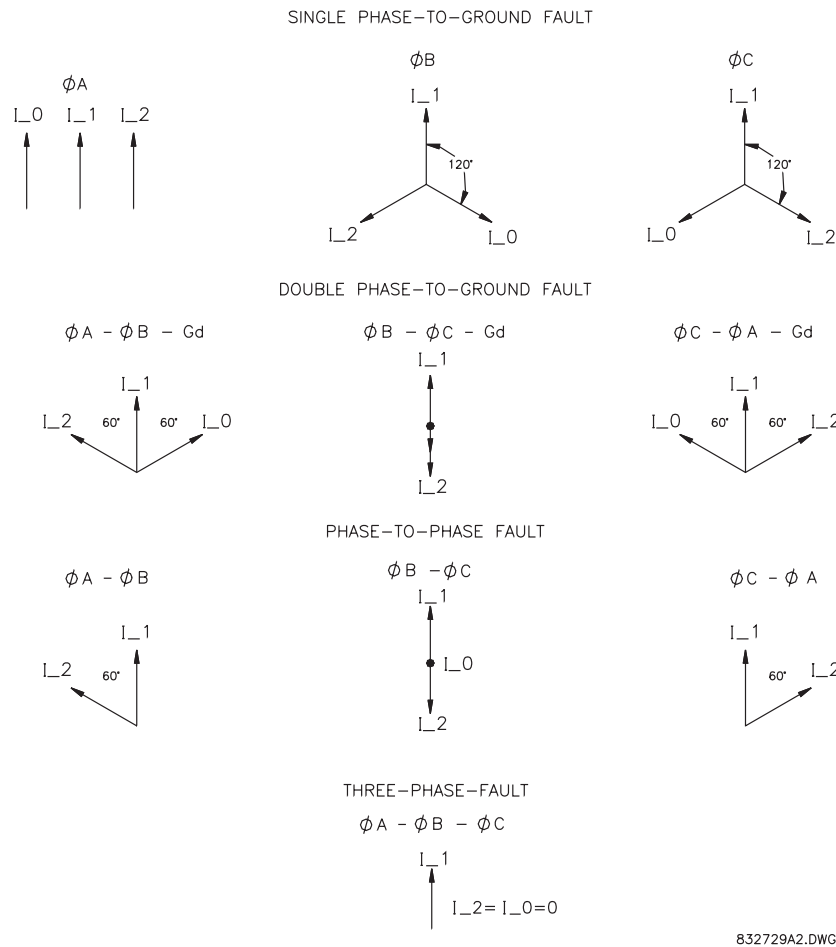


Figure 8-6: SEQUENCE NETWORK OUTPUTS

It is interesting to note that the phase positions of the sequence network outputs differ depending on the phase or phases that are faulted as well as the type of fault. For example, while the positive, negative, and zero sequence components are all in phase for a single-phase-A-to-ground fault, they are 120° out of phase with each other for phase-B-to-ground, and phase-C-to-ground faults.

It will be observed from Table 8-1 that positive sequence currents are available for all kinds of faults, negative sequence currents are available for all but three-phase faults, and zero sequence currents are available only for faults involving ground. Thus, it appears that if one single sequence component of current were to be selected for use to make the phase comparison, the positive sequence component would suffice. Actually, this is not the case in many if not most of the applications because of the presence of through load current during the fault.

For a single-phase-to-ground fault on the protected line, the positive sequence component of fault current entering one end will be in phase with that entering the other end. This is a tripping situation for the phase comparison scheme. However, any load flow across the line during the fault will produce a positive sequence component of load current entering one end of the line that is 180° out of phase with that entering the other end (That is, the positive sequence component of load current entering one end is in phase with that leaving the other end). This is a non-tripping situation for the phase comparison scheme. The phase position of the load component relative to the fault component depends on such factors as the direction of the load flow, power factor of the load flow, and the phase angles of the system impedances. The phase position of the “net” (load plus fault) positive sequence current entering one end of the line relative to that entering the other end will depend on these same factors plus the relative magnitude of the fault and load components of current.

In general, the heavier the fault current and the lighter the load current, the more suitable is the use of pure positive sequence for phase comparison. Heavier line loadings and lower fault currents will tend to make the scheme less apt to function properly for internal faults. Thus, pure positive sequence phase comparison appears practical only in a minority of the cases and so is not suitable for a scheme that is to be generally applicable.

Significant negative sequence currents are present only during faults, they are present in all but balanced three phase faults, and there is no significant negative sequence component of load current. All this combines to make pure negative sequence ideal for phase comparison except that it will not operate for balanced three phase faults. Similar comments may be made regarding pure zero sequence phase comparison with the additional limitation that it will not operate for phase-to-phase faults. Thus, there does not appear to be one single sequence component or one single phase current that could be used in a phase comparison scheme to protect against all types of faults.

There are a number of different approaches that are possible to provide a complete scheme. Probably, the most obvious would be to make the phase comparison on each phase separately. This is undesirable principally because the cost would be high since three communication channels would be required. Another approach would be to use two separate phase comparison measurements and communication channels, one for pure positive and the other for pure negative sequence currents. The latter would serve to protect against all unbalanced faults while the former would take care of three phase faults and also provide a measure of back-up protection for heavy unbalanced faults. Here again cost is an important factor.

As soon as consideration is given to the use of a separate positive and a separate negative phase sequence comparison, the idea of switching from one to the other presents itself. Such schemes are available. They include detectors separate from the phase comparison function that distinguish between three phase faults and all other types. For three phase faults the negative sequence network is unbalanced so that it produces an output for positive sequence current as well as for negative sequence current. The scheme operates normally to provide negative sequence phase comparison for all unbalanced faults. When a three phase fault occurs, the three-phase detectors at both ends of the line operate to automatically unbalance their respective negative sequence networks and make them sensitive to positive as well as negative sequence currents. Since the fault is three phase, there is no negative sequence current produced so the phase comparison is made on a pure positive sequence basis. This is all accomplished with a common communication channel for both modes.

Another similar approach would be to provide two separate sequence networks, one pure positive sequence and the other pure negative sequence. Then use the three-phase detector to switch the logic so that only for three phase faults the outputs of the positive sequence networks at both ends of the line are compared but for all other faults the negative sequence outputs are compared. Here again all this being accomplished over a common channel. This approach has never been used possibly because of the idea of using "Mixed Excitation." Mixed Excitation is a term used to describe a phase comparison scheme that mixes the outputs of the different sequence networks in a given proportion and phase angle and then makes a phase comparison for all faults based on this mix. Thus, all such schemes must include positive sequence plus negative sequence and/or zero sequence in order to operate for all faults. The two main questions to be resolved are:

1. Which sequence components should be mixed with the positive sequence?
2. What percentages of the full magnitude of each sequence component of current should be used?

Figure 8-7 illustrates a two-terminal line with an internal phase B-to-ground fault. The phasor diagrams indicate the phase positions of the sequence currents at both ends of the line assuming current flow into the line and also assuming a phase A reference as in equations (1), (2), and (3), previously shown.

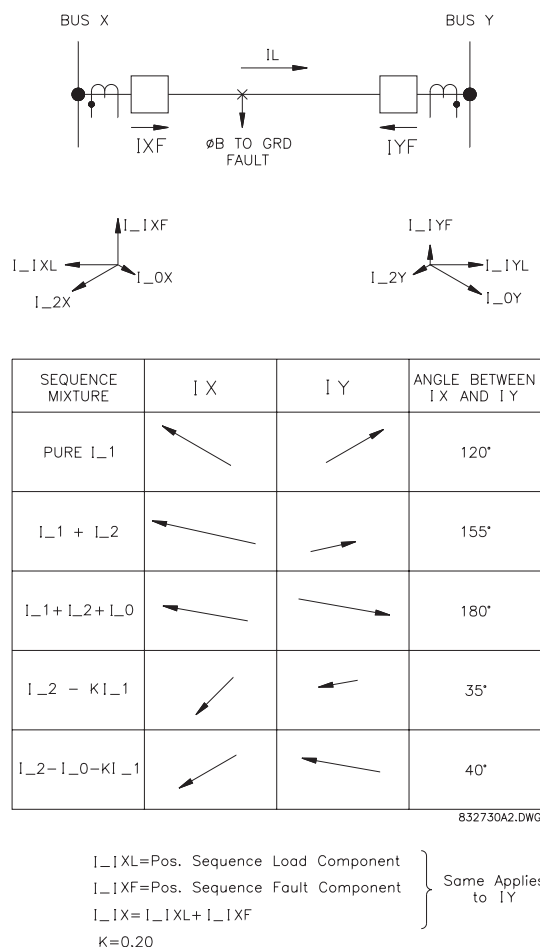


Figure 8-7: VECTOR RELATIONSHIPS IN A 2-TERMINAL FAULTED LINE (B-to-G)

At this point it should be recognized that the positive sequence component of current is made up of two parts, the load component (I_{1L}) and the fault component (I_{1F}). By an analysis utilizing superposition, the load component (I_{1L}) may be established as the current flowing just prior to the fault. The three fault components of current (I_{1F}, I_{2F}, and I_{0F}) are then calculated using the voltage that existed at the point of fault just prior to the fault. Since the load component of current is equal to the vector difference between Bus X and Bus Y voltages divided by the impedance of the line, and since the prefault voltage (at the point of fault) has a phase position somewhere between that of X and Y voltages, the positive sequence component of fault current will be displaced from the load component by about 90° ± about 30°. The phasor diagrams at the top of Figure 8-7 assume that load current flow is from bus X to bus Y.

The first row of the table in Figure 8-7 indicates that for the conditions assumed, the net positive sequence current entering both ends of the line are about 120° displaced from each other. Heavier fault current and lighter load current would reduce this angle toward zero while the converse would increase the angle toward 180°.

The second and third rows of the table of Figure 8-7 indicate the relative phase positions of the positive plus negative, and positive plus negative plus zero sequence components respectively. These appear to be more unsatisfactory. Rows 4 and 5 combine the components differently and both appear to yield much better results.

It is obvious from Figure 8-6, that a similar fault on a different phase would yield different results. This is illustrated in Figure 8-8 where a phase-A-to-ground fault at the same location is analyzed. As noted earlier, the integrator timers in phase comparison schemes are generally set for about 3 milliseconds. This will permit trip-

ping on internal faults with as much as 115° between the phase angles of the currents entering both ends of the lines. On this basis, only excitation by $I_2 - (0.20) \times I_1$ would prove satisfactory for the two cases studied in Figures 8–7 and 8–8.

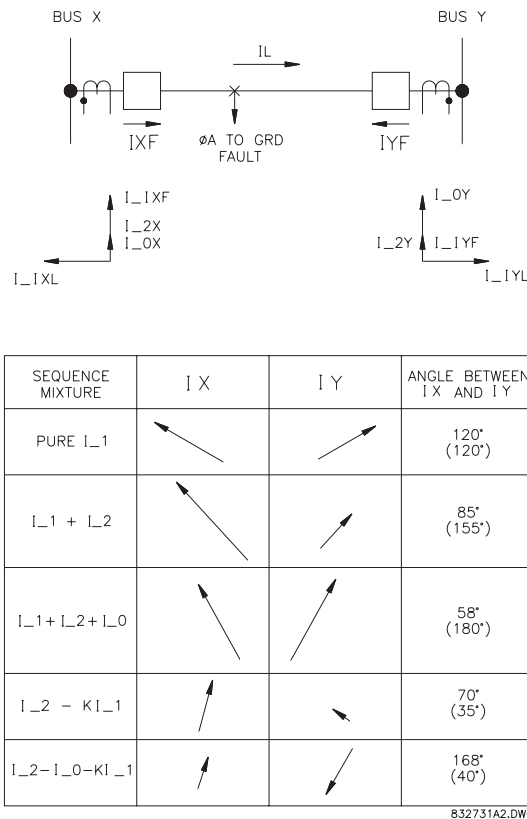


Figure 8–8: VECTOR RELATIONSHIPS IN A 2-TERMINAL FAULTED LINE (A-to-G)

Actually, only two simple faults were investigated. It is obvious that different results would have been obtained for these same kind of faults if the relative magnitudes of load current, positive sequence fault current, and zero sequence fault current had been assumed differently. Also, for the values of currents assumed, different results would obtain for other types of faults. In addition, if different combinations and weighting factors of the sequence components had been investigated still different answers would have resulted. In the proper selection of sequence components and weighting factors for Mixed Excitation phase comparison, the following points must be considered:

- Whatever combination and weighting factors are employed, the application rules should be simple enough to make the application practical.
- As a corollary to the above point, the fewest number of sequence components should be used.
- The effects of load current must be minimized. Thus, negative and/or zero sequence components should be weighted over the positive sequence components.
- The limits of application should be broad enough to render the scheme useful as a protection tool.

In line with the considerations stipulated above, the best overall results using mixed excitation would be attained by using $I_2 - KI_1$, where K is a constant that is adjustable within limits. While it is likely that the inclusion of zero sequence excitation would be helpful for one case or another, it is not generally employed because the problem of evaluating the overall performance of the scheme would be magnified considerably. This is true mainly because the current distribution in the zero sequence network is generally quite different from that in the positive and negative sequence networks where the current distributions are approximately the

same. For any given fault on a transmission line, the ratio of I_{1F} / I_{2F} at any terminal is the same as at any other terminal of that line. This is not true of either I_{1F} / I_{0F} or I_{2F} / I_{0F} . It is this that makes the use of zero sequence excitation undesirable.

a) MIXED EXCITATION PHASE COMPARISON

If the mixing network of Figure 8–5 were designed to produce an output that is proportional to $I_2 - KI_1$, this logic would then be a simplified representation of a mixed excitation phase comparison scheme. In such schemes, the pick up setting of FDH must be high enough so that the KI_1 output from the mixing network does not result in continuous phase comparison on load current (I_2 is normally zero during normal system conditions). Also, it may be desirable to have FDL set to pick-up at some level above full load so that channel is not keyed on and off continuously during normal load conditions. Since FDH is set higher than FDL, this requirement results in a still higher setting for FDH.

Because FDH controls tripping, this arrangement limits the applicability of the basic scheme to circuits where the minimum three phase fault current is significantly higher than the maximum load current.

The requirements for the satisfactory performance of a mixed excitation scheme using overcurrent fault detectors (FDH and FDL) are:

- Both the FDL and FDH fault detectors must be set above full load current.
- All internal faults regardless of type or the particular phases involved must produce enough $I_2 - KI_1$ to operate FDH at all ends of the line.
- FDL must be set with a lower pick-up than FDH at the remote end(s) of the line for security during external faults.
- The phase angle difference between the $I_2 - KI_1$ quantities obtained at all terminals of the protected line during all types of internal faults, and for any combination of phases, must be less than 115° .

b) ZERO SEQUENCE EXCITATION

With zero sequence excitation the phase comparison portion of the overall scheme would not be capable of operating for phase-to-phase and three-phase faults. For this reason the overall protective scheme must include measurement functions that can detect and operate for faults involving any two or more phases. Mho type phase distance functions have typically been employed for this protection.

It should be noted that distance relays designed to operate for faults involving two or more phases will operate for double-phase-to-ground faults and also for certain close-in single-phase-to-ground faults. Thus, it is reasonable to expect that both the phase comparison and distance protection will be activated for many faults.

c) NEGATIVE SEQUENCE EXCITATION

Since negative sequence phase comparison will protect against all unbalanced faults, the directional comparison functions are required only for three-phase fault protection. However, if these functions are designed to respond to all multi phase faults, then phase-to-phase and double phase-to-ground faults, will be protected by both modes while single-phase-to-ground faults will be protected by only the phase comparison mode, and three phase faults by only the directional comparison mode.

8.1.5 BLOCKING VS. TRIPPING SCHEMES

Earlier discussion in conjunction with Figure 8-2 provides a basis for further consideration of blocking vs. tripping pilot schemes. Figure 8-2C illustrates the comparator integrator logic for a tripping scheme using an ON-OFF type of pilot channel. In order to trip, a receiver output is required to be present during the half cycle that the local current is positive. Figure 8-2D is representative of a blocking pilot scheme where tripping will take place if there is no receiver output during the half cycle that the local current is positive.

If we consider that an input to, or an output from, a logic box is a positive going signal, the logic illustrated in Figures 8-2A and 2C assume that a received signal at the input of a receiver will produce a positive going voltage signal at the output of the receiver to the relay logic. This is not always true. Some types of receivers will produce negative (or reference) voltage outputs when a signal is present at the input, and a positive signal output when nothing is received. If this were the situation in Figure 8-2, Figure 8-2B would then represent a blocking scheme. In some applications where receiver outputs are inverted, the interface between the receiver and the relay logic includes an inverter (INV) which in effect inverts the receiver output signal so that a received signal produces a positive going signal at the output of the inverter. The same general statements regarding signal polarities applies to the keying requirements for transmitters. Some transmitters may require a positive signal while others a reference or negative signal to key them off of their quiescent states.

The main point to be gained from the foregoing discussion is that it is not always possible to determine from a logic diagram whether a scheme is of the blocking or tripping type unless an indication is given as to the receiver output voltages. This applies to frequency shift as well as ON-OFF communication equipment.

It will become apparent from subsequent discussion that it is extremely difficult, if not impossible, to provide a concise rigorous definition of the terms Blocking Scheme and Tripping Scheme. Possibly it would be well to proceed with a discussion of the different kinds of channels, their characteristics, and their application before attempting a definition.

a) TYPE OF CHANNELS

The total channel is composed of the communication equipment itself plus the path or link over which the signal is sent. For relaying purposes there are two basic types of communication equipment.

1. ON-OFF
2. Frequency-shift

The ON-OFF type, as the name implies, operates with the transmitter either being keyed on or off by the relay logic. That is, the transmitter at any given instant is either sending an unmodulated signal or it is sending nothing.

There are two types of frequency-shift equipment. The most prevalent is the two-frequency kind. With this type, the transmitter can send either of two closely spaced frequencies. When no keying signal is applied to the transmitter, it sends one of these two frequencies. When the transmitter is keyed, it shifts to the other frequency. It is always sending one or the other. The frequency-shift receiver has two separate outputs, one for each of the two transmitted signal frequencies. Thus, if the transmitter is sending the MARK frequency, the MARK output is present in the receiver. If the transmitter is sending the SPACE frequency, the receiver SPACE output is present. These types of receivers are basically FM receivers and utilize discriminators. Because of this, the SPACE and MARK outputs from the receiver cannot both be present simultaneously. Also, broad band noise at the input to the receiver tends to provide a balanced signal to the discriminator which forces its output towards zero. If the noise is severe enough to swamp out the real signal, it can cause random receiver output or all output to disappear.

The other kind of frequency-shift equipment is a three-frequency type. When this type of transmitter is in its quiescent state, it sends the center frequency. It has two separate keying inputs so that it can be keyed to shift high or low (MARK or SPACE) from the center frequency. The three-frequency receiver receives all three frequencies but provides only two outputs to the relay logic, the high shift and low shift outputs. When the receiver

receives the center frequency neither the high nor low outputs are present. Here again the MARK and SPACE outputs (high and low) cannot both be present simultaneously, and severe broad band noise at the receiver inputs can result in receiver output.

There are several characteristics of communication equipment directly related to phase comparison relaying performance that might well be discussed. Phase comparison types of schemes compare the phase angle of a current derived at one end of a line with a communication signal received from the remote end. The communication signal arrives in a MARK-SPACE arrangement that should represent the positive and negative half cycles of current at the transmitted end of the line. Actually this is not possible for several reasons:

1. There is a time lag from the instant a transmitter is keyed until the output reflects a change. This build up is generally a very short time and is usually insignificant.
2. There is the propagation time from the instant the transmitter sends until this signal arrives at the remote location, approximately 1 millisecond for every 290 km (180 miles) of distance. The same applies from the instant the transmitter stops until the remote signal is gone.
3. There is the build up time in the receiver from the instant the signal appears at its input until the output reflects the change of state. This time plus the build up time in the transmitter is called the channel operating time.
4. There is the tail off time in the transmitter from the instant the keying is removed until the output signal changes or disappears. This is generally very short and is usually insignificant.
5. There is the tail off time in the receiver from the instant the input changes until the output changes accordingly. This time plus the tail off time of the transmitter is called the channel release time.
6. In ON-OFF channels the operating and release times are not generally the same. They can vary with frequency and attenuation.
7. In frequency-shift channels the discriminator employed in the receiver can be balanced so that build up and tail off times are equal, or it can be unbalanced (biased) to the MARK or SPACE side. For example, if it is biased toward MARK and the input signal is symmetrical (half cycle MARK and half cycle SPACE), the output will be more than a half cycle MARK and less than a half cycle SPACE.
8. In general wide band channels tend to operate and release faster than narrow band channels. That is, faster channels use more spectrum than slower channels.

It is obvious from the foregoing that the received signal at any given terminal is not an exact analog of the remote current. There are techniques used in phase comparison schemes to compensate for this and they will be discussed subsequently. Until then it should be assumed that the received signal provides a true representation of the phase position of the remote current.

b) TYPES OF COMMUNICATION MEDIA

The communication medium over which the transmitted signal is propagated to the remote receiver can take several forms:

1. Directly over the power line (Power Line Carrier)
2. Multiplexed over the power line (Single Side Band Carrier)
3. Multiplexed over microwave (Microwave)
4. Pair of Wires (Pilot Wire)
5. Leased Facilities:
 - (a) Metallic pilot wire
 - (b) Microwave
 - (c) Cable

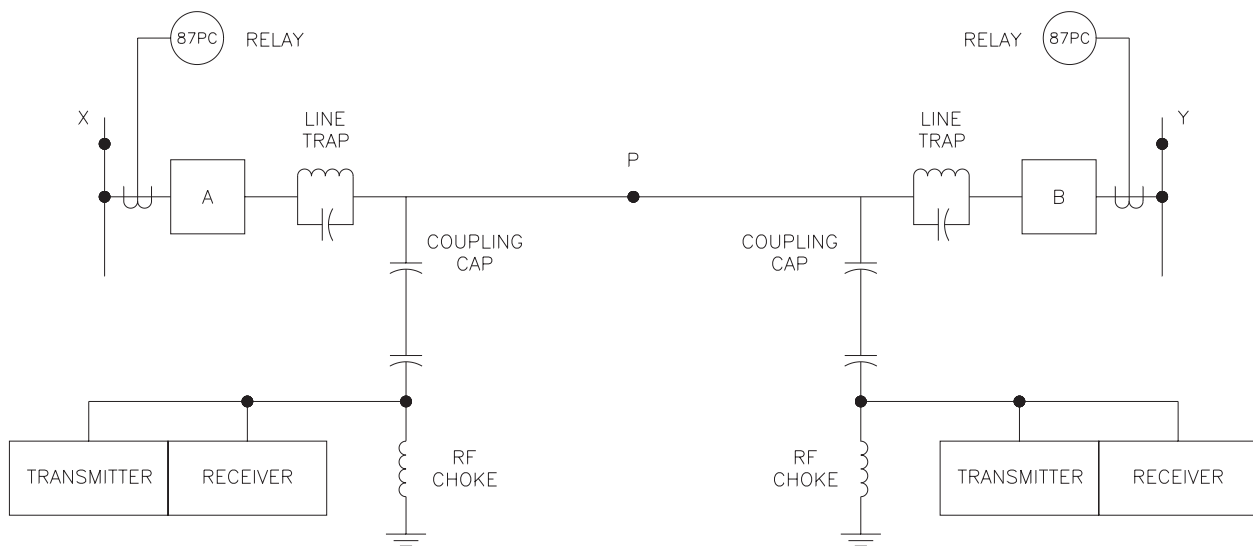
A distinction is made between leased facilities and the other (power company owned) facilities because in many cases the telephone company defines the characteristics of the channel without defining the type of link.

The ON-OFF type of communication equipment is used exclusively over power line carrier links. The transmitted signal is propagated along the power line between the transmitter and the remote receiver. This equipment usually operate in the frequency range of 30 to 200 kHz.

Frequency-shift equipment is available in several frequency ranges. First there are those in the audio range. These are generally employed over single side-band, microwave, pilot wires, and leased facilities. There are also frequency shift channels in the power line carrier frequency range. These are employed directly over the power line as are the ON-OFF types of equipment. Finally there is the frequency shift equipment that operate in and occasionally outside the power line carrier spectrum. These are employed over microwave and leased facilities.

c) POWER LINE CARRIER MEDIA

It is obvious that the performance of any channel that utilizes the protected power line itself as a communications medium will be affected in some way by faults on the power line. A fault on a transmission line can attenuate or completely block a signal, transmitted at one end of the line, from being received at the remote end. Faults external to the protected line have no effect on the signal attenuation since transmission lines that incorporate power line carrier channels are trapped at each end (See Figure 8-9).



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Figure 8-9: TYPICAL POWER LINE CARRIER ARRANGEMENT

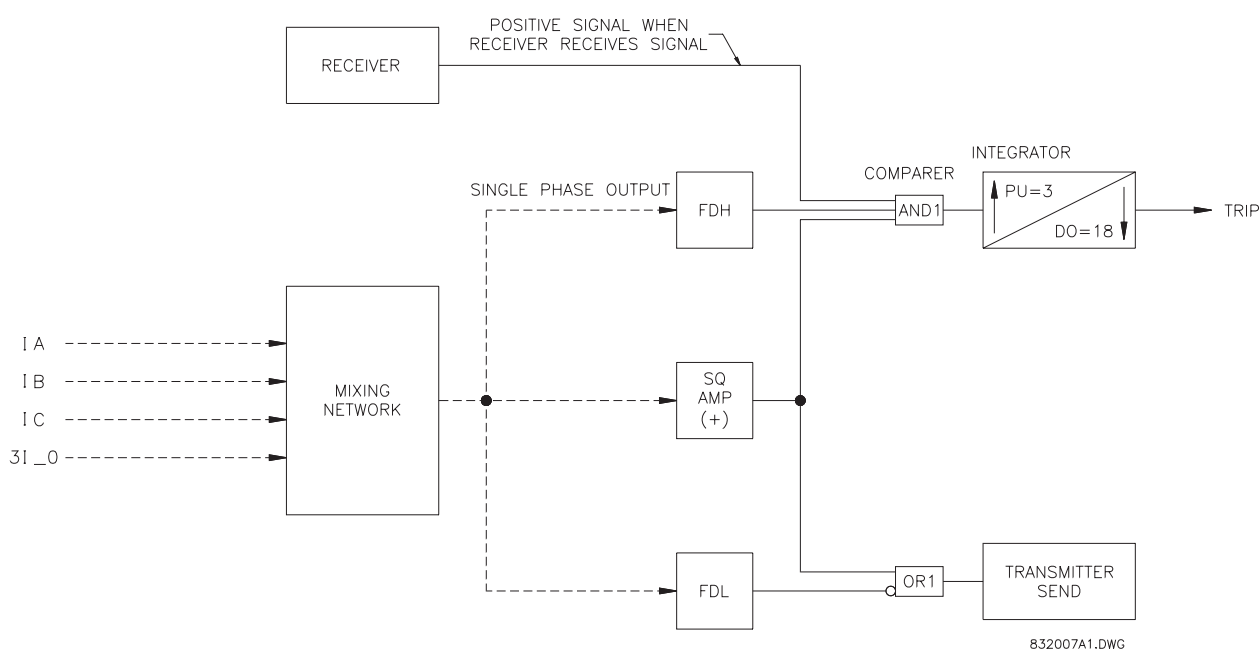
In the case of ON-OFF power line carrier channels, the operating frequencies of the equipment at all terminals of the protected line are generally the same. Thus, a signal transmitted from any terminal is received at all terminals. This is not a necessary requirement for using this kind of equipment. Rather it is desirable because the protection schemes that use ON-OFF channels can accommodate a single frequency arrangement and this conserves the carrier spectrum.

When frequency-shift equipment is used over power line carrier, the frequencies of each transmitter on the line must be different from all the others on the same line. For example, if the communication equipment in Figure 8-8 is of the frequency-shift type, the transmitter at the left end must operate at the same frequencies as the

receiver at the right end. Also, the right end transmitter and left end receiver must operate at the same frequencies while the frequencies of the two transmitters must be different. This is necessary because with frequency-shift equipment the transmitters associated with a given line protection scheme are not all generally sending the MARK or the SPACE frequencies at the same time. Thus, if a receiver were able to receive more than one transmitter, it could be simultaneously receiving a MARK signal from one and a SPACE signal from another.

This would not result in a workable protection scheme. When power line carrier channels are used, significant losses are present in the coupling equipment and the line itself. Depending on these losses and the ambient noise on the line, the transmitter power required may vary from about 1 to 10 watts and even more in extreme cases.

Consider an ON-OFF tripping type of scheme as defined by Figure 8-10. For a moment assume that FDL and NOT1 do not exist in the logic. During an internal fault, the currents out of the mixing (or sequence) networks at both ends of the line are in phase with each other so that the outputs of the SQ AMP are in phase at both ends of the line. The transmitters at both ends of the line are keyed on during the same half cycles that their associated SQ AMPs are attempting to trip via AND1. Thus, the receivers will be supplying the bottom input to AND1, and tripping will take place when FDH operates to provide the third input.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP(+) – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SINGLE PHASE CURRENT OUTPUT FROM THE MIXING NETWORK EXCEEDS THE PICK-UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SINGLE PHASE CURRENT OUTPUT FROM THE MIXING NETWORK EXCEEDS THE PICK-UP SETTING.

SQ. AMP(+) – PROVIDES AN OUTPUT ONLY ON THE POSITIVE HALF CYCLE.

NOTE: THIS SCHEME REQUIRES TRANSMITTERS OF DIFFERENT FREQUENCIES AT EACH LINE TERMINAL SO THAT A RECEIVER CANNOT RECEIVE.

Figure 8–10: SINGLE PHASE COMPARISON TRIPPING SCHEME PRINCIPLE

For external faults, the currents out of the mixing networks at the two ends of the line will be 180° out of phase with each other. Therefore, during the half cycle that the SQ AMP at one end of the line is producing an output, the one at the remote end is not, so no tripping will take place. It should be noted that a tripping type of scheme over an ON-OFF channel requires transmitters of different frequency at each end of the line so that no receiver can receive the locally-transmitted signals; otherwise tripping would occur during external faults. For this reason, such schemes are not generally applied.

It appears that the tripping scheme as described above has no need for an FDL function since no blocking coordination is required as is in a blocking scheme. However, this is not the case. The FDL and NOT1 functions provide a means for tripping when one end of the line is open as when picking up a faulted line from one end. For such a condition, the SQ AMP at the open end receives no current and so produces no output to key its transmitter. Without a received signal the closed end of the line cannot trip under any conditions even in the presence of a fault. The FDL function acts as a current detector. It is set with a very low pick up so that any significant output from the mixing network causes it to produce a continuous output. When the mixing network outputs goes to zero, FDL drops out causing an output from NOT1 which in turn keys the transmitter on continuously. This is received at the remote end to provide a continuous signal at the bottom input to AND1. Any fault that picks up FDL will then be tripped at the closed end of the line.

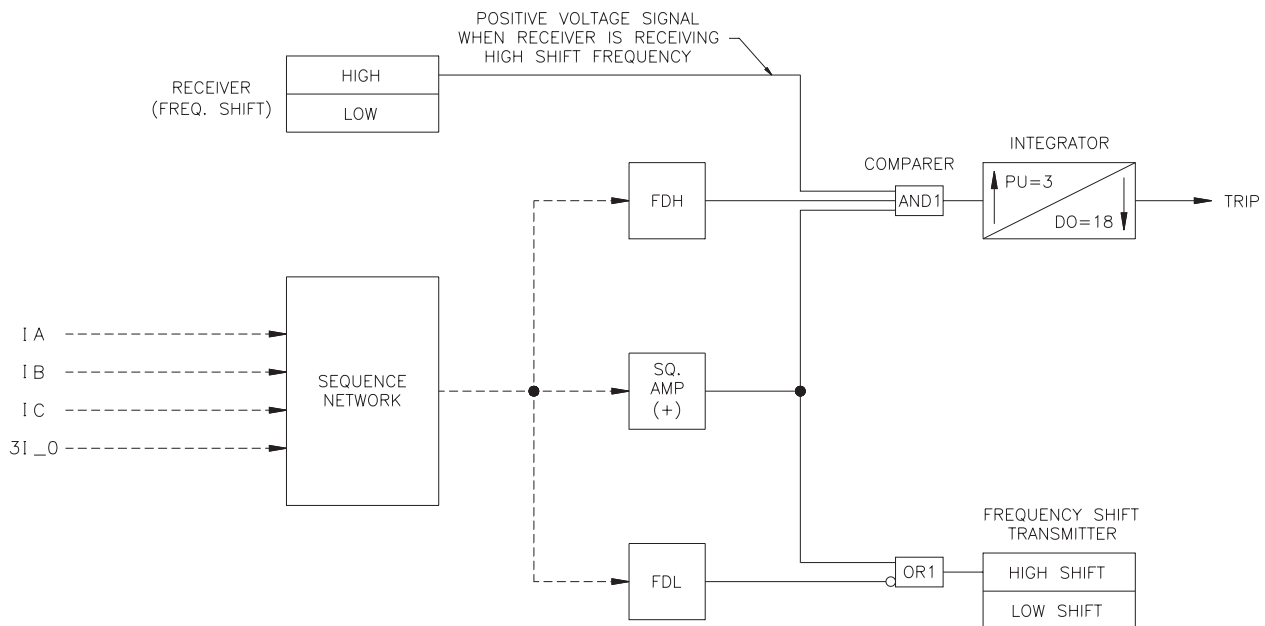
If the mixing network includes a positive sequence output, load current will keep FDL picked up continuously. If the mixing network includes only zero and/or negative sequence outputs, load current will not keep FDL picked up. Thus, with zero or negative sequence phase comparison the receivers at both ends of the line will be producing outputs to AND1 continuously. When a fault occurs, FDL picks-up very fast to restore the keying function to SQ AMP. This operation resembles a blocking scheme, although it is often called a permissive tripping scheme.

Another scheme to facilitate tripping on single end feed, uses a circuit breaker 52/b switch rather than FDL and NOT1. When the breaker is open, the 52/b switch closes and keys the associated transmitter on continuously. When the breaker is closed, the 52/b switch is open and keying is under control of the SQ AMP. While on the surface the use of 52/b appears simple and direct, the following problems arise that can require more complex logic and station wiring:

1. The 52/b contacts do not generally operate in synchronism with the main poles of the breaker so some timing functions must be included with the logic to compensate for this.
2. In multi-breaker schemes, such as ring buses, two breakers at each terminal are associated with each line so 52/b switches from each breaker are required in series.
3. In multi-breaker schemes one of the two breakers may be out of service but in the closed position. This would require a bypass of its 52/b switch which is open.

Regardless of which tripping scheme is used, it is obvious from Figure 8-9 that in order to trip either circuit breaker A or B for an internal fault at P it is necessary to get a carrier signal through the fault. If the fault attenuates the signal so that this does not happen, no tripping can take place. The amount of attenuation in signal that is produced by the fault will depend on the type of coupling (single phase, interphase, etc.), the type of fault, the phase involved, and the location of the fault on the line. The evaluation of these factors is outside the scope of this discussion.

Figure 8-11 illustrates the same tripping scheme as Figure 8-10 except that it utilizes a frequency shift rather than an ON-OFF communication set. The same comments apply to this scheme as do to that of Figure 8-9. A tripping scheme that operates over a power line carrier channel runs the risk of a failure to trip on internal faults because of signal attenuation. During external faults the line traps isolate the signal on the protected line from the fault. This is of no significance because attenuation or loss of signal on external faults cannot result in any maloperations. Conversely, a blocking scheme is unaffected by loss or attenuation of signal during internal faults because absence of a signal is required in order to trip. During external faults it is important that the blocking signal be isolated from the fault because loss of the signal can result in a false trip. The line traps provide this isolation.



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FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP(+) – SQUARING AMPLIFIER

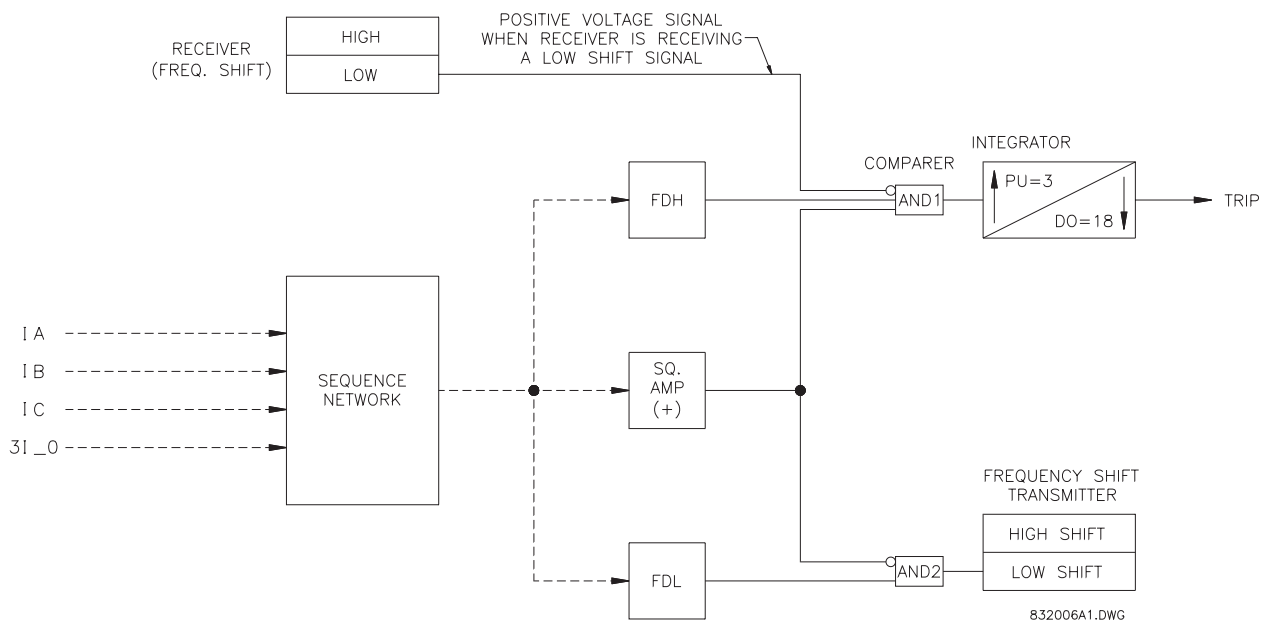
FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

SQ. AMP(+) – PROVIDES AN OUTPUT ONLY ON THE POSITIVE HALF CYCLE.

Figure 8–11: SINGLE PHASE COMPARISON TRIPPING SCHEME

Figures 8-5 and 8-12 illustrate phase comparison blocking schemes with ON-OFF and frequency-shift channels respectively. Figure 8-5 was discussed earlier and Figure 8-12 is exactly the same except for the high frequency shift which is not used in the protection scheme. While only one of the two frequencies of the frequency-shift equipment is used in the protection scheme, the second frequency does perform a useful function. It provides a means for continuous monitoring of the channel. Since one of the two frequencies is always being transmitted, it is possible to monitor the signal at each receiver continuously and incapacitate the protective scheme and/or provide indication at that terminal if the signal is lost.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP(+) – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

SQ. AMP(+) – PROVIDES AN OUTPUT ONLY ON THE POSITIVE HALF CYCLE.

Figure 8–12: SINGLE PHASE COMPARISON BLOCKING SCHEME

Most schemes that use an ON-OFF channel are arranged so that no transmission takes place during normal conditions (no fault). This does not lend itself to continuous monitoring. However, schemes are available that periodically start transmission of a signal at one end of a line which, when received at the remote end, initiates a return transmitted signal. Such schemes can be started manually or automatically on a time schedule. They are called carrier check-back schemes. They can be arranged so as not to affect the normal operation of the scheme even in the event of a fault during a check-back operation.

For the most part, phase comparison blocking carrier schemes use ON-OFF rather than frequency-shift channels, possibly for one or more of the following reasons:

1. The overall speed of the protective scheme is directly related to the speed of the channel. Until recently high speed frequency shift carrier channels were not available. Even today the ON-OFF channel is somewhat faster than the fastest frequency-shift channel.
2. Noise at the input of an ON-OFF channel receiver would tend to produce a blocking signal output. Noise at the input of a frequency-shift channel tends to drive its output to zero which is a tripping condition (in a blocking scheme). This tends to make the frequency-shift blocking scheme less secure against false tripping during external faults. It is possible to build channel condition detectors (signal to noise, loss of channel, etc.) into frequency-shift channels and block tripping when these detectors indicate trouble, but these features increase the complexity and the cost. This approach tends to make the blocking scheme resemble the tripping scheme since the receiver must now indicate an intact channel in order to trip.
3. Aside from the ability to accommodate continuous monitoring, the frequency-shift channel provides little advantage over the ON-OFF carrier channel.

There are very few if any phase comparison tripping schemes in service over carrier channels mainly because of the fear that it will not always be possible to get a trip signal through a fault.

There is another type of scheme that has recently been gaining some favor. This is called Unblocking. It is a cross between blocking and tripping in that it operates in the blocking mode but the blocking signal is sent continuously even in the quiescent state (no fault), and so it must be turned off in order to trip. Thus this scheme, as in the tripping schemes previously described, must include some means to stop the blocking signal from being transmitted at an open terminal in order to permit tripping of the closed remote terminal in the event of a fault. Here again the FDL logic of Figures 8-10 and 8-11 or the circuit breaker auxiliary 52/b switch could be used.

In general, unblocking utilizes frequency-shift channels because this permits monitoring of the continuous blocking signals. As they are usually applied, ON-OFF channels do not lend themselves to monitoring because the single frequency system transmits the same frequency from all transmitters and the loss of any one transmitter could not be detected. If applied in a normal duplex frequency basis (one in each direction) the ON-OFF channel would provide the monitoring features at the cost of carrier spectrum. However, this disadvantage can be overcome by the use of a new application of ON-OFF equipment where the transmitters at the different terminals are operating at frequencies offset from each other yet close enough to be nominally a single frequency system. This application permits monitoring, and at the same time has the advantage of a higher channel speed than the frequency-shift channels, while utilizing less channel spectrum in three terminal line applications.

d) MICROWAVE LINKS

Microwave links are quite commonly used for protective relaying including phase comparison schemes. However, because of the high cost of the microwave equipment, the applications are generally limited to cases where a large number of control and/or monitoring functions are needed between the same terminals as the relaying.

Since microwave links propagate through the atmosphere, rather than over the power line, they are generally unaffected by faults and noise on the power system. Thus, with a microwave link there is no problem of getting a signal through the fault, so tripping type schemes are very acceptable. On the other hand, since there is a possibility of fading of the microwave signal, there is some reluctance to use it in blocking schemes for fear of false tripping in the event of a fade during a nearby external fault. However, blocking schemes are used occasionally mainly because the tripping scheme requires special circuitry (as described earlier) in order to trip on single-end feed to a fault.

The communication equipment multiplexed on to a microwave system for protective relaying is invariably of the frequency-shift type, and usually of the high speed variety. Figures 8-11 and 8-12 are representative of the tripping and blocking schemes respectively. Since, as mentioned above, the microwave signal can fade, some of the frequency-shift receiver equipment includes channel status detectors that operate into the relay logic to incapacitate all tripping when the channel conditions are not normal. The ability to trip is then automatically reinstated when normality returns. With such an arrangement, complete loss of receiver output would incapacitate tripping. If the scheme were a blocking scheme similar to that of Figure 8-12, complete loss of channel during an external fault would permit a false trip unless an incapacitating feature were included in the scheme.

The receiver has only two outputs (high and low). Since the scheme trips on internal faults during the absence of the low-shift output, and since the absence of both the low and high shift outputs incapacitates tripping (where used), the implied requirement for tripping is the presence of the high-shift receiver output. While such a scheme is called a blocking scheme it appears to be, at least by implication, a tripping scheme.

In any case, there is nothing about a microwave channel to alter the previous discussion concerning phase comparison protection. The same basic schemes may be used with the understanding that the microwave signal can fade on occasion. For the most part, phase comparison relaying schemes over microwave channels have been of the tripping types.

e) PILOT WIRE LINKS

There are few, if any, privately owned pilot wires that are used as a link in phase comparison schemes. However, such applications would require a frequency-shift communication equipment used in either a tripping or blocking mode as indicated in Figures 8-11 and 8-12 respectively. Aside from the considerations involved in tripping for a fault with single-end feed, which were discussed previously, the selection between a blocking and a tripping scheme will generally result from a compromise between security and reliability. In order to make such a selection, consideration of the pilot pair, its protection, and its physical location in relation to power conductors must be evaluated.

In general, a high speed channel would require pilot wires that have a frequency response that is somewhat better than the standard telephone voice circuits.

Possibly because of the uncertainties of channel characteristics, plus the availability of pilot wire relays that are much lower in overall cost, phase comparison over privately owned pilot wires is not a common application.

f) LEASED (TELEPHONE COMPANY) FACILITIES

There has been some use of phase comparison relaying over leased facilities including voice grade pilot wire circuits. In general, if a customer requires or specifies the characteristics of a leased channel, the local telephone company could provide this link over microwave, cable, even pilot wires, or a combination of these. In such cases the selection between tripping and blocking schemes will depend on the performance of the channel as specified. The same basic schemes of Figures 8-11 and 8-12 would apply.

g) FIBER OPTICS

Fiber optic communications links are quite commonly used for protective relaying schemes. Since fiber optic links propagate through the fiber, rather than over the power line, they are generally unaffected by faults and noise on the power system. Thus, with a fiber link there is no problem of getting a signal through the fault, so tripping type schemes are very acceptable. An exception may occur when the fiber optic is embedded in the ground wire used on the line. In this case, the fault may be a result of a break in the ground wire which would prevent transmission of the signals.

In any case, there is nothing about a fiber channel to alter the previous discussion concerning phase comparison protection. The same basic schemes may be used with the understanding that the fiber optic signal can be lost on occasion. For the most part, phase comparison relaying schemes over fiber optic channels are of the tripping types.

h) SUMMATION OF BLOCKING vs. TRIPPING SCHEMES

The foregoing discussion of blocking and tripping schemes was presented without the benefit of a concise definition of these terms. As indicated in the discussion, the difficulty of making such definitions which would always apply is brought about by the channel status feature used in some frequency-shift blocking schemes. Such arrangements tend to be hybrids. Thus, the following simple definitions exclude any considerations of channel status features:

1. A blocking scheme is one that requires a specific output signal from the associated receiver in order to block tripping. Tripping can only take place during the time that this signal is absent.
2. A tripping scheme is one that requires a specific output signal from the associated receiver in order to permit tripping. Tripping can only take place during the time that this signal is present.
3. Where channel status logic is used, these definitions will have to be modified to meet the exact logic of the scheme.

In general, the selection of a blocking or a tripping scheme is one that should be made in conjunction with the chosen channel and with a knowledge of the channel characteristics in the face of system noise. Many different combinations are possible, but of these, only a selected few will meet any given set of requirements.

8.1.6 SINGLE vs. DUAL PHASE COMPARISON

In all the phase comparison schemes described so far, a trip attempt is made only every other half cycle. In the examples illustrated, this was every positive half cycle. Such schemes are termed single phase-comparison as against dual phase-comparison where a trip attempt is made every half cycle, positive and negative.

The only advantage of dual-comparison is that its maximum operating time to trip on internal faults will be a half cycle faster than the maximum time for the single phase-comparison. The minimum times for both schemes will be the same. This difference in maximum time results because a fault could occur at such an instant in time when the current is just going negative. Under such conditions, the single phase-comparison would have to wait till the next positive half cycle while the dual phase-comparison could trip on the upcoming negative half cycle.

While, as a general rule, high speed operation and security are on opposite sides of the coin, it is possible to design dual phase-comparison schemes that can provide the added speed with little or no loss in security. However, these schemes are somewhat more complex than equivalent single phase-comparison schemes. Figure 8-13 illustrates the dual phase-comparison tripping scheme that is the counterpart of the single phase-comparison scheme of Figure 8-11. The differences are noted below.

1. The dual scheme uses two separate comparer integrator combinations, one for the positive half cycle and the other for the negative half cycle.
2. A three-frequency, frequency-shift channel is used in dual phase comparison. The high-shift operates in conjunction with the positive half cycle while the low-shift works with the negative half cycle. When the channel is not keyed to either high or low, it operates on the center frequency. There is no center frequency output from the receiver into the relay tripping logic.
3. AND3 is included to make it impossible to key both frequencies simultaneously. It also gives preference to the low-shift which is sent continuously when FDL is dropped out. Thus, on single-end feed tripping can take place only on the negative half cycle.

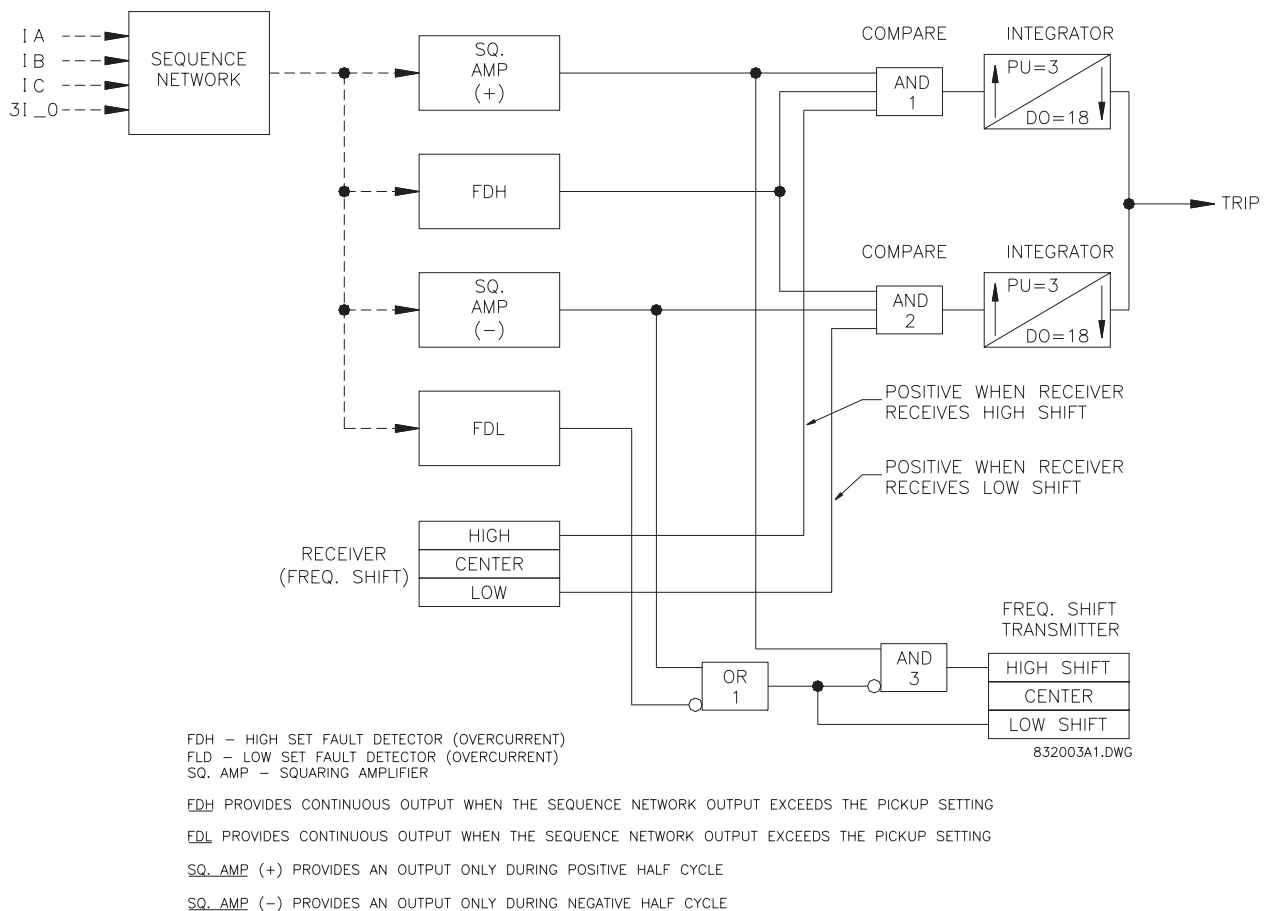
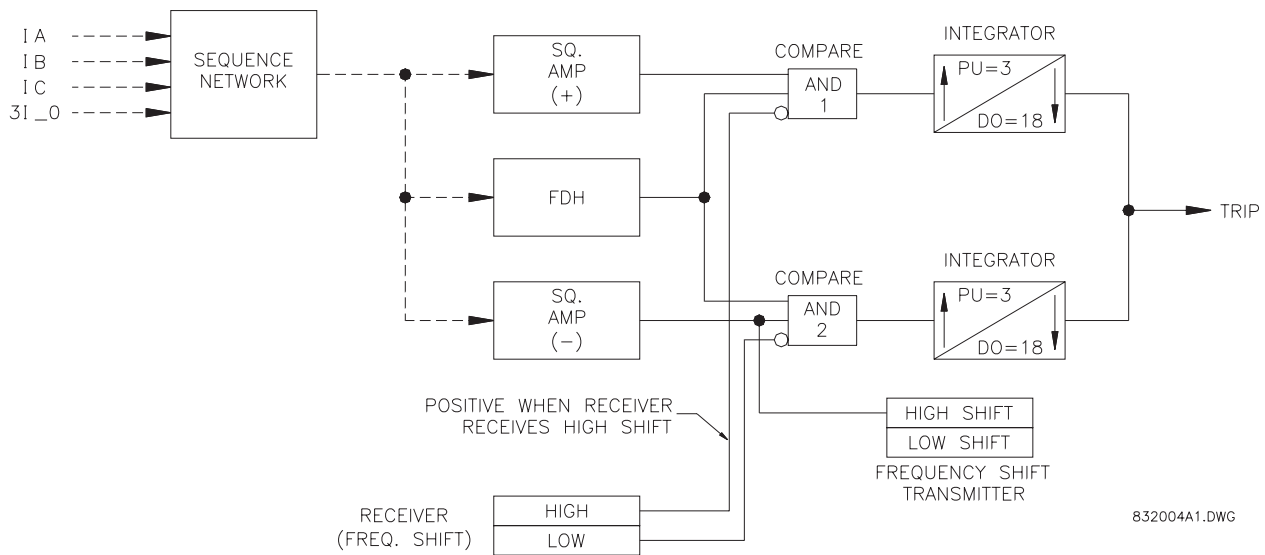


Figure 8-13: DUAL PHASE COMPARISON TRIPPING SCHEME

The center frequency, while not actually used in the relay tripping logic, adds security to the scheme during transient conditions.

The dual phase-comparison scheme of Figure 8-13 could be modified to operate over a two-frequency, frequency shift channel by eliminating AND3, FDL, NOT1, and the center frequency. The transmitter could then be arranged to send the low-shift frequency continuously except when keyed by the positive SQ. AMP to the high shift frequency. This arrangement, though simpler than the three frequency scheme, is deemed to be less secure.

Figure 8-14 illustrates a dual phase-comparison blocking scheme using a two-frequency, frequency-shift channel. Since one or the other of the two frequencies must be on at all times, and since both are blocking frequencies, there appears to be little need for an FDL function. Thus, it is not included. When the transmitter is not keyed, it sends low-shift continuously and when it is keyed by the negative squaring amplifier, it shifts to high for the negative half cycle. This scheme is simpler than that of Figure 8-13 but probably is not as secure.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICKUP SETTING

SQ. AMP (+) PROVIDES AN OUTPUT ONLY DURING POSITIVE HALF CYCLE

SQ. AMP (-) PROVIDES AN OUTPUT ONLY DURING NEGATIVE HALF CYCLE

Figure 8–14: DUAL PHASE COMPARISON BLOCKING SCHEME

There does not appear to be any good purpose for a three-frequency channel in dual phase-comparison blocking schemes since the center frequency would not add to the security, or otherwise improve the performance.

It is interesting to note that a dual phase-comparison scheme using an ON-OFF channel would have to be a combined blocking and tripping scheme. During one polarity of half cycle, it would have to trip on absence of any received signal (blocking), and on the other polarity of half cycle, it would have to trip in the presence of the received signal.

In general, it may be concluded that dual phase comparison may be accomplished in the blocking and in the tripping modes. The overall performance of the scheme will be dependent on the characteristics of the channel selected. While dual phase-comparison will reduce the maximum tripping time, it does so at the expense of simplicity and possibly some security depending on how it is accomplished.

8.1.7 REFINEMENTS TO BASIC SCHEMES

There are a number of standard refinements that are required and normally included in all phase comparison schemes. These will be discussed in terms of the basic blocking scheme of Figure 8-4, but will apply generally to all schemes, sometimes in a somewhat different form.

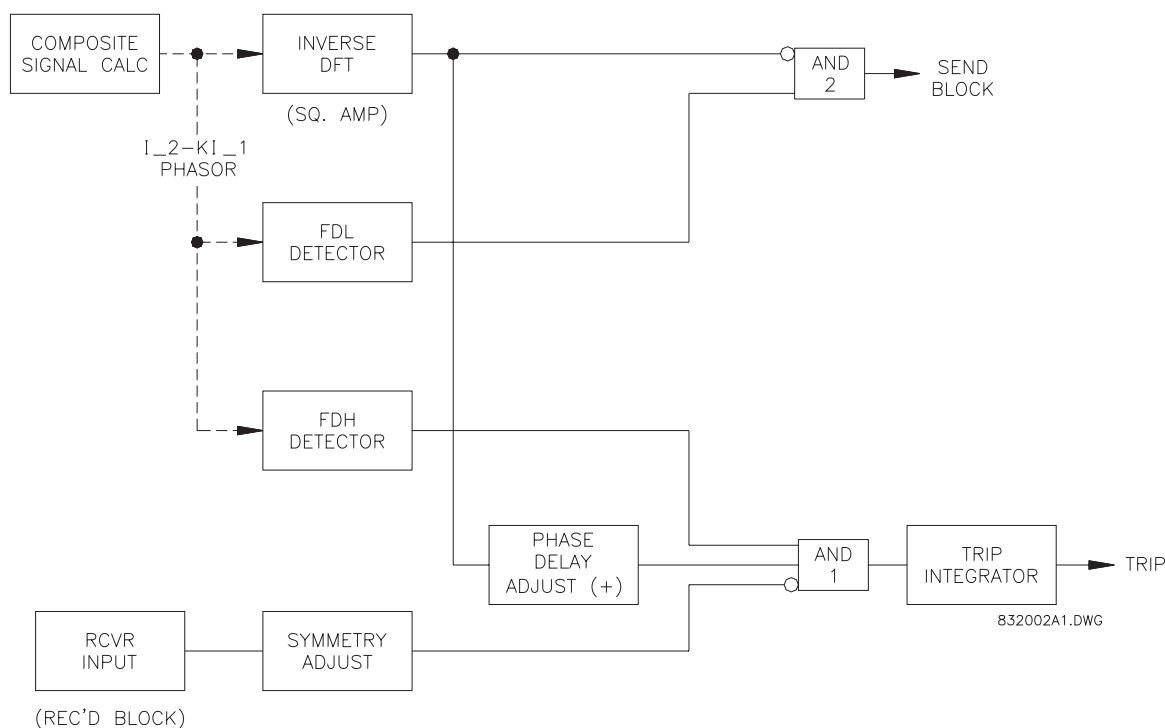
a) SYMMETRY ADJUSTMENT

As was noted in a previous section, receivers are not always symmetrical in their response. That is, if a transmitter is keyed on and off symmetrically every half cycle, the remote receiver output would not necessarily correspond exactly to the keying signal. For example, if an ON-OFF transmitter were keyed on for a half cycle and then off for a half cycle, and so on, the remote receiver output might be on for more than a half cycle and off for less than a half cycle. This affect is primarily due to the filter response in the receiver and is common with ON-OFF type of equipment. It is not a constant value but rather depends on operating frequencies as well as received signal strength. Thus, this asymmetry may vary from equipment to equipment and from time to time (as atmospheric conditions change) in service.

Frequency shift channels are generally symmetrical in their response when the discriminator in the receiver is balanced. If the discriminator is biased to one side or the other the receiver output tends to favor the side to which it is biased.

Because of this, all phase comparison schemes that may operate with asymmetrical channels are equipped with a symmetry adjustment.

The symmetry adjustment is in the receiver input circuit as shown in Figure 8-15. It is set with either a time delay pickup or a time delay drop out depending on whether the receiver elongates or shortens the received signal. The time setting is made in the field after the transmitters, receivers, and coupling equipment have all been tuned and adjusted for proper sensitivity. The proper setting is obtained by keying the transmitter on and off by means of a symmetrical sinusoidal output from the mixing network. Then, while this is taking place, the time delay pickup or dropout of the symmetry logic is adjusted so that the receiver yields a symmetrical output.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

Figure 8–15: BLOCKING SCHEME WITH SYMMETRY & PHASE DELAY ADJUSTMENTS

The receiver output is now symmetrical, but may be phase shifted in the lagging direction from the actual keying signal at the remote terminal. This latter result is not desirable, but fortunately it may be mitigated. In addition to this there is the propagation delay in getting the communication signal from the remote transmitter to the local receiver (1 millisecond per 186 miles) plus the delay in the receiver itself. All of these add to each other to produce a receiver output that may be significantly phase delayed from the current at the remote end of the line.

8

This is undesirable because it introduces an error in the phase comparison. There is no way to eliminate this phase delay but there is a way to compensate for it. This compensation is accomplished by the phase delay timer in the comparer input circuit.

b) PHASE DELAY ADJUSTMENT

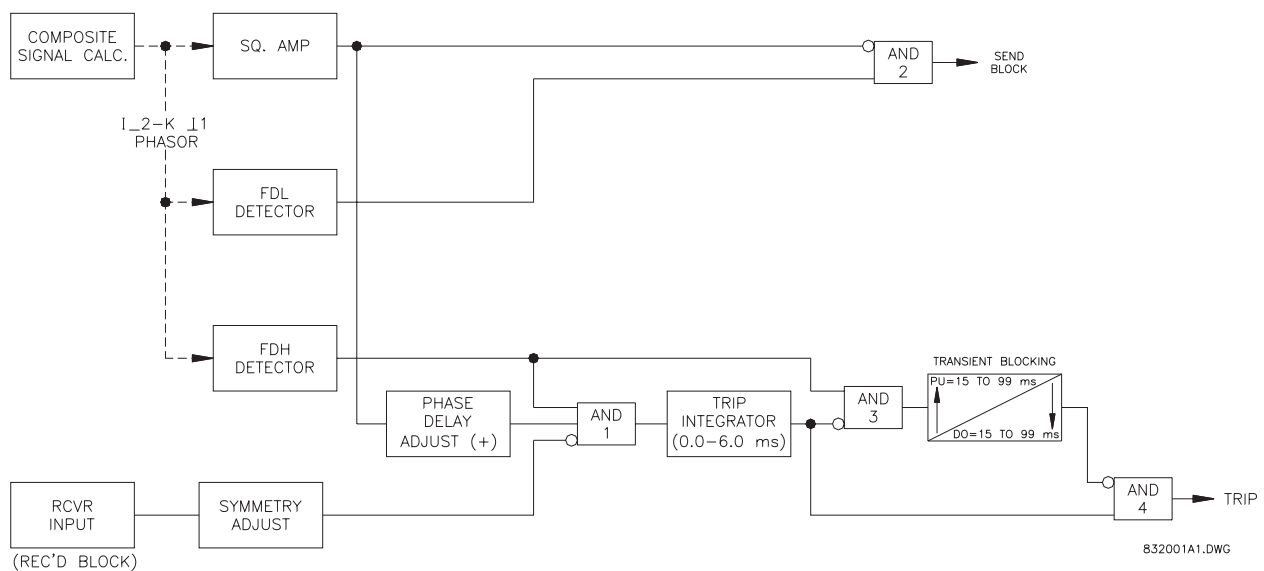
The phase delay adjustment is a timer that is set with a pickup and a dropout delay that are equal to each other so that it introduces a phase delay without affecting the symmetry of the input signal. Its output is the same shape as that of the squaring amplifier but delayed in time by the setting. This time delay setting is made in the field to be just equal to the sum of the three delays (symmetry adjustment, propagation, and receiver) discussed above. Thus, with this arrangement in the scheme of Figure 8-15, an external fault would produce an output from the symmetry adjustment logic exactly in phase and symmetrical with the output of the phase delay logic. This is necessary for proper blocking. For internal faults the output from the phase delay timer would be

symmetrical with, but 180 degrees out of phase with the receiver output. This is necessary for tripping. It should be recognized that any errors in these adjustments can reduce the tripping margins for internal faults and/or reduce the blocking margins during external faults.

It is interesting to note that the setting of the phase delay timer is dependent on the channel operating time, and that the total tripping time of the scheme is affected by this timer setting. Thus, the tripping speed of the scheme is to that degree dependent on the channel operating time.

c) TRANSIENT BLOCKING

Transient blocking is a feature that is included in all phase comparison schemes. It adds to the security of the scheme during and immediately after the clearing of external faults. Figure 8-16 is a representation of Figure 8-15 except with the transient blocking logic added. This consists of AND3, AND4 and the (15-99)/(15-99) transient blocking timer.



FDH – HIGH SET FAULT DETECTOR (OVERCURRENT)

FDL – LOW SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP – SQUARING AMPLIFIER

FDH PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

FDL PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

Figure 8-16: BLOCKING SCHEME WITH TRANSIENT BLOCKING LOGIC

The basic logic of the transient blocking scheme is such that if a fault is detected, as indicated by the operation of FDH, but no trip takes place, as indicated by no output from the trip integrator timer, AND3 produces an output to the transient blocking timer (15-99)/(15-99). If this condition persists for a time that is long enough for the transient blocking timer to produce an output, tripping is blocked via the NOT input to AND4. This blocking of a trip output persists for the dropout time setting of the transient blocking timer after the AND3 output disappears as a result of FDH resetting or the trip integrator producing an output.

The pickup time delay setting of the transient blocking timer must be longer than the expected time difference between FDH pickup and a trip integrator output during an internal fault. This insures no delay in tripping in the event of an internal fault, as well as prolonged blocking during the clearing of an external fault during which transient power reversals may tend to cause false tripping.

8.1.8 MULTI-TERMINAL LINES

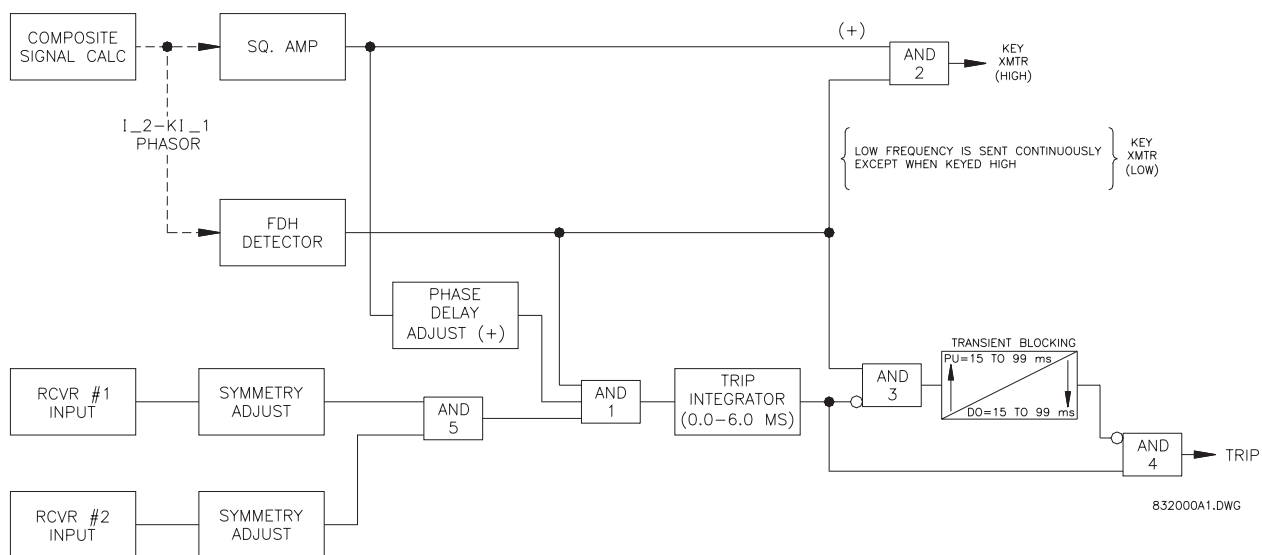
Up to this point these discussions have pertained principally to two-terminal lines. Phase comparison schemes are often applied to lines having more than two terminals and those applications differ somewhat depending on the channel equipment.

a) ON-OFF CHANNEL

The ON-OFF channel equipment is invariably used in blocking type carrier schemes similar to that of Figure 8-16. Since this type of scheme utilizes only one common frequency for all the transmitters and receivers, Figure 8-16 will apply to multi-terminal lines as well as two terminal lines. A blocking signal sent from any terminal will be received at all the other terminals to provide the necessary blocking via the single receiver at that terminal.

b) FREQUENCY-SHIFT CHANNEL

Frequency-shift channels are generally used in tripping type schemes. Figure 8-17 illustrates a three-terminal line tripping scheme using a frequency-shift channel. This arrangement requires two receivers at each terminal. One receiver is required for each remote transmitter because each transmitter is operated at a different frequency. In order to trip, a high-shift output is required from both receivers concurrently to AND5. A two-terminal line scheme would require only one receiver which would operate directly into AND1 without the need for AND5. Each channel has its own symmetry adjustment.



FDH - HIGH SET FAULT DETECTOR (OVERCURRENT)

SQ. AMP - SQUARING AMPLIFIER

FDH - PROVIDES CONTINUOUS OUTPUT WHEN THE SEQUENCE NETWORK OUTPUT EXCEEDS THE PICK-UP SETTING.

Figure 8-17: TRIPPING SCHEME FOR 3-TERMINAL LINE

9.1.1 DESCRIPTION

The L60 Phase Comparison relay is designed to provide high-speed protection of transmission lines against all phase and ground faults when operated in the "mixed-excitation" mode. The term "mixed-excitation", when applied to phase comparison, describes a scheme that first mixes different sequence quantities in a given proportion and phase angle, then performs a phase-comparison based on this mix.

A complete explanation of the Phase Comparison Element operation principles can be found in Chapter 8.

9.1.2 USAGE OF SETTINGS

87PC SIGNAL:

A mixed I₂-K_{I_1} signal or 3I₀ can be chosen as the operating signal for FDH and FDL excitation. In "mixed excitation" mode, the relay provides high-speed protection of transmission lines against all phase and ground faults. However, if a user wants the relay to operate only during ground faults, the 3I₀ mode can be chosen.

87PC MIXED SIGNAL K:

The K factor must be chosen for the mixed excitation operating signal. As indicated in Chapter 8: THEORY OF OPERATION, best results are obtained using a value of 0.2 (the default setting). The selected K value can range from 0.00 to 0.25. Setting K = 0 makes a phase comparison on the basis of negative-sequence excitation only. In such a scheme, the relay protects against all unbalanced faults; a suitable phase-distance relay should be used to protect against three-phase faults.

The user must remember that K is an important tool to set FDL and consequently FDH at the lower setting, especially in the cases when the margin between the maximum load current and the minimum fault current is very small. Reducing K to 0.15 or 0.10 makes phase comparison protection less sensitive to load current which in turn allows the user to provide enough sensitivity to the fault current. From the other hand it makes protection less sensitive to the balanced three-phase fault which in fact occurs very rarely.

87PC FDL PICKUP:

The main function of FDL is keying the transmitter. FDL pickup must be set above the K_{I_1} output of the mixing network for the maximum expected load. The recommended FDL setting is as follows;

- $FDL = 1.1 \times K \times I_{1L}$ where I_{1L} is the maximum line load current and K is a mixed signal factor as described above. Higher margin may be required to definitely avoid FDL pickup during normal load condition.
- If the 3I₀ operating signal has been chosen, FDL should be set as $FDL = 1.1 \times I_{1L}$ where I_{1L} is a maximum line load current.

It must be noted that in some cases a channel may also perform other functions if it is objectionable to key the transmitter constantly. In such cases, FDL could be set well below the K_{I_1} value of the mixing network resulting from maximum load but not less than 0.05 pu which defines the minimum required current from current transformers.

87PC FDH PICKUP:

The main function of FDH is to permit tripping as it arms the tripping output. FDH pickup must be set high enough so that it will not operate on maximum load. Also FDH must be set high enough to reset itself in the presence of heavy loads following clearing an external fault. The recommended setting for FDH is as follows:

$$FDH = (4/3) \times FDL + 0.375 \times I_{c1}$$

where I_{c1} is total positive-sequence charging current under normal conditions.

A distance relay is recommended as an external fault detector if the minimum internal three-phase fault is less than twice the maximum load current. It allows coincidence detector to start comparing the local and received signals and to make trip decision if FDH is not picked up. Setting FD INPUT described below is to be used for assigning a distance element or some other elements.

If 3I_0 operating signal has been chosen, FDH should be set at most 0.66 times but preferably 0.5 times the minimum internal ground fault current to provide reliable sensitivity of the fault.

87PC FD INPUT:

As is indicated above, the setting FD INPUT is to be used for assigning a distance element or some other elements. Z2 element, i.e. overreaching element associated with the same line distance protection with no time delay is most appropriate for this purpose. The user must be aware that a distance element assigned by the FD INPUT is not providing a tripping function but only gives permission to the coincidence detector to start comparing local and received signal in order to make trip/block decision. Another alternative is overcurrent protection.

87PC SYMMETRY CH 1(2):

This setting is used to make the local squared signal and the received signal from the remote terminal symmetrical. To set it properly, keying of the remote transmitter and an oscilloscope are required. If the received signal is ideally symmetrical with respect to the "Mark" and "Space" signals, a value of 0 ms (set as default) should be used. If for example, measured length of the "Mark" is longer than "Space" for 4.0 ms, setting "-2.0 ms" to be entered. If the measured length of the "Mark" is shorter than "Space" for 3.0 ms, setting "+1.5 ms" is to be entered. As sum of "Mark" and "Space" signals equals the length of the power cycle, corresponding scaling of the signals should be made for off nominal system frequencies.

Negative setting time is needed if the receiver elongates the received signal and positive setting time is needed if the receiver shortens the signal.

The L60 allows the customer to check and set channel symmetry without using an oscilloscope, by means of FlexLogic™ operands and applying the corresponding current to the relays which in turn key the PLC and consequently measure "Mark" and "Space" signals on the oscillography. Moving cursors and measuring an average from a few points time, the user can determine and enter setting.

87PC PHASE DELAY CH1(2):

This setting is made in the field to be equal to the sum of three delays; symmetry adjustment, propagation time of the line and receiver. Different methods can be used.

The L60 allows the customer to check and set phase delay without using an oscilloscope and by means of FlexLogic™ operands and applying the corresponding current to both relays. Oscillography shows the time difference (including PLC delay and line propagation time) between local and remote signals. Moving cursors and measuring an average from a few points time, the user can determine and apply the proper setting

87PC STABILITY ANGLE:

Stability angle setting must accommodate the security requirements for the external fault and dependability requirements for the internal fault. Default value 3 ms corresponds to about 65 degrees of blocking zone for a 60 Hz system. It overrides sources angular shift resulting from load, charging current, CT errors, etc.

The stability angle ϕ_s can be estimated as follows:

$$\phi_s = \phi_{load} + \phi_{capac} + \phi_{ct}$$

where: ϕ_{load} is a sources angular shift phase between the line terminal at maximum expected load, expressed in electrical degrees.

ϕ_{capac} is the capacitive current compensation angle evaluated as $\phi_{capac} = \arctan(I_{capac} / I_{FDH})$ expressed in electrical degrees, where I_{capac} is a line capacitive current, I_{FDH} -setting of FDH (fault detector high).

ϕ_{ct} is the CTs error and saturation compensation angle and can be adopted as equal 10° for most cases unless there is a special consideration or concern. For such cases ϕ_{ct} can be increased up to 20°.

87PC TRANS BLOCK PICKUP:

This setting is used to increase security during and after clearing of an external fault and to prevent false tripping during current reversals. The setting should be higher than the time difference in operation between FDH and output from the coincidence discriminator. A setting 10-30 ms gives sufficient security for most conditions.

87PC TRANS BLOCK RESET:

This setting is used to reset transient blocking and allow tripping. According to local conditions, setting should be considered as the sum of protection operating time and breaker opening time of the adjacent line and minus the Transient Pickup value to override uncertainty during clearing external faults. The faster the fault clearing at the adjacent line, the lower setting could be applied.

$$T_{tr_rst} = T_{prot_adj} + T_{break_adj} - T_{tr_pkp}$$

where: T_{prot_adj} is the expected time of main protection operation on the adjacent line,

T_{break_adj} is the operation time of the breaker on the adjacent line,

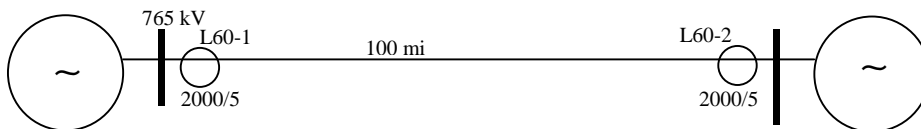
T_{tr_pkp} is selected Transient Pickup time.

87PC BLOCK:

The user can define some cases when blocking of the phase comparison scheme is required. This setting will block the tripping function. PLC alarm contacts indicating channel failure are usually assigned for this setting, especially in blocking schemes.

87PC CHNL LOSS TRIP WINDOW:

This setting is applicable to the 2TL-BL-DPC-2FL scheme only. The typical setting is 150 ms.

9.1.3 SETTINGS EXAMPLE

Consider settings for a single-circuit 765 kV line, 100 miles length, 50 Ohms primary impedance, 5520 ohms shunt capacitance of the line, maximum expected load of 2000A, CT ratio 2000/5, minimum expected internal 3-phase fault is 8000A.

1. Mixed signal factor $K=0.2$
2. FDL pickup: $I_{FDL} = 1.1 \times 2000 \times 0.2 = 440$ A or $440 / 400 = 1.1$ A secondary.
The setting is $1.1 / 5 = 0.22$ pu.
3. FDH pickup: $I_{FDH} = 4/3 \times I_{FDL} + 0.375 \times I_{capac} = 1.33 \times 440 + 0.375 \times 80 = 615.2$ A or $615.2 / 400 = 1.54$ A secondary; setting is $1.76 / 5 = 0.31$ pu. Where $I_{capac} = 765000 / (\sqrt{3} \times 5520) = 80$ A
4. Stability angle:

$$\phi_{load} = 2 \times \arcsin((2000 \times 50 \times \sqrt{3}) / (2 \times 765000)) = 13.0^\circ$$

$$\phi_{capac} = \arctan(I_{capac} / I_{FDH}) = \arctan(80 / 615.2) = 7.4^\circ$$

$$\phi_s(\text{deg}) = 13.0^\circ + 7.4^\circ + 10^\circ = 30.4^\circ$$

Minimum recommended setting 60° (set as default) should be applied.

5. Check against requirement for trip supervision by distance relay: As minimum internal 3-phase fault is much than twice the maximum line load current, no distance element is required for be assigned to FD INPUT setting.

The following tables are provided to keep a record of settings to be used on a relay.

10.1.1 SETTINGS

Table 10–1: PRODUCT SETUP (Sheet 1 of 16)

SETTING	VALUE
PASSWORD SECURITY	
Access Level	
Command Password	
Setting Password	
Encrypted Command Password	
Encrypted Setting Password	
DISPLAY PROPERTIES	
Flash Message Time	
Default Message Timeout	
Default Message Intensity	
REAL TIME CLOCK	
IRIG-B Signal Type	
COMMUNICATIONS > SERIAL PORTS	
RS485 COM1 Baud Rate	
RS485 COM1 Parity	
RS485 COM2 Baud Rate	
RS485 COM2 Parity	
COMMUNICATIONS > NETWORK	
IP Address	
Subnet IP Mask	
Gateway IP Address	
OSI Network Address (NSAP)	
Ethernet Primary Link Monitor	
Ethernet Secondary Link Monitor	
COMMUNICATIONS > MODBUS PROTOCOL	
Modbus Slave Address	
Modbus IP Port Number	
COMMUNICATIONS > DNP PROTOCOL	
DNP Port	
DNP Address	
DNP Network Client Address 1	
DNP Network Client Address 2	
DNP IP Port Number	

Table 10–1: PRODUCT SETUP (Sheet 2 of 16)

SETTING	VALUE
DNP Unsol Response Function	
DNP Unsol Response Timeout	
DNP Unsol Response Max Retries	
Unsol Response Dest Address	
User Map for DNP Analogs	
COMMUNICATIONS > UCA/MMS PROTOCOL	
Default GOOSE Update Time	
UCA Logical Device	
UCA/MMS IP Port Number	
COMMUNICATIONS > WEB SERVER HTTP PROT.	
HTTP IP Port Number	
COMMUNICATIONS > TFTP PROTOCOL	
TFTP Main IP Port Number	
TFTP Data IP Port 1 Number	
TFTP Data IP Port 2 Number	
OSCILLOGRAPHY	
Number of Records	
Trigger Mode	
Trigger Position	
Trigger Source	
AC Input Waveforms	
FAULT REPORT	
Fault Report Source	
Fault Report Trigger	
OSCILLOGRAPHY > DIGITAL CHANNELS	
Digital Channel 1	
Digital Channel 2	
Digital Channel 3	
Digital Channel 4	
Digital Channel 5	
Digital Channel 6	
Digital Channel 7	
Digital Channel 8	

Table 10–1: PRODUCT SETUP (Sheet 3 of 16)

SETTING	VALUE
Digital Channel 9	
Digital Channel 10	
Digital Channel 11	
Digital Channel 12	
Digital Channel 13	
Digital Channel 14	
Digital Channel 15	
Digital Channel 16	
Digital Channel 17	
Digital Channel 18	
Digital Channel 19	
Digital Channel 20	
Digital Channel 21	
Digital Channel 22	
Digital Channel 23	
Digital Channel 24	
Digital Channel 25	
Digital Channel 26	
Digital Channel 27	
Digital Channel 28	
Digital Channel 29	
Digital Channel 30	
Digital Channel 31	
Digital Channel 32	
Digital Channel 33	
Digital Channel 34	
Digital Channel 35	
Digital Channel 36	
Digital Channel 37	
Digital Channel 38	
Digital Channel 39	
Digital Channel 40	
Digital Channel 41	
Digital Channel 42	
Digital Channel 43	
Digital Channel 44	
Digital Channel 45	
Digital Channel 46	
Digital Channel 47	

Table 10–1: PRODUCT SETUP (Sheet 4 of 16)

SETTING	VALUE
Digital Channel 48	
Digital Channel 49	
Digital Channel 50	
Digital Channel 51	
Digital Channel 52	
Digital Channel 53	
Digital Channel 54	
Digital Channel 55	
Digital Channel 56	
Digital Channel 57	
Digital Channel 58	
Digital Channel 59	
Digital Channel 60	
Digital Channel 61	
Digital Channel 62	
Digital Channel 63	
Digital Channel 64	
OSCILLOGRAPHY > ANALOG CHANNELS	
Analog Channel 1	
Analog Channel 2	
Analog Channel 3	
Analog Channel 4	
Analog Channel 5	
Analog Channel 6	
Analog Channel 7	
Analog Channel 8	
Analog Channel 9	
Analog Channel 10	
Analog Channel 11	
Analog Channel 12	
Analog Channel 13	
Analog Channel 14	
Analog Channel 15	
Analog Channel 16	
DATA LOGGER	
Rate	
Channel 1	
Channel 2	
Channel 3	

Table 10–1: PRODUCT SETUP (Sheet 5 of 16)

SETTING	VALUE
Channel 4	
Channel 5	
Channel 6	
Channel 7	
Channel 8	
Channel 9	
Channel 10	
Channel 11	
Channel 12	
Channel 13	
Channel 14	
Channel 15	
Channel 16	
USER PROGRAMMABLE LEDES	
Trip LED Input	
Alarm LED Input	
LED 1 Operand	
LED 1 Type	
LED 2 Operand	
LED 2 Type	
LED 3 Operand	
LED 3 Type	
LED 4 Operand	
LED 4 Type	
LED 5 Operand	
LED 5 Type	
LED 6 Operand	
LED 6 Type	
LED 7 Operand	
LED 7 Type	
LED 8 Operand	
LED 8 Type	
LED 9 Operand	
LED 9 Type	
LED 10 Operand	
LED 10 Type	
LED 11 Operand	
LED 11 Type	
LED 12 Operand	

Table 10–1: PRODUCT SETUP (Sheet 6 of 16)

SETTING	VALUE
LED 12 Type	
LED 13 Operand	
LED 13 Type	
LED 14 Operand	
LED 14 Type	
LED 15 Operand	
LED 15 Type	
LED 16 Operand	
LED 16 Type	
LED 17 Operand	
LED 17 Type	
LED 18 Operand	
LED 18 Type	
LED 19 Operand	
LED 19 Type	
LED 20 Operand	
LED 20 Type	
LED 21 Operand	
LED 21 Type	
LED 22 Operand	
LED 22 Type	
LED 23 Operand	
LED 23 Type	
LED 24 Operand	
LED 24 Type	
LED 25 Operand	
LED 25 Type	
LED 26 Operand	
LED 26 Type	
LED 27 Operand	
LED 27 Type	
LED 28 Operand	
LED 28 Type	
LED 29 Operand	
LED 29 Type	
LED 30 Operand	
LED 30 Type	
LED 31 Operand	
LED 31 Type	

Table 10–1: PRODUCT SETUP (Sheet 7 of 16)

SETTING	VALUE
LED 32 Operand	
LED 32 Type	
LED 33 Operand	
LED 33 Type	
LED 34 Operand	
LED 34 Type	
LED 35 Operand	
LED 35 Type	
LED 36 Operand	
LED 36 Type	
LED 37 Operand	
LED 37 Type	
LED 38 Operand	
LED 38 Type	
LED 39 Operand	
LED 39 Type	
LED 40 Operand	
LED 40 Type	
LED 41 Operand	
LED 41 Type	
LED 42 Operand	
LED 42 Type	
LED 43 Operand	
LED 43 Type	
LED 44 Operand	
LED 44 Type	
LED 45 Operand	
LED 45 Type	
LED 46 Operand	
LED 46 Type	
LED 47 Operand	
LED 47 Type	
LED 48 Operand	
LED 48 Type	
FLEX STATE PARAMETERS	
Flex State Parameter 1	
Flex State Parameter 2	
Flex State Parameter 3	
Flex State Parameter 4	

Table 10–1: PRODUCT SETUP (Sheet 8 of 16)

SETTING	VALUE
Flex State Parameter 5	
Flex State Parameter 6	
Flex State Parameter 7	
Flex State Parameter 8	
Flex State Parameter 9	
Flex State Parameter 10	
Flex State Parameter 11	
Flex State Parameter 12	
Flex State Parameter 13	
Flex State Parameter 14	
Flex State Parameter 15	
Flex State Parameter 16	
Flex State Parameter 17	
Flex State Parameter 18	
Flex State Parameter 19	
Flex State Parameter 20	
Flex State Parameter 21	
Flex State Parameter 22	
Flex State Parameter 23	
Flex State Parameter 24	
Flex State Parameter 25	
Flex State Parameter 26	
Flex State Parameter 27	
Flex State Parameter 28	
Flex State Parameter 29	
Flex State Parameter 30	
Flex State Parameter 31	
Flex State Parameter 32	
Flex State Parameter 33	
Flex State Parameter 34	
Flex State Parameter 35	
Flex State Parameter 36	
Flex State Parameter 37	
Flex State Parameter 38	
Flex State Parameter 39	
Flex State Parameter 40	
Flex State Parameter 41	
Flex State Parameter 42	
Flex State Parameter 43	

Table 10–1: PRODUCT SETUP (Sheet 9 of 16)

SETTING	VALUE
Flex State Parameter 44	
Flex State Parameter 45	
Flex State Parameter 46	
Flex State Parameter 47	
Flex State Parameter 48	
Flex State Parameter 49	
Flex State Parameter 50	
Flex State Parameter 51	
Flex State Parameter 52	
Flex State Parameter 53	
Flex State Parameter 54	
Flex State Parameter 55	
Flex State Parameter 56	
Flex State Parameter 57	
Flex State Parameter 58	
Flex State Parameter 59	
Flex State Parameter 60	
Flex State Parameter 61	
Flex State Parameter 62	
Flex State Parameter 63	
Flex State Parameter 64	
Flex State Parameter 65	
Flex State Parameter 66	
Flex State Parameter 67	
Flex State Parameter 68	
Flex State Parameter 69	
Flex State Parameter 70	
Flex State Parameter 71	
Flex State Parameter 72	
Flex State Parameter 73	
Flex State Parameter 74	
Flex State Parameter 75	
Flex State Parameter 76	
Flex State Parameter 77	
Flex State Parameter 78	
Flex State Parameter 79	
Flex State Parameter 80	
Flex State Parameter 81	
Flex State Parameter 82	

Table 10–1: PRODUCT SETUP (Sheet 10 of 16)

SETTING	VALUE
Flex State Parameter 83	
Flex State Parameter 84	
Flex State Parameter 85	
Flex State Parameter 86	
Flex State Parameter 87	
Flex State Parameter 88	
Flex State Parameter 89	
Flex State Parameter 90	
Flex State Parameter 91	
Flex State Parameter 92	
Flex State Parameter 93	
Flex State Parameter 94	
Flex State Parameter 95	
Flex State Parameter 96	
Flex State Parameter 97	
Flex State Parameter 98	
Flex State Parameter 99	
Flex State Parameter 100	
Flex State Parameter 101	
Flex State Parameter 102	
Flex State Parameter 103	
Flex State Parameter 104	
Flex State Parameter 105	
Flex State Parameter 106	
Flex State Parameter 107	
Flex State Parameter 108	
Flex State Parameter 109	
Flex State Parameter 110	
Flex State Parameter 111	
Flex State Parameter 112	
Flex State Parameter 113	
Flex State Parameter 114	
Flex State Parameter 115	
Flex State Parameter 116	
Flex State Parameter 117	
Flex State Parameter 118	
Flex State Parameter 119	
Flex State Parameter 120	
Flex State Parameter 121	

Table 10–1: PRODUCT SETUP (Sheet 11 of 16)

SETTING	VALUE
Flex State Parameter 122	
Flex State Parameter 123	
Flex State Parameter 124	
Flex State Parameter 125	
Flex State Parameter 126	
Flex State Parameter 127	
Flex State Parameter 128	
Flex State Parameter 129	
Flex State Parameter 130	
Flex State Parameter 131	
Flex State Parameter 132	
Flex State Parameter 133	
Flex State Parameter 134	
Flex State Parameter 135	
Flex State Parameter 136	
Flex State Parameter 137	
Flex State Parameter 138	
Flex State Parameter 139	
Flex State Parameter 140	
Flex State Parameter 141	
Flex State Parameter 142	
Flex State Parameter 143	
Flex State Parameter 144	
Flex State Parameter 145	
Flex State Parameter 146	
Flex State Parameter 147	
Flex State Parameter 148	
Flex State Parameter 149	
Flex State Parameter 150	
Flex State Parameter 151	
Flex State Parameter 152	
Flex State Parameter 153	
Flex State Parameter 154	
Flex State Parameter 155	
Flex State Parameter 156	
Flex State Parameter 157	
Flex State Parameter 158	
Flex State Parameter 159	
Flex State Parameter 160	

Table 10–1: PRODUCT SETUP (Sheet 12 of 16)

SETTING	VALUE
Flex State Parameter 161	
Flex State Parameter 162	
Flex State Parameter 163	
Flex State Parameter 164	
Flex State Parameter 165	
Flex State Parameter 166	
Flex State Parameter 167	
Flex State Parameter 168	
Flex State Parameter 169	
Flex State Parameter 170	
Flex State Parameter 171	
Flex State Parameter 172	
Flex State Parameter 173	
Flex State Parameter 174	
Flex State Parameter 175	
Flex State Parameter 176	
Flex State Parameter 177	
Flex State Parameter 178	
Flex State Parameter 179	
Flex State Parameter 180	
Flex State Parameter 181	
Flex State Parameter 182	
Flex State Parameter 183	
Flex State Parameter 184	
Flex State Parameter 185	
Flex State Parameter 186	
Flex State Parameter 187	
Flex State Parameter 188	
Flex State Parameter 189	
Flex State Parameter 190	
Flex State Parameter 191	
Flex State Parameter 192	
Flex State Parameter 193	
Flex State Parameter 194	
Flex State Parameter 195	
Flex State Parameter 196	
Flex State Parameter 197	
Flex State Parameter 198	
Flex State Parameter 199	

Table 10–1: PRODUCT SETUP (Sheet 13 of 16)

SETTING	VALUE
Flex State Parameter 200	
Flex State Parameter 201	
Flex State Parameter 202	
Flex State Parameter 203	
Flex State Parameter 204	
Flex State Parameter 205	
Flex State Parameter 206	
Flex State Parameter 207	
Flex State Parameter 208	
Flex State Parameter 209	
Flex State Parameter 210	
Flex State Parameter 211	
Flex State Parameter 212	
Flex State Parameter 213	
Flex State Parameter 214	
Flex State Parameter 215	
Flex State Parameter 216	
Flex State Parameter 217	
Flex State Parameter 218	
Flex State Parameter 219	
Flex State Parameter 220	
Flex State Parameter 221	
Flex State Parameter 222	
Flex State Parameter 223	
Flex State Parameter 224	
Flex State Parameter 225	
Flex State Parameter 226	
Flex State Parameter 227	
Flex State Parameter 228	
Flex State Parameter 229	
Flex State Parameter 230	
Flex State Parameter 231	
Flex State Parameter 232	
Flex State Parameter 233	
Flex State Parameter 234	
Flex State Parameter 235	
Flex State Parameter 236	
Flex State Parameter 237	
Flex State Parameter 238	

Table 10–1: PRODUCT SETUP (Sheet 14 of 16)

SETTING	VALUE
Flex State Parameter 239	
Flex State Parameter 240	
Flex State Parameter 241	
Flex State Parameter 242	
Flex State Parameter 243	
Flex State Parameter 244	
Flex State Parameter 245	
Flex State Parameter 246	
Flex State Parameter 247	
Flex State Parameter 248	
Flex State Parameter 249	
Flex State Parameter 250	
Flex State Parameter 251	
Flex State Parameter 252	
Flex State Parameter 253	
Flex State Parameter 254	
Flex State Parameter 255	
Flex State Parameter 256	
USER DISPLAY 1	
Top Line	
Bottom Line	
Item 1	
Item 2	
Item 3	
Item 4	
Item 5	
USER DISPLAY 2	
Top Line	
Bottom Line	
Item 1	
Item 2	
Item 3	
Item 4	
Item 5	
USER DISPLAY 3	
Top Line	
Bottom Line	
Item 1	
Item 2	

Table 10–1: PRODUCT SETUP (Sheet 15 of 16)

SETTING	VALUE
Item 3	
Item 4	
Item 5	
USER DISPLAY 4	
Top Line	
Bottom Line	
Item 1	
Item 2	
Item 3	
Item 4	
Item 5	
USER DISPLAY 5	
Top Line	
Bottom Line	
Item 1	
Item 2	
Item 3	
Item 4	
Item 5	
USER DISPLAY 6	
Top Line	
Bottom Line	
Item 1	
Item 2	
Item 3	
Item 4	
Item 5	
USER DISPLAY 7	
Top Line	
Bottom Line	
Item 1	
Item 2	
Item 3	
Item 4	
Item 5	
USER DISPLAY 8	
Top Line	
Bottom Line	
Item 1	

Table 10–1: PRODUCT SETUP (Sheet 16 of 16)

SETTING	VALUE
Item 2	
Item 3	
Item 4	
Item 5	
INSTALLATION	
Relay Settings	
Relay Name	

10.2.1 SETTINGS

Table 10–2: SYSTEM SETUP (Sheet 1 of 4)

SETTING	VALUE
CURRENT BANK 1	
Phase CT _____ Primary	
Phase CT _____ Secondary	
Ground CT _____ Primary	
Ground CT _____ Secondary	
CURRENT BANK 2	
Phase CT _____ Primary	
Phase CT _____ Secondary	
Ground CT _____ Primary	
Ground CT _____ Secondary	
CURRENT BANK 3	
Phase CT _____ Primary	
Phase CT _____ Secondary	
Ground CT _____ Primary	
Ground CT _____ Secondary	
CURRENT BANK 4	
Phase CT _____ Primary	
Phase CT _____ Secondary	
Ground CT _____ Primary	
Ground CT _____ Secondary	
CURRENT BANK 5	
Phase CT _____ Primary	
Phase CT _____ Secondary	
Ground CT _____ Primary	
Ground CT _____ Secondary	
CURRENT BANK 6	
Phase CT _____ Primary	
Phase CT _____ Secondary	
Ground CT _____ Primary	
Ground CT _____ Secondary	
VOLTAGE BANK 1	
Phase VT _____ Connection	
Phase VT _____ Secondary	
Phase VT _____ Ratio	
Auxiliary VT _____ Connection	
Auxiliary VT _____ Secondary	

Table 10–2: SYSTEM SETUP (Sheet 2 of 4)

SETTING	VALUE
Auxiliary VT _____ Ratio	
VOLTAGE BANK 2	
Phase VT _____ Connection	
Phase VT _____ Secondary	
Phase VT _____ Ratio	
Auxiliary VT _____ Connection	
Auxiliary VT _____ Secondary	
Auxiliary VT _____ Ratio	
VOLTAGE BANK 3	
Phase VT _____ Connection	
Phase VT _____ Secondary	
Phase VT _____ Ratio	
Auxiliary VT _____ Connection	
Auxiliary VT _____ Secondary	
Auxiliary VT _____ Ratio	
POWER SYSTEM	
Nominal Frequency	
Phase Rotation	
Frequency and Phase Reference	
Frequency Tracking	
SIGNAL SOURCE 1	
Source Name	
Phase CT	
Ground CT	
Phase VT	
Auxiliary VT	
SIGNAL SOURCE 2	
Source Name	
Phase CT	
Ground CT	
Phase VT	
Auxiliary VT	
SIGNAL SOURCE 3	
Source Name	
Phase CT	
Ground CT	

Table 10–2: SYSTEM SETUP (Sheet 3 of 4)

SETTING	VALUE
Phase VT	
Auxiliary VT	
SIGNAL SOURCE 4	
Source Name	
Phase CT	
Ground CT	
Phase VT	
Auxiliary VT	
SIGNAL SOURCE 5	
Source Name	
Phase CT	
Ground CT	
Phase VT	
Auxiliary VT	
SIGNAL SOURCE 6	
Source Name	
Phase CT	
Ground CT	
Phase VT	
Auxiliary VT	
L60 POWER SYSTEM	
Number of Terminals	
Number of Channels	
LINE	
Pos. Seq. Impedance Magnitude	
Pos. Seq. Impedance Angle	
Zero Seq. Impedance Magnitude	
Zero Seq. Impedance Angle	
Line Length Units	
Line Length	
BREAKER 1	
Function	
Pushbutton Control	
Name	
Mode	
Open	
Close	
Φ A/3-Pole	
Φ B	

Table 10–2: SYSTEM SETUP (Sheet 4 of 4)

SETTING	VALUE
Φ C	
Ext Alarm	
Alarm Delay	
Manual Close Recall Time	
BREAKER 2	
Function	
Pushbutton Control	
Name	
Mode	
Open	
Close	
Φ A/3-Pole	
Φ B	
Φ C	
Ext Alarm	
Alarm Delay	
Manual Close Recall Time	

FLEXCURVE A

Table 10–3: FLEXCURVE™ TABLE

RESET	TIME ms	RESET	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms
0.00		0.68		1.03		2.9		4.9		10.5	
0.05		0.70		1.05		3.0		5.0		11.0	
0.10		0.72		1.1		3.1		5.1		11.5	
0.15		0.74		1.2		3.2		5.2		12.0	
0.20		0.76		1.3		3.3		5.3		12.5	
0.25		0.78		1.4		3.4		5.4		13.0	
0.30		0.80		1.5		3.5		5.5		13.5	
0.35		0.82		1.6		3.6		5.6		14.0	
0.40		0.84		1.7		3.7		5.7		14.5	
0.45		0.86		1.8		3.8		5.8		15.0	
0.48		0.88		1.9		3.9		5.9		15.5	
0.50		0.90		2.0		4.0		6.0		16.0	
0.52		0.91		2.1		4.1		6.5		16.5	
0.54		0.92		2.2		4.2		7.0		17.0	
0.56		0.93		2.3		4.3		7.5		17.5	
0.58		0.94		2.4		4.4		8.0		18.0	
0.60		0.95		2.5		4.5		8.5		18.5	
0.62		0.96		2.6		4.6		9.0		19.0	
0.64		0.97		2.7		4.7		9.5		19.5	
0.66		0.98		2.8		4.8		10.0		20.0	

FLEXCURVE B

Table 10–4: FLEXCURVE™ TABLE

RESET	TIME ms	RESET	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms	OPERATE	TIME ms
0.00		0.68		1.03		2.9		4.9		10.5	
0.05		0.70		1.05		3.0		5.0		11.0	
0.10		0.72		1.1		3.1		5.1		11.5	
0.15		0.74		1.2		3.2		5.2		12.0	
0.20		0.76		1.3		3.3		5.3		12.5	
0.25		0.78		1.4		3.4		5.4		13.0	
0.30		0.80		1.5		3.5		5.5		13.5	
0.35		0.82		1.6		3.6		5.6		14.0	
0.40		0.84		1.7		3.7		5.7		14.5	
0.45		0.86		1.8		3.8		5.8		15.0	
0.48		0.88		1.9		3.9		5.9		15.5	
0.50		0.90		2.0		4.0		6.0		16.0	
0.52		0.91		2.1		4.1		6.5		16.5	
0.54		0.92		2.2		4.2		7.0		17.0	
0.56		0.93		2.3		4.3		7.5		17.5	
0.58		0.94		2.4		4.4		8.0		18.0	
0.60		0.95		2.5		4.5		8.5		18.5	
0.62		0.96		2.6		4.6		9.0		19.0	
0.64		0.97		2.7		4.7		9.5		19.5	
0.66		0.98		2.8		4.8		10.0		20.0	

10.3.1 SETTINGS

Table 10–5: FLEXLOGIC™ (Sheet 1 of 17)

SETTING	VALUE
FLEXLOGIC EQUATION EDITOR	
FlexLogic Entry 1	
FlexLogic Entry 2	
FlexLogic Entry 3	
FlexLogic Entry 4	
FlexLogic Entry 5	
FlexLogic Entry 6	
FlexLogic Entry 7	
FlexLogic Entry 8	
FlexLogic Entry 9	
FlexLogic Entry 10	
FlexLogic Entry 11	
FlexLogic Entry 12	
FlexLogic Entry 13	
FlexLogic Entry 14	
FlexLogic Entry 15	
FlexLogic Entry 16	
FlexLogic Entry 17	
FlexLogic Entry 18	
FlexLogic Entry 19	
FlexLogic Entry 20	
FlexLogic Entry 21	
FlexLogic Entry 22	
FlexLogic Entry 23	
FlexLogic Entry 24	
FlexLogic Entry 25	
FlexLogic Entry 26	
FlexLogic Entry 27	
FlexLogic Entry 28	
FlexLogic Entry 29	
FlexLogic Entry 30	
FlexLogic Entry 31	
FlexLogic Entry 32	
FlexLogic Entry 33	
FlexLogic Entry 34	
FlexLogic Entry 35	

Table 10–5: FLEXLOGIC™ (Sheet 2 of 17)

SETTING	VALUE
FlexLogic Entry 36	
FlexLogic Entry 37	
FlexLogic Entry 38	
FlexLogic Entry 39	
FlexLogic Entry 40	
FlexLogic Entry 41	
FlexLogic Entry 42	
FlexLogic Entry 43	
FlexLogic Entry 44	
FlexLogic Entry 45	
FlexLogic Entry 46	
FlexLogic Entry 47	
FlexLogic Entry 48	
FlexLogic Entry 49	
FlexLogic Entry 50	
FlexLogic Entry 51	
FlexLogic Entry 52	
FlexLogic Entry 53	
FlexLogic Entry 54	
FlexLogic Entry 55	
FlexLogic Entry 56	
FlexLogic Entry 57	
FlexLogic Entry 58	
FlexLogic Entry 59	
FlexLogic Entry 60	
FlexLogic Entry 61	
FlexLogic Entry 62	
FlexLogic Entry 63	
FlexLogic Entry 64	
FlexLogic Entry 65	
FlexLogic Entry 66	
FlexLogic Entry 67	
FlexLogic Entry 68	
FlexLogic Entry 69	
FlexLogic Entry 70	
FlexLogic Entry 71	

Table 10–5: FLEXLOGIC™ (Sheet 3 of 17)

SETTING	VALUE
FlexLogic Entry 72	
FlexLogic Entry 73	
FlexLogic Entry 74	
FlexLogic Entry 75	
FlexLogic Entry 76	
FlexLogic Entry 77	
FlexLogic Entry 78	
FlexLogic Entry 79	
FlexLogic Entry 80	
FlexLogic Entry 81	
FlexLogic Entry 82	
FlexLogic Entry 83	
FlexLogic Entry 84	
FlexLogic Entry 85	
FlexLogic Entry 86	
FlexLogic Entry 87	
FlexLogic Entry 88	
FlexLogic Entry 89	
FlexLogic Entry 90	
FlexLogic Entry 91	
FlexLogic Entry 92	
FlexLogic Entry 93	
FlexLogic Entry 94	
FlexLogic Entry 95	
FlexLogic Entry 96	
FlexLogic Entry 97	
FlexLogic Entry 98	
FlexLogic Entry 99	
FlexLogic Entry 100	
FlexLogic Entry 101	
FlexLogic Entry 102	
FlexLogic Entry 103	
FlexLogic Entry 104	
FlexLogic Entry 105	
FlexLogic Entry 106	
FlexLogic Entry 107	
FlexLogic Entry 108	
FlexLogic Entry 109	
FlexLogic Entry 110	

Table 10–5: FLEXLOGIC™ (Sheet 4 of 17)

SETTING	VALUE
FlexLogic Entry 111	
FlexLogic Entry 112	
FlexLogic Entry 113	
FlexLogic Entry 114	
FlexLogic Entry 115	
FlexLogic Entry 116	
FlexLogic Entry 117	
FlexLogic Entry 118	
FlexLogic Entry 119	
FlexLogic Entry 120	
FlexLogic Entry 121	
FlexLogic Entry 122	
FlexLogic Entry 123	
FlexLogic Entry 124	
FlexLogic Entry 125	
FlexLogic Entry 126	
FlexLogic Entry 127	
FlexLogic Entry 128	
FlexLogic Entry 129	
FlexLogic Entry 130	
FlexLogic Entry 131	
FlexLogic Entry 132	
FlexLogic Entry 133	
FlexLogic Entry 134	
FlexLogic Entry 135	
FlexLogic Entry 136	
FlexLogic Entry 137	
FlexLogic Entry 138	
FlexLogic Entry 139	
FlexLogic Entry 140	
FlexLogic Entry 141	
FlexLogic Entry 142	
FlexLogic Entry 143	
FlexLogic Entry 144	
FlexLogic Entry 145	
FlexLogic Entry 146	
FlexLogic Entry 147	
FlexLogic Entry 148	
FlexLogic Entry 149	

Table 10–5: FLEXLOGIC™ (Sheet 5 of 17)

SETTING	VALUE
FlexLogic Entry 150	
FlexLogic Entry 151	
FlexLogic Entry 152	
FlexLogic Entry 153	
FlexLogic Entry 154	
FlexLogic Entry 155	
FlexLogic Entry 156	
FlexLogic Entry 157	
FlexLogic Entry 158	
FlexLogic Entry 159	
FlexLogic Entry 160	
FlexLogic Entry 161	
FlexLogic Entry 162	
FlexLogic Entry 163	
FlexLogic Entry 164	
FlexLogic Entry 165	
FlexLogic Entry 166	
FlexLogic Entry 167	
FlexLogic Entry 168	
FlexLogic Entry 169	
FlexLogic Entry 170	
FlexLogic Entry 171	
FlexLogic Entry 172	
FlexLogic Entry 173	
FlexLogic Entry 174	
FlexLogic Entry 175	
FlexLogic Entry 176	
FlexLogic Entry 177	
FlexLogic Entry 178	
FlexLogic Entry 179	
FlexLogic Entry 180	
FlexLogic Entry 181	
FlexLogic Entry 182	
FlexLogic Entry 183	
FlexLogic Entry 184	
FlexLogic Entry 185	
FlexLogic Entry 186	
FlexLogic Entry 187	
FlexLogic Entry 188	

Table 10–5: FLEXLOGIC™ (Sheet 6 of 17)

SETTING	VALUE
FlexLogic Entry 189	
FlexLogic Entry 190	
FlexLogic Entry 191	
FlexLogic Entry 192	
FlexLogic Entry 193	
FlexLogic Entry 194	
FlexLogic Entry 195	
FlexLogic Entry 196	
FlexLogic Entry 197	
FlexLogic Entry 198	
FlexLogic Entry 199	
FlexLogic Entry 200	
FlexLogic Entry 201	
FlexLogic Entry 202	
FlexLogic Entry 203	
FlexLogic Entry 204	
FlexLogic Entry 205	
FlexLogic Entry 206	
FlexLogic Entry 207	
FlexLogic Entry 208	
FlexLogic Entry 209	
FlexLogic Entry 210	
FlexLogic Entry 211	
FlexLogic Entry 212	
FlexLogic Entry 213	
FlexLogic Entry 214	
FlexLogic Entry 215	
FlexLogic Entry 216	
FlexLogic Entry 217	
FlexLogic Entry 218	
FlexLogic Entry 219	
FlexLogic Entry 220	
FlexLogic Entry 221	
FlexLogic Entry 222	
FlexLogic Entry 223	
FlexLogic Entry 224	
FlexLogic Entry 225	
FlexLogic Entry 226	
FlexLogic Entry 227	

Table 10–5: FLEXLOGIC™ (Sheet 7 of 17)

SETTING	VALUE
FlexLogic Entry 228	
FlexLogic Entry 229	
FlexLogic Entry 230	
FlexLogic Entry 231	
FlexLogic Entry 232	
FlexLogic Entry 233	
FlexLogic Entry 234	
FlexLogic Entry 235	
FlexLogic Entry 236	
FlexLogic Entry 237	
FlexLogic Entry 238	
FlexLogic Entry 239	
FlexLogic Entry 240	
FlexLogic Entry 241	
FlexLogic Entry 242	
FlexLogic Entry 243	
FlexLogic Entry 244	
FlexLogic Entry 245	
FlexLogic Entry 246	
FlexLogic Entry 247	
FlexLogic Entry 248	
FlexLogic Entry 249	
FlexLogic Entry 250	
FlexLogic Entry 251	
FlexLogic Entry 252	
FlexLogic Entry 253	
FlexLogic Entry 254	
FlexLogic Entry 255	
FlexLogic Entry 256	
FlexLogic Entry 257	
FlexLogic Entry 258	
FlexLogic Entry 259	
FlexLogic Entry 260	
FlexLogic Entry 261	
FlexLogic Entry 262	
FlexLogic Entry 263	
FlexLogic Entry 264	
FlexLogic Entry 265	
FlexLogic Entry 266	

Table 10–5: FLEXLOGIC™ (Sheet 8 of 17)

SETTING	VALUE
FlexLogic Entry 267	
FlexLogic Entry 268	
FlexLogic Entry 269	
FlexLogic Entry 270	
FlexLogic Entry 271	
FlexLogic Entry 272	
FlexLogic Entry 273	
FlexLogic Entry 274	
FlexLogic Entry 275	
FlexLogic Entry 276	
FlexLogic Entry 277	
FlexLogic Entry 278	
FlexLogic Entry 279	
FlexLogic Entry 280	
FlexLogic Entry 281	
FlexLogic Entry 282	
FlexLogic Entry 283	
FlexLogic Entry 284	
FlexLogic Entry 285	
FlexLogic Entry 286	
FlexLogic Entry 287	
FlexLogic Entry 288	
FlexLogic Entry 289	
FlexLogic Entry 290	
FlexLogic Entry 291	
FlexLogic Entry 292	
FlexLogic Entry 293	
FlexLogic Entry 294	
FlexLogic Entry 295	
FlexLogic Entry 296	
FlexLogic Entry 297	
FlexLogic Entry 298	
FlexLogic Entry 299	
FlexLogic Entry 300	
FlexLogic Entry 301	
FlexLogic Entry 302	
FlexLogic Entry 303	
FlexLogic Entry 304	
FlexLogic Entry 305	

Table 10–5: FLEXLOGIC™ (Sheet 9 of 17)

SETTING	VALUE
FlexLogic Entry 306	
FlexLogic Entry 307	
FlexLogic Entry 308	
FlexLogic Entry 309	
FlexLogic Entry 310	
FlexLogic Entry 311	
FlexLogic Entry 312	
FlexLogic Entry 313	
FlexLogic Entry 314	
FlexLogic Entry 315	
FlexLogic Entry 316	
FlexLogic Entry 317	
FlexLogic Entry 318	
FlexLogic Entry 319	
FlexLogic Entry 320	
FlexLogic Entry 321	
FlexLogic Entry 322	
FlexLogic Entry 323	
FlexLogic Entry 324	
FlexLogic Entry 325	
FlexLogic Entry 326	
FlexLogic Entry 327	
FlexLogic Entry 328	
FlexLogic Entry 329	
FlexLogic Entry 330	
FlexLogic Entry 331	
FlexLogic Entry 332	
FlexLogic Entry 333	
FlexLogic Entry 334	
FlexLogic Entry 335	
FlexLogic Entry 336	
FlexLogic Entry 337	
FlexLogic Entry 338	
FlexLogic Entry 339	
FlexLogic Entry 340	
FlexLogic Entry 341	
FlexLogic Entry 342	
FlexLogic Entry 343	
FlexLogic Entry 344	

Table 10–5: FLEXLOGIC™ (Sheet 10 of 17)

SETTING	VALUE
FlexLogic Entry 345	
FlexLogic Entry 346	
FlexLogic Entry 347	
FlexLogic Entry 348	
FlexLogic Entry 349	
FlexLogic Entry 350	
FlexLogic Entry 351	
FlexLogic Entry 352	
FlexLogic Entry 353	
FlexLogic Entry 354	
FlexLogic Entry 355	
FlexLogic Entry 356	
FlexLogic Entry 357	
FlexLogic Entry 358	
FlexLogic Entry 359	
FlexLogic Entry 360	
FlexLogic Entry 361	
FlexLogic Entry 362	
FlexLogic Entry 363	
FlexLogic Entry 364	
FlexLogic Entry 365	
FlexLogic Entry 366	
FlexLogic Entry 367	
FlexLogic Entry 368	
FlexLogic Entry 369	
FlexLogic Entry 370	
FlexLogic Entry 371	
FlexLogic Entry 372	
FlexLogic Entry 373	
FlexLogic Entry 374	
FlexLogic Entry 375	
FlexLogic Entry 376	
FlexLogic Entry 377	
FlexLogic Entry 378	
FlexLogic Entry 379	
FlexLogic Entry 380	
FlexLogic Entry 381	
FlexLogic Entry 382	
FlexLogic Entry 383	

Table 10–5: FLEXLOGIC™ (Sheet 11 of 17)

SETTING	VALUE
FlexLogic Entry 384	
FlexLogic Entry 385	
FlexLogic Entry 386	
FlexLogic Entry 387	
FlexLogic Entry 388	
FlexLogic Entry 389	
FlexLogic Entry 390	
FlexLogic Entry 391	
FlexLogic Entry 392	
FlexLogic Entry 393	
FlexLogic Entry 394	
FlexLogic Entry 395	
FlexLogic Entry 396	
FlexLogic Entry 397	
FlexLogic Entry 398	
FlexLogic Entry 399	
FlexLogic Entry 400	
FlexLogic Entry 401	
FlexLogic Entry 402	
FlexLogic Entry 403	
FlexLogic Entry 404	
FlexLogic Entry 405	
FlexLogic Entry 406	
FlexLogic Entry 407	
FlexLogic Entry 408	
FlexLogic Entry 409	
FlexLogic Entry 410	
FlexLogic Entry 411	
FlexLogic Entry 412	
FlexLogic Entry 413	
FlexLogic Entry 414	
FlexLogic Entry 415	
FlexLogic Entry 416	
FlexLogic Entry 417	
FlexLogic Entry 418	
FlexLogic Entry 419	
FlexLogic Entry 420	
FlexLogic Entry 421	
FlexLogic Entry 422	

Table 10–5: FLEXLOGIC™ (Sheet 12 of 17)

SETTING	VALUE
FlexLogic Entry 423	
FlexLogic Entry 424	
FlexLogic Entry 425	
FlexLogic Entry 426	
FlexLogic Entry 427	
FlexLogic Entry 428	
FlexLogic Entry 429	
FlexLogic Entry 430	
FlexLogic Entry 431	
FlexLogic Entry 432	
FlexLogic Entry 433	
FlexLogic Entry 434	
FlexLogic Entry 435	
FlexLogic Entry 436	
FlexLogic Entry 437	
FlexLogic Entry 438	
FlexLogic Entry 439	
FlexLogic Entry 440	
FlexLogic Entry 441	
FlexLogic Entry 442	
FlexLogic Entry 443	
FlexLogic Entry 444	
FlexLogic Entry 445	
FlexLogic Entry 446	
FlexLogic Entry 447	
FlexLogic Entry 448	
FlexLogic Entry 449	
FlexLogic Entry 450	
FlexLogic Entry 451	
FlexLogic Entry 452	
FlexLogic Entry 453	
FlexLogic Entry 454	
FlexLogic Entry 455	
FlexLogic Entry 456	
FlexLogic Entry 457	
FlexLogic Entry 458	
FlexLogic Entry 459	
FlexLogic Entry 460	
FlexLogic Entry 461	

Table 10–5: FLEXLOGIC™ (Sheet 13 of 17)

SETTING	VALUE
FlexLogic Entry 462	
FlexLogic Entry 463	
FlexLogic Entry 464	
FlexLogic Entry 465	
FlexLogic Entry 466	
FlexLogic Entry 467	
FlexLogic Entry 468	
FlexLogic Entry 469	
FlexLogic Entry 470	
FlexLogic Entry 471	
FlexLogic Entry 472	
FlexLogic Entry 473	
FlexLogic Entry 474	
FlexLogic Entry 475	
FlexLogic Entry 476	
FlexLogic Entry 477	
FlexLogic Entry 478	
FlexLogic Entry 479	
FlexLogic Entry 480	
FlexLogic Entry 481	
FlexLogic Entry 482	
FlexLogic Entry 483	
FlexLogic Entry 484	
FlexLogic Entry 485	
FlexLogic Entry 486	
FlexLogic Entry 487	
FlexLogic Entry 488	
FlexLogic Entry 489	
FlexLogic Entry 490	
FlexLogic Entry 491	
FlexLogic Entry 492	
FlexLogic Entry 493	
FlexLogic Entry 494	
FlexLogic Entry 495	
FlexLogic Entry 496	
FlexLogic Entry 497	
FlexLogic Entry 498	
FlexLogic Entry 499	
FlexLogic Entry 500	

Table 10–5: FLEXLOGIC™ (Sheet 14 of 17)

SETTING	VALUE
FlexLogic Entry 501	
FlexLogic Entry 502	
FlexLogic Entry 503	
FlexLogic Entry 504	
FlexLogic Entry 505	
FlexLogic Entry 506	
FlexLogic Entry 507	
FlexLogic Entry 508	
FlexLogic Entry 509	
FlexLogic Entry 510	
FlexLogic Entry 511	
FlexLogic Entry 512	
FLEXLOGIC TIMER 1	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 2	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 3	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 4	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 5	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 6	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 7	
FlexLogic Timer Type	
FlexLogic Timer Pickup	

Table 10–5: FLEXLOGIC™ (Sheet 15 of 17)

SETTING	VALUE
Dropout Delay	
FLEXLOGIC TIMER 8	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 9	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 10	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 11	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 12	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 13	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 14	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 15	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 1	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 16	
FlexLogic Timer Type	

Table 10–5: FLEXLOGIC™ (Sheet 16 of 17)

SETTING	VALUE
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 17	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 18	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 19	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 20	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 21	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 22	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 23	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 24	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 25	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	

Table 10–5: FLEXLOGIC™ (Sheet 17 of 17)

SETTING	VALUE
FLEXLOGIC TIMER 26	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 27	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 28	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 29	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 30	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 31	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	
FLEXLOGIC TIMER 32	
FlexLogic Timer Type	
FlexLogic Timer Pickup	
Dropout Delay	

10.4.1 SETTINGS

Table 10–6: GROUPED ELEMENTS (Sheet 1 of 9)

SETTING	VALUE
LINE ELEMENTS	
LINE PICKUP	
Line Pickup Function	
Line Pickup Signal Source	
Phase IOC Line Pickup	
Positive Seq. UV Pickup	
Line End Open Pickup Delay	
Line End Open Reset Delay	
Positive Seq. OV Pickup Delay	
AR CO-ORD Bypass	
AR CO-ORD Pickup Delay	
AR CO-ORD Reset Delay	
Line Pickup Block	
Line Pickup Target	
Line Pickup Events	
DISTANCE ELEMENTS	
DISTANCE	
Distance Source	
Memory Duration	
PHASE DISTANCE Z2 MHO	
Function	
Supervision	
Reach	
Direction	
Comp. Limit	
Delay	
Block	
Target	
Events	
GROUND DISTANCE Z2 MHO	
Function	
Supervision	
Reach	
Direction	
Comp. Limit	
Delay	

Table 10–6: GROUPED ELEMENTS (Sheet 2 of 9)

SETTING	VALUE
Block	
Target	
Events	
POWER SWING DETECT	
Power Swing Function	
Power Swing Source	
Power Swing Mode	
Power Swing Supv.	
Power Swing Fwd. Reach	
Power Swing Fwd. RCA	
Power Swing Rev. Reach	
Power Swing Outer Limit Angle	
Power Swing Middle Limit Angle	
Power Swing Inner Limit Angle	
Power Swing Pickup Delay 1	
Power Swing Reset Delay 1	
Power Swing Pickup Delay 2	
Power Swing Pickup Delay 3	
Power Swing Pickup Delay 4	
Power Swing Seal-In Delay 1	
Power Swing Trip Mode	
Power Swing Block	
Power Swing Target	
Power Swing Events	
CURRENT ELEMENTS	
PHASE TOC1	
Phase TOC1 Function	
Phase TOC1 Signal Source	
Phase TOC1 Input	
Phase TOC1 Pickup	
Phase TOC1 Curve	
Phase TOC1 Multiplier	
Phase TOC1 Reset	
Phase TOC1 Voltage Restraint	
Phase TOC1 Block A	
Phase TOC1 Block B	

Table 10–6: GROUPED ELEMENTS (Sheet 3 of 9)

SETTING	VALUE
Phase TOC1 Block C	
Phase TOC1 Target	
Phase TOC1 Events	
PHASE TOC2	
Phase TOC2 Function	
Phase TOC2 Signal Source	
Phase TOC2 Input	
Phase TOC2 Pickup	
Phase TOC2 Curve	
Phase TOC2 Multiplier	
Phase TOC2 Reset	
Phase TOC2 Voltage Restraint	
Phase TOC2 Block A	
Phase TOC2 Block B	
Phase TOC2 Block C	
Phase TOC2 Target	
Phase TOC2 Events	
PHASE IOC1	
Phase IOC1 Function	
Phase IOC1 Signal Source	
Phase IOC1 Pickup	
Phase IOC1 Pickup Delay	
Phase IOC1 Reset Delay	
Phase IOC1 Block A	
Phase IOC1 Block B	
Phase IOC1 Block C	
Phase IOC1 Target	
Phase IOC1 Events	
PHASE IOC2	
Phase IOC2 Function	
Phase IOC2 Signal Source	
Phase IOC2 Pickup	
Phase IOC2 Pickup Delay	
Phase IOC2 Reset Delay	
Phase IOC2 Block A	
Phase IOC2 Block B	
Phase IOC2 Block C	
Phase IOC2 Target	
Phase IOC2 Events	

Table 10–6: GROUPED ELEMENTS (Sheet 4 of 9)

SETTING	VALUE
NEUTRAL TOC1	
Neutral TOC1 Function	
Neutral TOC1 Signal Source	
Neutral TOC1 Input	
Neutral TOC1 Pickup	
Neutral TOC1 Curve	
Neutral TOC1 TD Multiplier	
Neutral TOC1 Reset	
Neutral TOC1 Block	
Neutral TOC1 Target	
Neutral TOC1 Events	
NEUTRAL TOC2	
Neutral TOC2 Function	
Neutral TOC2 Signal Source	
Neutral TOC2 Input	
Neutral TOC2 Pickup	
Neutral TOC2 Curve	
Neutral TOC2 TD Multiplier	
Neutral TOC2 Reset	
Neutral TOC2 Block	
Neutral TOC2 Target	
Neutral TOC2 Events	
NEUTRAL IOC1	
Neutral IOC1 Function	
Neutral IOC1 Signal Source	
Neutral IOC1 Pickup	
Neutral IOC1 Pickup Delay	
Neutral IOC1 Reset Delay	
Neutral IOC1 Block	
Neutral IOC1 Target	
Neutral IOC1 Events	
NEUTRAL IOC2	
Neutral IOC2 Function	
Neutral IOC2 Signal Source	
Neutral IOC2 Pickup	
Neutral IOC2 Pickup Delay	
Neutral IOC2 Reset Delay	
Neutral IOC2 Block	
Neutral IOC2 Target	

Table 10–6: GROUPED ELEMENTS (Sheet 5 of 9)

SETTING	VALUE
Neutral IOC2 Events	
GROUND TOC1	
Ground TOC1 Function	
Ground TOC1 Signal Source	
Ground TOC1 Input	
Ground TOC1 Pickup	
Ground TOC1 Curve	
Ground TOC1 TD Multiplier	
Ground TOC1 Reset	
Ground TOC1 Block	
Ground TOC1 Target	
Ground TOC1 Events	
GROUND TOC2	
Ground TOC2 Function	
Ground TOC2 Signal Source	
Ground TOC2 Input	
Ground TOC2 Pickup	
Ground TOC2 Curve	
Ground TOC2 TD Multiplier	
Ground TOC2 Reset	
Ground TOC2 Block	
Ground TOC2 Target	
Ground TOC2 Events	
GROUND IOC1	
Ground IOC1 Function	
Ground IOC1 Signal Source	
Ground IOC1 Pickup	
Ground IOC1 Pickup Delay	
Ground IOC1 Reset Delay	
Ground IOC1 Block	
Ground IOC1 Target	
Ground IOC1 Events	
GROUND IOC2	
Ground IOC2 Function	
Ground IOC2 Signal Source	
Ground IOC2 Pickup	
Ground IOC2 Pickup Delay	
Ground IOC2 Reset Delay	
Ground IOC2 Block	

Table 10–6: GROUPED ELEMENTS (Sheet 6 of 9)

SETTING	VALUE
Ground IOC2 Target	
Ground IOC2 Events	
NEG SEQ TOC1	
Neg. Seq. TOC1 Function	
Neg. Seq. TOC1 Signal Source	
Neg. Seq. TOC1 Pickup	
Neg. Seq. TOC1 Curve	
Neg. Seq. TOC1 TD Multiplier	
Neg. Seq. TOC1 Reset	
Neg. Seq. TOC1 Block	
Neg. Seq. TOC1 Target	
Neg. Seq. TOC1 Events	
NEG SEQ TOC2	
Neg. Seq. TOC2 Function	
Neg. Seq. TOC2 Signal Source	
Neg. Seq. TOC2 Pickup	
Neg. Seq. TOC2 Curve	
Neg. Seq. TOC2 TD Multiplier	
Neg. Seq. TOC2 Reset	
Neg. Seq. TOC2 Block	
Neg. Seq. TOC2 Target	
Neg. Seq. TOC2 Events	
NEG SEQ IOC1	
Neg. Seq. IOC1 Function	
Neg. Seq. IOC1 Signal Source	
Neg. Seq. IOC1 Pickup	
Neg. Seq. IOC1 Pickup Delay	
Neg. Seq. IOC1 Reset Delay	
Neg. Seq. IOC1 Block	
Neg. Seq. IOC1 Target	
Neg. Seq. IOC1 Events	
NEG SEQ IOC2	
Neg. Seq. IOC2 Function	
Neg. Seq. IOC2 Signal Source	
Neg. Seq. IOC2 Pickup	
Neg. Seq. IOC2 Pickup Delay	
Neg. Seq. IOC2 Reset Delay	
Neg. Seq. IOC2 Block	
Neg. Seq. IOC2 Target	

Table 10–6: GROUPED ELEMENTS (Sheet 7 of 9)

SETTING	VALUE
Neg. Seq. IOC2 Events	
BREAKER FAILURE ELEMENTS	
BREAKER FAILURE 1	
Function	
Mode	
Use AMP SUPV	
Use Seal-In	
3-Pole Initiate	
Block	
PH AMP SUPV	
N AMP SUPV	
Use Timer 1	
Timer 1 Pickup Delay	
Use Timer 2	
Timer 2 Pickup Delay	
Use Timer 3	
Timer 3 Pickup Delay	
BKR POS1 Φ A/3P	
BKR POS2 Φ A/3P	
Breaker Test On	
PH AMP HASET	
N AMP HASET	
PH AMP LOSET	
N AMP LOSET	
LOSET Time Delay	
Trip Dropout Delay	
Target	
Events	
PH A Initiate	
PH B Initiate	
PH C Initiate	
BKR POS1 Φ B	
BKR POS1 Φ C	
BKR POS2 Φ B	
BKR POS2 Φ C	
BREAKER FAILURE 2	
Function	
Mode	
Use AMP SUPV	

Table 10–6: GROUPED ELEMENTS (Sheet 8 of 9)

SETTING	VALUE
Use Seal-In	
3-Pole Initiate	
Block	
PH AMP SUPV	
N AMP SUPV	
Use Timer 1	
Timer 1 Pickup Delay	
Use Timer 2	
Timer 2 Pickup Delay	
Use Timer 3	
Timer 3 Pickup Delay	
BKR POS1 Φ A/3P	
BKR POS2 Φ A/3P	
Breaker Test On	
PH AMP HASET	
N AMP HASET	
PH AMP LOSET	
N AMP LOSET	
LOSET Time Delay	
Trip Dropout Delay	
Target	
Events	
PH A Initiate	
PH B Initiate	
PH C Initiate	
BKR POS1 Φ B	
BKR POS1 Φ C	
BKR POS2 Φ B	
BKR POS2 Φ C	
VOLTAGE ELEMENTS	
PHASE UNDERVOLTAGE 1	
Function	
Signal Source	
Mode	
Pickup	
Curve	
Delay	
Minimum Voltage	
Block	

Table 10–6: GROUPED ELEMENTS (Sheet 9 of 9)

SETTING	VALUE
Target	
Events	
PHASE UNDERVOLTAGE 2	
Function	
Signal Source	
Mode	
Pickup	
Curve	
Delay	
Minimum Voltage	
Block	
Target	
Events	
PHASE OVERVOLTAGE 1	
Function	
Signal Source	
Pickup	
Delay	
Reset Delay	
Block	
Target	
Events	
SUPERVISING ELEMENTS	
DISTURBANCE DETECTOR	
DD Function	
DD Non-Current Supervision	
DD Control Logic	
DD Logic Seal-In	
DD Events	

10.5.1 SETTINGS

Table 10–7: CONTROL ELEMENTS (Sheet 1 of 11)

SETTING	VALUE
SETTINGS GROUPS	
Setting Groups Function	
Setting Groups Block	
Group 2 Activate On	
Group 3 Activate On	
Group 4 Activate On	
Group 5 Activate On	
Group 6 Activate On	
Group 7 Activate On	
Group 8 Activate On	
Setting Group Events	
SYNCHROCHECK 1	
Function	
Block	
V1 Source	
V2 Source	
Max. Voltage Difference	
Max. Angle Difference	
Max. Frequency Difference	
Dead Source Select	
Dead V1 Max. Volt	
Dead V2 Max. Volt	
Line V1 Min. Volt	
Line V2 Min. Volt	
Target	
Events	
SYNCHROCHECK 2	
Function	
Block	
V1 Source	
V2 Source	
Max. Voltage Difference	
Max. Angle Difference	
Max. Frequency Difference	
Dead Source Select	
Dead V1 Max. Volt	

Table 10–7: CONTROL ELEMENTS (Sheet 2 of 11)

SETTING	VALUE
Dead V2 Max. Volt	
Line V1 Min. Volt	
Line V2 Min. Volt	
Target	
Events	
AUTORECLOSE 1	
Function	
Initiate	
Block	
Max. Number of Shots	
Reduce Maximum to 1	
Reduce Maximum to 2	
Reduce Maximum to 3	
Manual Close	
Manual Reset from Lockout	
Reset Lockout If Breaker Closed	
Reset Lockout on Manual Close	
Breaker Closed	
Breaker Open	
Block Time Upon Manual Close	
Dead Time 1	
Dead Time 2	
Dead Time 3	
Dead Time 4	
Add Delay 1	
Delay 1	
Add Delay 2	
Delay 2	
Reset Lockout Delay	
Reset Time	
Incomplete Sequence Time	
Events	
DIGITAL ELEMENT 1	
Digital Element Function	
Digital Element Name	
Digital Element Input	

Table 10–7: CONTROL ELEMENTS (Sheet 3 of 11)

SETTING	VALUE
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 2	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 3	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 4	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 5	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	

Table 10–7: CONTROL ELEMENTS (Sheet 4 of 11)

SETTING	VALUE
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 6	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 7	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 8	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 9	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	

Table 10–7: CONTROL ELEMENTS (Sheet 5 of 11)

SETTING	VALUE
DIGITAL ELEMENT 10	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 11	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 12	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 13	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 14	
Digital Element Function	
Digital Element Name	

Table 10–7: CONTROL ELEMENTS (Sheet 6 of 11)

SETTING	VALUE
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 15	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL ELEMENT 16	
Digital Element Function	
Digital Element Name	
Digital Element Input	
Digital Element Pickup Delay	
Digital Element Reset Delay	
Digital Element Block	
Digital Element Target	
Digital Element Events	
DIGITAL COUNTER 1	
Counter 1 Function	
Counter 1 Name	
Counter 1 Units	
Counter 1 Preset	
Counter 1 Compare	
Counter 1 Up	
Counter 1 Down	
Counter 1 Block	
Counter 1 Set to Preset	
Counter 1 Reset	
Counter 1 Freeze/Reset	
Counter 1 Freeze/Count	
DIGITAL COUNTER 2	
Counter 2 Function	

Table 10–7: CONTROL ELEMENTS (Sheet 7 of 11)

SETTING	VALUE
Counter 2 Name	
Counter 2 Units	
Counter 2 Preset	
Counter 2 Compare	
Counter 2 Up	
Counter 2 Down	
Counter 2 Block	
Counter 2 Set to Preset	
Counter 2 Reset	
Counter 2 Freeze/Reset	
Counter 2 Freeze/Count	
DIGITAL COUNTER 3	
Counter 3 Function	
Counter 3 Name	
Counter 3 Units	
Counter 3 Preset	
Counter 3 Compare	
Counter 3 Up	
Counter 3 Down	
Counter 3 Block	
Counter 3 Set to Preset	
Counter 3 Reset	
Counter 3 Freeze/Reset	
Counter 3 Freeze/Count	
DIGITAL COUNTER 4	
Counter 4 Function	
Counter 4 Name	
Counter 4 Units	
Counter 4 Preset	
Counter 4 Compare	
Counter 4 Up	
Counter 4 Down	
Counter 4 Block	
Counter 4 Set to Preset	
Counter 4 Reset	
Counter 4 Freeze/Reset	
Counter 4 Freeze/Count	
DIGITAL COUNTER 5	
Counter 5 Function	

Table 10–7: CONTROL ELEMENTS (Sheet 8 of 11)

SETTING	VALUE
Counter 5 Name	
Counter 5 Units	
Counter 5 Preset	
Counter 5 Compare	
Counter 5 Up	
Counter 5 Down	
Counter 5 Block	
Counter 5 Set to Preset	
Counter 5 Reset	
Counter 5 Freeze/Reset	
Counter 5 Freeze/Count	
DIGITAL COUNTER 6	
Counter 6 Function	
Counter 6 Name	
Counter 6 Units	
Counter 6 Preset	
Counter 6 Compare	
Counter 6 Up	
Counter 6 Down	
Counter 6 Block	
Counter 6 Set to Preset	
Counter 6 Reset	
Counter 6 Freeze/Reset	
Counter 6 Freeze/Count	
DIGITAL COUNTER 7	
Counter 7 Function	
Counter 7 Name	
Counter 7 Units	
Counter 7 Preset	
Counter 7 Compare	
Counter 7 Up	
Counter 7 Down	
Counter 7 Block	
Counter 7 Set to Preset	
Counter 7 Reset	
Counter 7 Freeze/Reset	
Counter 7 Freeze/Count	
DIGITAL COUNTER 8	
Counter 8 Function	

Table 10–7: CONTROL ELEMENTS (Sheet 9 of 11)

SETTING	VALUE
Counter 8 Name	
Counter 8 Units	
Counter 8 Preset	
Counter 8 Compare	
Counter 8 Up	
Counter 8 Down	
Counter 8 Block	
Counter 8 Set to Preset	
Counter 8 Reset	
Counter 8 Freeze/Reset	
Counter 8 Freeze/Count	
BREAKER 1 ARCING CURRENT	
Function	
Source	
INIT	
Delay	
Limit	
Block	
Target	
Events	
BREAKER 2 ARCING CURRENT	
Function	
Source	
INIT	
Delay	
Limit	
Block	
Target	
Events	
CONTINUOUS MONITOR	
Function	
I-OP	
I-SUPV	
V-OP	
V-SUPV	
Target	
Events	
CT FAILURE DETECTOR	
Function	

Table 10–7: CONTROL ELEMENTS (Sheet 10 of 11)

SETTING	VALUE
Block	
I_0 Input 1	
I_0 Input 1 Pickup	
I_0 Input 2	
I_0 Input 2 Pickup	
V_0 Input	
V_0 Input Pickup	
Pickup Delay	
Target	
Events	
VT FUSE FAILURE	
Function	
POTT SCHEME	
Function	
Permissive Echo	
RX Pickup Delay	
Trans Block Pickup Delay	
Trans Block Reset Delay	
Echo Duration	
Line End Open Pickup Delay	
Seal-In Delay	
Gnd Directional O/C Forward	
RX	
87PC SCHEME	
Function	
Signal Source	
Scheme Select	
Signal	
Mixed Signal K	
FDL Pickup	
FDH Pickup	
FD Input	
Symmetry Ch. 1	
Symmetry Ch. 2	
Phase Delay Ch. 1	
Phase Delay Ch. 2	
Stability Angle	
Channel Fail	
Transient Pickup	

Table 10–7: CONTROL ELEMENTS (Sheet 11 of

SETTING	VALUE
Transient Reset	
Invert Ch. 1	
Invert Ch. 2	
Block	
Target	
Events	
OPEN BREAKER ECHO	
Open Breaker Keying	
Brk 1 Aux. Contact	
Brk 1 Contact Supv.	
Brk 2 Aux. Contact	
Brk 2 Contact Supv.	
Open Breaker Keying PKP Delay	
Open Breaker Keying RST Delay	
Weak-Infeed Keying	
Weak-Infeed Supv	
Weak-Infeed PKP Dly	
Weak-Infeed RST Dly	

10.6.1 CONTACT INPUTS

Table 10–8: CONTACT INPUTS

[illegible]

10.6.2 VIRTUAL INPUTS

Table 10–9: VIRTUAL INPUTS

VIRTUAL INPUT	FUNCTION	ID	TYPE	EVENTS
Virtual Input 1				
Virtual Input 2				
Virtual Input 3				
Virtual Input 4				
Virtual Input 5				
Virtual Input 6				
Virtual Input 7				
Virtual Input 8				
Virtual Input 9				
Virtual Input 10				
Virtual Input 11				
Virtual Input 12				
Virtual Input 13				
Virtual Input 14				
Virtual Input 15				
Virtual Input 16				
Virtual Input 17				
Virtual Input 18				
Virtual Input 19				
Virtual Input 20				
Virtual Input 21				
Virtual Input 22				
Virtual Input 23				
Virtual Input 24				
Virtual Input 25				
Virtual Input 26				
Virtual Input 27				
Virtual Input 28				
Virtual Input 29				
Virtual Input 30				
Virtual Input 31				
Virtual Input 32				

Table 10–10: UCA SBO TIMER

SETTING	VALUE
UCA SBO TIMER	
UCA SBO Timeout	

10.6.4 CONTACT OUTPUTS

Table 10–11: CONTACT OUTPUTS

[illegible]

10.6.5 VIRTUAL OUTPUTS

Table 10-12: VIRTUAL OUTPUTS (Sheet 1 of 2)

VIRTUAL OUTPUT	ID	EVENTS
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		

Table 10-12: VIRTUAL OUTPUTS (Sheet 2 of 2)

VIRTUAL OUTPUT	ID	EVENTS
36		
37		
38		
39		
40		
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
54		
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56		
57		
58		
59		
60		
61		
62		
63		
64		

10.6.6 REMOTE DEVICES

Table 10–13: REMOTE DEVICES

REMOTE DEVICE	ID
Remote Device 1	
Remote Device 2	
Remote Device 3	
Remote Device 4	
Remote Device 5	
Remote Device 6	
Remote Device 7	
Remote Device 8	
Remote Device 9	
Remote Device 10	
Remote Device 11	
Remote Device 12	
Remote Device 13	
Remote Device 14	
Remote Device 15	
Remote Device 16	

10.6.7 REMOTE INPUTS

Table 10–14: REMOTE INPUTS

REMOTE INPUT	REMOTE DEVICE	BIT PAIR	DEFAULT STATE	EVENTS
Remote Input 1				
Remote Input 2				
Remote Input 3				
Remote Input 4				
Remote Input 5				
Remote Input 6				
Remote Input 7				
Remote Input 8				
Remote Input 9				
Remote Input 10				
Remote Input 11				
Remote Input 12				
Remote Input 13				
Remote Input 14				
Remote Input 15				
Remote Input 16				
Remote Input 17				
Remote Input 18				
Remote Input 19				
Remote Input 20				
Remote Input 21				
Remote Input 22				
Remote Input 23				
Remote Input 24				
Remote Input 25				
Remote Input 26				
Remote Input 27				
Remote Input 28				
Remote Input 29				
Remote Input 30				
Remote Input 31				
Remote Input 32				

10.6.8 REMOTE OUTPUTS

Table 10-15: REMOTE OUTPUTS (Sheet 1 of 2)

REMOTE OUTPUT	OPERAND	EVENTS
REMOTE OUTPUTS – DNA		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
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20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		

Table 10-15: REMOTE OUTPUTS (Sheet 2 of 2)

REMOTE OUTPUT	OPERAND	EVENTS
REMOTE OUTPUTS – UserSt		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		

Table 10–16: RESETTING

SETTING	VALUE
RESETTING	
Reset Operand	

10.7.1 DCMA INPUTS

Table 10–17: DCMA INPUTS

[illegible]

10.7.2 RTD INPUTS

Table 10–18: RTD INPUTS

[illegible]

Table 10–19: FORCE CONTACT INPUTS

[illegible]

Table 10–20: FORCE CONTACT OUTPUTS

[illegible]

SETTING	CHANNEL1	CHANNEL 2
Loopback Function		
Symmetry Function		
Echoback Function		

A.1.1 FLEXANALOG PARAMETER LIST

A

Table A-1: FLEXANALOG PARAMETERS (Sheet 1 of 4)

SETTING	DISPLAY TEXT	DESCRIPTION
0	Off	Placeholder for unused settings
6144	SRC 1 Ia RMS	SRC 1 Phase A Current RMS (A)
6146	SRC 1 Ib RMS	SRC 1 Phase B Current RMS (A)
6148	SRC 1 Ic RMS	SRC 1 Phase C Current RMS (A)
6150	SRC 1 In RMS	SRC 1 Neutral Current RMS (A)
6152	SRC 1 Ia Mag	SRC 1 Phase A Current Magnitude (A)
6154	SRC 1 Ia Angle	SRC 1 Phase A Current Angle (°)
6155	SRC 1 Ib Mag	SRC 1 Phase B Current Magnitude (A)
6157	SRC 1 Ib Angle	SRC 1 Phase B Current Angle (°)
6158	SRC 1 Ic Mag	SRC 1 Phase C Current Magnitude (A)
6160	SRC 1 Ic Angle	SRC 1 Phase C Current Angle (°)
6161	SRC 1 In Mag	SRC 1 Neutral Current Magnitude (A)
6163	SRC 1 In Angle	SRC 1 Neutral Current Angle (°)
6164	SRC 1 Ig RMS	SRC 1 Ground Current RMS (A)
6166	SRC 1 Ig Mag	SRC 1 Ground Current Magnitude (A)
6168	SRC 1 Ig Angle	SRC 1 Ground Current Angle (°)
6169	SRC 1 I ₀ Mag	SRC 1 Zero Sequence Current Magnitude (A)
6171	SRC 1 I ₀ Angle	SRC 1 Zero Sequence Current Angle (°)
6172	SRC 1 I ₁ Mag	SRC 1 Positive Sequence Current Magnitude (A)
6174	SRC 1 I ₁ Angle	SRC 1 Positive Sequence Current Angle (°)
6175	SRC 1 I ₂ Mag	SRC 1 Negative Sequence Current Magnitude (A)
6177	SRC 1 I ₂ Angle	SRC 1 Negative Sequence Current Angle (°)
6178	SRC 1 Igd Mag	SRC 1 Differential Ground Current Magnitude (A)
6180	SRC 1 Igd Angle	SRC 1 Differential Ground Current Angle (°)
6208	SRC 2 Ia RMS	SRC 2 Phase A Current RMS (A)
6210	SRC 2 Ib RMS	SRC 2 Phase B Current RMS (A)
6212	SRC 2 Ic RMS	SRC 2 Phase C Current RMS (A)
6214	SRC 2 In RMS	SRC 2 Neutral Current RMS (A)
6216	SRC 2 Ia Mag	SRC 2 Phase A Current Magnitude (A)
6218	SRC 2 Ia Angle	SRC 2 Phase A Current Angle (°)
6219	SRC 2 Ib Mag	SRC 2 Phase B Current Magnitude (A)
6221	SRC 2 Ib Angle	SRC 2 Phase B Current Angle (°)
6222	SRC 2 Ic Mag	SRC 2 Phase C Current Magnitude (A)
6224	SRC 2 Ic Angle	SRC 2 Phase C Current Angle (°)
6225	SRC 2 In Mag	SRC 2 Neutral Current Magnitude (A)
6227	SRC 2 In Angle	SRC 2 Neutral Current Angle (°)
6228	SRC 2 Ig RMS	SRC 2 Ground Current RMS (A)
6230	SRC 2 Ig Mag	SRC 2 Ground Current Magnitude (A)
6232	SRC 2 Ig Angle	SRC 2 Ground Current Angle (°)
6233	SRC 2 I ₀ Mag	SRC 2 Zero Sequence Current Magnitude (A)
6235	SRC 2 I ₀ Angle	SRC 2 Zero Sequence Current Angle (°)

A

Table A-1: FLEXANALOG PARAMETERS (Sheet 2 of 4)

SETTING	DISPLAY TEXT	DESCRIPTION
6236	SRC 2 I ₁ Mag	SRC 2 Positive Sequence Current Magnitude (A)
6238	SRC 2 I ₁ Angle	SRC 2 Positive Sequence Current Angle (°)
6239	SRC 2 I ₂ Mag	SRC 2 Negative Sequence Current Magnitude (A)
6241	SRC 2 I ₂ Angle	SRC 2 Negative Sequence Current Angle (°)
6242	SRC 2 Igd Mag	SRC 2 Differential Ground Current Magnitude (A)
6244	SRC 2 Igd Angle	SRC 2 Differential Ground Current Angle (°)
6656	SRC 1 Vag RMS	SRC 1 Phase AG Voltage RMS (V)
6658	SRC 1 Vbg RMS	SRC 1 Phase BG Voltage RMS (V)
6660	SRC 1 Vcg RMS	SRC 1 Phase CG Voltage RMS (V)
6662	SRC 1 Vag Mag	SRC 1 Phase AG Voltage Magnitude (V)
6664	SRC 1 Vag Angle	SRC 1 Phase AG Voltage Angle (°)
6665	SRC 1 Vbg Mag	SRC 1 Phase BG Voltage Magnitude (V)
6667	SRC 1 Vbg Angle	SRC 1 Phase BG Voltage Angle (°)
6668	SRC 1 Vcg Mag	SRC 1 Phase CG Voltage Magnitude (V)
6670	SRC 1 Vcg Angle	SRC 1 Phase CG Voltage Angle (°)
6671	SRC 1 Vab RMS	SRC 1 Phase AB Voltage RMS (V)
6673	SRC 1 Vbc RMS	SRC 1 Phase BC Voltage RMS (V)
6675	SRC 1 Vca RMS	SRC 1 Phase CA Voltage RMS (V)
6677	SRC 1 Vab Mag	SRC 1 Phase AB Voltage Magnitude (V)
6679	SRC 1 Vab Angle	SRC 1 Phase AB Voltage Angle (°)
6680	SRC 1 Vbc Mag	SRC 1 Phase BC Voltage Magnitude (V)
6682	SRC 1 Vbc Angle	SRC 1 Phase BC Voltage Angle (°)
6683	SRC 1 Vca Mag	SRC 1 Phase CA Voltage Magnitude (V)
6685	SRC 1 Vca Angle	SRC 1 Phase CA Voltage Angle (°)
6686	SRC 1 Vx RMS	SRC 1 Auxiliary Voltage RMS (V)
6688	SRC 1 Vx Mag	SRC 1 Auxiliary Voltage Magnitude (V)
6690	SRC 1 Vx Angle	SRC 1 Auxiliary Voltage Angle (°)
6691	SRC 1 V ₀ Mag	SRC 1 Zero Sequence Voltage Magnitude (V)
6693	SRC 1 V ₀ Angle	SRC 1 Zero Sequence Voltage Angle (°)
6694	SRC 1 V ₁ Mag	SRC 1 Positive Sequence Voltage Magnitude (V)
6696	SRC 1 V ₁ Angle	SRC 1 Positive Sequence Voltage Angle (°)
6697	SRC 1 V ₂ Mag	SRC 1 Negative Sequence Voltage Magnitude (V)
6699	SRC 1 V ₂ Angle	SRC 1 Negative Sequence Voltage Angle (°)
6720	SRC 2 Vag RMS	SRC 2 Phase AG Voltage RMS (V)
6722	SRC 2 Vbg RMS	SRC 2 Phase BG Voltage RMS (V)
6724	SRC 2 Vcg RMS	SRC 2 Phase CG Voltage RMS (V)
6726	SRC 2 Vag Mag	SRC 2 Phase AG Voltage Magnitude (V)
6728	SRC 2 Vag Angle	SRC 2 Phase AG Voltage Angle (°)
6729	SRC 2 Vbg Mag	SRC 2 Phase BG Voltage Magnitude (V)
6731	SRC 2 Vbg Angle	SRC 2 Phase BG Voltage Angle (°)
6732	SRC 2 Vcg Mag	SRC 2 Phase CG Voltage Magnitude (V)
6734	SRC 2 Vcg Angle	SRC 2 Phase CG Voltage Angle (°)
6735	SRC 2 Vab RMS	SRC 2 Phase AB Voltage RMS (V)
6737	SRC 2 Vbc RMS	SRC 2 Phase BC Voltage RMS (V)

Table A–1: FLEXANALOG PARAMETERS (Sheet 3 of 4)

SETTING	DISPLAY TEXT	DESCRIPTION
6739	SRC 2 Vca RMS	SRC 2 Phase CA Voltage RMS (V)
6741	SRC 2 Vab Mag	SRC 2 Phase AB Voltage Magnitude (V)
6743	SRC 2 Vab Angle	SRC 2 Phase AB Voltage Angle (°)
6744	SRC 2 Vbc Mag	SRC 2 Phase BC Voltage Magnitude (V)
6746	SRC 2 Vbc Angle	SRC 2 Phase BC Voltage Angle (°)
6747	SRC 2 Vca Mag	SRC 2 Phase CA Voltage Magnitude (V)
6749	SRC 2 Vca Angle	SRC 2 Phase CA Voltage Angle (°)
6750	SRC 2 Vx RMS	SRC 2 Auxiliary Voltage RMS (V)
6752	SRC 2 Vx Mag	SRC 2 Auxiliary Voltage Magnitude (V)
6754	SRC 2 Vx Angle	SRC 2 Auxiliary Voltage Angle (°)
6755	SRC 2 V_0 Mag	SRC 2 Zero Sequence Voltage Magnitude (V)
6757	SRC 2 V_0 Angle	SRC 2 Zero Sequence Voltage Angle (°)
6758	SRC 2 V_1 Mag	SRC 2 Positive Sequence Voltage Magnitude (V)
6760	SRC 2 V_1 Angle	SRC 2 Positive Sequence Voltage Angle (°)
6761	SRC 2 V_2 Mag	SRC 2 Negative Sequence Voltage Magnitude (V)
6763	SRC 2 V_2 Angle	SRC 2 Negative Sequence Voltage Angle (°)
7168	SRC 1 P	SRC 1 Three Phase Real Power (W)
7170	SRC 1 Pa	SRC 1 Phase A Real Power (W)
7172	SRC 1 Pb	SRC 1 Phase B Real Power (W)
7174	SRC 1 Pc	SRC 1 Phase C Real Power (W)
7176	SRC 1 Q	SRC 1 Three Phase Reactive Power (var)
7178	SRC 1 Qa	SRC 1 Phase A Reactive Power (var)
7180	SRC 1 Qb	SRC 1 Phase B Reactive Power (var)
7182	SRC 1 Qc	SRC 1 Phase C Reactive Power (var)
7184	SRC 1 S	SRC 1 Three Phase Apparent Power (VA)
7186	SRC 1 Sa	SRC 1 Phase A Apparent Power (VA)
7188	SRC 1 Sb	SRC 1 Phase B Apparent Power (VA)
7190	SRC 1 Sc	SRC 1 Phase C Apparent Power (VA)
7192	SRC 1 PF	SRC 1 Three Phase Power Factor
7193	SRC 1 Phase A PF	SRC 1 Phase A Power Factor
7194	SRC 1 Phase B PF	SRC 1 Phase B Power Factor
7195	SRC 1 Phase C PF	SRC 1 Phase C Power Factor
7200	SRC 2 P	SRC 2 Three Phase Real Power (W)
7202	SRC 2 Pa	SRC 2 Phase A Real Power (W)
7204	SRC 2 Pb	SRC 2 Phase B Real Power (W)
7206	SRC 2 Pc	SRC 2 Phase C Real Power (W)
7208	SRC 2 Q	SRC 2 Three Phase Reactive Power (var)
7210	SRC 2 Qa	SRC 2 Phase A Reactive Power (var)
7212	SRC 2 Qb	SRC 2 Phase B Reactive Power (var)
7214	SRC 2 Qc	SRC 2 Phase C Reactive Power (var)
7216	SRC 2 S	SRC 2 Three Phase Apparent Power (VA)
7218	SRC 2 Sa	SRC 2 Phase A Apparent Power (VA)
7220	SRC 2 Sb	SRC 2 Phase B Apparent Power (VA)
7222	SRC 2 Sc	SRC 2 Phase C Apparent Power (VA)

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Table A-1: FLEXANALOG PARAMETERS (Sheet 4 of 4)

SETTING	DISPLAY TEXT	DESCRIPTION
7224	SRC 2 PF	SRC 2 Three Phase Power Factor
7225	SRC 2 Phase A PF	SRC 2 Phase A Power Factor
7226	SRC 2 Phase B PF	SRC 2 Phase B Power Factor
7227	SRC 2 Phase C PF	SRC 2 Phase C Power Factor
7552	SRC 1 Frequency	SRC 1 Frequency (Hz)
7553	SRC 2 Frequency	SRC 2 Frequency (Hz)
8704	Brk 1 Arc Amp A	Breaker 1 Arcing Amp Phase A (kA2-cyc)
8706	Brk 1 Arc Amp B	Breaker 1 Arcing Amp Phase B (kA2-cyc)
8708	Brk 1 Arc Amp C	Breaker 1 Arcing Amp Phase C (kA2-cyc)
8710	Brk 2 Arc Amp A	Breaker 2 Arcing Amp Phase A (kA2-cyc)
8712	Brk 2 Arc Amp B	Breaker 2 Arcing Amp Phase B (kA2-cyc)
8714	Brk 2 Arc Amp C	Breaker 2 Arcing Amp Phase C (kA2-cyc)
9216	Synchchk 1 Delta V	Synchrocheck 1 Delta Voltage (V)
9218	Synchchk 1 Delta F	Synchrocheck 1 Delta Frequency (Hz)
9219	Synchchk 1 Delta Phs	Synchrocheck 1 Delta Phase (°)
9220	Synchchk 2 Delta V	Synchrocheck 2 Delta Voltage (V)
9222	Synchchk 2 Delta F	Synchrocheck 2 Delta Frequency (Hz)
9223	Synchchk 2 Delta Phs	Synchrocheck 2 Delta Phase (°)
9248	1 S1 S2 Angle	Power Swing S1 S2 Angle (°)
32768	Tracking Frequency	Tracking Frequency (Hz)
40960	Communications Group	Communications Group
40971	Active Setting Group	Current Setting Group

B.1.1 INTRODUCTION

The UR type relays communicate with other computerized equipment such as programmable logic controllers, personal computers, or plant master computers, by using the AEG Modicon or **Modbus® RTU Protocol**. Following are some general notes:

- The units always act as slave devices, meaning that they never initiate communications; they only listen and respond to requests issued by a master computer.
- For Modbus®, a subset of the Remote Terminal Unit (RTU) format of the protocol is supported which allows extensive monitoring, programming and control functions using read and write register commands.

B.1.2 PHYSICAL LAYER

The Modbus® RTU protocol is hardware-independent so that the physical layer can be any of a variety of standard hardware configurations including RS232, RS485, fiber optics, 10BaseT or 10BaseF Ethernet, etc. The relay unit includes a faceplate (front panel) RS232 port and two rear terminal communications ports, which may be configured as RS485, fiber optic, 10BaseT, or 10BaseF. Data flow is half duplex in all configurations. See Chapter 3: HARDWARE for details on wiring.

Each data byte is transmitted in an asynchronous format consisting of 1 start bit, 8 data bits, 1 stop bit, and possibly 1 parity bit. This produces a 10 or 11 bit data frame. This is important for transmission through modems at high bit rates (11 bit data frames are not supported by many modems at baud rates greater than 300).

The baud rate and parity are independently programmable for each communications port. Baud rates of 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, or 115200 bps are available. Even, odd, and no parity are available. See Chapter 5: SETTINGS \ PRODUCT SETUP \ COMMUNICATIONS for further details.

The master device in any system must know the address of the slave device with which it is to communicate. The unit will not act on a request from a master if the address in the request does not match the relay's slave address (unless the address is the broadcast address -- see below).

A single setting selects the slave address used for all ports, with the exception that for the faceplate port, the relay will accept any address when the Modbus® RTU protocol is used. The slave address is otherwise the same regardless of the protocol in use, but note that the broadcast address is 0 for Modbus®. The relay recognizes and processes a master request (under conditions that are protocol-specific) if the broadcast address is used but never returns a response.

B.1.3 DATA LINK LAYER

Communications takes place in packets which are groups of asynchronously framed byte data. The master transmits a packet to the slave and the slave responds with a packet. The end of a packet is marked by 'dead-time' on the communications line. The following describes general format for both transmit and receive packets. For exact details on packet formatting, refer to subsequent sections describing each function code.

Table B-1: MODBUS PACKET FORMAT

DESCRIPTION	SIZE
SLAVE ADDRESS	1 byte
FUNCTION CODE	1 byte
DATA	N bytes
CRC	2 bytes
DEAD TIME	3.5 bytes transmission time

SLAVE ADDRESS

This is the address of the slave device that is intended to receive the packet sent by the master and to perform the desired action. Each slave device on a communications bus must have a unique address to prevent bus contention. All of the relay's ports have the same address which is programmable from 1 to 254; see Chapter 5 for details. Only the addressed slave will respond to a packet that starts with its address. Note that the face-plate port is an exception to this rule; it will act on a message containing any slave address.

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A master transmit packet with a slave address of 0 indicates a broadcast command. All slaves on the communication link will take action based on the packet, but none will respond to the master. Broadcast mode is only recognized when associated with FUNCTION CODE 05h. For any other function code, a packet with broadcast mode slave address 0 will be ignored.

FUNCTION CODE

This is one of the supported functions codes of the unit which tells the slave what action to perform. See the SUPPORTED FUNCTION CODES section for complete details. An exception response from the slave is indicated by setting the high order bit of the function code in the response packet. See the EXCEPTION RESPONSES section for further details.

DATA

This will be a variable number of bytes depending on the function code. This may include actual values, settings, or addresses sent by the master to the slave or by the slave to the master.

CRC

This is a two byte error checking code. The RTU version of Modbus[®] includes a 16 bit cyclic redundancy check (CRC-16) with every packet which is an industry standard method used for error detection. If a Modbus[®] slave device receives a packet in which an error is indicated by the CRC, the slave device will not act upon or respond to the packet thus preventing any erroneous operations. See the CRC-16 ALGORITHM section for a description of how to calculate the CRC.

DEAD TIME

A packet is terminated when no data is received for a period of 3.5 byte transmission times (about 15 ms at 2400 bps, 2 ms at 19200 bps, and 300 μ s at 115200 bps). Consequently, the transmitting device must not allow gaps between bytes longer than this interval. Once the dead time has expired without a new byte transmission, all slaves start listening for a new packet from the master except for the addressed slave.

B.1.4 CRC-16 ALGORITHM

The CRC-16 algorithm essentially treats the entire data stream (data bits only; start, stop and parity ignored) as one continuous binary number. This number is first shifted left 16 bits and then divided by a characteristic polynomial (11000000000000101B). The 16 bit remainder of the division is appended to the end of the packet, MSByte first. The resulting packet including CRC, when divided by the same polynomial at the receiver will give a zero remainder if no transmission errors have occurred. This algorithm requires the characteristic polynomial to be reverse bit ordered. The most significant bit of the characteristic polynomial is dropped, since it does not affect the value of the remainder.

Note: A C programming language implementation of the CRC algorithm will be provided upon request.

Table B-2: CRC-16 ALGORITHM

SYMBOLS:	-->	data transfer	
	A	16 bit working register	
	Alow	low order byte of A	
	Ahigh	high order byte of A	
	CRC	16 bit CRC-16 result	
	i,j	loop counters	
	(+)	logical EXCLUSIVE-OR operator	
	N	total number of data bytes	
	Di	i-th data byte (i = 0 to N-1)	
	G	16 bit characteristic polynomial = 1010000000000001 (binary) with MSbit dropped and bit order reversed	
	shr (x)	right shift operator (th LSbit of x is shifted into a carry flag, a '0' is shifted into the MSbit of x, all other bits are shifted right one location)	
ALGORITHM:	1.	FFFF (hex) --> A	
	2.	0 --> i	
	3.	0 --> j	
	4.	Di (+) Alow --> Alow	
	5.	j + 1 --> j	
	6.	shr (A)	
	7.	Is there a carry?	No: go to 8 Yes: G (+) A --> A and continue.
	8.	Is j = 8?	No: go to 5 Yes: continue
	9.	i + 1 --> i	
	10.	Is i = N?	No: go to 3 Yes: continue
	11.	A --> CRC	

B.2.1 SUPPORTED FUNCTION CODES

Modbus® officially defines function codes from 1 to 127 though only a small subset is generally needed. The relay supports some of these functions, as summarized in the following table. Subsequent sections describe each function code in detail.

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FUNCTION CODE		MODBUS® DEFINITION	GE POWER MANAGEMENT DEFINITION
HEX	DEC		
03	3	Read Holding Registers	Read Actual Values or Settings
04	4	Read Holding Registers	Read Actual Values or Settings
05	5	Force Single Coil	Execute Operation
06	6	Preset Single Register	Store Single Setting
10	16	Preset Multiple Registers	Store Multiple Settings

B.2.2 FUNCTION CODE 03H/04H - READ ACTUAL VALUES or SETTINGS

This function code allows the master to read one or more consecutive data registers (actual values or settings) from a relay. Data registers are always 16 bit (two byte) values transmitted with high order byte first. The maximum number of registers that can be read in a single packet is 125. See the section MODBUS® MEMORY MAP for exact details on the data registers.

Since some PLC implementations of Modbus® only support one of function codes 03h and 04h, the relay interpretation allows either function code to be used for reading one or more consecutive data registers. The data starting address will determine the type of data being read. Function codes 03h and 04h are therefore identical.

The following table shows the format of the master and slave packets. The example shows a master device requesting 3 register values starting at address 4050h from slave device 11h (17 decimal); the slave device responds with the values 40, 300, and 0 from registers 4050h, 4051h, and 4052h, respectively.

Table B-3: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION		SLAVE RESPONSE	
PACKET FORMAT	EXAMPLE (hex)	PACKET FORMAT	EXAMPLE (hex)
SLAVE ADDRESS	11	SLAVE ADDRESS	11
FUNCTION CODE	04	FUNCTION CODE	04
DATA STARTING ADDRESS - hi	40	BYTE COUNT	06
DATA STARTING ADDRESS - lo	50	DATA #1 - hi	00
NUMBER OF REGISTERS - hi	00	DATA #1 - lo	28
NUMBER OF REGISTERS - lo	03	DATA #2 - hi	01
CRC - lo	A7	DATA #2 - lo	2C
CRC - hi	4A	DATA #3 - hi	00
		DATA #3 - lo	00
		CRC - lo	0D
		CRC - hi	60

B.2.3 FUNCTION CODE 05H - EXECUTE OPERATION

This function code allows the master to perform various operations in the relay. Available operations are in the table SUMMARY OF OPERATION CODES.

The following table shows the format of the master and slave packets. The example shows a master device requesting the slave device 11H (17 dec) to perform a reset. The hi and lo CODE VALUE bytes always have the values 'FF' and '00' respectively and are a remnant of the original Modbus[®] definition of this function code.

Table B-4: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION		SLAVE RESPONSE	
PACKET FORMAT	EXAMPLE (hex)	PACKET FORMAT	EXAMPLE (hex)
SLAVE ADDRESS	11	SLAVE ADDRESS	11
FUNCTION CODE	05	FUNCTION CODE	05
OPERATION CODE - hi	00	OPERATION CODE - hi	00
OPERATION CODE - lo	01	OPERATION CODE - lo	01
CODE VALUE - hi	FF	CODE VALUE - hi	FF
CODE VALUE - lo	00	CODE VALUE - lo	00
CRC - lo	DF	CRC - lo	DF
CRC - hi	6A	CRC - hi	6A

Table B-5: SUMMARY OF OPERATION CODES (Function Code 05h)

OPERATION CODE (hex)	DEFINITION	DESCRIPTION
0000	NO OPERATION	Does not do anything.
0001	RESET	Performs the same function as the faceplate <i>RESET</i> key.
0005	CLEAR EVENT RECORDS	Performs the same function as the faceplate <i>CLEAR EVENTS RECORD</i> menu command.
0006	CLEAR OSCILLOGRAPHY	Clears all oscillography records.
1000 to 101F	VIRTUAL IN 1-32 ON/OFF	Sets the states of Virtual Inputs 1 to 32 either "ON" or "OFF".

B.2.4 FUNCTION CODE 06H - STORE SINGLE SETTING

This function code allows the master to modify the contents of a single setting register in an relay. Setting registers are always 16 bit (two byte) values transmitted high order byte first.

The following table shows the format of the master and slave packets. The example shows a master device storing the value 200 at memory map address 4051h to slave device 11h (17 dec).

Table B-6: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION		SLAVE RESPONSE	
PACKET FORMAT	EXAMPLE (hex)	PACKET FORMAT	EXAMPLE (hex)
SLAVE ADDRESS	11	SLAVE ADDRESS	11
FUNCTION CODE	06	FUNCTION CODE	06
DATA STARTING ADDRESS - hi	40	DATA STARTING ADDRESS - hi	40
DATA STARTING ADDRESS - lo	51	DATA STARTING ADDRESS - lo	51
DATA - hi	00	DATA - hi	00
DATA - lo	C8	DATA - lo	C8
CRC - lo	CE	CRC - lo	CE
CRC - hi	DD	CRC - hi	DD

B.2.5 FUNCTION CODE 10H - STORE MULTIPLE SETTINGS

This function code allows the master to modify the contents of a one or more consecutive setting registers in a relay. Setting registers are 16-bit (two byte) values transmitted high order byte first. The maximum number of setting registers that can be stored in a single packet is 60. The following table shows the format of the master and slave packets. The example shows a master device storing the value 200 at memory map address 4051h, and the value 1 at memory map address 4052h to slave device 11h (17 dec).

Table B-7: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION		SLAVE RESPONSE	
PACKET FORMAT	EXAMPLE (hex)	PACKET FORMAT	EXAMPLE (hex)
SLAVE ADDRESS	11	SLAVE ADDRESS	11
FUNCTION CODE	10	FUNCTION CODE	10
DATA STARTING ADDRESS - hi	40	DATA STARTING ADDRESS - hi	40
DATA STARTING ADDRESS - lo	51	DATA STARTING ADDRESS - lo	51
NUMBER OF SETTINGS - hi	00	NUMBER OF SETTINGS - hi	00
NUMBER OF SETTINGS - lo	02	NUMBER OF SETTINGS - lo	02
BYTE COUNT	04	CRC - lo	07
DATA #1 - high order byte	00	CRC - hi	64
DATA #1 - low order byte	C8		
DATA #2 - high order byte	00		
DATA #2 - low order byte	01		
CRC - low order byte	12		
CRC - high order byte	62		

B.3.1 EXCEPTION RESPONSES

Programming or operation errors happen because of illegal data in a packet, hardware or software problems in the slave device, etc. These errors result in an exception response from the slave. The slave detecting one of these errors sends a response packet to the master with the high order bit of the function code set to 1.

The following table shows the format of the master and slave packets. The example shows a master device sending the unsupported function code 39h to slave device 11.

Table B–8: MASTER AND SLAVE DEVICE PACKET TRANSMISSION EXAMPLE

MASTER TRANSMISSION		SLAVE RESPONSE	
PACKET FORMAT	EXAMPLE (hex)	PACKET FORMAT	EXAMPLE (hex)
SLAVE ADDRESS	11	SLAVE ADDRESS	11
FUNCTION CODE	39	FUNCTION CODE	B9
CRC - low order byte	CD	ERROR CODE	01
CRC - high order byte	F2	CRC - low order byte	93
		CRC - high order byte	95

B.4.1 OBTAINING UR FILES USING MODBUS® PROTOCOL

The UR relay has a generic file transfer facility, meaning that you use the same method to obtain all of the different types of files from the unit.

The Modbus® registers that implement file transfer are found in the "Modbus File Transfer (Read/Write)" and "Modbus File Transfer (Read Only)" modules, starting at address 3100 in the Modbus® Memory Map. To read a file from the UR relay, use the following steps:

1. Write the filename to the "Name of file to read" register using a write multiple registers command. If the name is shorter than 80 characters, you may write only enough registers to include all the text of the filename. Filenames are not case sensitive.
2. Repeatedly read all the registers in "Modbus File Transfer (Read Only)" using a read multiple registers command. It is not necessary to read the entire data block, since the UR relay will remember which was the last register you read. The "position" register is initially zero and thereafter indicates how many bytes (2 times the number of registers) you have read so far. The "size of..." register indicates the number of bytes of data remaining to read, to a maximum of 244.
3. Keep reading until the "size of..." register is smaller than the number of bytes you are transferring. This condition indicates end of file. Discard any bytes you have read beyond the indicated block size.
4. If you need to re-try a block, read only the "size of.." and "block of data", without reading the position. The file pointer is only incremented when you read the position register, so the same data block will be returned as was read in the previous operation. On the next read, check to see if the position is where you expect it to be, and discard the previous block if it is not (this condition would indicate that the UR relay did not process your original read request).

The UR relay retains connection-specific file transfer information, so files may be read simultaneously on multiple modbus connections.

a) OBTAINING FILES FROM THE UR USING OTHER PROTOCOLS

All the files available via Modbus® may also be retrieved using the standard file transfer mechanisms in other protocols.

b) COMTRADE, OSCILLOGRAPHY AND DATA LOGGER FILES

Oscillography and data logger files are formatted using the COMTRADE file format per IEEE PC37.111 Draft 7c (02 September 1997). The files may be obtained in either text or binary COMTRADE format.

c) READING OSCILLOGRAPHY FILES

In order to understand the description that follows, familiarity with the oscillography feature is required: refer to Chapter 5 SETTINGS \ PRODUCT SETUP \ OSCILLOGRAPHY for details.

The Oscillography_Number_of_Triggers register is incremented by one every time a new oscillography file is triggered (captured). Oscillography_Number_of_Triggers register is cleared to zero when oscillography data is cleared. When a new trigger occurs, the associated oscillography file is assigned a file identifier number equal to the incremented value of this register; the newest file will have a number equal to the Oscillography_Number_of_Triggers register. This register can be used to determine if any new data has been captured by periodically reading it to see if the value has changed; if the number has increased then there is new data available.

The Oscillography_Number_of_Records setting specifies the maximum number of files (and the number of cycles of data per file) that can be stored in memory of the relay. The Oscillography_Available_Records register specifies the actual number of files that are stored and still available to be read out of the relay.

Writing 'Yes' (i.e. the value 1) to the Oscillography_Clear_Data register clears oscillography data files, clears both Oscillography_Number_of_Triggers and Oscillography_Available_Records registers to zero, and sets the Oscillography_Last_Cleared_Date to the present date and time.

To read binary COMTRADE oscillography files, read the following filenames:

- OSCnnnn.CFG
- OSCnnn.DAT

Replace "nnn" with the desired oscillography trace number.

For ascii format, use the following file names

- OSCAnnnn.CFG
- OSCAnnn.DAT

d) READING DATA LOGGER FILES

In order to understand the description that follows, familiarity with the data logger feature is required: refer to Chapter 5 SETTINGS \ PRODUCT SETUP \ DATA LOGGER for details.

To read the entire data logger in binary COMTRADE format, read the following files.

- datalog.cfg
- datalog.dat

To read the entire data logger in ascii COMTRADE format, read the following files.

- dataloga.cfg
- dataloga.dat

To limit the range of records to be returned in the COMTRADE files, append the following to the filename before writing it:

To read from a specific time to the end of the log: <space> startTime

To read a specific range of records: <space> startTime <space> endTime

Replace <startTime> and <endTime> with Julian dates (seconds since Jan. 1 1970) as numeric text.

e) READING EVENT RECORDER FILES

To read the entire event recorder contents in ascii format (the only available format), use the following filename:

- EVT.TXT

To read from a specific record to the end of the log, use the following filename:

- EVTnnn.TXT

Replace "nnn" with the desired starting record number.

f) READING FAULT REPORT FILES

Fault report data has been available via the UR file retrieval mechanism since firmware version 2.00.

The file name is **faultReport#####.htm**. The ##### is the fault report record number that is desired to be read. The fault report number is a counter that indicates how many fault reports have ever occurred. The counter rolls over at a value of 65535. Only the last ten fault reports are available for retrieval; a request for a non-existent fault report file will yield a null file. The current value fault report counter is available in “Number of Fault Reports” Modbus register at location 0x3020.

For example, if 14 fault reports have occurred then the files faultReport5.htm, faultReport6.htm, up to faultReport14.htm are available to be read. The expected use of this feature has an external master periodically polling the “Number of Fault Reports” register. If the value changes, then the master reads all the new files.

The contents of the file is in standard HTML notation and can be viewed via any commercial browser.

g) FILE FORMATS

"Normal" file format:

FORMAT,SHORT_EVENT,Event Number,Date/Time,Cause <Hex>,Cause <text>

e.g.: SHORT_EVENT,1,May 12 2000 14:17:31.000123,7C00,EVENTS CLEARED

B.4.2 MODBUS® PASSWORD OPERATION

The COMMAND password can be set up at memory location 4000. Storing a value of zero removes the COMMAND password protection. When reading the password setting, the encrypted value (zero if no password is set) will be returned. COMMAND security is required to change the COMMAND password. Similarly, the SETTING password can be set up at memory location 4002. These are the same settings and encrypted values found in the Settings / Product Setup / Password Security menu via the faceplate keypad/display. Enabling password security for the faceplate display will also enable it for Modbus®, and vice-versa.

To gain COMMAND level security access, the COMMAND password must be entered at memory location 4008. To gain SETTING level security access, the SETTING password must be entered at memory location 400A. The entered SETTING password must match the current SETTING password setting, or must be zero, to change settings or download firmware.

COMMAND and SETTING passwords each have a 30-minute timer. Each timer starts when you enter the particular password, and is re-started whenever you “use” it. For example, writing a setting re-starts the SETTING password timer and writing a command register or forcing a coil re-starts the COMMAND password timer.

The value read at memory location 4010 can be used to confirm whether a COMMAND password is enabled or disabled (0 for Disabled). The value read at memory location 4011 can be used to confirm whether a SETTING password is enabled or disabled.

COMMAND or SETTING password security access is restricted to the particular port or particular TCP/IP connection on which the entry was made. Passwords must be entered when accessing the relay through other ports or connections, and the passwords must be re-entered after disconnecting and re-connecting on TCP/IP.

B.5.1 MODBUS® MEMORY MAP SUMMARY

Table B–9: L60 MEMORY MAP SUMMARY (Sheet 1 of 3)

MODULE	START ADDRESS	LAST ADDRESS	NUMBER OF REGISTERS	GAP TO NEXT MODULE
Product Information (Read Only)	0000	0002	3	13
Product Information (Read Only -- Written by Factory)	0010	00FF	240	256
Self Test Targets (Read Only)	0200	0203	4	0
Front Panel (Read Only)	0204	0247	68	56
Keypress Emulation (Read/Write)	0280	0280	1	383
Virtual Input Commands (Read/Write Command)[32 modules]	0400	041F	32	992
Digital Counter States (Read Only Non-Volatile)[8 modules]	0800	083F	64	192
FlexStates (Read Only)	0900	090F	16	1776
Element States (Read Only)	1000	103F	64	64
User Displays Actuals (Read Only)	1080	111F	160	224
Modbus User Map Actuals (Read Only)	1200	12FF	256	448
Element Targets (Read Only)	14C0	14C1	2	0
Element Targets (Read/Write)	14C2	14C2	1	0
Element Targets (Read Only)	14C3	14D6	20	41
Digital I/O States (Read Only)	1500	1533	52	12
Remote I/O States (Read Only)	1540	1550	17	0
Remote Device Status (Read Only)[16 modules]	1551	1590	64	127
Ethernet Fibre Channel Status (Read/Write)	1610	1611	2	6
Data Logger Actuals (Read Only)	1618	161D	6	35
Phase Comparison Channel Status (Read Only)[2 modules]	1641	1644	4	443
Source Current (Read Only)[6 modules]	1800	197F	384	128
Source Voltage (Read Only)[6 modules]	1A00	1B7F	384	128
Source Power (Read Only)[6 modules]	1C00	1CBF	192	192
Source Frequency (Read Only)[6 modules]	1D80	1D85	6	1146
Breaker Arcing Current Actuals (Read Only Non-Volatile)[2 modules]	2200	220B	12	0
Breaker Arcing Current Commands (Read/Write Command) [2 modules]	220C	220D	2	498
Synchrocheck Actuals (Read Only)[2 modules]	2400	2407	8	8
Autoreclose Status (Read Only)[6 modules]	2410	2415	6	10
Power Swing Detect Actual Values (Read Only)	2420	2420	1	1759
Expanded FlexStates (Read Only)	2B00	2BFF	256	256
Expanded Digital I/O states (Read Only)	2D00	2E3F	320	192
Expanded Remote I/O Status (Read Only)	2F00	2F9F	160	96
Oscillography Values (Read Only)	3000	3004	5	0
Oscillography Commands (Read/Write Command)	3005	3011	13	14
Fault Report Indexing (Read Only Non-Volatile)	3020	3020	1	15
Fault Reports (Read Only Non-Volatile)[10 modules]	3030	3043	20	188
Modbus File Transfer (Read/Write)	3100	3127	40	216
Modbus File Transfer (Read Only)	3200	327C	125	387
Event Recorder (Read Only)	3400	3405	6	0

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Table B–9: L60 MEMORY MAP SUMMARY (Sheet 2 of 3)

MODULE	START ADDRESS	LAST ADDRESS	NUMBER OF REGISTERS	GAP TO NEXT MODULE
Event Recorder (Read/Write Command)	3406	3406	1	185
DCMA Input Values (Read Only)[24 modules]	34C0	34EF	48	0
RTD Input Values (Read Only)[48 modules]	34F0	351F	48	0
Ohm Input Values (Read Only)[2 modules]	3520	3521	2	2782
Passwords (Read/Write Command)	4000	4001	2	0
Passwords (Read/Write Setting)	4002	4003	2	4
Passwords (Read/Write)	4008	400B	4	4
Passwords (Read Only)	4010	4011	2	62
Preferences (Read/Write Setting)	4050	4052	3	43
Communications (Read/Write Setting)	407E	40C7	74	168
Data Logger Commands (Read/Write Command)	4170	4170	1	15
Data Logger (Read/Write Setting)	4180	4190	17	15
Clock (Read/Write Command)	41A0	41A1	2	0
Clock (Read/Write Setting)	41A2	41A6	5	9
Fault Report Settings and Commands (Read/Write Setting)	41B0	41B1	2	0
Fault Report Settings and Commands (Read/Write Command)	41B2	41B2	1	13
Oscillography (Read/Write Setting)	41C0	423E	127	33
Trip and Alarm LEDs (Read/Write Setting)	4260	4261	2	30
User Programmable LEDs (Read/Write Setting)[48 modules]	4280	42DF	96	256
Installation (Read/Write Setting)	43E0	43EA	11	149
CT Settings (Read/Write Setting)[6 modules]	4480	4497	24	104
VT Settings (Read/Write Setting)[3 modules]	4500	4517	24	104
Source Settings (Read/Write Setting)[6 modules]	4580	45A9	42	86
Power System (Read/Write Setting)	4600	4603	4	204
Line (Read/Write Setting)	46D0	46D5	6	26
Breaker Control Global Settings (Read/Write Setting)	46F0	46F0	1	15
Breaker Control (Read/Write Setting)[2 modules]	4700	472F	48	80
Synchrocheck (Read/Write Setting)[2 modules]	4780	479F	32	96
Flexcurve A (Read/Write Setting)	4800	4877	120	120
Flexcurve B (Read/Write Setting)	48F0	4967	120	152
Modbus User Map (Read/Write Setting)	4A00	4AFF	256	256
User Displays Settings (Read/Write Setting)[8 modules]	4C00	4CFF	256	768
Flexlogic (Read/Write Setting)	5000	51FF	512	1536
Flexlogic Timers (Read/Write Setting)[32 modules]	5800	58FF	256	0
Phase TOC (Read/Write Grouped Setting)[6 modules]	5900	595F	96	160
Phase IOC (Read/Write Grouped Setting)[12 modules]	5A00	5ABF	192	64
Neutral TOC (Read/Write Grouped Setting)[6 modules]	5B00	5B5F	96	160
Neutral IOC (Read/Write Grouped Setting)[12 modules]	5C00	5CBF	192	64
Ground TOC (Read/Write Grouped Setting)[6 modules]	5D00	5D5F	96	160
Ground IOC (Read/Write Grouped Setting)[12 modules]	5E00	5EBF	192	96
Disturbance Detector (Read/Write Grouped Setting)	5F20	5F24	5	443
Phase Comparison Open Breaker Keying (Read/Write Setting)	60E0	60EA	11	5

Table B–9: L60 MEMORY MAP SUMMARY (Sheet 3 of 3)

MODULE	START ADDRESS	LAST ADDRESS	NUMBER OF REGISTERS	GAP TO NEXT MODULE
Phase Comparison Trip Scheme (Read/Write Setting)	60F0	6114	37	11
CT Fail (Read/Write Setting)	6120	612A	11	5
Cont Monitor (Read/Write Setting)	6130	6136	7	265
Autoreclose (Read/Write Setting)[6 modules]	6240	62F3	180	12
Negative Sequence TOC (Read/Write Grouped Setting)[2 modules]	6300	631F	32	224
Negative Sequence IOC (Read/Write Grouped Setting)[2 modules]	6400	641F	32	416
Power Swing Detect (Read/Write Grouped Setting)	65C0	65D4	21	2603
Phase Undervoltage (Read/Write Grouped Setting)[2 modules]	7000	701F	32	224
Phase Overvoltage (Read/Write Grouped Setting)	7100	710F	16	32
Distance (Read/Write Grouped Setting)	7130	7131	2	142
Line Pickup (Read/Write Grouped Setting)	71C0	71CC	13	51
Breaker Failure (Read/Write Grouped Setting)[2 modules]	7200	724D	78	114
Breaker Arcing Current Settings (Read/Write Setting)[2 modules]	72C0	72CF	16	48
DCMA Inputs (Read/Write Setting)[24 modules]	7300	753F	576	0
RTD Inputs (Read/Write Setting)[48 modules]	7540	783F	768	0
Ohm Inputs (Read/Write Setting)[2 modules]	7840	785F	32	448
Backup Phase Distance (Read/Write Grouped Setting)	7A20	7A28	9	7
Backup Ground Distance (Read/Write Grouped Setting)	7A30	7A38	9	1479
Frequency (Read Only)	8000	8000	1	2047
FlexState Settings (Read/Write Setting)	8800	88FF	256	5888
Setting Groups (Read/Write Setting)	A000	A00A	11	0
Setting Groups (Read Only)	A00B	A00B	1	52
VT Fuse Failure (Read/Write Setting)[6 modules]	A040	A045	6	42
Pilot POTT (Read/Write Setting)	A070	A07A	11	3973
Digital Elements (Read/Write Setting)[16 modules]	B000	B1FF	512	256
Digital Counter (Read/Write Setting)[8 modules]	B300	B3FF	256	3072
Contact Inputs (Read/Write Setting)[96 modules]	C000	C3BF	960	576
Contact Input Thresholds (Read/Write Setting)	C600	C617	24	104
Virtual Inputs Global Settings (Read/Write Setting)	C680	C680	1	15
Virtual Inputs (Read/Write Setting)[32 modules]	C690	C88F	512	1024
Virtual Outputs (Read/Write Setting)[64 modules]	CC90	D08F	1024	496
Mandatory (Read/Write Setting)	D280	D280	1	15
Contact Outputs (Read/Write Setting)[64 modules]	D290	D68F	1024	368
Reset (Read/Write Setting)	D800	D800	1	175
Force Contact Inputs (Read/Write Setting)	D8B0	D90F	96	0
Force Contact Outputs (Read/Write Setting)	D910	D94F	64	209
Phase Comparison Channel Tests (Read/Write Command) [2 modules]	DA21	DA26	6	1497
Remote Devices (Read/Write Setting)[16 modules]	E000	E09F	160	96
Remote Inputs (Read/Write Setting)[32 modules]	E100	E17F	128	1152
Remote Output DNA Pairs (Read/Write Setting)[32 modules]	E600	E67F	128	0
Remote Output UserSt Pairs (Read/Write Setting)[32 modules]	E680	FFFF	128	0

B.5.2 MODBUS® MEMORY MAP DATA FORMATS

Table B-10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 1 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F001	UR_UINT16	UNSIGNED 16 BIT INTEGER
F002	UR_SINT16	SIGNED 16 BIT INTEGER
F003	UR_UINT32	UNSIGNED 32 BIT INTEGER (2 registers) High order word is stored in the first register. Low order word is stored in the second register.
F004	UR_SINT32	SIGNED 32 BIT INTEGER (2 registers) High order word is stored in the first register. Low order word is stored in the second register.
F005	UR_UINT8	UNSIGNED 8 BIT INTEGER
F006	UR_SINT8	SIGNED 8 BIT INTEGER
F011	UR_UINT16	FLEXCURVE DATA (120 POINTS) A FlexCurve is an array of 120 consecutive data points (x,y) which are interpolated to generate a smooth curve. The y-axis is the user defined trip or operation time setting; the x-axis is the pickup ratio and is pre-defined. Refer to format F119 for a listing of the pickup ratios; the enumeration value for the pickup ratio indicates the offset into the FlexCurve base address where the corresponding time value is stored.
F012	DISPLAY_SCALE	DISPLAY SCALING (UNSIGNED 16 BIT INTEGER) MSB indicates the SI units as a power of ten. LSB indicates the number of decimal points to display. Example: Current values are stored as 32 bit numbers with three decimal places and base units in Amps. If the retrieved value is 12345.678 A and the display scale equals 0x0302 then the displayed value on the unit is 12.35 kA.
F013	POWER_FACTOR	POWER FACTOR (SIGNED 16 BIT INTEGER) Positive values indicate lagging power factor; negative values indicate leading.
F040	UR_UINT48	48-BIT UNSIGNED INTEGER
F050	UR_UINT32	TIME and DATE (UNSIGNED 32 BIT INTEGER) Gives the current time in seconds elapsed since 00:00:00 January 1, 1970.
F051	UR_UINT32	DATE in SR style format (alternate format for F050) first 16 bits (MM/DD/xxxx); Month (1=January, 2=February,..., 12=December); Day (1 to 31 in steps of 1) last 16 bits Year (xx/xx/YYYY); 1970 to 2106 in steps of 1
F052	UR_UINT32	TIME in SR style format (alternate format for F050) first 16 bits Hours/Minutes (HH:MM:xx.xxx), Hours (0=12am, 1=1am,..., 12=12pm, ..., 23=11pm), Minutes(0 to 59 in steps of 1) last 16 bits Seconds (xx:xx:SS.SSS), (0=00.000s, 1=00.001,..., 59999=59.999s)
F060	FLOATING_POINT	IEE FLOATING POINT (32 bits)
F070	HEX2	2 BYTES - 4 ASCII DIGITS
F071	HEX4	4 BYTES - 8 ASCII DIGITS
F072	HEX6	6 BYTES - 12 ASCII DIGITS
F073	HEX8	8 BYTES - 16 ASCII DIGITS
F074	HEX20	20 BYTES - 40 ASCII DIGITS
F100	ENUMERATION	VT CONNECTION TYPE 0 Wye 1 Delta
F101	ENUMERATION	MESSAGE DISPLAY INTENSITY 0 25% 1 50% 2 75% 3 100%

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 2 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F102	ENUMERATION	DISABLED/ENABLED
	0	Disabled
	1	Enabled
F103	ENUMERATION	CURVE SHAPES
	0	IEEE Moderately Inverse
	1	IEEE Very Inverse
	2	IEEE Extremely Inverse
	3	IEC Curve A
	4	IEC Curve B
	5	IEC Curve C
	6	IEC Short Inverse
	7	IAC Extremely Inverse
	8	IAC Very Inverse
	9	IAC Inverse
	10	IAC Short Inverse
	11	I2t
	12	Definite Time
	13	Flexcurve A
	14	Flexcurve B
F104	ENUMERATION	RESET TYPE
	0	Instantaneous
	1	Timed
F105	ENUMERATION	LOGIC INPUT
	0	Disabled
	1	Input 1
	2	Input 2
F106	ENUMERATION	PHASE ROTATION
	0	ABC
	1	ACB
F108	ENUMERATION	OFF/ON
	0	OFF
	1	ON
F109	ENUMERATION	CONTACT OUTPUT OPERATION
	0	Self-Reset
	1	Latched
	2	Disabled
F110	ENUMERATION	CONTACT OUTPUT LED CONTROL
	0	Trip
	1	Alarm
	2	None
F111	ENUMERATION	UNDERVOLTAGE CURVE SHAPES
	0	Definite Time
	1	Inverse Time

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 3 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F112	ENUMERATION	RS485 BAUD RATES
	0	300 baud
	1	1200 baud
	2	2400 baud
	3	4800 baud
	4	9600 baud
	5	19200 baud
	6	38400 baud
	7	57600 baud
	8	115200 baud
F113	ENUMERATION	PARITY
	0	None
	1	Odd
	2	Even
F114	ENUMERATION	IRIG-B SIGNAL TYPE
	0	None
	1	DC Shift
	2	Amplitude Modulated
F115	ENUMERATION	BREAKER STATUS
	0	Auxiliary A
	1	Auxiliary B
F117	ENUMERATION	NUMBER OF OSCILLOGRAPHY RECORDS
	0	1 x 72 cycles
	1	3 x 36 cycles
	2	7 x 18 cycles
	3	15 x 9 cycles
F118	ENUMERATION	OSCILLOGRAPHY MODE
	0	Automatic Overwrite
	1	Protected
F119	ENUMERATION	FLEXCURVE PICKUP RATIOS
	0	0
	1	0.05
	2	0.1
	3	0.15
	4	0.2
	5	0.25
	6	0.3
	7	0.35
	8	0.4
	9	0.45
	10	0.48
	11	0.5
	12	0.52
	13	0.54
	14	0.56
	15	0.58

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 4 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F119 continued	16	0.6
	17	0.62
	18	0.64
	19	0.66
	20	0.68
	21	0.7
	22	0.72
	23	0.74
	24	0.76
	25	0.78
	26	0.8
	27	0.82
	28	0.84
	29	0.86
	30	0.88
	31	0.9
	32	0.91
	33	0.92
	34	0.93
	35	0.94
	36	0.95
	37	0.96
	38	0.97
	39	0.98
	40	1.03
	41	1.05
	42	1.1
	43	1.2
	44	1.3
	45	1.4
	46	1.5
	47	1.6
	48	1.7
	49	1.8
	50	1.9
	51	2
	52	2.1
	53	2.2
	54	2.3
	55	2.4
	56	2.5
	57	2.6
	58	2.7
	59	2.8
	60	2.9

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 5 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F119 continued	61	3
	62	3.1
	63	3.2
	64	3.3
	65	3.4
	66	3.5
	67	3.6
	68	3.7
	69	3.8
	70	3.9
	71	4
	72	4.1
	73	4.2
	74	4.3
	75	4.4
	76	4.5
	77	4.6
	78	4.7
	79	4.8
	80	4.9
	81	5
	82	5.1
	83	5.2
	84	5.3
	85	5.4
	86	5.5
	87	5.6
	88	5.7
	89	5.8
	90	5.9
	91	6
	92	6.5
	93	7
	94	7.5
	95	8
	96	8.5
	97	9
	98	9.5
	99	10
	100	10.5
	101	11
	102	11.5
	103	12
	104	12.5
	105	13

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 6 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F119 continued	106	13.5
	107	14
	108	14.5
	109	15
	110	15.5
	111	16
	112	16.5
	113	17
	114	17.5
	115	18
	116	18.5
	117	19
	118	19.5
	119	20
F122	ENUMERATION	ELEMENT INPUT SIGNAL TYPE
	0	Phasor
	1	RMS
F123	ENUMERATION	CT SECONDARY
	0	1 A
	1	5 A
F124	ENUMERATION	LIST OF ELEMENTS
	0	PHASE IOC1
	1	PHASE IOC2
	2	PHASE IOC3
	3	PHASE IOC4
	4	PHASE IOC5
	5	PHASE IOC6
	6	PHASE IOC7
	7	PHASE IOC8
	8	PHASE IOC9
	9	PHASE IOC10
	10	PHASE IOC11
	11	PHASE IOC12
	16	16 = PHASE TOC1
	17	17 = PHASE TOC2
	18	18 = PHASE TOC3
	19	19 = PHASE TOC4
	20	20 = PHASE TOC5
	21	PHASE TOC6
	24	PH DIR1
	25	PH DIR2
	32	NEUTRAL IOC1
	33	NEUTRAL IOC2
	34	NEUTRAL IOC3
	35	NEUTRAL IOC4

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 7 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F124 continued	36	NEUTRAL IOC5
	37	NEUTRAL IOC6
	38	NEUTRAL IOC7
	39	NEUTRAL IOC8
	40	NEUTRAL IOC9
	41	NEUTRAL IOC10
	42	NEUTRAL IOC11
	43	NEUTRAL IOC12
	48	NEUTRAL TOC1
	49	NEUTRAL TOC2
	50	NEUTRAL TOC3
	51	NEUTRAL TOC4
	52	NEUTRAL TOC5
	53	NEUTRAL TOC6
	56	NTRL DIR OC1
	57	NTRL DIR OC2
	60	NEG SEQ DIR OC1
	61	NEG SEQ DIR OC2
	64	GROUND IOC1
	65	GROUND IOC2
	66	GROUND IOC3
	67	GROUND IOC4
	68	GROUND IOC5
	69	GROUND IOC6
	70	GROUND IOC7
	71	GROUND IOC8
	72	GROUND IOC9
	73	GROUND IOC10
	74	GROUND IOC11
	75	GROUND IOC12
	80	GROUND TOC1
	81	GROUND TOC2
	82	GROUND TOC3
	83	GROUND TOC4
	84	GROUND TOC5
	85	GROUND TOC6
	86	RESTD GND FT1
	87	RESTD GND FT2
	88	RESTD GND FT3
	89	RESTD GND FT4
	90	RESTD GND FT5
	91	RESTD GND FT6
	96	NEG SEQ IOC1
	97	NEG SEQ IOC2
	112	NEG SEQ TOC1

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 8 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F124 continued	113	NEG SEQ TOC2
	128	HI-Z
	129	BUS 1
	130	BUS 2
	144	PHASE UV1
	145	PHASE UV2
	152	PHASE OV1
	160	PH DIST Z1
	161	PH DIST Z2
	162	PH DIST Z3
	163	PH DIST Z4
	168	LINE PICKUP
	176	GND DIST Z1
	177	GND DIST Z2
	178	GND DIST Z3
	179	GND DIST Z4
	184	DUTT
	185	PUTT
	186	POTT
	187	HYBRID POTT
	188	BLOCK SCHEME
	208	XFMR INST DIFF
	209	XFMR PCNT DIFF
	224	SRC1 VT FUSE FAIL
	225	SRC2 VT FUSE FAIL
	226	SRC3 VT FUSE FAIL
	227	SRC4 VT FUSE FAIL
	228	SRC5 VT FUSE FAIL
	229	SRC6 VT FUSE FAIL
	232	SRC1 50DD
	233	SRC2 50DD
	234	SRC3 50DD
	235	SRC4 50DD
	236	SRC5 50DD
	237	SRC6 50DD
	240	87L DIFF
	242	OPEN POLE
	244	50DD
	245	CONT MONITOR
	246	CT FAIL
	247	CT TROUBLE1
	248	CT TROUBLE2
	249	87L TRIP
	250	STUB BUS
	256	87PC

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 9 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F124 continued	272	BREAKER 1
	273	BREAKER 2
	280	BKR FAIL 1
	281	BKR FAIL 2
	288	BKR ARC 1
	289	BKR ARC 2
	304	AR 1
	305	AR 2
	306	AR 3
	307	AR 4
	308	AR 5
	309	AR 6
	312	SYNC 1
	313	SYNC 2
	320	COLD LOAD 1
	321	COLD LOAD 2
	336	SETTING GROUP
	337	RESET
	352	UNDERFREQ 1
	353	UNDERFREQ 2
	354	UNDERFREQ 3
	355	UNDERFREQ 4
	356	UNDERFREQ 5
	357	UNDERFREQ 6
	512	DIG ELEM 1
	513	DIG ELEM 2
	514	DIG ELEM 3
	515	DIG ELEM 4
	516	DIG ELEM 5
	517	DIG ELEM 6
	518	DIG ELEM 7
	519	DIG ELEM 8
	520	DIG ELEM 9
	521	DIG ELEM 10
	522	DIG ELEM 11
	523	DIG ELEM 12
	524	DIG ELEM 13
	525	DIG ELEM 14
	526	DIG ELEM 15
	527	DIG ELEM 16
	544	COUNTER 1
	545	COUNTER 2
	546	COUNTER 3
	547	COUNTER 4

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 10 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F124 continued	548	COUNTER 5
	549	COUNTER 6
	550	COUNTER 7
	551	COUNTER 8
F125	ENUMERATION	ACCESS LEVEL
	0	Restricted
	1	Command
	2	Setting
F126	ENUMERATION	NO/YES CHOICE
	0	No
	1	Yes
F127	ENUMERATION	LATCHED OR SELF-RESETTING
	0	Latched
	1	Self-Reset
F128	ENUMERATION	CONTACT INPUT THRESHOLD
	0	16 Vdc
	1	30 Vdc
	2	80 Vdc
F129	ENUMERATION	FLEXLOGIC TIMER TYPE
	0	millisecond
	1	second
	2	minute
F130	ENUMERATION	SIMULATION MODE
	0	Off
	1	Pre-Fault
	2	Fault
F131	ENUMERATION	FORCED CONTACT OUTPUT STATE
	0	Disabled
	1	Energized
	2	De-energized
F133	ENUMERATION	PROGRAM STATE
	0	Not Programmed
	1	Programmed
F134	ENUMERATION	PASS/FAIL
	0	Fail
	1	OK
	2	n/a
F135	ENUMERATION	GAIN CALIBRATION
	0	x1
	1	x16

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 11 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F136	ENUMERATION	NUMBER OF OSCILLOGRAPHY RECORDS
	0	31 x 8 cycles
	1	15 x 16 cycles
	2	7 x 32 cycles
	3	3 x 64 cycles
	4	1 x 128 cycles
F138	ENUMERATION	OSCILLOGRAPHY FILE TYPE
	0	Data File
	1	Configuration File
F140	ENUMERATION	CURRENT, SENS CURRENT, VOLTAGE, DISABLED
	0	Disabled
	1	Current 46A
	2	Voltage 280V
	3	Current 4.6A
	4	Current 2A
	5	Notched 4.6A
	6	Notched 2A
F141	ENUMERATION	SELF TEST ERROR
	0	Any Self-Tests
	1	IRIG-B FAILURE
	2	DSP ERROR
	4	NO DSP INTERRUPTS
	5	UNIT NOT CALIBRATED
	7	CLOCK NOT SET
	8	FACTORY SERVICE MODE
	9	PROTOTYPE FIRMWARE
	10	FLEXLOGIC ERR TOKEN
	11	EQUIPMENT MISMATCH
	12	RAM CODE FAILURE
	13	UNIT NOT PROGRAMMED
	14	SYSTEM EXCEPTION
	15	SYNCHRONIZING
F141 continued	16	CHANNEL 1 FAILED
	17	CHANNEL 2 FAILED
	18	FLASH PROGRAMMING
	19	BATTERY FAIL
	20	PRI ETHERNET FAIL
	21	SEC ETHERNET FAIL
	22	EEPROM DATA ERROR
	23	SRAM DATA ERROR
	24	PROGRAM MEMORY
	25	WATCHDOG ERROR
	26	LOW ON MEMORY
	27	REMOTE DEVICE OFF

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 12 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F142	ENUMERATION	EVENT RECORDER ACCESS FILE TYPE
	0	All Record Data
	1	Headers Only
	2	Numeric Event Cause
F143	UR_UINT32	32 BIT ERROR CODE (F141 specifies the bit number)
		A bit value of 0 = no error, 1 = error
F144	ENUMERATION	FORCED CONTACT INPUT STATE
	0	Disabled
	1	Open
	2	Closed
F145	ENUMERATION	ALPHABET LETTER
	0	null
	1	A
	2	B
	↓	↓
	26	Z
F146	ENUMERATION	MISC. EVENT CAUSES
	0	EVENTS CLEARED
	1	OSCILLOGRAPHY TRIG'D
	2	DATE/TIME CHANGED
	3	DEF SETTINGS LOADED
	4	TEST MODE ON
	5	TEST MODE OFF
	6	POWER ON
	7	POWER OFF
	8	RELAY IN SERVICE
	9	RELAY OUT OF SERVICE
	10	WATCHDOG RESET
	11	OSCILLOGRAPHY CLEAR
F147	ENUMERATION	LINE LENGTH UNITS
	0	km
	1	miles
F148	ENUMERATION	FAULT TYPE
	0	NA
	1	AG
	2	BG
	3	CG
	4	AB
	5	BC
	6	AC
	7	ABG
	8	BCG
	9	ACG
	10	ABC
	11	ABCG

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 13 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F149	ENUMERATION	87L PHASE COMP SCHEME SELECTION
	0	2TL-PT-DPC-3FC
	1	2TL-PT-SPC-2FC
	2	2TL-PT-DPC-2FC
	3	2TL-BL-DPC-2FC
	4	2/3TL-BL-SPC-AMC
	5	3TL-PT-SPC-2FC
	6	3TL-BL-SPC-2FC
F150	ENUMERATION	87L PHASE COMP SCHEME SIGNAL SELECTION
	0	MIXED
	1	3L_0
F152	ENUMERATION	SETTING GROUP
	0	Active Group
	1	Group 1
	2	Group 2
	3	Group 3
	4	Group 4
	5	Group 5
	6	Group 6
	7	Group 7
F154	ENUMERATION	DISTANCE DIRECTION
	0	Forward
	1	Reverse
F155	ENUMERATION	REMOTE DEVICE STATE
	0	Offline
	1	Online

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 14 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F156	ENUMERATION	REMOTE INPUT BIT PAIRS
	0	None
	1	DNA-1
	2	DNA-2
	3	DNA-3
	4	DNA-4
	5	DNA-5
	6	DNA-6
	7	DNA-7
	8	DNA-8
	9	DNA-9
	10	DNA-10
	11	DNA-11
	12	DNA-12
	13	DNA-13
	14	DNA-14
	15	DNA-15
	16	DNA-16
	17	DNA-17
	18	DNA-18
	19	DNA-19
	20	DNA-20
	21	DNA-21
	22	DNA-22
	23	DNA-23
	24	DNA-24
	25	DNA-25
	26	DNA-26
	27	DNA-27
	28	DNA-28
	29	DNA-29
	30	DNA-30
	31	DNA-31
	32	DNA-32
	33	UserSt-1
	34	UserSt-2
	35	UserSt-3
	36	UserSt-4
	37	UserSt-5
	38	UserSt-6
	39	UserSt-7
	40	UserSt-8
	41	UserSt-9

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 15 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F156 continued	42	UserSt-10
	43	UserSt-11
	44	UserSt-12
	45	UserSt-13
	46	UserSt-14
	47	UserSt-15
	48	UserSt-16
	49	UserSt-17
	50	UserSt-18
	51	UserSt-19
	52	UserSt-20
	53	UserSt-21
	54	UserSt-22
	55	UserSt-23
	56	UserSt-24
	57	UserSt-25
	58	UserSt-26
	59	UserSt-27
	60	UserSt-28
	61	UserSt-29
	62	UserSt-30
	63	UserSt-31
	64	UserSt-32
F157	ENUMERATION	BREAKER MODE
	0	3-Pole
	1	1-Pole
F158	ENUMERATION	SCHEME CALIBRATION TEST
	0	Normal
	1	Symmetry 1
	2	Symmetry 2
	3	Delay 1
	4	Delay 2
F159	ENUMERATION	BREAKER AUX CONTACT KEYING
	0	52a
	1	52b
	2	None
F166	ENUMERATION	AUXILIARY VT CONNECTION TYPE
	0	Vn
	1	Vag
	2	Vbg
	3	Vcg
	4	Vab
	5	Vbc
	6	Vca

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 16 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F167	ENUMERATION	SIGNAL SOURCE
	0	SRC 1
	1	SRC 2
	2	SRC 3
	3	SRC 4
	4	SRC 5
	5	SRC 6
F168	ENUMERATION	INRUSH INHIBIT FUNCTION
	0	Disabled
	1	2nd
F169	ENUMERATION	OVEREXCITATION INHIBIT FUNCTION
	0	Disabled
	1	5th
F170	ENUMERATION	LOW/HIGH OFFSET & GAIN TRANSDUCER I/O SELECTION
	0	LOW
	1	HIGH
F171	ENUMERATION	TRANSDUCER CHANNEL INPUT TYPE
	0	dcmA IN
	1	OHMS IN
	2	RTD IN
	3	dcmA OUT
F172	ENUMERATION	SLOT LETTERS
	0	F
	1	G
	2	H
	3	J
	4	K
	5	L
	6	M
	7	N
	8	P
	9	R
	10	S
	11	T
	12	U
	13	V
	14	W
	15	X
F173	ENUMERATION	TRANSDUCER DCMA INPUT/OUTPUT RANGE
	0	0 to -1 mA
	1	0 to 1 mA
	2	-1 to 1 mA
	3	0 to 5 mA
	4	0 to 10 mA
	5	0 to 20 mA
	6	4 to 20 mA

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 17 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F174	ENUMERATION	TRANSDUCER RTD INPUT TYPE
	0	100 Ohm Platinum
	1	120 Ohm Nickel
	2	100 Ohm Nickel
	3	10 Ohm Copper
F175	ENUMERATION	PHASE LETTERS
	0	A
	1	B
F176	ENUMERATION	SYNCHROCHECK DEAD SOURCE SELECT
	0	None
	1	LV1 and DV2
	2	DV1 and LV2
	3	DV1 or DV2
	4	DV1 Xor DV2
	5	DV1 and DV2
F177	ENUMERATION	COMMUNICATION PORT
	0	None
	1	COM1 - RS485
	2	COM2 - RS485
	3	Front Panel - RS232
F178	ENUMERATION	DATA LOGGER RATES
	0	1 sec
	1	1 min
	2	5 min
	3	10 min
	4	15 min
	5	20 min
	6	30 min
	7	60 min
F180	ENUMERATION	PHASE/GROUND
	0	Phase
F181	ENUMERATION	ODD/EVEN/NONE
	0	Odd
	1	Even
F183	ENUMERATION	AC INPUT WAVEFORMS
	0	Off
	1	8 samples/cycle
	2	16 samples/cycle
	3	32 samples/cycle
	4	64 samples/cycle

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 18 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F185	ENUMERATION	PHASE A,B,C, GROUND SELECTOR
	0	A
	1	B
	2	C
	3	G
F186	ENUMERATION	MEASUREMENT MODE
	0	Phase to Ground
	1	Phase to Phase
F190	ENUMERATION	SIMULATED KEYPRESS
	0	No key -- use between real keys
	1	1
	2	2
	3	3
	4	4
	5	5
	6	6
	7	7
	8	8
	9	9
	10	0
	11	Decimal Point
	12	Plus/Minus
	13	Value Up
	14	Value Down
	15	Message Up
	16	Message Down
	17	Message Left
	18	Message Right
	19	Menu
	20	Help
	21	Escape
	22	Enter
	23	Reset
	24	User 1
	25	User 2
	26	User 3
F200	TEXT40	40 CHARACTER ASCII TEXT
		20 registers -16 Bits: 1st Char MSB, 2nd Char. LSB
F201	TEXT8	8 CHARACTER ASCII PASSCODE
		4 registers -16 Bits: 1st Char MSB, 2nd Char. LSB
F202	TEXT20	20 CHARACTER ASCII TEXT
		10 registers -16 Bits: 1st Char MSB, 2nd Char. LSB
F203	TEXT16	16 CHARACTER ASCII TEXT
F204	TEXT80	80 CHARACTER ASCII TEXT
F205	TEXT12	12 CHARACTER ASCII TEXT
F206	TEXT6	6 CHARACTER ASCII TEXT
F207	TEXT4	4 CHARACTER ASCII TEXT

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 19 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F208	TEXT2	2 CHARACTER ASCII TEXT
F222	ENUMERATION	TEST ENUMERATION
	0	Test Enumeration 0
	1	Test Enumeration 1
F230	ENUMERATION	DIRECTIONAL POLARIZING
	0	Voltage
	1	Current
	2	Dual
F300	UR_UINT16	FLEXLOGIC BASE TYPE (6 bit type) The flexlogic BASE type is 6 bits and is combined with a 9 bit descriptor and 1 bit for protection element to form a 16 bit value. The combined bits are of the form : PTTTTTDDDDDDDD where P bit if set, indicates that the flexlogic type is associated with a protection element state and T represents bits for the BASE type, and D represents bits for the descriptor. The values in square brackets indicate the base type with P prefix [PTTTTT] and the values in round brackets indicate the descriptor range. [0] Off(0) this is boolean FALSE value [0] On (1) This is boolean TRUE value [2] CONTACT INPUTS (1 - 96) [3] CONTACT INPUTS OFF (1-96) [4] VIRTUAL INPUTS (1-64) [6] VIRTUAL OUTPUTS (1-64) [10] CONTACT OUTPUTS VOLTAGE DETECTED (1-64) [11] CONTACT OUTPUTS VOLTAGE OFF DETECTED (1-64) [12] CONTACT OUTPUTS CURRENT DETECTED (1-64) [13] CONTACT OUTPUTS CURRENT OFF DETECTED (1-64) [14] REMOTE INPUTS (1-32) [28] INSERT (Via Keypad only) [32] END [34] NOT (1 INPUT) [36] 2 INPUT XOR (0) [38] LATCH SET/RESET (2 INPUTS) [40] OR (2-16 INPUTS) [42] AND (2-16 INPUTS) [44] NOR (2-16 INPUTS) [46] NAND (2-16 INPUTS) [48] TIMER (1-32) [50] ASSIGN VIRTUAL OUTPUT (1 - 64) [52] SELF-TEST ERROR (See F141 for range) [56] ACTIVE SETTING GROUP (1-8) [62] MISCELLANEOUS EVENTS (See F146 for range) [64-127] ELEMENT STATES (Refer to Memory Map Element States Section)
F400	UR_UINT16	CT/VT BANK SELECTION
	0	Card 1 Contact 1 to 4
	1	Card 1 Contact 5 to 8
	2	Card 2 Contact 1 to 4
	3	Card 2 Contact 5 to 8
	4	Card 3 Contact 1 to 4
	5	Card 3 Contact 5 to 8
F500	UR_UINT16	PACKED BITFIELD First register indicates I/O state with bits 0(MSB)-15(LSB) corresponding to I/O state 1-16 Second register indicates I/O state with bits 0-15 corresponding to I/O state 17-32 Third register indicates I/O state with bits 0-15 corresponding to I/O state 33-48 Fourth register indicates I/O state with bits 0-15 corresponding to I/O state 49-64 A bit value of 0 = Off, 1 = On
F501	UR_UINT16	LED STATUS Low byte of register indicates LED status with bit 0 representing the top LED and bit 7 the bottom LED. A bit value of 1 indicates the LED is on, 0 indicates the LED is off.
F502	BITFIELD	ELEMENT OPERATE STATES Each bit contains the operate state for an element. See the F124 format code for a list of element IDs. The operate bit for element ID X is bit [X mod 16] in register [X/16].

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 20 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F504	BITFIELD	3 PHASE ELEMENT STATE
	0	Pickup
	1	Operate
	2	Pickup Phase A
	3	Pickup Phase B
	4	Pickup Phase C
	5	Operate Phase A
	6	Operate Phase B
	7	Operate Phase C
F505	BITFIELD	CONTACT OUTPUT STATE
	0	Contact State
	1	Voltage Detected
F506	BITFIELD	1 PHASE ELEMENT STATE
	0	Pickup
	1	Operate
F507	BITFIELD	COUNTER ELEMENT STATE
	0	Count Greater Than
	1	Count Equal To
F509	BITFIELD	SIMPLE ELEMENT STATE
	0	Operate
F510	BITFIELD	87L ELEMENT STATE
	0	Operate A
	1	Operate B
	2	Operate C
	3	Received DTT
	4	Operate
	5	Key DTT
	6	PFL Fail
	7	PFL OK
	8	Channel 1 Fail
	9	Channel 2 Fail
	10	Channel 1 Lost Packet
	11	Channel 2 Lost Packet
	12	Channel 1 CRC Fail
	13	Channel 2 CRC Fail
F511	BITFIELD	3 PHASE SIMPLE ELEMENT STATE
	0	Operate
	1	Operate A
	2	Operate B
F511	BITFIELD	3 PHASE SIMPLE ELEMENT STATE
	0	Operate
	1	Operate A
	2	Operate B
F511	BITFIELD	3 PHASE SIMPLE ELEMENT STATE
	0	Operate
	1	Operate A
	2	Operate B
F511	BITFIELD	3 PHASE SIMPLE ELEMENT STATE
	0	Operate
	1	Operate A
	2	Operate B

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Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 21 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
F512	ENUMERATION	HARMONIC NUMBER
	0	2ND
	1	3RD
	2	4TH
	3	5TH
	4	6TH
	5	7TH
	6	8TH
	7	9TH
	8	10TH
	9	11TH
	10	12TH
	11	13TH
	12	14TH
	13	15TH
	14	16TH
	15	17TH
	16	18TH
	17	19TH
	18	20TH
	19	21ST
	20	22ND
	21	23RD
	22	24TH
	23	25TH
F600	UR_UINT16	FLEXANALOG PARAMETER
		The 16-bit value corresponds to the modbus address
		of the value to be used when this parameter is selected.
		Only certain values may be used as FlexAnalog (basically all the metering quantities used in protection)
MMI_FLASH	ENUMERATION	FLASH MESSAGE DEFINITIONS FOR FRONT PANEL MMI
	0	
	1	ADJUSTED VALUE HAS BEEN STORED
	2	ENTERED PASSCODE IS INVALID
	3	COMMAND EXECUTED
	4	DEFAULT MESSAGE HAS BEEN ADDED
	5	DEFAULT MESSAGE HAS BEEN REMOVED
	6	INPUT FUNCTION IS ALREADY ASSIGNED
	7	PRESS [ENTER] TO ADD AS DEFAULT
	8	PRESS [ENTER] TO REMOVE MESSAGE
	9	PRESS [ENTER] TO BEGIN TEXT EDIT
	10	ENTRY MISMATCH - CODE NOT STORED
	11	PRESSED KEY IS INVALID HERE
	12	INVALID KEY: MUST BE IN LOCAL MODE
	13	NEW PASSWORD HAS BEEN STORED

Table B–10: MODBUS® MEMORY MAP DATA FORMATS (Sheet 22 of 22)

FORMAT CODE	FORMAT TYPE/ BITMASK	FORMAT DEFINITION
MMI_FLASH continued	14	PLEASE ENTER A NON-ZERO PASSCODE
	15	NO ACTIVE TARGETS (TESTING LEDS)
	16	OUT OF RANGE - VALUE NOT STORED
	17	RESETTING LATCHED CONDITIONS
	18	SETPOINT ACCESS IS NOW ALLOWED
	19	SETPOINT ACCESS DENIED (PASSCODE)
	20	SETPOINT ACCESS IS NOW RESTRICTED
	21	NEW SETTING HAS BEEN STORED
	22	SETPOINT ACCESS DENIED (SWITCH)
	23	DATA NOT ACCEPTED
	24	NOT ALL CONDITIONS HAVE BEEN RESET
	25	DATE NOT ACCEPTED IRIGB IS ENABLED
	26	NOT EXECUTED
	27	DISPLAY ADDED TO USER DISPLAY LIST
	28	DISPLAY NOT ADDED TO USER DISPLAY LIST
	29	DISPLAY REMOVED FROM USER DISPLAY LIST
MMI_PASS WORD_TY PE	ENUMERATION	PASSWORD TYPES FOR DISPLAY IN PASSWORD PROMPT
	0	NO
	1	MASTER
	2	SETTING
	3	COMMAND
	4	FACTORY
MMI_SETTI NG_TYPE	ENUMERATION	SETTING TYPES FOR DISPLAY IN WEB PAGES
	0	Unrestricted Setting
	1	Master-accessed Setting
	2	Setting
	3	Command
	4	Factory Setting

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B.5.3 MODBUS® MEMORY MAP

Table B–11: MODBUS® MEMORY MAP (Sheet 1 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Product Information (Read Only)						
0000	UR Product Type	0 to 65535	---	1	F001	0
0002	Product Version	0 to 655.35	---	0.01	F001	1
Product Information (Read Only – Written by Factory)						
0010	Serial Number	---	---	---	F203	"0"
0020	Manufacturing Date	0 to 4294967295	---	1	F050	0
0022	Modification Number	0 to 65535	---	1	F001	0
0040	Order Code	---	---	---	F204	"Order Code x "
0090	Ethernet MAC Address	---	---	---	F072	0
0093	Reserved (13 items)	---	---	---	F001	0
00A0	CPU Module Serial Number	---	---	---	F203	(none)
00B0	CPU Supplier Serial Number	---	---	---	F203	(none)
00C0	Ethernet Sub Module Serial Number (8 items)	---	---	---	F203	(none)
Self Test Targets (Read Only)						
0200	Self Test States (2 items)	0 to 4294967295	0	1	F143	0
Front Panel (Read Only)						
0204	LED Column x State (9 items)	0 to 65535	---	1	F501	0
0220	Display Message	---	---	---	F204	(none)
Keypress Emulation (Read/Write)						
0280	Simulated keypress -- write zero before each keystroke	0 to 26	---	1	F190	0 (No key; use between real key)
Virtual Input Commands (Read/Write Command) (32 modules)						
0400	Virtual Input x State	0 to 1	---	1	F108	0 (Off)
0401	...Repeated for module number 2					
0402	...Repeated for module number 3					
0403	...Repeated for module number 4					
0404	...Repeated for module number 5					
0405	...Repeated for module number 6					
0406	...Repeated for module number 7					
0407	...Repeated for module number 8					
0408	...Repeated for module number 9					
0409	...Repeated for module number 10					
040A	...Repeated for module number 11					
040B	...Repeated for module number 12					
040C	...Repeated for module number 13					
040D	...Repeated for module number 14					
040E	...Repeated for module number 15					
040F	...Repeated for module number 16					
0410	...Repeated for module number 17					
0411	...Repeated for module number 18					
0412	...Repeated for module number 19					
0413	...Repeated for module number 20					
0414	...Repeated for module number 21					
0415	...Repeated for module number 22					
0416	...Repeated for module number 23					

Table B–11: MODBUS® MEMORY MAP (Sheet 2 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
0417	...Repeated for module number 24					
0418	...Repeated for module number 25					
0419	...Repeated for module number 26					
041A	...Repeated for module number 27					
041B	...Repeated for module number 28					
041C	...Repeated for module number 29					
041D	...Repeated for module number 30					
041E	...Repeated for module number 31					
041F	...Repeated for module number 32					
Digital Counter States (Read Only Non-Volatile) (8 modules)						
0800	Digital Counter x Value	-2147483647 to 2147483647	---	1	F004	0
0802	Digital Counter x Frozen	-2147483647 to 2147483647	---	1	F004	0
0804	Digital Counter x Frozen Time Stamp	0 to 4294967295	---	1	F050	0
0806	Digital Counter x Frozen Time Stamp us	0 to 4294967295	---	1	F003	0
0808	...Repeated for module number 2					
0810	...Repeated for module number 3					
0818	...Repeated for module number 4					
0820	...Repeated for module number 5					
0828	...Repeated for module number 6					
0830	...Repeated for module number 7					
0838	...Repeated for module number 8					
FlexStates (Read Only)						
0900	FlexState Bits (16 items)	0 to 65535	---	1	F001	0
Element States (Read Only)						
1000	Element Operate States (64 items)	0 to 65535	---	1	F502	0
User Displays Actuals (Read Only)						
1080	Formatted user-definable displays (8 items)	---	---	---	F200	(none)
Modbus User Map Actuals (Read Only)						
1200	User Map Values (256 items)	0 to 65535	---	1	F001	0
Element Targets (Read Only)						
14C0	Target Sequence	0 to 65535	---	1	F001	0
14C1	Number of Targets	0 to 65535	---	1	F001	0
Element Targets (Read/Write)						
14C2	Target to Read	0 to 65535	---	1	F001	0
Element Targets (Read Only)						
14C3	Target Message	---	---	---	F200	".."
Digital I/O States (Read Only)						
1500	Contact Input States (6 items)	0 to 65535	---	1	F500	0
1508	Virtual Input States (2 items)	0 to 65535	---	1	F500	0
1510	Contact Output States (4 items)	0 to 65535	---	1	F500	0
1518	Contact Output Current States (4 items)	0 to 65535	---	1	F500	0
1520	Contact Output Voltage States (4 items)	0 to 65535	---	1	F500	0
1528	Virtual Output States (4 items)	0 to 65535	---	1	F500	0
1530	Contact Output Detectors (4 items)	0 to 65535	---	1	F500	0
Remote I/O States (Read Only)						
1540	Remote Device x States	0 to 65535	---	1	F500	0

Table B–11: MODBUS® MEMORY MAP (Sheet 3 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
1542	Remote Input x States (2 items)	0 to 65535	---	1	F500	0
1550	Remote Devices Online	0 to 1	---	1	F126	0 (No)
Remote Device Status (Read Only) (16 modules)						
1551	Remote Device x StNum	0 to 4294967295	---	1	F003	0
1553	Remote Device x SqNum	0 to 4294967295	---	1	F003	0
1555	...Repeated for module number 2					
1559	...Repeated for module number 3					
155D	...Repeated for module number 4					
1561	...Repeated for module number 5					
1565	...Repeated for module number 6					
1569	...Repeated for module number 7					
156D	...Repeated for module number 8					
1571	...Repeated for module number 9					
1575	...Repeated for module number 10					
1579	...Repeated for module number 11					
157D	...Repeated for module number 12					
1581	...Repeated for module number 13					
1585	...Repeated for module number 14					
1589	...Repeated for module number 15					
158D	...Repeated for module number 16					
Ethernet Fibre Channel Status (Read/Write)						
1610	Ethernet Primary Fibre Channel Status	0 to 2	---	1	F134	0 (Fail)
1611	Ethernet Secondary Fibre Channel Status	0 to 2	---	1	F134	0 (Fail)
Data Logger Actuals (Read Only)						
1618	Data Logger Channel Count	0 to 16	CHNL	1	F001	0
1619	Time of oldest available samples	0 to 4294967295	seconds	1	F050	0
161B	Time of newest available samples	0 to 4294967295	seconds	1	F050	0
161D	Data Logger Duration	0 to 999.9	DAYS	0.1	F001	0
Phase Comparison Channel Status (Read Only) (2 modules)						
1641	Channel X Loopback Status	0 to 2	---	1	F134	2 (n/a)
1642	Channel X Delay	0 to 65.535	ms	0.001	F001	0
1643	...Repeated for module number 2					
Source Current (Read Only) (6 modules)						
1800	Phase A Current RMS	0 to 999999.999	A	0.001	F060	0
1802	Phase B Current RMS	0 to 999999.999	A	0.001	F060	0
1804	Phase C Current RMS	0 to 999999.999	A	0.001	F060	0
1806	Neutral Current RMS	0 to 999999.999	A	0.001	F060	0
1808	Phase A Current Magnitude	0 to 999999.999	A	0.001	F060	0
180A	Phase A Current Angle	-359.9 to 0	°	0.1	F002	0
180B	Phase B Current Magnitude	0 to 999999.999	A	0.001	F060	0
180D	Phase B Current Angle	-359.9 to 0	°	0.1	F002	0
180E	Phase C Current Magnitude	0 to 999999.999	A	0.001	F060	0
1810	Phase C Current Angle	-359.9 to 0	°	0.1	F002	0
1811	Neutral Current Magnitude	0 to 999999.999	A	0.001	F060	0
1813	Neutral Current Angle	-359.9 to 0	°	0.1	F002	0
1814	Ground Current RMS	0 to 999999.999	A	0.001	F060	0
1816	Ground Current Magnitude	0 to 999999.999	A	0.001	F060	0

Table B–11: MODBUS® MEMORY MAP (Sheet 4 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
1818	Ground Current Angle	-359.9 to 0	°	0.1	F002	0
1819	Zero Sequence Current Magnitude	0 to 999999.999	A	0.001	F060	0
181B	Zero Sequence Current Angle	-359.9 to 0	°	0.1	F002	0
181C	Positive Sequence Current Magnitude	0 to 999999.999	A	0.001	F060	0
181E	Positive Sequence Current Angle	-359.9 to 0	°	0.1	F002	0
181F	Negative Sequence Current Magnitude	0 to 999999.999	A	0.001	F060	0
1821	Negative Sequence Current Angle	-359.9 to 0	°	0.1	F002	0
1822	Differential Ground Current Magnitude	0 to 999999.999	A	0.001	F060	0
1824	Differential Ground Current Angle	-359.9 to 0	°	0.1	F002	0
1825	Reserved (27 items)	---	---	---	F001	0
1840	...Repeated for module number 2					
1880	...Repeated for module number 3					
18C0	...Repeated for module number 4					
1900	...Repeated for module number 5					
1940	...Repeated for module number 6					
Source Voltage (Read Only) (6 modules)						
1A00	Phase AG Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A02	Phase BG Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A04	Phase CG Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A06	Phase AG Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A08	Phase AG Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A09	Phase BG Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A0B	Phase BG Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A0C	Phase CG Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A0E	Phase CG Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A0F	Phase AB or AC Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A11	Phase BC or BA Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A13	Phase CA or CB Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A15	Phase AB or AC Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A17	Phase AB or AC Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A18	Phase BC or BA Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A1A	Phase BC or BA Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A1B	Phase CA or CB Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A1D	Phase CA or CB Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A1E	Auxiliary Voltage RMS	0 to 999999.999	V	0.001	F060	0
1A20	Auxiliary Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A22	Auxiliary Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A23	Zero Sequence Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A25	Zero Sequence Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A26	Positive Sequence Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A28	Positive Sequence Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A29	Negative Sequence Voltage Magnitude	0 to 999999.999	V	0.001	F060	0
1A2B	Negative Sequence Voltage Angle	-359.9 to 0	°	0.1	F002	0
1A2C	Reserved (20 items)	---	---	---	F001	0
1A40	...Repeated for module number 2					
1A80	...Repeated for module number 3					
1AC0	...Repeated for module number 4					

Table B–11: MODBUS® MEMORY MAP (Sheet 5 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
1B00	...Repeated for module number 5					
1B40	...Repeated for module number 6					
Source Power (Read Only) (6 modules)						
1C00	Three Phase Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C02	Phase A Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C04	Phase B Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C06	Phase C Real Power	-1000000000000 to 1000000000000	W	0.001	F060	0
1C08	Three Phase Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C0A	Phase A Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C0C	Phase B Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C0E	Phase C Reactive Power	-1000000000000 to 1000000000000	var	0.001	F060	0
1C10	Three Phase Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C12	Phase A Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C14	Phase B Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C16	Phase C Apparent Power	-1000000000000 to 1000000000000	VA	0.001	F060	0
1C18	Three Phase Power Factor	-0.999 to 1	---	0.001	F013	0
1C19	Phase A Power Factor	-0.999 to 1	---	0.001	F013	0
1C1A	Phase B Power Factor	-0.999 to 1	---	0.001	F013	0
1C1B	Phase C Power Factor	-0.999 to 1	---	0.001	F013	0
1C1C	Reserved (4 items)	---	---	---	F001	0
1C20	...Repeated for module number 2					
1C40	...Repeated for module number 3					
1C60	...Repeated for module number 4					
1C80	...Repeated for module number 5					
1CA0	...Repeated for module number 6					
Source Frequency (Read Only) (6 modules)						
1D80	Frequency	2 to 90	Hz	0.01	F001	0
1D81	...Repeated for module number 2					
1D82	...Repeated for module number 3					
1D83	...Repeated for module number 4					
1D84	...Repeated for module number 5					
1D85	...Repeated for module number 6					
Breaker Arcing Current Actuals (Read Only Non-Volatile) (2 modules)						
2200	Breaker x Arcing Amp Phase A	0 to 99999999	kA2-cyc	1	F060	0
2202	Breaker x Arcing Amp Phase B	0 to 99999999	kA2-cyc	1	F060	0
2204	Breaker x Arcing Amp Phase C	0 to 99999999	kA2-cyc	1	F060	0
2206	...Repeated for module number 2					
Breaker Arcing Current Commands (Read/Write Command) (2 modules)						
220C	Breaker x Arcing Clear Command	0 to 1	---	1	F126	0 (No)
220D	...Repeated for module number 2					

Table B–11: MODBUS® MEMORY MAP (Sheet 6 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Synchrocheck Actuals (Read Only) (2 modules)						
2400	Synchrocheck X Delta Voltage	-1000000000000 to 1000000000000	V	1	F060	0
2402	Synchrocheck X Delta Frequency	0 to 655.35	Hz	0.01	F001	0
2403	Synchrocheck X Delta Phase	0 to 359.9	°	0.1	F001	0
2404	...Repeated for module number 2					
Autoreclose Status (Read Only) (6 modules)						
2410	Autoreclose Count	0 to 65535	---	1	F001	0
2411	...Repeated for module number 2					
2412	...Repeated for module number 3					
2413	...Repeated for module number 4					
2414	...Repeated for module number 5					
2415	...Repeated for module number 6					
Power Swing Detect Actual Values (Read Only)						
2420	Power Swing S1 S2 Angle	-180 to 180	°	0.01	F001	0
Expanded FlexStates (Read Only)						
2B00	FlexStates, one per register (256 items)	0 to 1	---	1	F108	0 (Off)
Expanded Digital I/O states (Read Only)						
2D00	Contact Input States, one per register (96 items)	0 to 1	---	1	F108	0 (Off)
2D80	Contact Out States, one per register (64 items)	0 to 1	---	1	F108	0 (Off)
2E00	Virtual Output States, one per register (64 items)	0 to 1	---	1	F108	0 (Off)
Expanded Remote I/O Status (Read Only)						
2F00	Remote Device States, one / register (16 items)	0 to 1	---	1	F155	0 (Offline)
2F80	Remote Input States, one per register (32 items)	0 to 1	---	1	F108	0 (Off)
Oscillography Values (Read Only)						
3000	Oscillography Number of Triggers	0 to 65535	---	1	F001	0
3001	Oscillography Available Records	0 to 65535	---	1	F001	0
3002	Oscillography Last Cleared Date	0 to 400000000	---	1	F050	0
3004	Oscillography Number Of Cycles Per Record	0 to 65535	---	1	F001	0
Oscillography Commands (Read/Write Command)						
3005	Oscillography Force Trigger	0 to 1	---	1	F126	0 (No)
3011	Oscillography Clear Data	0 to 1	---	1	F126	0 (No)
Fault Report Indexing (Read Only Non-Volatile)						
3020	Number Of Fault Reports	0 to 65535	---	1	F001	0
Fault Reports (Read Only Non-Volatile) (10 modules)						
3030	Fault Time	0 to 4294967295	---	1	F050	0
3032	...Repeated for module number 2					
3034	...Repeated for module number 3					
3036	...Repeated for module number 4					
3038	...Repeated for module number 5					
303A	...Repeated for module number 6					
303C	...Repeated for module number 7					
303E	...Repeated for module number 8					
3040	...Repeated for module number 9					
3042	...Repeated for module number 10					
Modbus File Transfer (Read/Write)						
3100	Name of file to read	---	---	---	F204	(none)

Table B–11: MODBUS® MEMORY MAP (Sheet 7 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Modbus File Transfer (Read Only)						
3200	Character position of current block within file	0 to 4294967295	---	1	F003	0
3202	Size of currently-available data block	0 to 65535	---	1	F001	0
3203	Block of data from requested file (122 items)	0 to 65535	---	1	F001	0
Event Recorder (Read Only)						
3400	Events Since Last Clear	0 to 4294967295	---	1	F003	0
3402	Number of Available Events	0 to 4294967295	---	1	F003	0
3404	Event Recorder Last Cleared Date	0 to 4294967295	---	1	F050	0
Event Recorder (Read/Write Command)						
3406	Event Recorder Clear Command	0 to 1	---	1	F126	0 (No)
DCMA Input Values (Read Only) (24 modules)						
34C0	DCMA Inputs x Value	-9999.999 to 9999.999	---	0.001	F004	0
34C2	...Repeated for module number 2					
34C4	...Repeated for module number 3					
34C6	...Repeated for module number 4					
34C8	...Repeated for module number 5					
34CA	...Repeated for module number 6					
34CC	...Repeated for module number 7					
34CE	...Repeated for module number 8					
34D0	...Repeated for module number 9					
34D2	...Repeated for module number 10					
34D4	...Repeated for module number 11					
34D6	...Repeated for module number 12					
34D8	...Repeated for module number 13					
34DA	...Repeated for module number 14					
34DC	...Repeated for module number 15					
34DE	...Repeated for module number 16					
34E0	...Repeated for module number 17					
34E2	...Repeated for module number 18					
34E4	...Repeated for module number 19					
34E6	...Repeated for module number 20					
34E8	...Repeated for module number 21					
34EA	...Repeated for module number 22					
34EC	...Repeated for module number 23					
34EE	...Repeated for module number 24					
RTD Input Values (Read Only) (48 modules)						
34F0	RTD Inputs x Value	-32768 to 32767	°C	1	F002	0
34F1	...Repeated for module number 2					
34F2	...Repeated for module number 3					
34F3	...Repeated for module number 4					
34F4	...Repeated for module number 5					
34F5	...Repeated for module number 6					
34F6	...Repeated for module number 7					
34F7	...Repeated for module number 8					
34F8	...Repeated for module number 9					
34F9	...Repeated for module number 10					
34FA	...Repeated for module number 11					

Table B–11: MODBUS® MEMORY MAP (Sheet 8 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
34FB	...Repeated for module number 12					
34FC	...Repeated for module number 13					
34FD	...Repeated for module number 14					
34FE	...Repeated for module number 15					
34FF	...Repeated for module number 16					
3500	...Repeated for module number 17					
3501	...Repeated for module number 18					
3502	...Repeated for module number 19					
3503	...Repeated for module number 20					
3504	...Repeated for module number 21					
3505	...Repeated for module number 22					
3506	...Repeated for module number 23					
3507	...Repeated for module number 24					
3508	...Repeated for module number 25					
3509	...Repeated for module number 26					
350A	...Repeated for module number 27					
350B	...Repeated for module number 28					
350C	...Repeated for module number 29					
350D	...Repeated for module number 30					
350E	...Repeated for module number 31					
350F	...Repeated for module number 32					
3510	...Repeated for module number 33					
3511	...Repeated for module number 34					
3512	...Repeated for module number 35					
3513	...Repeated for module number 36					
3514	...Repeated for module number 37					
3515	...Repeated for module number 38					
3516	...Repeated for module number 39					
3517	...Repeated for module number 40					
3518	...Repeated for module number 41					
3519	...Repeated for module number 42					
351A	...Repeated for module number 43					
351B	...Repeated for module number 44					
351C	...Repeated for module number 45					
351D	...Repeated for module number 46					
351E	...Repeated for module number 47					
351F	...Repeated for module number 48					
Ohm Input Values (Read Only) (2 modules)						
3520	Ohm Inputs x Value	0 to 65535	P	1	F001	0
3521	...Repeated for module number 2					
Passwords (Read/Write Command)						
4000	Command Password Setting	0 to 4294967295	---	1	F003	0
Passwords (Read/Write Setting)						
4002	Setting Password Setting	0 to 4294967295	---	1	F003	0
Passwords (Read/Write)						
4008	Command Password Entry	0 to 4294967295	---	1	F003	0
400A	Setting Password Entry	0 to 4294967295	---	1	F003	0

Table B–11: MODBUS® MEMORY MAP (Sheet 9 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Passwords (Read Only)						
4010	Command Password Status	0 to 1	---	1	F102	0 (Disabled)
4011	Setting Password Status	0 to 1	---	1	F102	0 (Disabled)
Preferences (Read/Write Setting)						
4050	Flash Message Time	0.5 to 10	s	0.1	F001	10
4051	Default Message Timeout	10 to 900	s	1	F001	300
4052	Default Message Intensity	0 to 3	---	1	F101	0 (25 %)
Communications (Read/Write Setting)						
407E	COM1 minimum response time	0 to 1000	ms	10	F001	0
407F	COM2 minimum response time	0 to 1000	ms	10	F001	0
4080	Modbus Slave Address	1 to 254	---	1	F001	254
4083	RS485 Com1 Baud Rate	0 to 11	---	1	F112	8 (115200)
4084	RS485 Com1 Parity	0 to 2	---	1	F113	0 (None)
4085	RS485 Com2 Baud Rate	0 to 11	---	1	F112	8 (115200)
4086	RS485 Com2 Parity	0 to 2	---	1	F113	0 (None)
4087	IP Address	0 to 4294967295	---	1	F003	56554706
4089	IP Subnet Mask	0 to 4294967295	---	1	F003	4294966272
408B	Gateway IP Address	0 to 4294967295	---	1	F003	56554497
408D	Network Address NSAP	---	---	---	F074	0
4097	Default GOOSE Update Time	1 to 60	s	1	F001	60
4098	Ethernet Primary Fibre Channel Link Monitor	0 to 1	---	1	F102	0 (Disabled)
4099	Ethernet Secondary Fibre Channel Link Monitor	0 to 1	---	1	F102	0 (Disabled)
409A	DNP Port	0 to 4	---	1	F177	0 (NONE)
409B	DNP Address	0 to 65519	---	1	F001	1
409C	DNP Client Address (2 items)	0 to 4294967295	---	1	F003	0
40A0	IP port number for the Modbus protocol	1 to 65535	---	1	F001	502
40A1	IP Port Number for the DNP Protocol	1 to 65535	---	1	F001	20000
40A2	IP Port Number for the UCA/MMS Protocol	1 to 65535	---	1	F001	102
40A3	IP Port No. for the HTTP (Web Server) Protocol	1 to 65535	---	1	F001	80
40A4	Main IP Port Number for the TFTP Protocol	1 to 65535	---	1	F001	69
40A5	Data Transfer IP Port Numbers for the TFTP Protocol (zero means "automatic") (2 items)	0 to 65535	---	1	F001	0
40A7	DNP Unsolicited Responses Function	0 to 1	---	1	F102	0 (Disabled)
40A8	DNP Unsolicited Responses Timeout	0 to 60	s	1	F001	0
40A9	DNP Unsolicited Responses Max Retries	1 to 255	---	1	F001	10
40AA	DNP Unsolicited Responses Destination Address	0 to 65519	---	1	F001	1
40AB	Ethernet Operation Mode	0 to 1	---	1	F192	0 (Half-Duplex)
40AC	Communications Reserved (20 items)	0 to 1	---	1	F001	0
40C0	UCA Logical Device Name	0 to 65534	---	1	F203	"UCADevice"
Data Logger Commands (Read/Write Command)						
4170	Clear Data Logger	0 to 1	---	1	F126	0 (No)
Data Logger (Read/Write Setting)						
4180	Data Logger Rate	0 to 7	---	1	F178	1 (1 min.)
4181	Data Logger Channel Settings (16 items)	---	---	---	F600	0
Clock (Read/Write Command)						
41A0	RTC Set Time	0 to 235959	---	1	F003	0
Clock (Read/Write Setting)						
41A2	SR Date Format	0 to 4294967295	---	1	F051	0

Table B–11: MODBUS® MEMORY MAP (Sheet 10 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
41A4	SR Time Format	0 to 4294967295	---	1	F052	0
41A6	IRIG-B Signal Type	0 to 2	---	1	F114	0 (None)
Fault Report Settings and Commands (Read/Write Setting)						
41B0	Fault Report Source	0 to 5	---	1	F167	0 (SRC 1)
41B1	Fault Report Trigger	0 to 65535	---	1	F300	0
Fault Report Settings and Commands (Read/Write Command)						
41B2	Fault Reports Clear Data Command	0 to 1	---	1	F126	0 (No)
Oscillography (Read/Write Setting)						
41C0	Oscillography Number of Records	1 to 64	---	1	F001	15
41C1	Oscillography Trigger Mode	0 to 1	---	1	F118	0 (Auto Overwrite)
41C2	Oscillography Trigger Position	0 to 100	%	1	F001	50
41C3	Oscillography Trigger Source	0 to 65535	---	1	F300	0
41C4	Oscillography AC Input Waveforms	0 to 4	---	1	F183	2 (16 samps./cyc)
41D0	Oscillography Analog Channel X (16 items)	0 to 65535	---	1	F600	0
4200	Oscillography Digital Channel X (63 items)	0 to 65535	---	1	F300	0
Trip and Alarm LEDs (Read/Write Setting)						
4260	Trip LED Input FlexLogic Operand	0 to 65535	---	1	F300	0
4261	Alarm LED Input FlexLogic Operand	0 to 65535	---	1	F300	0
User Programmable LEDs (Read/Write Setting) (48 modules)						
4280	FlexLogic Operand to Activate LED	0 to 65535	---	1	F300	0
4281	User LED type (latched or self-resetting)	0 to 1	---	1	F127	1 (Self-Reset)
4282	...Repeated for module number 2					
4284	...Repeated for module number 3					
4286	...Repeated for module number 4					
4288	...Repeated for module number 5					
428A	...Repeated for module number 6					
428C	...Repeated for module number 7					
428E	...Repeated for module number 8					
4290	...Repeated for module number 9					
4292	...Repeated for module number 10					
4294	...Repeated for module number 11					
4296	...Repeated for module number 12					
4298	...Repeated for module number 13					
429A	...Repeated for module number 14					
429C	...Repeated for module number 15					
429E	...Repeated for module number 16					
42A0	...Repeated for module number 17					
42A2	...Repeated for module number 18					
42A4	...Repeated for module number 19					
42A6	...Repeated for module number 20					
42A8	...Repeated for module number 21					
42AA	...Repeated for module number 22					
42AC	...Repeated for module number 23					
42AE	...Repeated for module number 24					
42B0	...Repeated for module number 25					
42B2	...Repeated for module number 26					
42B4	...Repeated for module number 27					

Table B–11: MODBUS® MEMORY MAP (Sheet 11 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
42B6	...Repeated for module number 28					
42B8	...Repeated for module number 29					
42BA	...Repeated for module number 30					
42BC	...Repeated for module number 31					
42BE	...Repeated for module number 32					
42C0	...Repeated for module number 33					
42C2	...Repeated for module number 34					
42C4	...Repeated for module number 35					
42C6	...Repeated for module number 36					
42C8	...Repeated for module number 37					
42CA	...Repeated for module number 38					
42CC	...Repeated for module number 39					
42CE	...Repeated for module number 40					
42D0	...Repeated for module number 41					
42D2	...Repeated for module number 42					
42D4	...Repeated for module number 43					
42D6	...Repeated for module number 44					
42D8	...Repeated for module number 45					
42DA	...Repeated for module number 46					
42DC	...Repeated for module number 47					
42DE	...Repeated for module number 48					
Installation (Read/Write Setting)						
43E0	Relay Programmed State	0 to 1	---	1	F133	0 (Not Progm'd)
43E1	Relay Name	---	---	---	F202	"Relay-1"
CT Settings (Read/Write Setting) (6 modules)						
4480	Phase CT Primary	1 to 65000	A	1	F001	1
4481	Phase CT Secondary	0 to 1	---	1	F123	0 (1 A)
4482	Ground CT Primary	1 to 65000	A	1	F001	1
4483	Ground CT Secondary	0 to 1	---	1	F123	0 (1 A)
4484	...Repeated for module number 2					
4488	...Repeated for module number 3					
448C	...Repeated for module number 4					
4490	...Repeated for module number 5					
4494	...Repeated for module number 6					
VT Settings (Read/Write Setting) (3 modules)						
4500	Phase VT Connection	0 to 1	---	1	F100	0 (Wye)
4501	Phase VT Secondary	50 to 240	V	0.1	F001	664
4502	Phase VT Ratio	1 to 24000	:1	1	F060	1
4504	Auxiliary VT Connection	0 to 6	---	1	F166	1 (Vag)
4505	Auxiliary VT Secondary	50 to 240	V	0.1	F001	664
4506	Auxiliary VT Ratio	1 to 24000	:1	1	F060	1
4508	...Repeated for module number 2					
4510	...Repeated for module number 3					
Source Settings (Read/Write Setting) (6 modules)						
4580	Source Name	---	---	---	F206	"SRC 1 "
4583	Source Phase CT	0 to 63	---	1	F400	0
4584	Source Ground CT	0 to 63	---	1	F400	0

Table B–11: MODBUS® MEMORY MAP (Sheet 12 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
4585	Source Phase VT	0 to 63	---	1	F400	0
4586	Source Auxiliary VT	0 to 63	---	1	F400	0
4587	...Repeated for module number 2					
458E	...Repeated for module number 3					
4595	...Repeated for module number 4					
459C	...Repeated for module number 5					
45A3	...Repeated for module number 6					
Power System (Read/Write Setting)						
4600	Nominal Frequency	25 to 60	Hz	1	F001	60
4601	Phase Rotation	0 to 1	---	1	F106	0 (ABC)
4602	Frequency And Phase Reference	0 to 5	---	1	F167	0 (SRC 1)
4603	Frequency Tracking	0 to 1	---	1	F102	1 (Enabled)
Line (Read/Write Setting)						
46D0	Line Pos Seq Impedance	0.01 to 250	Ω	0.01	F001	300
46D1	Line Pos Seq Impedance Angle	25 to 90	°	1	F001	75
46D2	Line Zero Seq Impedance	0.01 to 650	Ω	0.01	F001	900
46D3	Line Zero Seq Impedance Angle	25 to 90	°	1	F001	75
46D4	Line Length Units	0 to 1	---	1	F147	0 (km)
46D5	Line Length	0 to 2000	---	0.1	F001	1000
Breaker Control Global Settings (Read/Write Setting)						
46F0	UCA XCBR x SelTimOut	1 to 60	s	1	F001	30
Breaker Control (Read/Write Setting) (2 modules)						
4700	Breaker x Function	0 to 1	---	1	F102	0 (Disabled)
4701	Breaker x Name	---	---	---	F206	"Bkr 1 "
4704	Breaker x Mode	0 to 1	---	1	F157	0 (3-Pole)
4705	Breaker x Open	0 to 65535	---	1	F300	0
4706	Breaker x Close	0 to 65535	---	1	F300	0
4707	Breaker x Phase A 3 Pole	0 to 65535	---	1	F300	0
4708	Breaker x Phase B	0 to 65535	---	1	F300	0
4709	Breaker x Phase C	0 to 65535	---	1	F300	0
470A	Breaker x External Alarm	0 to 65535	---	1	F300	0
470B	Breaker x Alarm Delay	0 to 1000000	s	0.001	F003	0
470D	Breaker x Push Button Control	0 to 1	---	1	F102	0 (Disabled)
470E	Breaker x Manual Close Recal Time	0 to 1000000	s	0.001	F003	0
4710	Breaker x UCA XCBR x SBOClass	1 to 2	---	1	F001	1
4711	Breaker x UCA XCBR x SBOEna	0 to 1	---	1	F102	0 (Disabled)
4712	Breaker x Reserved (6 items)	0 to 65535		1	F001	0
4718	...Repeated for module number 2					
Synchrocheck (Read/Write Setting) (2 modules)						
4780	Synchrocheck Function	0 to 1	---	1	F102	0 (Disabled)
4781	Synchrocheck V1 Source	0 to 5	---	1	F167	0 (SRC 1)
4782	Synchrocheck V2 Source	0 to 5	---	1	F167	1 (SRC 2)
4783	Synchrocheck Max Volt Diff	0 to 100000	V	1	F060	10000
4785	Synchrocheck Max Angle Diff	0 to 100	°	1	F001	30
4786	Synchrocheck Max Freq Diff	0 to 2	Hz	0.01	F001	100
4787	Synchrocheck Dead Source Select	0 to 5	---	1	F176	1 (LV1 and DV2)
4788	Synchrocheck Dead V1 Max Volt	0 to 1.25	pu	0.01	F001	30

Table B–11: MODBUS® MEMORY MAP (Sheet 13 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
4789	Synchrocheck Dead V2 Max Volt	0 to 1.25	pu	0.01	F001	30
478A	Synchrocheck Live V1 Min Volt	0 to 1.25	pu	0.01	F001	70
478B	Synchrocheck Live V2 Min Volt	0 to 1.25	pu	0.01	F001	70
478C	Synchrocheck Target	0 to 2	---	1	F109	0 (Self-reset)
478D	Synchrocheck Events	0 to 1	---	1	F102	0 (Disabled)
478E	Synchrocheck Block	0 to 65535	---	1	F300	0
478F	Synchrocheck X Reserved	0 to 65535	---	1	F001	0
4790	...Repeated for module number 2					
Flexcurve A (Read/Write Setting)						
4800	FlexCurve A (120 items)	0 to 65535	ms	1	F011	0
Flexcurve B (Read/Write Setting)						
48F0	FlexCurve B (120 items)	0 to 65535	ms	1	F011	0
Modbus User Map (Read/Write Setting)						
4A00	Modbus Addr Settings for User Map (256 items)	0 to 65535	---	1	F001	0
User Displays Settings (Read/Write Setting) (8 modules)						
4C00	User display top line text	---	---	---	F202	" "
4C0A	User display bottom line text	---	---	---	F202	" "
4C14	Modbus addresses of displayed items (5 items)	0 to 65535	---	1	F001	0
4C19	Reserved (7 items)	---	---	---	F001	0
4C20	...Repeated for module number 2					
4C40	...Repeated for module number 3					
4C60	...Repeated for module number 4					
4C80	...Repeated for module number 5					
4CA0	...Repeated for module number 6					
4CC0	...Repeated for module number 7					
4CE0	...Repeated for module number 8					
Flexlogic (Read/Write Setting)						
5000	FlexLogic Entry (512 items)	0 to 65535	---	1	F300	16384
Flexlogic Timers (Read/Write Setting) (32 modules)						
5800	Timer x Type	0 to 2	---	1	F129	0 (millisecond)
5801	Timer x Pickup Delay	0 to 60000	---	1	F001	0
5802	Timer x Dropout Delay	0 to 60000	---	1	F001	0
5803	Timer x Reserved (5 items)	0 to 65535	---	1	F001	0
5808	...Repeated for module number 2					
5810	...Repeated for module number 3					
5818	...Repeated for module number 4					
5820	...Repeated for module number 5					
5828	...Repeated for module number 6					
5830	...Repeated for module number 7					
5838	...Repeated for module number 8					
5840	...Repeated for module number 9					
5848	...Repeated for module number 10					
5850	...Repeated for module number 11					
5858	...Repeated for module number 12					
5860	...Repeated for module number 13					
5868	...Repeated for module number 14					
5870	...Repeated for module number 15					

Table B–11: MODBUS® MEMORY MAP (Sheet 14 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
5878	...Repeated for module number 16					
5880	...Repeated for module number 17					
5888	...Repeated for module number 18					
5890	...Repeated for module number 19					
5898	...Repeated for module number 20					
58A0	...Repeated for module number 21					
58A8	...Repeated for module number 22					
58B0	...Repeated for module number 23					
58B8	...Repeated for module number 24					
58C0	...Repeated for module number 25					
58C8	...Repeated for module number 26					
58D0	...Repeated for module number 27					
58D8	...Repeated for module number 28					
58E0	...Repeated for module number 29					
58E8	...Repeated for module number 30					
58F0	...Repeated for module number 31					
58F8	...Repeated for module number 32					
Phase TOC (Read/Write Grouped Setting) (6 modules)						
5900	Phase TOC Function	0 to 1	---	1	F102	0 (Disabled)
5901	Phase TOC Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5902	Phase TOC Input	0 to 1	---	1	F122	0 (Phasor)
5903	Phase TOC Pickup	0 to 30	pu	0.001	F001	1000
5904	Phase TOC Curve	0 to 14	---	1	F103	0 (IEEE Mod Inv)
5905	Phase TOC Multiplier	0 to 600	---	0.01	F001	100
5906	Phase TOC Reset	0 to 1	---	1	F104	0 (Instantaneous)
5907	Phase TOC Voltage Restraint	0 to 1	---	1	F102	0 (Disabled)
5908	Phase TOC Block For Each Phase (3 items)	0 to 65535	---	1	F300	0
590B	Phase TOC Target	0 to 2	---	1	F109	0 (Self-reset)
590C	Phase TOC Events	0 to 1	---	1	F102	0 (Disabled)
590D	Reserved (3 items)	0 to 1	---	1	F001	0
5910	...Repeated for module number 2					
5920	...Repeated for module number 3					
5930	...Repeated for module number 4					
5940	...Repeated for module number 5					
5950	...Repeated for module number 6					
Phase IOC (Read/Write Grouped Setting) (12 modules)						
5A00	Phase IOC1 Function	0 to 1	---	1	F102	0 (Disabled)
5A01	Phase IOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5A02	Phase IOC1 Pickup	0 to 30	pu	0.001	F001	1000
5A03	Phase IOC1 Delay	0 to 600	s	0.01	F001	0
5A04	Phase IOC1 Reset Delay	0 to 600	s	0.01	F001	0
5A05	Phase IOC1 Block For Each Phase (3 items)	0 to 65535	---	1	F300	0
5A08	Phase IOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
5A09	Phase IOC1 Events	0 to 1	---	1	F102	0 (Disabled)
5A0A	Reserved (6 items)	0 to 1	---	1	F001	0
5A10	...Repeated for module number 2					
5A20	...Repeated for module number 3					

Table B–11: MODBUS® MEMORY MAP (Sheet 15 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
5A30	...Repeated for module number 4					
5A40	...Repeated for module number 5					
5A50	...Repeated for module number 6					
5A60	...Repeated for module number 7					
5A70	...Repeated for module number 8					
5A80	...Repeated for module number 9					
5A90	...Repeated for module number 10					
5AA0	...Repeated for module number 11					
5AB0	...Repeated for module number 12					
Neutral TOC (Read/Write Grouped Setting) (6 modules)						
5B00	Neutral TOC1 Function	0 to 1	---	1	F102	0 (Disabled)
5B01	Neutral TOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5B02	Neutral TOC1 Input	0 to 1	---	1	F122	0 (Phasor)
5B03	Neutral TOC1 Pickup	0 to 30	pu	0.001	F001	1000
5B04	Neutral TOC1 Curve	0 to 14	---	1	F103	0 (IEEE Mod Inv)
5B05	Neutral TOC1 Multiplier	0 to 600	---	0.01	F001	100
5B06	Neutral TOC1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
5B07	Neutral TOC1 Block	0 to 65535	---	1	F300	0
5B08	Neutral TOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
5B09	Neutral TOC1 Events	0 to 1	---	1	F102	0 (Disabled)
5B0A	Reserved (6 items)	0 to 1	---	1	F001	0
5B10	...Repeated for module number 2					
5B20	...Repeated for module number 3					
5B30	...Repeated for module number 4					
5B40	...Repeated for module number 5					
5B50	...Repeated for module number 6					
Neutral IOC (Read/Write Grouped Setting) (12 modules)						
5C00	Neutral IOC1 Function	0 to 1	---	1	F102	0 (Disabled)
5C01	Neutral IOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5C02	Neutral IOC1 Pickup	0 to 30	pu	0.001	F001	1000
5C03	Neutral IOC1 Delay	0 to 600	s	0.01	F001	0
5C04	Neutral IOC1 Reset Delay	0 to 600	s	0.01	F001	0
5C05	Neutral IOC1 Block	0 to 65535	---	1	F300	0
5C06	Neutral IOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
5C07	Neutral IOC1 Events	0 to 1	---	1	F102	0 (Disabled)
5C08	Reserved (8 items)	0 to 1	---	1	F001	0
5C10	...Repeated for module number 2					
5C20	...Repeated for module number 3					
5C30	...Repeated for module number 4					
5C40	...Repeated for module number 5					
5C50	...Repeated for module number 6					
5C60	...Repeated for module number 7					
5C70	...Repeated for module number 8					
5C80	...Repeated for module number 9					
5C90	...Repeated for module number 10					
5CA0	...Repeated for module number 11					
5CB0	...Repeated for module number 12					

Table B–11: MODBUS® MEMORY MAP (Sheet 16 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Ground TOC (Read/Write Grouped Setting) (6 modules)						
5D00	Ground TOC1 Function	0 to 1	---	1	F102	0 (Disabled)
5D01	Ground TOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5D02	Ground TOC1 Input	0 to 1	---	1	F122	0 (Phasor)
5D03	Ground TOC1 Pickup	0 to 30	pu	0.001	F001	1000
5D04	Ground TOC1 Curve	0 to 14	---	1	F103	0 (IEEE Mod Inv)
5D05	Ground TOC1 Multiplier	0 to 600	---	0.01	F001	100
5D06	Ground TOC1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
5D07	Ground TOC1 Block	0 to 65535	---	1	F300	0
5D08	Ground TOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
5D09	Ground TOC1 Events	0 to 1	---	1	F102	0 (Disabled)
5D0A	Reserved (6 items)	0 to 1	---	1	F001	0
5D10	...Repeated for module number 2					
5D20	...Repeated for module number 3					
5D30	...Repeated for module number 4					
5D40	...Repeated for module number 5					
5D50	...Repeated for module number 6					
Ground IOC (Read/Write Grouped Setting) (12 modules)						
5E00	Ground IOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
5E01	Ground IOC1 Function	0 to 1	---	1	F102	0 (Disabled)
5E02	Ground IOC1 Pickup	0 to 30	pu	0.001	F001	1000
5E03	Ground IOC1 Delay	0 to 600	s	0.01	F001	0
5E04	Ground IOC1 Reset Delay	0 to 600	s	0.01	F001	0
5E05	Ground IOC1 Block	0 to 65535	---	1	F300	0
5E06	Ground IOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
5E07	Ground IOC1 Events	0 to 1	---	1	F102	0 (Disabled)
5E08	Reserved (8 items)	0 to 1	---	1	F001	0
5E10	...Repeated for module number 2					
5E20	...Repeated for module number 3					
5E30	...Repeated for module number 4					
5E40	...Repeated for module number 5					
5E50	...Repeated for module number 6					
5E60	...Repeated for module number 7					
5E70	...Repeated for module number 8					
5E80	...Repeated for module number 9					
5E90	...Repeated for module number 10					
5EA0	...Repeated for module number 11					
5EB0	...Repeated for module number 12					
Disturbance Detector (Read/Write Grouped Setting)						
5F20	DD Function	0 to 1	---	1	F102	0 (Disabled)
5F21	DD Non Cur Supervision	0 to 65535	---	1	F300	0
5F22	DD Control Logic	0 to 65535	---	1	F300	0
5F23	DD Logic Seal In	0 to 65535	---	1	F300	0
5F24	DD Events	0 to 1	---	1	F102	0 (Disabled)
Phase Comparison Open Breaker Keying (Read/Write Setting)						
60E0	Open Brk Keying	0 to 1	---	1	F102	0 (Disabled)
60E1	Brk1 Aux Contact	0 to 65535	---	1	F300	0

Table B–11: MODBUS® MEMORY MAP (Sheet 17 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
60E2	Brk1 Supv	0 to 65535	---	1	F300	0
60E3	Brk2 Aux Contact	0 to 65535	---	1	F300	0
60E4	Brk2 Supv Element	0 to 65535	---	1	F300	0
60E5	Weak-Infeed Keying	0 to 65535	---	1	F300	0
60E6	Supv Element	0 to 65535	---	1	F300	0
60E7	Infeed Pickup Delay	0 to 50	s	0.001	F001	0
60E8	Infeed Reset Delay	0 to 50	s	0.001	F001	35
60E9	Open Brk Keying Pickup Delay	0 to 50	s	0.001	F001	0
60EA	Open Brk Keying Reset Delay	0 to 50	s	0.001	F001	0
Phase Comparison Trip Scheme (Read/Write Setting)						
60F0	87PC Function	0 to 1	---	1	F102	0 (Disabled)
60F1	87PC ChannelLoss	0 to 65.535	s	0.001	F001	0
60F2	87PC Block	0 to 65535	---	1	F300	0
60F3	87PC Target	0 to 2	---	1	F109	0 (Self-reset)
60F4	87PC Events	0 to 1	---	1	F102	0 (Disabled)
60F5	87PC Scheme Select	0 to 6	---	1	F149	1 (2TL-BL-DPC-3FC)
60F6	87PC Scheme Signal	0 to 1	---	1	F150	0 (MIXED I_2-K*I_1)
60F7	87PC Signal Source	0 to 5	---	1	F167	0 (SRC 1)
60F8	87PC FDL Pickup	0.01 to 15	pu	0.01	F001	50
60F9	87PC FDM Pickup	0.01 to 5	pu	0.01	F001	50
60FA	87PC FDH Pickup	0.01 to 15	pu	0.01	F001	75
60FB	87PC Mixed Signal K	0 to 0.25	---	0.01	F001	20
60FE	87PC Phase Delay Ch1	0 to 65.535	ms	0.001	F003	0
6100	87PC Phase Delay Ch2	0 to 65.535	ms	0.001	F003	0
6106	87PC Transient Pickup	0 to 65.535	s	0.001	F003	30
610A	87PC Symmetry Ch1	-20 to 20	ms	0.1	F004	0
610E	87PC Symmetry Ch2	-20 to 20	ms	0.1	F004	0
6110	87PC Stability Angle	40 to 140	deg	10	F003	75
6112	87PC Transient Reset	0 to 65.535	s	0.001	F003	30
6114	87PC FD Input	0 to 65535	---	1	F300	0
CT Fail (Read/Write Setting)						
6120	CT Fail Function	0 to 1	---	1	F102	0 (Disabled)
6121	CT Fail Block	0 to 65535	---	1	F300	0
6122	CT Fail Current Source 1	0 to 5	---	1	F167	0 (SRC 1)
6123	CT Fail Current Pickup 1	0 to 2	pu	0.1	F001	2
6124	CT Fail Current Source 2	0 to 5	---	1	F167	1 (SRC 2)
6125	CT Fail Current Pickup 2	0 to 2	pu	0.1	F001	2
6126	CT Fail Voltage Source	0 to 5	---	1	F167	0 (SRC 1)
6127	CT Fail Voltage Pickup	0 to 2	pu	0.1	F001	2
6128	CT Fail Pickup Delay	0 to 65.535	s	0.001	F001	1000
6129	CT Fail Target	0 to 2	---	1	F109	0 (Self-reset)
612A	CT Fail Events	0 to 1	---	1	F102	0 (Disabled)
Cont Monitor (Read/Write Setting)						
6130	Cont Monitor Function	0 to 1	---	1	F102	0 (Disabled)
6131	Cont Monitor I OP	0 to 65535	---	1	F300	0
6132	Cont Monitor I Supervision	0 to 65535	---	1	F300	0
6133	Cont Monitor V OP	0 to 65535	---	1	F300	0

Table B–11: MODBUS® MEMORY MAP (Sheet 18 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
6134	Cont Monitor V Supervision	0 to 65535	---	1	F300	0
6135	Cont Monitor Target	0 to 2	---	1	F109	0 (Self-reset)
6136	Cont Monitor Events	0 to 1	---	1	F102	0 (Disabled)
Autoreclose (Read/Write Setting) (6 modules)						
6240	Autoreclose Function	0 to 1	---	1	F102	0 (Disabled)
6241	Autoreclose Initiate	0 to 65535	---	1	F300	0
6242	Autoreclose Block	0 to 65535	---	1	F300	0
6243	Autoreclose Max Number of Shots	1 to 4	---	1	F001	1
6244	Autoreclose Manual Close	0 to 65535	---	1	F300	0
6245	Autoreclose Manual Reset from LO	0 to 65535	---	1	F300	0
6246	Autoreclose Reset Lockout if Breaker Closed	0 to 1	---	1	F108	0 (Off)
6247	Autoreclose Reset Lockout On Manual Close	0 to 1	---	1	F108	0 (Off)
6248	Autoreclose Breaker Closed	0 to 65535	---	1	F300	0
6249	Autoreclose Breaker Open	0 to 65535	---	1	F300	0
624A	Autoreclose Block Time Upon Manual Close	0 to 65.535	s	0.001	F001	10000
624B	Autoreclose Dead Time Shot 1	0 to 65.535	s	0.001	F001	1000
624C	Autoreclose Dead Time Shot 2	0 to 65.535	s	0.001	F001	2000
624D	Autoreclose Dead Time Shot 3	0 to 65.535	s	0.001	F001	3000
624E	Autoreclose Dead Time Shot 4	0 to 65.535	s	0.001	F001	4000
624F	Autoreclose Reset Lockout Delay	0 to 65.535	---	0.001	F001	60000
6250	Autoreclose Reset Time	0 to 65.535	s	0.001	F001	60000
6251	Autoreclose Incomplete Sequence Time	0 to 65.535	s	0.001	F001	5000
6252	Autoreclose Events	0 to 1	---	1	F102	0 (Disabled)
6253	Autoreclose Reduce Max 1	0 to 65535	---	1	F300	0
6254	Autoreclose Reduce Max 2	0 to 65535	---	1	F300	0
6255	Autoreclose Reduce Max 3	0 to 65535	---	1	F300	0
6256	Autoreclose Add Delay 1	0 to 65535	---	1	F300	0
6257	Autoreclose Delay 1	0 to 65.535	s	0.001	F001	0
6258	Autoreclose Add Delay 2	0 to 65535	---	1	F300	0
6259	Autoreclose Delay 2	0 to 65.535	s	0.001	F001	0
625A	Autoreclose Reserved (4 items)	0 to 0.001	---	0.001	F001	0
625E	...Repeated for module number 2					
627C	...Repeated for module number 3					
629A	...Repeated for module number 4					
62B8	...Repeated for module number 5					
62D6	...Repeated for module number 6					
Negative Sequence TOC (Read/Write Grouped Setting) (2 modules)						
6300	Negative Sequence TOC1 Function	0 to 1	---	1	F102	0 (Disabled)
6301	Negative Sequence TOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
6302	Negative Sequence TOC1 Pickup	0 to 30	pu	0.001	F001	1000
6303	Negative Sequence TOC1 Curve	0 to 14	---	1	F103	0 (IEEE Mod Inv)
6304	Negative Sequence TOC1 Multiplier	0 to 600	---	0.01	F001	100
6305	Negative Sequence TOC1 Reset	0 to 1	---	1	F104	0 (Instantaneous)
6306	Negative Sequence TOC1 Block	0 to 65535	---	1	F300	0
6307	Negative Sequence TOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
6308	Negative Sequence TOC1 Events	0 to 1	---	1	F102	0 (Disabled)
6309	Reserved (7 items)	0 to 1	---	1	F001	0

Table B–11: MODBUS® MEMORY MAP (Sheet 19 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
6310	...Repeated for module number 2					
Negative Sequence IOC (Read/Write Grouped Setting) (2 modules)						
6400	Negative Sequence IOC1 Function	0 to 1	---	1	F102	0 (Disabled)
6401	Negative Sequence IOC1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
6402	Negative Sequence IOC1 Pickup	0 to 30	pu	0.001	F001	1000
6403	Negative Sequence IOC1 Delay	0 to 600	s	0.01	F001	0
6404	Negative Sequence IOC1 Reset Delay	0 to 600	s	0.01	F001	0
6405	Negative Sequence IOC1 Block	0 to 65535	---	1	F300	0
6406	Negative Sequence IOC1 Target	0 to 2	---	1	F109	0 (Self-reset)
6407	Negative Sequence IOC1 Events	0 to 1	---	1	F102	0 (Disabled)
6408	Reserved (8 items)	0 to 1	---	1	F001	0
6410	...Repeated for module number 2					
Power Swing Detect (Read/Write Grouped Setting)						
65C0	Power Swing Function	0 to 1	---	1	F102	0 (Disabled)
65C1	Power Swing Source	0 to 5	---	1	F167	0 (SRC 1)
65C2	Power Swing Mode	0 to 1	---	1	F513	0 (Two Step)
65C3	Power Swing Supv	0.05 to 30	pu	0.001	F001	600
65C4	Power Swing Fwd Reach	0.1 to 500	ohms	0.01	F001	5000
65C5	Power Swing Fwd Rca	40 to 90	°	1	F001	75
65C6	Power Swing Rev Reach	0.1 to 500	ohms	0.01	F001	5000
65C7	Power Swing Rev Rca	40 to 90	°	1	F001	75
65C8	Outer Limit Angle	40 to 140	°	1	F001	120
65C9	Middle Limit Angle	40 to 140	°	1	F001	90
65CA	Inner Limit Angle	40 to 140	°	1	F001	60
65CB	Delay 1 Pickup	0 to 65.535	s	0.001	F001	30
65CC	Delay 1 Reset	0 to 65.535	s	0.001	F001	50
65CD	Delay 2 Pickup	0 to 65.535	s	0.001	F001	17
65CE	Delay 3 Pickup	0 to 65.535	s	0.001	F001	9
65CF	Delay 4 Pickup	0 to 65.535	s	0.001	F001	17
65D0	Seal In Delay	0 to 65.535	s	0.001	F001	400
65D1	Trip Mode	0 to 1	---	1	F514	0 (Delayed)
65D2	Power Swing Block	0 to 65535	---	1	F300	0
65D3	Power Swing Target	0 to 2	---	1	F109	0 (Self-reset)
65D4	Power Swing Event	0 to 1	---	1	F102	0 (Disabled)
Phase Undervoltage (Read/Write Grouped Setting) (2 modules)						
7000	Phase UV1 Function	0 to 1	---	1	F102	0 (Disabled)
7001	Phase UV1 Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7002	Phase UV1 Pickup	0 to 3	pu	0.001	F001	1000
7003	Phase UV1 Curve	0 to 1	---	1	F111	0 (Definite Time)
7004	Phase UV1 Delay	0 to 600	s	0.01	F001	100
7005	Phase UV1 Minimum Voltage	0 to 3	pu	0.001	F001	100
7006	Phase UV1 Block	0 to 65535	---	1	F300	0
7007	Phase UV1 Target	0 to 2	---	1	F109	0 (Self-reset)
7008	Phase UV1 Events	0 to 1	---	1	F102	0 (Disabled)
7009	Phase UV Measurement Mode	0 to 1	---	1	F186	0 (Ph to Ground)
700A	Reserved (6 items)	0 to 1	---	1	F001	0
7010	...Repeated for module number 2					

Table B–11: MODBUS® MEMORY MAP (Sheet 20 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Phase Overvoltage (Read/Write Grouped Setting)						
7100	Phase OV1 Function	0 to 1	---	1	F102	0 (Disabled)
7101	Phase OV1 Source	0 to 5	---	1	F167	0 (SRC 1)
7102	Phase OV1 Pickup	0 to 3	pu	0.001	F001	1000
7103	Phase OV1 Delay	0 to 600	s	0.01	F001	100
7104	Phase OV1 Reset Delay	0 to 600	s	0.01	F001	100
7105	Phase OV1 Block	0 to 65535	---	1	F300	0
7106	Phase OV1 Target	0 to 2	---	1	F109	0 (Self-reset)
7107	Phase OV1 Events	0 to 1	---	1	F102	0 (Disabled)
7108	Reserved (8 items)	0 to 1	---	1	F001	0
Distance (Read/Write Grouped Setting)						
7130	Distance Signal Source	0 to 5	---	1	F167	0 (SRC 1)
7131	Memory Duration	5 to 25	cycles	1	F001	10
Line Pickup (Read/Write Grouped Setting)						
71C0	Line Pickup Function	0 to 1	---	1	F102	0 (Disabled)
71C1	Line Pickup Signal Source	0 to 5	---	1	F167	0 (SRC 1)
71C2	Line Pickup Phase IOC Pickup	0 to 30	pu	0.001	F001	1000
71C3	Line Pickup Pos Seq UV Pickup	0 to 3	pu	0.001	F001	700
71C4	Line End Open Pickup Delay	0 to 65.535	s	0.001	F001	150
71C5	Line End Open Reset Delay	0 to 65.535	s	0.001	F001	90
71C6	Line Pickup Pos Seq OV Pickup Delay	0 to 65.535	s	0.001	F001	40
71C7	Autoreclose Coordination Pickup Delay	0 to 65.535	s	0.001	F001	45
71C8	Autoreclose Coordination Reset Delay	0 to 65.535	s	0.001	F001	5
71C9	Autoreclose Coordination Bypass	0 to 1	---	1	F102	1 (Enabled)
71CA	Line Pickup Block	0 to 65535	---	1	F300	0
71CB	Line Pickup Target	0 to 2	---	1	F109	0 (Self-reset)
71CC	Line Pickup Events	0 to 1	---	1	F102	0 (Disabled)
Breaker Failure (Read/Write Grouped Setting) (2 modules)						
7200	Breaker Failure x Function	0 to 1	---	1	F102	0 (Disabled)
7201	Breaker Failure x Mode	0 to 1	---	1	F157	0 (3-Pole)
7208	Breaker Failure x Source	0 to 5	---	1	F167	0 (SRC 1)
7209	Breaker Failure x Amp Supervision	0 to 1	---	1	F126	1 (Yes)
720A	Breaker Failure x Use Seal-In	0 to 1	---	1	F126	1 (Yes)
720B	Breaker Failure x Three Pole Initiate	0 to 65535	---	1	F300	0
720C	Breaker Failure x Block	0 to 65535	---	1	F300	0
720D	Breaker Failure x Phase Amp Supv Pickup	0.001 to 30	pu	0.001	F001	1050
720E	Breaker Failure x Neutral Amp Supv Pickup	0.001 to 30	pu	0.001	F001	1050
720F	Breaker Failure x Use Timer 1	0 to 1	---	1	F126	1 (Yes)
7210	Breaker Failure x Timer 1 Pickup	0 to 65.535	s	0.001	F001	0
7211	Breaker Failure x Use Timer 2	0 to 1	---	1	F126	1 (Yes)
7212	Breaker Failure x Timer 2 Pickup	0 to 65.535	s	0.001	F001	0
7213	Breaker Failure x Use Timer 3	0 to 1	---	1	F126	1 (Yes)
7214	Breaker Failure x Timer 3 Pickup	0 to 65.535	s	0.001	F001	0
7215	Breaker Failure x Breaker Status 1 Phase A/3P	0 to 65535	---	1	F300	0
7216	Breaker Failure x Breaker Status 2 Phase A/3P	0 to 65535	---	1	F300	0
7217	Breaker Failure x Breaker Test On	0 to 65535	---	1	F300	0
7218	Breaker Failure x Phase Amp Hiset Pickup	0.001 to 30	pu	0.001	F001	1050

Table B–11: MODBUS® MEMORY MAP (Sheet 21 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
7219	Breaker Failure x Neutral Amp Hiset Pickup	0.001 to 30	pu	0.001	F001	1050
721A	Breaker Failure x Phase Amp Loset Pickup	0.001 to 30	pu	0.001	F001	1050
721B	Breaker Failure x Neutral Amp Loset Pickup	0.001 to 30	pu	0.001	F001	1050
721C	Breaker Failure x Loset Time	0 to 65.535	s	0.001	F001	0
721D	Breaker Failure x Trip Dropout Delay	0 to 65.535	s	0.001	F001	0
721E	Breaker Failure x Target	0 to 2	---	1	F109	0 (Self-reset)
721F	Breaker Failure x Events	0 to 1	---	1	F102	0 (Disabled)
7220	Breaker Failure x Phase A Initiate	0 to 65535	---	1	F300	0
7221	Breaker Failure x Phase B Initiate	0 to 65535	---	1	F300	0
7222	Breaker Failure x Phase C Initiate	0 to 65535	---	1	F300	0
7223	Breaker Failure x Breaker Status 1 Phase B	0 to 65535	---	1	F300	0
7224	Breaker Failure x Breaker Status 1 Phase C	0 to 65535	---	1	F300	0
7225	Breaker Failure x Breaker Status 2 Phase B	0 to 65535	---	1	F300	0
7226	Breaker Failure x Breaker Status 2 Phase C	0 to 65535	---	1	F300	0
7227	...Repeated for module number 2					
Breaker Arcing Current Settings (Read/Write Setting) (2 modules)						
72C0	Breaker x Arcing Amp Function	0 to 1	---	1	F102	0 (Disabled)
72C1	Breaker x Arcing Amp Source	0 to 5	---	1	F167	0 (SRC 1)
72C2	Breaker x Arcing Amp Init	0 to 65535	---	1	F300	0
72C3	Breaker x Arcing Amp Delay	0 to 65.535	s	0.001	F001	0
72C4	Breaker x Arcing Amp Limit	0 to 50000	kA2-cyc	1	F001	1000
72C5	Breaker x Arcing Amp Block	0 to 65535	---	1	F300	0
72C6	Breaker x Arcing Amp Target	0 to 2	---	1	F109	0 (Self-reset)
72C7	Breaker x Arcing Amp Events	0 to 1	---	1	F102	0 (Disabled)
72C8	...Repeated for module number 2					
DCMA Inputs (Read/Write Setting) (24 modules)						
7300	DCMA Inputs x Function	0 to 1	---	1	F102	0 (Disabled)
7301	DCMA Inputs x ID	---	---	---	F205	"DCMA Ip 1 "
7307	DCMA Inputs x Reserved 1 (4 items)	0 to 65535	---	1	F001	0
730B	DCMA Inputs x Units	---	---	---	F206	"mA"
730E	DCMA Inputs x Range	0 to 6	---	1	F173	6 (4 to 20 mA)
730F	DCMA Inputs x Minimum Value	-9999.999 to 9999.999	---	0.001	F004	4000
7311	DCMA Inputs x Maximum Value	-9999.999 to 9999.999	---	0.001	F004	20000
7313	DCMA Inputs x Reserved (5 items)	0 to 65535	---	1	F001	0
7318	...Repeated for module number 2					
7330	...Repeated for module number 3					
7348	...Repeated for module number 4					
7360	...Repeated for module number 5					
7378	...Repeated for module number 6					
7390	...Repeated for module number 7					
73A8	...Repeated for module number 8					
73C0	...Repeated for module number 9					
73D8	...Repeated for module number 10					
73F0	...Repeated for module number 11					
7408	...Repeated for module number 12					
7420	...Repeated for module number 13					

Table B–11: MODBUS® MEMORY MAP (Sheet 22 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
7438	...Repeated for module number 14					
7450	...Repeated for module number 15					
7468	...Repeated for module number 16					
7480	...Repeated for module number 17					
7498	...Repeated for module number 18					
74B0	...Repeated for module number 19					
74C8	...Repeated for module number 20					
74E0	...Repeated for module number 21					
74F8	...Repeated for module number 22					
7510	...Repeated for module number 23					
7528	...Repeated for module number 24					
RTD Inputs (Read/Write Setting) (48 modules)						
7540	RTD Inputs x Function	0 to 1	---	1	F102	0 (Disabled)
7541	RTD Inputs x ID	---	---	---	F205	"RTD Ip 1 "
7547	RTD Inputs x Reserved 1 (4 items)	0 to 65535	---	1	F001	0
754B	RTD Inputs x Type	0 to 3	---	1	F174	0 (100Ω Platinum)
754C	RTD Inputs x Reserved 2 (4 items)	0 to 65535	---	1	F001	0
7550	...Repeated for module number 2					
7560	...Repeated for module number 3					
7570	...Repeated for module number 4					
7580	...Repeated for module number 5					
7590	...Repeated for module number 6					
75A0	...Repeated for module number 7					
75B0	...Repeated for module number 8					
75C0	...Repeated for module number 9					
75D0	...Repeated for module number 10					
75E0	...Repeated for module number 11					
75F0	...Repeated for module number 12					
7600	...Repeated for module number 13					
7610	...Repeated for module number 14					
7620	...Repeated for module number 15					
7630	...Repeated for module number 16					
7640	...Repeated for module number 17					
7650	...Repeated for module number 18					
7660	...Repeated for module number 19					
7670	...Repeated for module number 20					
7680	...Repeated for module number 21					
7690	...Repeated for module number 22					
76A0	...Repeated for module number 23					
76B0	...Repeated for module number 24					
76C0	...Repeated for module number 25					
76D0	...Repeated for module number 26					
76E0	...Repeated for module number 27					
76F0	...Repeated for module number 28					
7700	...Repeated for module number 29					
7710	...Repeated for module number 30					
7720	...Repeated for module number 31					

Table B–11: MODBUS® MEMORY MAP (Sheet 23 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
7730	...Repeated for module number 32					
7740	...Repeated for module number 33					
7750	...Repeated for module number 34					
7760	...Repeated for module number 35					
7770	...Repeated for module number 36					
7780	...Repeated for module number 37					
7790	...Repeated for module number 38					
77A0	...Repeated for module number 39					
77B0	...Repeated for module number 40					
77C0	...Repeated for module number 41					
77D0	...Repeated for module number 42					
77E0	...Repeated for module number 43					
77F0	...Repeated for module number 44					
7800	...Repeated for module number 45					
7810	...Repeated for module number 46					
7820	...Repeated for module number 47					
7830	...Repeated for module number 48					
Ohm Inputs (Read/Write Setting) (2 modules)						
7840	Ohm Inputs x Function	0 to 1	---	1	F102	0 (Disabled)
7841	Ohm Inputs x ID	---	---	---	F205	"Ohm Ip 1 "
7847	Ohm Inputs x Reserved (9 items)	0 to 65535	---	1	F001	0
7850	...Repeated for module number 2					
Backup Phase Distance (Read/Write Grouped Setting)						
7A20	Phase Distance Z2 Function	0 to 1	---	1	F102	0 (Disabled)
7A21	Phase Distance Z2 Current Supervision	0.05 to 30	pu	0.001	F001	200
7A22	Phase Distance Z2 Reach	0.02 to 250	p	0.01	F001	200
7A23	Phase Distance Z2 Direction	0 to 1	---	1	F154	0 (Forward)
7A24	Phase Distance Z2 Comparator Limit	60 to 90	°	1	F001	90
7A25	Phase Distance Z2 Delay	0 to 65.535	s	0.001	F001	0
7A26	Phase Distance Z2 Block	0 to 65535	---	1	F300	0
7A27	Phase Distance Z2 Target	0 to 2	---	1	F109	0 (Self-reset)
7A28	Phase Distance Z2 Events	0 to 1	---	1	F102	0 (Disabled)
Backup Ground Distance (Read/Write Grouped Setting)						
7A30	Ground Distance Z2 Function	0 to 1	---	1	F102	0 (Disabled)
7A31	Ground Distance Z2 Current Supervision	0.05 to 30	pu	0.001	F001	200
7A32	Ground Distance Z2 Reach	0.02 to 250	p	0.01	F001	200
7A33	Ground Distance Z2 Direction	0 to 1	---	1	F154	0 (Forward)
7A34	Ground Distance Z2 Comp Limit	60 to 90	°	1	F001	90
7A35	Ground Distance Z2 Delay	0 to 65.535	s	0.001	F001	0
7A36	Ground Distance Z2 Block	0 to 65535	---	1	F300	0
7A37	Ground Distance Z2 Target	0 to 2	---	1	F109	0 (Self-reset)
7A38	Ground Distance Z2 Events	0 to 1	---	1	F102	0 (Disabled)
Frequency (Read Only)						
8000	Tracking Frequency	2 to 90	Hz	0.01	F001	0
FlexState Settings (Read/Write Setting)						
8800	FlexState Parameters (256 items)	---	---	---	F300	0

Table B–11: MODBUS® MEMORY MAP (Sheet 24 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
Setting Groups (Read/Write Setting)						
A000	Setting Group for Comms (0 means group 1)	0 to 7	---	1	F001	0
A001	Setting Groups Block	0 to 65535	---	1	F300	0
A002	FlexLogic Ops to Activate Groups 2 to 8 (7 items)	0 to 65535	---	1	F300	0
A009	Setting Group Function	0 to 1	---	1	F102	0 (Disabled)
A00A	Setting Group Events	0 to 1	---	1	F102	0 (Disabled)
Setting Groups (Read Only)						
A00B	Current Setting Group	0 to 7	---	1	F001	0
VT Fuse Failure (Read/Write Setting) (6 modules)						
A040	VT Fuse Failure Function	0 to 1	---	1	F102	0 (Disabled)
A041	...Repeated for module number 2					
A042	...Repeated for module number 3					
A043	...Repeated for module number 4					
A044	...Repeated for module number 5					
A045	...Repeated for module number 6					
Pilot POTT (Read/Write Setting)						
A070	POTT Scheme Function	0 to 1	---	1	F102	0 (Disabled)
A071	POTT Permissive Echo	0 to 1	---	1	F102	0 (Disabled)
A072	POTT Rx Pickup Delay	0 to 65.535	s	0.001	F001	0
A073	POTT Transient Block Pickup Delay	0 to 65.535	s	0.001	F001	20
A074	POTT Transient Block Reset Delay	0 to 65.535	s	0.001	F001	90
A075	POTT Echo Duration	0 to 65.535	s	0.001	F001	100
A076	POTT Line End Open Pickup Delay	0 to 65.535	s	0.001	F001	50
A077	POTT Seal In Delay	0 to 65.535	s	0.001	F001	400
A078	POTT Ground Direction OC Forward	0 to 65535	---	1	F300	0
A079	POTT Rx	0 to 65535	---	1	F300	0
A07A	POTT Echo Lockout	0 to 65.535	s	0.001	F001	250
Digital Elements (Read/Write Setting) (16 modules)						
B000	Digital Element x Function	0 to 1	---	1	F102	0 (Disabled)
B001	Digital Element x Name	---	---	---	F203	"Dig Element 1 "
B015	Digital Element x Input	0 to 65535	---	1	F300	0
B016	Digital Element x Pickup Delay	0 to 999999.999	s	0.001	F003	0
B018	Digital Element x Reset Delay	0 to 999999.999	s	0.001	F003	0
B01A	Digital Element x Block	0 to 65535	---	1	F300	0
B01B	Digital Element x Target	0 to 2	---	1	F109	0 (Self-reset)
B01C	Digital Element x Events	0 to 1	---	1	F102	0 (Disabled)
B01D	Digital Element x Reserved (3 items)	---	---	---	F001	0
B020	...Repeated for module number 2					
B040	...Repeated for module number 3					
B060	...Repeated for module number 4					
B080	...Repeated for module number 5					
B0A0	...Repeated for module number 6					
B0C0	...Repeated for module number 7					
B0E0	...Repeated for module number 8					
B100	...Repeated for module number 9					
B120	...Repeated for module number 10					
B140	...Repeated for module number 11					

Table B–11: MODBUS® MEMORY MAP (Sheet 25 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
B160	...Repeated for module number 12					
B180	...Repeated for module number 13					
B1A0	...Repeated for module number 14					
B1C0	...Repeated for module number 15					
B1E0	...Repeated for module number 16					
Digital Counter (Read/Write Setting) (8 modules)						
B300	Digital Counter x Function	0 to 1	---	1	F102	0 (Disabled)
B301	Digital Counter x Name	---	---	---	F205	"Counter 1 "
B307	Digital Counter x Units	---	---	---	F206	(none)
B30A	Digital Counter x Block	0 to 65535	---	1	F300	0
B30B	Digital Counter x Up	0 to 65535	---	1	F300	0
B30C	Digital Counter x Down	0 to 65535	---	1	F300	0
B30D	Digital Counter x Preset	-2147483647 to 2147483647	---	1	F004	0
B30F	Digital Counter x Compare	-2147483647 to 2147483647	---	1	F004	0
B311	Digital Counter x Reset	0 to 65535	---	1	F300	0
B312	Digital Counter x Freeze/Reset	0 to 65535	---	1	F300	0
B313	Digital Counter x Freeze/Count	0 to 65535	---	1	F300	0
B314	Digital Counter Set To Preset	0 to 65535	---	1	F300	0
B315	Digital Counter x Reserved (11 items)	---	---	---	F001	0
B320	...Repeated for module number 2					
B340	...Repeated for module number 3					
B360	...Repeated for module number 4					
B380	...Repeated for module number 5					
B3A0	...Repeated for module number 6					
B3C0	...Repeated for module number 7					
B3E0	...Repeated for module number 8					
Contact Inputs (Read/Write Setting) (96 modules)						
C000	Contact Input x Name	---	---	---	F205	"Cont Ip 1 "
C006	Contact Input x Events	0 to 1	---	1	F102	0 (Disabled)
C007	Contact Input x Reserved (3 items)	---	---	---	F001	0
C00A	...Repeated for module number 2					
C014	...Repeated for module number 3					
C01E	...Repeated for module number 4					
C028	...Repeated for module number 5					
C032	...Repeated for module number 6					
C03C	...Repeated for module number 7					
C046	...Repeated for module number 8					
C050	...Repeated for module number 9					
C05A	...Repeated for module number 10					
C064	...Repeated for module number 11					
C06E	...Repeated for module number 12					
C078	...Repeated for module number 13					
C082	...Repeated for module number 14					
C08C	...Repeated for module number 15					
C096	...Repeated for module number 16					
C0A0	...Repeated for module number 17					

Table B–11: MODBUS® MEMORY MAP (Sheet 26 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C0AA	...Repeated for module number 18					
C0B4	...Repeated for module number 19					
C0BE	...Repeated for module number 20					
C0C8	...Repeated for module number 21					
C0D2	...Repeated for module number 22					
C0DC	...Repeated for module number 23					
C0E6	...Repeated for module number 24					
C0F0	...Repeated for module number 25					
C0FA	...Repeated for module number 26					
C104	...Repeated for module number 27					
C10E	...Repeated for module number 28					
C118	...Repeated for module number 29					
C122	...Repeated for module number 30					
C12C	...Repeated for module number 31					
C136	...Repeated for module number 32					
C140	...Repeated for module number 33					
C14A	...Repeated for module number 34					
C154	...Repeated for module number 35					
C15E	...Repeated for module number 36					
C168	...Repeated for module number 37					
C172	...Repeated for module number 38					
C17C	...Repeated for module number 39					
C186	...Repeated for module number 40					
C190	...Repeated for module number 41					
C19A	...Repeated for module number 42					
C1A4	...Repeated for module number 43					
C1AE	...Repeated for module number 44					
C1B8	...Repeated for module number 45					
C1C2	...Repeated for module number 46					
C1CC	...Repeated for module number 47					
C1D6	...Repeated for module number 48					
C1E0	...Repeated for module number 49					
C1EA	...Repeated for module number 50					
C1F4	...Repeated for module number 51					
C1FE	...Repeated for module number 52					
C208	...Repeated for module number 53					
C212	...Repeated for module number 54					
C21C	...Repeated for module number 55					
C226	...Repeated for module number 56					
C230	...Repeated for module number 57					
C23A	...Repeated for module number 58					
C244	...Repeated for module number 59					
C24E	...Repeated for module number 60					
C258	...Repeated for module number 61					
C262	...Repeated for module number 62					
C26C	...Repeated for module number 63					
C276	...Repeated for module number 64					

Table B–11: MODBUS® MEMORY MAP (Sheet 27 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C280	...Repeated for module number 65					
C28A	...Repeated for module number 66					
C294	...Repeated for module number 67					
C29E	...Repeated for module number 68					
C2A8	...Repeated for module number 69					
C2B2	...Repeated for module number 70					
C2BC	...Repeated for module number 71					
C2C6	...Repeated for module number 72					
C2D0	...Repeated for module number 73					
C2DA	...Repeated for module number 74					
C2E4	...Repeated for module number 75					
C2EE	...Repeated for module number 76					
C2F8	...Repeated for module number 77					
C302	...Repeated for module number 78					
C30C	...Repeated for module number 79					
C316	...Repeated for module number 80					
C320	...Repeated for module number 81					
C32A	...Repeated for module number 82					
C334	...Repeated for module number 83					
C33E	...Repeated for module number 84					
C348	...Repeated for module number 85					
C352	...Repeated for module number 86					
C35C	...Repeated for module number 87					
C366	...Repeated for module number 88					
C370	...Repeated for module number 89					
C37A	...Repeated for module number 90					
C384	...Repeated for module number 91					
C38E	...Repeated for module number 92					
C398	...Repeated for module number 93					
C3A2	...Repeated for module number 94					
C3AC	...Repeated for module number 95					
C3B6	...Repeated for module number 96					
Contact Input Thresholds (Read/Write Setting)						
C600	Contact Input x Threshold (24 items)	0 to 3	---	1	F128	1 (30 Vdc)
Virtual Inputs Global Settings (Read/Write Setting)						
C680	Virtual Inputs SBO Timeout	1 to 60	s	1	F001	30
Virtual Inputs (Read/Write Setting) (32 modules)						
C690	Virtual Input x Function	0 to 1	---	1	F102	0 (Disabled)
C691	Virtual Input x Name	---	---	---	F205	"Virt Ip 1 "
C69B	Virtual Input x Programmed Type	0 to 1	---	1	F127	0 (Latched)
C69C	Virtual Input x Events	0 to 1	---	1	F102	0 (Disabled)
C69D	Virtual Input x UCA SBOClass	1 to 2	---	1	F001	1
C69E	Virtual Input x UCA SBOEna	0 to 1	---	1	F102	0 (Disabled)
C69F	Virtual Input x Reserved	---	---	---	F001	0
C6A0	...Repeated for module number 2					
C6B0	...Repeated for module number 3					
C6C0	...Repeated for module number 4					

Table B–11: MODBUS® MEMORY MAP (Sheet 28 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
C6D0	...Repeated for module number 5					
C6E0	...Repeated for module number 6					
C6F0	...Repeated for module number 7					
C700	...Repeated for module number 8					
C710	...Repeated for module number 9					
C720	...Repeated for module number 10					
C730	...Repeated for module number 11					
C740	...Repeated for module number 12					
C750	...Repeated for module number 13					
C760	...Repeated for module number 14					
C770	...Repeated for module number 15					
C780	...Repeated for module number 16					
C790	...Repeated for module number 17					
C7A0	...Repeated for module number 18					
C7B0	...Repeated for module number 19					
C7C0	...Repeated for module number 20					
C7D0	...Repeated for module number 21					
C7E0	...Repeated for module number 22					
C7F0	...Repeated for module number 23					
C800	...Repeated for module number 24					
C810	...Repeated for module number 25					
C820	...Repeated for module number 26					
C830	...Repeated for module number 27					
C840	...Repeated for module number 28					
C850	...Repeated for module number 29					
C860	...Repeated for module number 30					
C870	...Repeated for module number 31					
C880	...Repeated for module number 32					
Virtual Outputs (Read/Write Setting) (64 modules)						
CC90	Virtual Output x Name	---	---	---	F205	"Virt Op 1 "
CC9A	Virtual Output x Events	0 to 1	---	1	F102	0 (Disabled)
CC9B	Virtual Output x Reserved (5 items)	---	---	---	F001	0
CCA0	...Repeated for module number 2					
CCB0	...Repeated for module number 3					
CCC0	...Repeated for module number 4					
CCD0	...Repeated for module number 5					
CCE0	...Repeated for module number 6					
CCF0	...Repeated for module number 7					
CD00	...Repeated for module number 8					
CD10	...Repeated for module number 9					
CD20	...Repeated for module number 10					
CD30	...Repeated for module number 11					
CD40	...Repeated for module number 12					
CD50	...Repeated for module number 13					
CD60	...Repeated for module number 14					
CD70	...Repeated for module number 15					
CD80	...Repeated for module number 16					

Table B–11: MODBUS® MEMORY MAP (Sheet 29 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
CD90	...Repeated for module number 17					
CDA0	...Repeated for module number 18					
CDB0	...Repeated for module number 19					
CDC0	...Repeated for module number 20					
CDD0	...Repeated for module number 21					
CDE0	...Repeated for module number 22					
CDF0	...Repeated for module number 23					
CE00	...Repeated for module number 24					
CE10	...Repeated for module number 25					
CE20	...Repeated for module number 26					
CE30	...Repeated for module number 27					
CE40	...Repeated for module number 28					
CE50	...Repeated for module number 29					
CE60	...Repeated for module number 30					
CE70	...Repeated for module number 31					
CE80	...Repeated for module number 32					
CE90	...Repeated for module number 33					
CEA0	...Repeated for module number 34					
CEB0	...Repeated for module number 35					
CEC0	...Repeated for module number 36					
CED0	...Repeated for module number 37					
CEE0	...Repeated for module number 38					
CEF0	...Repeated for module number 39					
CF00	...Repeated for module number 40					
CF10	...Repeated for module number 41					
CF20	...Repeated for module number 42					
CF30	...Repeated for module number 43					
CF40	...Repeated for module number 44					
CF50	...Repeated for module number 45					
CF60	...Repeated for module number 46					
CF70	...Repeated for module number 47					
CF80	...Repeated for module number 48					
CF90	...Repeated for module number 49					
CFA0	...Repeated for module number 50					
CFB0	...Repeated for module number 51					
CFC0	...Repeated for module number 52					
CFD0	...Repeated for module number 53					
CFE0	...Repeated for module number 54					
CFF0	...Repeated for module number 55					
D000	...Repeated for module number 56					
D010	...Repeated for module number 57					
D020	...Repeated for module number 58					
D030	...Repeated for module number 59					
D040	...Repeated for module number 60					
D050	...Repeated for module number 61					
D060	...Repeated for module number 62					
D070	...Repeated for module number 63					

Table B–11: MODBUS® MEMORY MAP (Sheet 30 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
D080	...Repeated for module number 64					
Mandatory (Read/Write Setting)						
D280	Test Mode Function	0 to 1	---	1	F102	0 (Disabled)
Contact Outputs (Read/Write Setting) (64 modules)						
D290	Contact Output x Name	---	---	---	F205	"Cont Op 1 "
D29A	Contact Output x Operation	0 to 65535	---	1	F300	0
D29B	Contact Output x Seal In	0 to 65535	---	1	F300	0
D29C	Reserved	---	---	1	F001	0
D29D	Contact Output x Events	0 to 1	---	1	F102	1 (Enabled)
D29E	Reserved (2 items)	---	---	---	F001	0
D2A0	...Repeated for module number 2					
D2B0	...Repeated for module number 3					
D2C0	...Repeated for module number 4					
D2D0	...Repeated for module number 5					
D2E0	...Repeated for module number 6					
D2F0	...Repeated for module number 7					
D300	...Repeated for module number 8					
D310	...Repeated for module number 9					
D320	...Repeated for module number 10					
D330	...Repeated for module number 11					
D340	...Repeated for module number 12					
D350	...Repeated for module number 13					
D360	...Repeated for module number 14					
D370	...Repeated for module number 15					
D380	...Repeated for module number 16					
D390	...Repeated for module number 17					
D3A0	...Repeated for module number 18					
D3B0	...Repeated for module number 19					
D3C0	...Repeated for module number 20					
D3D0	...Repeated for module number 21					
D3E0	...Repeated for module number 22					
D3F0	...Repeated for module number 23					
D400	...Repeated for module number 24					
D410	...Repeated for module number 25					
D420	...Repeated for module number 26					
D430	...Repeated for module number 27					
D440	...Repeated for module number 28					
D450	...Repeated for module number 29					
D460	...Repeated for module number 30					
D470	...Repeated for module number 31					
D480	...Repeated for module number 32					
D490	...Repeated for module number 33					
D4A0	...Repeated for module number 34					
D4B0	...Repeated for module number 35					
D4C0	...Repeated for module number 36					
D4D0	...Repeated for module number 37					
D4E0	...Repeated for module number 38					

Table B–11: MODBUS® MEMORY MAP (Sheet 31 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
D4F0	...Repeated for module number 39					
D500	...Repeated for module number 40					
D510	...Repeated for module number 41					
D520	...Repeated for module number 42					
D530	...Repeated for module number 43					
D540	...Repeated for module number 44					
D550	...Repeated for module number 45					
D560	...Repeated for module number 46					
D570	...Repeated for module number 47					
D580	...Repeated for module number 48					
D590	...Repeated for module number 49					
D5A0	...Repeated for module number 50					
D5B0	...Repeated for module number 51					
D5C0	...Repeated for module number 52					
D5D0	...Repeated for module number 53					
D5E0	...Repeated for module number 54					
D5F0	...Repeated for module number 55					
D600	...Repeated for module number 56					
D610	...Repeated for module number 57					
D620	...Repeated for module number 58					
D630	...Repeated for module number 59					
D640	...Repeated for module number 60					
D650	...Repeated for module number 61					
D660	...Repeated for module number 62					
D670	...Repeated for module number 63					
D680	...Repeated for module number 64					
Reset (Read/Write Setting)						
D800	FlexLogic operand which initiates a reset	0 to 65535	---	1	F300	0
Force Contact Inputs (Read/Write Setting)						
D8B0	Force Contact Input x State (96 items)	0 to 2	---	1	F144	0 (Disabled)
Force Contact Outputs (Read/Write Setting)						
D910	Force Contact Output x State (64 items)	0 to 3	---	1	F131	0 (Disabled)
Phase Comparison Channel Tests (Read/Write Command) (2 modules)						
DA21	Channel X Loopback Function	0 to 1	---	1	F126	0 (No)
DA23	Channel X Echoback Function	0 to 1	---	1	F126	0 (No)
DA24	...Repeated for module number 2					
Remote Devices (Read/Write Setting) (16 modules)						
E000	Remote Device x ID	---	---	---	F202	"Remote Device 1 "
E00A	...Repeated for module number 2					
E014	...Repeated for module number 3					
E01E	...Repeated for module number 4					
E028	...Repeated for module number 5					
E032	...Repeated for module number 6					
E03C	...Repeated for module number 7					
E046	...Repeated for module number 8					
E050	...Repeated for module number 9					
E05A	...Repeated for module number 10					

Table B–11: MODBUS® MEMORY MAP (Sheet 32 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
E064	...Repeated for module number 11					
E06E	...Repeated for module number 12					
E078	...Repeated for module number 13					
E082	...Repeated for module number 14					
E08C	...Repeated for module number 15					
E096	...Repeated for module number 16					
Remote Inputs (Read/Write Setting) (32 modules)						
E100	Remote Input x Device	1 to 16	---	1	F001	1
E101	Remote Input x Bit Pair	0 to 64	---	1	F156	0 (None)
E102	Remote Input x Default State	0 to 1	---	1	F108	0 (Off)
E103	Remote Input x Events	0 to 1	---	1	F102	0 (Disabled)
E104	...Repeated for module number 2					
E108	...Repeated for module number 3					
E10C	...Repeated for module number 4					
E110	...Repeated for module number 5					
E114	...Repeated for module number 6					
E118	...Repeated for module number 7					
E11C	...Repeated for module number 8					
E120	...Repeated for module number 9					
E124	...Repeated for module number 10					
E128	...Repeated for module number 11					
E12C	...Repeated for module number 12					
E130	...Repeated for module number 13					
E134	...Repeated for module number 14					
E138	...Repeated for module number 15					
E13C	...Repeated for module number 16					
E140	...Repeated for module number 17					
E144	...Repeated for module number 18					
E148	...Repeated for module number 19					
E14C	...Repeated for module number 20					
E150	...Repeated for module number 21					
E154	...Repeated for module number 22					
E158	...Repeated for module number 23					
E15C	...Repeated for module number 24					
E160	...Repeated for module number 25					
E164	...Repeated for module number 26					
E168	...Repeated for module number 27					
E16C	...Repeated for module number 28					
E170	...Repeated for module number 29					
E174	...Repeated for module number 30					
E178	...Repeated for module number 31					
E17C	...Repeated for module number 32					
Remote Output DNA Pairs (Read/Write Setting) (32 modules)						
E600	Remote Output DNA x Operand	0 to 65535	---	1	F300	0
E601	Remote Output DNA x Events	0 to 1	---	1	F102	0 (Disabled)
E602	Remote Output DNA x Reserved (2 items)	0 to 1	---	1	F001	0
E604	...Repeated for module number 2					

Table B–11: MODBUS® MEMORY MAP (Sheet 33 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
E608	...Repeated for module number 3					
E60C	...Repeated for module number 4					
E610	...Repeated for module number 5					
E614	...Repeated for module number 6					
E618	...Repeated for module number 7					
E61C	...Repeated for module number 8					
E620	...Repeated for module number 9					
E624	...Repeated for module number 10					
E628	...Repeated for module number 11					
E62C	...Repeated for module number 12					
E630	...Repeated for module number 13					
E634	...Repeated for module number 14					
E638	...Repeated for module number 15					
E63C	...Repeated for module number 16					
E640	...Repeated for module number 17					
E644	...Repeated for module number 18					
E648	...Repeated for module number 19					
E64C	...Repeated for module number 20					
E650	...Repeated for module number 21					
E654	...Repeated for module number 22					
E658	...Repeated for module number 23					
E65C	...Repeated for module number 24					
E660	...Repeated for module number 25					
E664	...Repeated for module number 26					
E668	...Repeated for module number 27					
E66C	...Repeated for module number 28					
E670	...Repeated for module number 29					
E674	...Repeated for module number 30					
E678	...Repeated for module number 31					
E67C	...Repeated for module number 32					
Remote Output UserSt Pairs (Read/Write Setting) (32 modules)						
E680	Remote Output UserSt x Operand	0 to 65535	---	1	F300	0
E681	Remote Output UserSt x Events	0 to 1	---	1	F102	0 (Disabled)
E682	Remote Output UserSt x Reserved (2 items)	0 to 1	---	1	F001	0
E684	...Repeated for module number 2					
E688	...Repeated for module number 3					
E68C	...Repeated for module number 4					
E690	...Repeated for module number 5					
E694	...Repeated for module number 6					
E698	...Repeated for module number 7					
E69C	...Repeated for module number 8					
E6A0	...Repeated for module number 9					
E6A4	...Repeated for module number 10					
E6A8	...Repeated for module number 11					
E6AC	...Repeated for module number 12					
E6B0	...Repeated for module number 13					
E6B4	...Repeated for module number 14					

Table B–11: MODBUS® MEMORY MAP (Sheet 34 of 34)

ADDR	REGISTER NAME	RANGE	UNITS	STEP	FORMAT	DEFAULT
E6B8	...Repeated for module number 15					
E6BC	...Repeated for module number 16					
E6C0	...Repeated for module number 17					
E6C4	...Repeated for module number 18					
E6C8	...Repeated for module number 19					
E6CC	...Repeated for module number 20					
E6D0	...Repeated for module number 21					
E6D4	...Repeated for module number 22					
E6D8	...Repeated for module number 23					
E6DC	...Repeated for module number 24					
E6E0	...Repeated for module number 25					
E6E4	...Repeated for module number 26					
E6E8	...Repeated for module number 27					
E6EC	...Repeated for module number 28					
E6F0	...Repeated for module number 29					
E6F4	...Repeated for module number 30					
E6F8	...Repeated for module number 31					
E6FC	...Repeated for module number 32					

B

C.1.1 UCA

The **Utility Communications Architecture** (UCA) version 2 represents an attempt by utilities and vendors of electronic equipment to produce standardized communications systems. There is a set of reference documents available from the Electric Power Research Institute (EPRI) and vendors of UCA/MMS software libraries that describe the complete capabilities of the UCA. Following, is a description of the subset of UCA/MMS features that are supported by the UR relay. The reference document set includes:

- Introduction to UCA version 2
- Generic Object Models for Substation & Feeder Equipment (GOMSFE)
- Common Application Service Models (CASM) and Mapping to MMS
- UCA Version 2 Profiles

These documents can be obtained from <ftp://www.sisconet.com/epri/subdemo/uca2.0>. It is strongly recommended that all those involved with any UCA implementation obtain this document set.

COMMUNICATION PROFILES:

The UCA specifies a number of possibilities for communicating with electronic devices based on the OSI Reference Model. The UR relay uses the seven layer OSI stack (TP4/CLNP and TCP/IP profiles). Refer to the "UCA Version 2 Profiles" reference document for details.

The TP4/CLNP profile requires the UR relay to have a network address or Network Service Access Point (NSAP) in order to establish a communication link. The TCP/IP profile requires the UR relay to have an IP address in order to establish a communication link. These addresses can be set in the COMMUNICATIONS \ NETWORK submenu of the SETTINGS \ PRODUCT SETUP menu. Note that the UR relay supports UCA operation over the TP4/CLNP or the TCP/IP stacks and also supports operation over both stacks simultaneously. It is possible to have up to two simultaneous connections. This is in addition to DNP and Modbus/TCP (non-UCA) connections.

C.1.2 MMS

The UCA specifies the use of the **Manufacturing Message Specification** (MMS) at the upper (Application) layer for transfer of real-time data. This protocol has been in existence for a number of years and provides a set of services suitable for the transfer of data within a substation LAN environment. Data can be grouped to form objects and be mapped to MMS services. Refer to the "GOMSFE" and "CASM" reference documents for details.

SUPPORTED OBJECTS:

The "GOMSFE" document describes a number of communication objects. Within these objects are items, some of which are mandatory and some of which are optional, depending on the implementation. The UR relay supports the following GOMSFE objects:

• DI (device identity)	• PHIZ (high impedance ground detector)
• GCTL (generic control)	• PIOC (instantaneous overcurrent relay)
• GIND (generic indicator)	• POVR (overvoltage relay)
• GLOBE (global data)	• PTOC (time overcurrent relay)
• MMXU (polyphase measurement unit)	• PUVR (under voltage relay)
• PBRL (phase balance current relay)	• PVPH (volts per hertz relay)
• PBRO (basic relay object)	• ctRATO (CT ratio information)
• PDIF (differential relay)	• vtRATO (VT ratio information)
• PDIS (distance)	• RREC (reclosing relay)
• PDOC (directional overcurrent)	• RSYN (synchronizing or synchronism-check relay)
• PFRQ (frequency relay)	• XCBR (circuit breaker)

UCA data can be accessed through the "UCADevice" MMS domain.

PEER-TO-PEER COMMUNICATION:

Peer-to-peer communication of digital state information, using the UCA GOOSE data object, is supported via the use of the UR Remote Inputs/Outputs feature. This feature allows digital points to be transferred between any UCA conforming devices.

FILE SERVICES:

MMS file services are supported to allow transfer of Oscillography, Event Record, or other files from a UR relay.

COMMUNICATION SOFTWARE UTILITIES:

The exact structure and values of the implemented objects implemented can be seen by connecting to a UR relay with an MMS browser, such as the "MMS Object Explorer and AXS4-MMS DDE/OPC" server from Sisco Inc.

NON-UCA DATA:

The UR relay makes available a number of non-UCA data items. These data items can be accessed through the "UR" MMS domain. UCA data can be accessed through the "UCADevice" MMS domain.

C.1.3 PROTOCOL IMPLEMENTATION & CONFORMANCE STATEMENT (PICS)



The UR relay functions as a server only; a UR relay cannot be configured as a client. Thus, the following list of supported services is for server operation only:

NOTE

The MMS supported services are as follows:

CONNECTION MANAGEMENT SERVICES:

- Initiate
- Conclude
- Cancel
- Abort
- Reject

VMD SUPPORT SERVICES:

- Status
- GetNameList
- Identify

VARIABLE ACCESS SERVICES:

- Read
- Write
- InformationReport
- GetVariableAccessAttributes
- GetNamedVariableListAttributes

OPERATOR COMMUNICATION SERVICES:

(none)

SEMAPHORE MANAGEMENT SERVICES:

(none)

DOMAIN MANAGEMENT SERVICES:

- GetDomainAttributes

PROGRAM INVOCATION MANAGEMENT SERVICES:

(none)

EVENT MANAGEMENT SERVICES

(none)

JOURNAL MANAGEMENT SERVICES

(none)

FILE MANAGEMENT SERVICES

- ObtainFile
- FileOpen
- FileRead
- FileClose
- FileDirectory

The following MMS parameters are supported:

- STR1 (Arrays)
- STR2 (Structures)
- NEST (Nesting Levels of STR1 and STR2) - 1
- VNAM (Named Variables)
- VADR (Unnamed Variables)
- VALT (Alternate Access Variables)
- VLIS (Named Variable Lists)
- REAL (ASN.1 REAL Type)

C

h) MODEL IMPLEMENTATION CONFORMANCE (MIC)

This section provides details of the UCA object models supported by the UR relay. Note that not all of the protective device functions are applicable to all UR relays.

Table C-1: DEVICE IDENTITY – DI

NAME	M/O	RWEC
Name	m	rw
Class	o	rw
d	o	rw
Own	o	rw
Loc	o	rw
VndID	m	r
CommID	o	rw

Table C-2: GENERIC CONTROL – GCTL

FC	NAME	CLASS	RWECS	DESCRIPTION
ST	BO<n>	SI	rw	Generic Single Point Indication
CO	BO<n>	SI	rw	Generic Binary Output
CF	BO<n>	SBOCF	rw	SBO Configuration
DC	LN	d	rw	Description for brick
	BO<n>	d	rw	Description for each point



Actual instantiation of GCTL objects is as follows:

GCTL1 = Virtual Inputs (32 total points – SI1 to SI32); includes SBO functionality.

NOTE

Table C-3: GENERIC INDICATOR – GIND

FC	NAME	CLASS	RWECS	DESCRIPTION
ST	SIG<n>	SIG	r	Generic Indication (block of 16)
DC	LN	d	rw	Description for brick
RP	BrCbST	BasRCB	rw	Controls reporting of STATUS

**NOTE**

Actual instantiation of GIND objects is as follows:

GIND1 = Contact Inputs (96 total points – SIG1 to SIG6)
 GIND2 = Contact Outputs (64 total points – SIG1 to SIG4)
 GIND3 = Virtual Inputs (32 total points – SIG1 to SIG2)
 GIND4 = Virtual Outputs (64 total points – SIG1 to SIG4)
 GIND5 = Remote Inputs (32 total points – SIG1 to SIG2)
 GIND6 = Flexstates (16 total points – SIG1 representing Flexstates 1 to 16)

Table C-4: GLOBAL DATA – GLOBE

FC	OBJECT NAME	CLASS	RWECS	DESCRIPTION
ST	ModeDS	SIT	r	Device is: in test, off-line, available, or unhealthy
	LocRemDS	SIT	r	The mode of control, local or remote (DevST)
	ActSG	INT8U	r	Active Settings Group
	EditSG	INT8u	r	Settings Group selected for read/write operation
CO	CopySG	INT8U	w	Selects Settings Group for read/writer operation
	IndRs	BOOL	w	Resets ALL targets
CF	ClockTOD	BTIME	rw	Date and time
RP	GOOSE	PACT	rw	Reports IED Inputs and Ouputs

Table C-5: MEASUREMENT UNIT (POLYPHASE) – MMXU

OBJECT NAME	CLASS	RWECS	DESCRIPTION
V	WYE	rw	Voltage on phase A, B, C to G
PPV	DELTA	rw	Voltage on AB, BC, CA
A	WYE	rw	Current in phase A, B, C, and N
W	WYE	rw	Watts in phase A, B, C
TotW	AI	rw	Total watts in all three phases
Var	WYE	rw	Vars in phase A, B, C
TotVar	AI	rw	Total vars in all three phases
VA	WYE	rw	VA in phase A, B, C
TotVA	AI	rw	Total VA in all 3 phases
PF	WYE	rw	Power Factor for phase A, B, C
AvgPF	AI	rw	Average Power Factor for all three phases
Hz	AI	rw	Power system frequency
All MMXU.MX	ACF	rw	Configuration of ALL included MMXU.MX
LN	d	rw	Description for brick
All MMXU.MX	d	rw	Description of ALL included MMXU.MX
BrcbMX	BasRCB	rw	Controls reporting of measurements



Actual instantiation of MMXU objects is as follows:

1 MMXU per Source (as determined from the 'product order code')

Table C-6: PROTECTIVE ELEMENTS

FC	OBJECT NAME	CLASS	RWECS	DESCRIPTION
ST	Out	BOOL	r	1 = Element operated, 2 = Element not operated
	Tar	PhsTar	r	Targets since last reset
	FctDS	SIT	r	Function is enabled/disabled
	PuGrp	INT8U	r	Settings group selected for use
CO	EnaDisFct	DCO	w	1 = Element function enabled, 0 = disabled
	RsTar	BO	w	Reset ALL Elements/Targets
	RsLat	BO	w	Reset ALL Elements/Targets
DC	LN	d	rw	Description for brick
	ElementSt	d	r	Element state string

The following GOMSFE objects are defined by the object model described via the above table:

- PBRO (basic relay object)
- PDIF (differential relay)
- PDIS (distance)
- PDOC (directional overcurrent)
- PFRQ (frequency relay)
- PHIZ (high impedance ground detector)
- PIOC (instantaneous overcurrent relay)
- POVR (over voltage relay)
- PTOC (time overcurrent relay)
- PUVR (under voltage relay)
- RSYN (synchronizing or synchronism-check relay)
- POVR (overvoltage)
- PVPH (volts per hertz relay)
- PBRL (phase balance current relay)



Actual instantiation of these objects is determined by the number of the corresponding elements present in the UR as per the 'product order code'.

NOTE**Table C-7: CT RATIO INFORMATION – ctRATO**

OBJECT NAME	CLASS	RWECS	DESCRIPTION
PhsARat	RATIO	rw	Primary/secondary winding ratio
NeutARat	RATIO	rw	Primary/secondary winding ratio
LN	d	rw	Description for brick



Actual instantiation of ctRATO objects is as follows:

1 ctRATO per Source (as determined from the 'product order code').

NOTE

Table C-8: VT RATIO INFORMATION – vtRATO

OBJECT NAME	CLASS	RWECS	DESCRIPTION
PhsVRat	RATIO	rw	Primary/secondary winding ratio
LN	d	rw	Description for brick



Actual instantiation of vtRATO objects is as follows:

1 vtRATO per Source (as determined from the 'product order code').

NOTE

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Table C-9: RECLOSING RELAY – RREC

FC	OBJECT NAME	CLASS	RWECS	DESCRIPTION
ST	Out	BOOL	r	1 = Element operated, 2 = Element not operated
	FctDS	SIT	r	Function is enabled/disabled
	PuGrp	INT8U	r	Settings group selected for use
SG	ReclSeq	SHOTS	rw	Reclosing Sequence
CO	EnaDisFct	DCO	w	1 = Element function enabled, 0 = disabled
	RsTar	BO	w	Reset ALL Elements/Targets
	RsLat	BO	w	Reset ALL Elements/Targets
CF	ReclSeq	ACF	rw	Configuration for RREC.SG
DC	LN	d	rw	Description for brick
	ElementSt	d	r	Element state string



Actual instantiation of RREC objects is determined by the number of autoreclose elements present in the UR as per the 'product order code'.

NOTE

Also note that the SHOTS class data (i.e. Tmr1, Tmr2, Tmr3, Tmr4, RsTmr) is specified to be of type INT16S (16 bit signed integer); this data type is not large enough to properly display the full range of these settings from the UR. Numbers larger than 32768 will be displayed incorrectly.

C.1.4 UCA REPORTING

A built-in TCP/IP connection timeout of two minutes is employed by the UR to detect "dead" connections. If there is no data traffic on a TCP connection for greater than two minutes, the connection will be aborted by the UR. This frees up the connection to be used by other clients. Therefore, when using UCA reporting, clients should configure BasRCB objects such that an integrity report will be issued at least every 2 minutes (120000 ms). This ensures that the UR will not abort the connection. If other MMS data is being polled on the same connection at least once every 2 minutes, this timeout will not apply.

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 1 of 7)

ABBREVIATION	MEANING
A	ampere
AC	alternating current
A/D	analog to digital
AE	accidental energization
AE	application entity
AMP	ampere
ANSI	american national standards institute
AR	automatic reclosure
AUTO	automatic
AUX	auxiliary
AVG	average
BER	bit error rate
BF	breaker fail
BFI	breaker failure initiate
BKR	breaker
BLK	block
BLKG	blocking
BPNT	breakpoint of a characteristic
CAP	capacitor
CC	coupling capacitor
CCVT	coupling capacitor voltage transformer
CFG	configure / configurable
.CFG	file name extension for oscillography files
CHK	check
CHNL	channel
CLS	close
CLSD	closed
CMND	command
CMPRSN	comparison
CO	contact output
COM	communication
COMM	communications
COMP	compensated
CONN	connection
CO-ORD	coordination
CPU	central processing unit
CRT, CRNT	current

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 2 of 7)

ABBREVIATION	MEANING
CT	current transformer
CVT	capacitive voltage transformer
D/A	digital to analog
DC (dc)	direct current
DD	disturbance detector
DFLT	default
DGNST	diagnostics
DI	digital input
DIFF	differential
DIR	directional
DISCREP	discrepancy
DIST	distance
DMD	demand
DPO	dropout
DSP	digital signal processor
DTT	direct transfer trip
DUTT	direct under-reaching transfer trip
EPRI	Electric Power Research Institute
.EVT	file name extension for event recorder files
EXT	extension
F	field
FAIL	failure
FD	fault detector
FDH	fault detector high-set
FDL	fault detector low-set
FLA	full load current
FO	fiber optic
FREQ	frequency
FSK	frequency-shift keying
FWD	forward
G	generator
GE	General Electric
GND	ground
GNTR	generator
GOOSE	general object oriented substation event
HARM	harmonic / harmonics
HGF	high-impedance ground fault (CT)

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 3 of 7)

ABBREVIATION	MEANING
HIZ	high-impedance & arcing ground
HMI	human-machine interface
HYB	hybrid
I	instantaneous
I ₀	zero sequence current
I ₁	positive sequence current
I ₂	negative sequence current
IA	phase A current
IAB	phase A minus B current
IB	phase B current
IBC	phase B minus C current
IC	phase C current
ICA	phase C minus A current
ID	identification
IEEE	Institute of Electrical & Electronic Engineers
IG	ground (not residual) current
Igd	differential ground current
IN	CT residual current (3I ₀) or input
INC SEQ	incomplete sequence
INIT	initiate
INST	instantaneous
INV	inverse
I/O	input/output
IOC	instantaneous overcurrent
IOV	instantaneous overvoltage
IRIG	inter-range instrumentation group
IUV	instantaneous undervoltage
K0	zero sequence current compensation
kA	kiloAmpere
kV	kiloVolt
LED	light emitting diode
LEO	line end open
LOOP	loopback
LPU	line pickup
LRA	locked-rotor current
LTC	load tap-changer
M	machine

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 4 of 7)

ABBREVIATION	MEANING
mA	milliAmpere
MAN	manual / manually
MMI	man machine interface
MMS	Manufacturing Message Specification
MSG	message
MTA	maximum torque angle
MTR	motor
MVA	MegaVolt-Ampere (total 3-phase)
MVA_A	MegaVolt-Ampere (phase A)
MVA_B	MegaVolt-Ampere (phase B)
MVA_C	MegaVolt-Ampere (phase C)
MVAR	MegaVar (total 3-phase)
MVAR_A	MegaVar (phase A)
MVAR_B	MegaVar (phase B)
MVAR_C	MegaVar (phase C)
MVARH	MegaVar-Hour
MW	MegaWatt (total 3-phase)
MW_A	MegaWatt (phase A)
MW_B	MegaWatt (phase B)
MW_C	MegaWatt (phase C)
MWH	MegaWatt-Hour
N	neutral
N/A, n/a	not applicable
NEG	negative
NMPLT	nameplate
NOM	nominal
NTR	neutral
O	over
OC, O/C	overcurrent
O/P, Op	output
OP	operate
OPER	operate
OPERATG	operating
O/S	operating system
OSB	out-of-step blocking
OUT	output
OV	overvoltage
OVERFREQ	overfrequency

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 5 of 7)

ABBREVIATION	MEANING
OVLD	overload
P	phase
PC	phase comparison, personal computer
PCNT	percent
PF	power factor (total 3-phase)
PF_A	power factor (phase A)
PF_B	power factor (phase B)
PF_C	power factor (phase C)
PHS	phase
PKP	pickup
PLC	power line carrier
POS	positive
POTT	permissive over-reaching transfer trip
PRESS	pressure
PROT	protection
PSEL	presentation selector
pu	per unit
PUIB	pickup current block
PUIT	pickup current trip
PUTT	permissive under-reaching transfer trip
PWM	pulse width modulated
PWR	power
R	rate, reverse
REM	remote
REV	reverse
RI	reclose initiate
RIP	reclose in progress
ROD	remote open detector
RST	reset
RSTR	restrained
RTD	resistance temperature detector
RTU	remote terminal unit
RX (Rx)	receive, receiver
s	second
S	sensitive
SAT	CT saturation
SBO	select before operate
SEL	select / selector / selection

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 6 of 7)

ABBREVIATION	MEANING
SENS	sensitive
SEQ	sequence
SIR	source impedance ratio
SRC	source
SSB	single side band
SSEL	session selector
STATS	statistics
SUPN	supervision
SUPV	supervise / supervision
SV	supervision
SYNCHCHK	synchrocheck
T	time, transformer
TC	thermal capacity
TD MULT	time dial multiplier
TEMP	temperature
THD	total harmonic distortion
TOC	time overcurrent
TOV	time overvoltage
TRANS	transient
TRANSF	transfer
TSEL	transport selector
TUC	time undercurrent
TUV	time undervoltage
TX (Tx)	transmit, transmitter
U	under
UC	undercurrent
UCA	Utility Communications Architecture
UNBAL	unbalance
UR	universal relay
.URS	file name extension for settings files
UV	undervoltage
V/Hz	Volts per Hertz
V_0	zero sequence voltage
V_1	positive sequence voltage
V_2	negative sequence voltage
VA	phase A voltage
VAB	phase A to B voltage
VAG	phase A to ground voltage

Table D–1: UR PRODUCT STANDARD ABBREVIATIONS (Sheet 7 of 7)

ABBREVIATION	MEANING
VARH	var-hour voltage
VB	phase B voltage
VBA	phase B to A voltage
VBG	phase B to ground voltage
VC	phase C voltage
VCA	phase C to A voltage
VCG	phase C to ground voltage
VF	variable frequency
VIBR	vibration
VT	voltage transformer
VTFF	voltage transformer fuse failure
VTLOS	voltage transformer loss of signal
WDG	winding
WH	Watt-hour
w/ opt	with option
WRT	with respect to
X	reactance
XDUCER	transducer
XFMR	transformer
Z	impedance

D

E.1.1 DNP V3.00 DEVICE PROFILE

The following table provides a “Device Profile Document” in the standard format defined in the DNP 3.0 Subset Definitions Document.

Table E–1: DNP V3.00 DEVICE PROFILE (Sheet 1 of 3)

(Also see the IMPLEMENTATION TABLE in the following section)	
Vendor Name: General Electric Power Management	
Device Name: UR Series Relay	
Highest DNP Level Supported: For Requests: Level 2 For Responses: Level 2	Device Function: <input type="checkbox"/> Master <input checked="" type="checkbox"/> Slave
Notable objects, functions, and/or qualifiers supported in addition to the Highest DNP Levels Supported (the complete list is described in the attached table): Binary Inputs (Object 1) Binary Input Changes (Object 2) Binary Outputs (Object 10) Binary Counters (Object 20) Frozen Counters (Object 21) Counter Change Event (Object 22) Frozen Counter Event (Object 23) Analog Inputs (Object 30) Analog Input Changes (Object 32) Analog Deadbands (Object 34)	
Maximum Data Link Frame Size (octets): Transmitted: 292 Received: 292	Maximum Application Fragment Size (octets): Transmitted: 240 Received: 2048
Maximum Data Link Re-tries: <input type="checkbox"/> None <input checked="" type="checkbox"/> Fixed at 2 <input type="checkbox"/> Configurable	Maximum Application Layer Re-tries: <input checked="" type="checkbox"/> None <input type="checkbox"/> Configurable
Requires Data Link Layer Confirmation: <input checked="" type="checkbox"/> Never <input type="checkbox"/> Always <input type="checkbox"/> Sometimes <input type="checkbox"/> Configurable	

Table E-1: DNP V3.00 DEVICE PROFILE (Sheet 2 of 3)

Requires Application Layer Confirmation:				
<input type="checkbox"/> Never <input type="checkbox"/> Always <input checked="" type="checkbox"/> When reporting Event Data <input checked="" type="checkbox"/> When sending multi-fragment responses <input type="checkbox"/> Sometimes <input type="checkbox"/> Configurable				
Timeouts while waiting for:				
Data Link Confirm:	<input type="checkbox"/> None	<input checked="" type="checkbox"/> Fixed at 3 s	<input type="checkbox"/> Variable	<input type="checkbox"/> Configurable
Complete Appl. Fragment:	<input checked="" type="checkbox"/> None	<input type="checkbox"/> Fixed at ____	<input type="checkbox"/> Variable	<input type="checkbox"/> Configurable
Application Confirm:	<input type="checkbox"/> None	<input checked="" type="checkbox"/> Fixed at 10 s	<input type="checkbox"/> Variable	<input type="checkbox"/> Configurable
Complete Appl. Response:	<input checked="" type="checkbox"/> None	<input type="checkbox"/> Fixed at ____	<input type="checkbox"/> Variable	<input type="checkbox"/> Configurable
Others:				
Transmission Delay:	No intentional delay			
Inter-character Timeout:	50 ms			
Need Time Delay:	24 hours			
Select/Operate Arm Timeout:	10 s			
Binary input change scanning period:	8 times per power system cycle			
Packed binary change process period:	1 s			
Analog input change scanning period:	500 ms			
Counter change scanning period:	500 ms			
Frozen counter event scanning period:	500 ms			
Unsolicited response notification delay:	500 ms			
Unsolicited response retry delay	configurable 0 to 60 sec.			
Sends/Executes Control Operations:				
WRITE Binary Outputs	<input checked="" type="checkbox"/> Never	<input type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
SELECT/OPERATE	<input type="checkbox"/> Never	<input checked="" type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
DIRECT OPERATE	<input type="checkbox"/> Never	<input checked="" type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
DIRECT OPERATE – NO ACK	<input type="checkbox"/> Never	<input checked="" type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Count > 1	<input checked="" type="checkbox"/> Never	<input type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Pulse On	<input type="checkbox"/> Never	<input type="checkbox"/> Always	<input checked="" type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Pulse Off	<input type="checkbox"/> Never	<input type="checkbox"/> Always	<input checked="" type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Latch On	<input type="checkbox"/> Never	<input type="checkbox"/> Always	<input checked="" type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Latch Off	<input type="checkbox"/> Never	<input type="checkbox"/> Always	<input checked="" type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Queue	<input checked="" type="checkbox"/> Never	<input type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Clear Queue	<input checked="" type="checkbox"/> Never	<input type="checkbox"/> Always	<input type="checkbox"/> Sometimes	<input type="checkbox"/> Configurable
Explanation of 'Sometimes': Object 12 points are mapped to UR Virtual Inputs. The persistence of Virtual Inputs is determined by the VIRTUAL INPUT X TYPE settings in the UR. Both "Pulse On" and "Latch On" operations perform the same function in the UR; that is, the appropriate Virtual Input is put into the "ON" state. If the Virtual Input is set to SELF-RESET, it will reset after one pass of FlexLogic™. The On/Off times and Count value are ignored.				

Table E–1: DNP V3.00 DEVICE PROFILE (Sheet 3 of 3)

Reports Binary Input Change Events when no specific variation requested: <ul style="list-style-type: none"> <input type="checkbox"/> Never <input checked="" type="checkbox"/> Only time-tagged <input type="checkbox"/> Only non-time-tagged <input type="checkbox"/> Configurable 	Reports time-tagged Binary Input Change Events when no specific variation requested: <ul style="list-style-type: none"> <input type="checkbox"/> Never <input checked="" type="checkbox"/> Binary Input Change With Time <input type="checkbox"/> Binary Input Change With Relative Time <input type="checkbox"/> Configurable (attach explanation)
Sends Unsolicited Responses: <ul style="list-style-type: none"> <input type="checkbox"/> Never <input checked="" type="checkbox"/> Configurable <input type="checkbox"/> Only certain objects <input type="checkbox"/> Sometimes (attach explanation) <input checked="" type="checkbox"/> ENABLE/DISABLE unsolicited Function codes supported 	Sends Static Data in Unsolicited Responses: <ul style="list-style-type: none"> <input checked="" type="checkbox"/> Never <input type="checkbox"/> When Device Restarts <input type="checkbox"/> When Status Flags Change <p>No other options are permitted.</p>
Default Counter Object/Variation: <ul style="list-style-type: none"> <input type="checkbox"/> No Counters Reported <input type="checkbox"/> Configurable (attach explanation) <input checked="" type="checkbox"/> Default Object: 20 <input checked="" type="checkbox"/> Default Variation: 1 <input checked="" type="checkbox"/> Point-by-point list attached 	Counters Roll Over at: <ul style="list-style-type: none"> <input type="checkbox"/> No Counters Reported <input type="checkbox"/> Configurable (attach explanation) <input checked="" type="checkbox"/> 16 Bits (Counter 8) <input checked="" type="checkbox"/> 32 Bits (Counters 0 to 7, 9) <input type="checkbox"/> Other Value: _____ <input checked="" type="checkbox"/> Point-by-point list attached
Sends Multi-Fragment Responses: <ul style="list-style-type: none"> <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No 	

E.2.1 IMPLEMENTATION TABLE

The following table identifies the variations, function codes, and qualifiers supported by the UR in both request messages and in response messages.

For static (non-change-event) objects, requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01. Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28. For change-event objects, qualifiers 17 or 28 are always responded.

Table E–2: IMPLEMENTATION TABLE (Sheet 1 of 4)

OBJECT			REQUEST		RESPONSE	
Object Number	Variation Number	Description	Function Codes (dec)	Qualifier Codes (hex)	Function Codes (dec)	Qualifier Codes (hex)
1	0	Binary Input (Variation 0 is used to request default variation)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)		
	1	Binary Input	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	2	Binary Input with Status (default – see Note 1)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
2	0	Binary Input Change (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited qty)		
	1	Binary Input Change without Time	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	2	Binary Input Change with Time (default – see Note 1)	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
10	0	Binary Output Status (Variation 0 is used to request default variation)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)		
	2	Binary Output Status (default – see Note 1)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
12	1	Control Relay Output Block	3 (select) 4 (operate) 5 (direct op) 6 (dir. op, noack)	00, 01 (start-stop) 07, 08 (limited qty) 17, 28 (index)	129 (response)	echo of request

Table E–2: IMPLEMENTATION TABLE (Sheet 2 of 4)

OBJECT			REQUEST		RESPONSE	
Object Number	Variation Number	Description	Function Codes (dec)	Qualifier Codes (hex)	Function Codes (dec)	Qualifier Codes (hex)
20	0	Binary Counter (Variation 0 is used to request default variation)	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)		
	1	32-Bit Binary Counter (default – see Note 1)	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	2	16-Bit Binary Counter	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	5	32-Bit Binary Counter without Flag	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	6	16-Bit Binary Counter without Flag	1 (read) 7 (freeze) 8 (freeze noack) 9 (freeze clear) 10 (frz. cl. noack) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
21	0	Frozen Counter (Variation 0 is used to request default variation)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)		
	1	32-Bit Frozen Counter (default – see Note 1)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	2	16-Bit Frozen Counter	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	9	32-Bit Frozen Counter without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	10	16-Bit Frozen Counter without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
22	0	Counter Change Event (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited qty)		
	1	32-Bit Counter Change Event (default – see Note 1)	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	5	32-Bit Counter Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)

Table E–2: IMPLEMENTATION TABLE (Sheet 3 of 4)

OBJECT			REQUEST		RESPONSE	
Object Number	Variation Number	Description	Function Codes (dec)	Qualifier Codes (hex)	Function Codes (dec)	Qualifier Codes (hex)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited qty)		
	1	32-Bit Frozen Counter Event (default – see Note 1)	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	5	32-Bit Frozen Counter Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
30	0	Analog Input (Variation 0 is used to request default variation)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)		
	1	32-Bit Analog Input (default – see Note 1)	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	2	16-Bit Analog Input	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	3	32-Bit Analog Input without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	4	16-Bit Analog Input without Flag	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	5	short floating point	1 (read) 22 (assign class)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
32	0	Analog Change Event (Variation 0 is used to request default variation)	1 (read)	06 (no range, or all) 07, 08 (limited qty)		
	1	32-Bit Analog Change Event without Time (default – see Note 1)	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	2	16-Bit Analog Change Event without Time	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	3	32-Bit Analog Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
	4	16-Bit Analog Change Event with Time	1 (read)	06 (no range, or all) 07, 08 (limited qty)	129 (response) 130 (unsol. resp.)	17, 28 (index)
34	0	Analog Input Reporting Deadband (Variation 0 is used to request default variation)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)		
	1	16-bit Analog Input Reporting Deadband (default – see Note 1)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
			2 (write)	00, 01 (start-stop) 07, 08 (limited qty) 17, 28 (index)		

Table E–2: IMPLEMENTATION TABLE (Sheet 4 of 4)

OBJECT			REQUEST		RESPONSE	
Object Number	Variation Number	Description	Function Codes (dec)	Qualifier Codes (hex)	Function Codes (dec)	Qualifier Codes (hex)
34 con't	2	32-bit Analog Input Reporting Deadband (default – see Note 1)	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
			2 (write)	00, 01 (start-stop) 07, 08 (limited qty) 17, 28 (index)		
	3	Short floating point Analog Input Reporting Deadband	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
50	0	Time and Date	1 (read)	00, 01 (start-stop) 06 (no range, or all) 07, 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
	1	Time and Date (default – see Note 1)	1 (read) 2 (write)	00, 01 (start-stop) 06 (no range, or all) 07 (limited qty=1) 08 (limited qty) 17, 28 (index)	129 (response)	00, 01 (start-stop) 17, 28 (index) (see Note 2)
52	2	Time Delay Fine			129 (response)	07 (limited qty) (qty = 1)
60	0	Class 0, 1, 2, and 3 Data	1 (read) 20 (enable unsol) 21 (disable unsol) 22 (assign class)	06 (no range, or all)		
	1	Class 0 Data	1 (read) 22 (assign class)	06 (no range, or all)		
	2	Class 1 Data	1 (read) 20 (enable unsol) 21 (disable unsol) 22 (assign class)	06 (no range, or all) 07, 08 (limited qty)		
	3	Class 2 Data	1 (read) 20 (enable unsol) 21 (disable unsol) 22 (assign class)	06 (no range, or all) 07, 08 (limited qty)		
	4	Class 3 Data	1 (read) 20 (enable unsol) 21 (disable unsol) 22 (assign class)	06 (no range, or all) 07, 08 (limited qty)		
80	1	Internal Indications	2 (write)	00 (start-stop) (index must =7)		
---		No Object (function code only) – see Note 3	13 (cold restart)			
---		No Object (function code only)	14 (warm restart)			
---		No Object (function code only)	23 (delay meas.)			

- Note 1:** A Default variation refers to the variation responded when variation 0 is requested and/or in class 0, 1, 2, or 3 scans. Type 30 (Analog Input) data is limited to data that is actually possible to be used in the UR, based on the product order code. For example, Signal Source data from source numbers that cannot be used is not included. This optimizes the class 0 poll data size.
- Note 2:** For static (non-change-event) objects, qualifiers 17 or 28 are only responded when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded with qualifiers 00 or 01 (for change-event objects, qualifiers 17 or 28 are always responded.)
- Note 3:** Cold restarts are implemented the same as warm restarts – the UR is not restarted, but the DNP process is restarted.

E.3.1 BINARY INPUT POINTS

The following table lists both Binary Counters (Object 20) and Frozen Counters (Object 21). When a freeze function is performed on a Binary Counter point, the frozen value is available in the corresponding Frozen Counter point.

BINARY INPUT POINTS

Static (Steady-State) Object Number: **1**

Change Event Object Number: **2**

Request Function Codes supported: **1 (read), 22 (assign class)**

Static Variation reported when variation 0 requested: **2 (Binary Input with status)**

Change Event Variation reported when variation 0 requested: **2 (Binary Input Change with Time)**

Change Event Scan Rate: **8 times per power system cycle**

Table E-3: BINARY INPUTS (Sheet 1 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
0	Virtual Input 1	2
1	Virtual Input 2	2
2	Virtual Input 3	2
3	Virtual Input 4	2
4	Virtual Input 5	2
5	Virtual Input 6	2
6	Virtual Input 7	2
7	Virtual Input 8	2
8	Virtual Input 9	2
9	Virtual Input 10	2
10	Virtual Input 11	2
11	Virtual Input 12	2
12	Virtual Input 13	2
13	Virtual Input 14	2
14	Virtual Input 15	2
15	Virtual Input 16	2
16	Virtual Input 17	2
17	Virtual Input 18	2
18	Virtual Input 19	2
19	Virtual Input 20	2
20	Virtual Input 21	2
21	Virtual Input 22	2
22	Virtual Input 23	2
23	Virtual Input 24	2
24	Virtual Input 25	2
25	Virtual Input 26	2
26	Virtual Input 27	2
27	Virtual Input 28	2
28	Virtual Input 29	2

Table E-3: BINARY INPUTS (Sheet 2 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
29	Virtual Input 30	2
30	Virtual Input 31	2
31	Virtual Input 32	2
32	Virtual Output 1	2
33	Virtual Output 2	2
34	Virtual Output 3	2
35	Virtual Output 4	2
36	Virtual Output 5	2
37	Virtual Output 6	2
38	Virtual Output 7	2
39	Virtual Output 8	2
40	Virtual Output 9	2
41	Virtual Output 10	2
42	Virtual Output 11	2
43	Virtual Output 12	2
44	Virtual Output 13	2
45	Virtual Output 14	2
46	Virtual Output 15	2
47	Virtual Output 16	2
48	Virtual Output 17	2
49	Virtual Output 18	2
50	Virtual Output 19	2
51	Virtual Output 20	2
52	Virtual Output 21	2
53	Virtual Output 22	2
54	Virtual Output 23	2
55	Virtual Output 24	2
56	Virtual Output 25	2
57	Virtual Output 26	2

Table E-3: BINARY INPUTS (Sheet 3 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
58	Virtual Output 27	2
59	Virtual Output 28	2
60	Virtual Output 29	2
61	Virtual Output 30	2
62	Virtual Output 31	2
63	Virtual Output 32	2
64	Virtual Output 33	2
65	Virtual Output 34	2
66	Virtual Output 35	2
67	Virtual Output 36	2
68	Virtual Output 37	2
69	Virtual Output 38	2
70	Virtual Output 39	2
71	Virtual Output 40	2
72	Virtual Output 41	2
73	Virtual Output 42	2
74	Virtual Output 43	2
75	Virtual Output 44	2
76	Virtual Output 45	2
77	Virtual Output 46	2
78	Virtual Output 47	2
79	Virtual Output 48	2
80	Virtual Output 49	2
81	Virtual Output 50	2
82	Virtual Output 51	2
83	Virtual Output 52	2
84	Virtual Output 53	2
85	Virtual Output 54	2
86	Virtual Output 55	2
87	Virtual Output 56	2
88	Virtual Output 57	2
89	Virtual Output 58	2
90	Virtual Output 59	2
91	Virtual Output 60	2
92	Virtual Output 61	2
93	Virtual Output 62	2
94	Virtual Output 63	2
95	Virtual Output 64	2
96	Contact Input 1	1
97	Contact Input 2	1
98	Contact Input 3	1
99	Contact Input 4	1
100	Contact Input 5	1
101	Contact Input 6	1
102	Contact Input 7	1
103	Contact Input 8	1
104	Contact Input 9	1

Table E-3: BINARY INPUTS (Sheet 4 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
105	Contact Input 10	1
106	Contact Input 11	1
107	Contact Input 12	1
108	Contact Input 13	1
109	Contact Input 14	1
110	Contact Input 15	1
111	Contact Input 16	1
112	Contact Input 17	1
113	Contact Input 18	1
114	Contact Input 19	1
115	Contact Input 20	1
116	Contact Input 21	1
117	Contact Input 22	1
118	Contact Input 23	1
119	Contact Input 24	1
120	Contact Input 25	1
121	Contact Input 26	1
122	Contact Input 27	1
123	Contact Input 28	1
124	Contact Input 29	1
125	Contact Input 30	1
126	Contact Input 31	1
127	Contact Input 32	1
128	Contact Input 33	1
129	Contact Input 34	1
130	Contact Input 35	1
131	Contact Input 36	1
132	Contact Input 37	1
133	Contact Input 38	1
134	Contact Input 39	1
135	Contact Input 40	1
136	Contact Input 41	1
137	Contact Input 42	1
138	Contact Input 43	1
139	Contact Input 44	1
140	Contact Input 45	1
141	Contact Input 46	1
142	Contact Input 47	1
143	Contact Input 48	1
144	Contact Input 49	1
145	Contact Input 50	1
146	Contact Input 51	1
147	Contact Input 52	1
148	Contact Input 53	1
149	Contact Input 54	1
150	Contact Input 55	1
151	Contact Input 56	1

Table E–3: BINARY INPUTS (Sheet 5 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
152	Contact Input 57	1
153	Contact Input 58	1
154	Contact Input 59	1
155	Contact Input 60	1
156	Contact Input 61	1
157	Contact Input 62	1
158	Contact Input 63	1
159	Contact Input 64	1
160	Contact Input 65	1
161	Contact Input 66	1
162	Contact Input 67	1
163	Contact Input 68	1
164	Contact Input 69	1
165	Contact Input 70	1
166	Contact Input 71	1
167	Contact Input 72	1
168	Contact Input 73	1
169	Contact Input 74	1
170	Contact Input 75	1
171	Contact Input 76	1
172	Contact Input 77	1
173	Contact Input 78	1
174	Contact Input 79	1
175	Contact Input 80	1
176	Contact Input 81	1
177	Contact Input 82	1
178	Contact Input 83	1
179	Contact Input 84	1
180	Contact Input 85	1
181	Contact Input 86	1
182	Contact Input 87	1
183	Contact Input 88	1
184	Contact Input 89	1
185	Contact Input 90	1
186	Contact Input 91	1
187	Contact Input 92	1
188	Contact Input 93	1
189	Contact Input 94	1
190	Contact Input 95	1
191	Contact Input 96	1
192	Contact Output 1	1
193	Contact Output 2	1
194	Contact Output 3	1
195	Contact Output 4	1
196	Contact Output 5	1
197	Contact Output 6	1
198	Contact Output 7	1

Table E–3: BINARY INPUTS (Sheet 6 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
199	Contact Output 8	1
200	Contact Output 9	1
201	Contact Output 10	1
202	Contact Output 11	1
203	Contact Output 12	1
204	Contact Output 13	1
205	Contact Output 14	1
206	Contact Output 15	1
207	Contact Output 16	1
208	Contact Output 17	1
209	Contact Output 18	1
210	Contact Output 19	1
211	Contact Output 20	1
212	Contact Output 21	1
213	Contact Output 22	1
214	Contact Output 23	1
215	Contact Output 24	1
216	Contact Output 25	1
217	Contact Output 26	1
218	Contact Output 27	1
219	Contact Output 28	1
220	Contact Output 29	1
221	Contact Output 30	1
222	Contact Output 31	1
223	Contact Output 32	1
224	Contact Output 33	1
225	Contact Output 34	1
226	Contact Output 35	1
227	Contact Output 36	1
228	Contact Output 37	1
229	Contact Output 38	1
230	Contact Output 39	1
231	Contact Output 40	1
232	Contact Output 41	1
233	Contact Output 42	1
234	Contact Output 43	1
235	Contact Output 44	1
236	Contact Output 45	1
237	Contact Output 46	1
238	Contact Output 47	1
239	Contact Output 48	1
240	Contact Output 49	1
241	Contact Output 50	1
242	Contact Output 51	1
243	Contact Output 52	1
244	Contact Output 53	1
245	Contact Output 54	1

Table E-3: BINARY INPUTS (Sheet 7 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
246	Contact Output 55	1
247	Contact Output 56	1
248	Contact Output 57	1
249	Contact Output 58	1
250	Contact Output 59	1
251	Contact Output 60	1
252	Contact Output 61	1
253	Contact Output 62	1
254	Contact Output 63	1
255	Contact Output 64	1
256	Remote Input 1	1
257	Remote Input 2	1
258	Remote Input 3	1
259	Remote Input 4	1
260	Remote Input 5	1
261	Remote Input 6	1
262	Remote Input 7	1
263	Remote Input 8	1
264	Remote Input 9	1
265	Remote Input 10	1
266	Remote Input 11	1
267	Remote Input 12	1
268	Remote Input 13	1
269	Remote Input 14	1
270	Remote Input 15	1
271	Remote Input 16	1
272	Remote Input 17	1
273	Remote Input 18	1
274	Remote Input 19	1
275	Remote Input 20	1
276	Remote Input 21	1
277	Remote Input 22	1
278	Remote Input 23	1
279	Remote Input 24	1
280	Remote Input 25	1
281	Remote Input 26	1
282	Remote Input 27	1
283	Remote Input 28	1
284	Remote Input 29	1
285	Remote Input 30	1
286	Remote Input 31	1
287	Remote Input 32	1
288	Remote Device 1	1
289	Remote Device 2	1
290	Remote Device 3	1
291	Remote Device 4	1
292	Remote Device 5	1

Table E-3: BINARY INPUTS (Sheet 8 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
293	Remote Device 6	1
294	Remote Device 7	1
295	Remote Device 8	1
296	Remote Device 9	1
297	Remote Device 10	1
298	Remote Device 11	1
299	Remote Device 12	1
300	Remote Device 13	1
301	Remote Device 14	1
302	Remote Device 15	1
303	Remote Device 16	1
304	PHASE IOC1 Element OP	1
305	PHASE IOC2 Element OP	1
306	Not Used	---
↓	↓	↓
315	Not Used	---
316	Not Used	---
317	Not Used	---
318	Not Used	---
319	Not Used	---
320	PHASE TOC1 Element OP	1
321	PHASE TOC2 Element OP	1
322	Not Used	---
↓	↓	↓
325	Not Used	---
326	Not Used	---
327	Not Used	---
328	PH DIR1 Element OP	1
329	PH DIR2 Element OP	1
330	Not Used	---
↓	↓	↓
335	Not Used	---
336	NEUTRAL IOC1 Element OP	1
337	NEUTRAL IOC2 Element OP	1
338	NEUTRAL IOC3 Element OP	1
339	NEUTRAL IOC4 Element OP	1
340	NEUTRAL IOC5 Element OP	1
341	NEUTRAL IOC6 Element OP	1
342	NEUTRAL IOC7 Element OP	1
343	NEUTRAL IOC8 Element OP	1
344	NEUTRAL IOC9 Element OP	1
345	NEUTRAL IOC10 Element OP	1
346	NEUTRAL IOC11 Element OP	1
347	NEUTRAL IOC12 Element OP	1
348	Not Used	---
349	Not Used	---
350	Not Used	---

Table E–3: BINARY INPUTS (Sheet 9 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
351	Not Used	---
352	NEUTRAL TOC1 Element OP	1
353	NEUTRAL TOC2 Element OP	1
354	NEUTRAL TOC3 Element OP	1
355	NEUTRAL TOC4 Element OP	1
356	NEUTRAL TOC5 Element OP	1
357	NEUTRAL TOC6 Element OP	1
358	Not Used	---
359	Not Used	---
360	NTRL DIR OC1 Element OP	1
361	NTRL DIR OC2 Element OP	1
362	Not Used	---
363	Not Used	---
364	NEG SEQ DIR OC1 Elem OP	1
365	NEG SEQ DIR OC2 Elem OP	1
366	Not Used	---
367	Not Used	---
368	GROUND IOC1 Element OP	1
369	GROUND IOC2 Element OP	1
370	GROUND IOC3 Element OP	1
371	GROUND IOC4 Element OP	1
372	GROUND IOC5 Element OP	1
373	GROUND IOC6 Element OP	1
374	GROUND IOC7 Element OP	1
375	GROUND IOC8 Element OP	1
376	GROUND IOC9 Element OP	1
377	GROUND IOC10 Element OP	1
378	GROUND IOC11 Element OP	1
379	GROUND IOC12 Element OP	1
380	Not Used	---
381	Not Used	---
382	Not Used	---
383	Not Used	---
384	GROUND TOC1 Element OP	1
385	GROUND TOC2 Element OP	1
386	GROUND TOC3 Element OP	1
387	GROUND TOC4 Element OP	1
388	GROUND TOC5 Element OP	1
389	GROUND TOC6 Element OP	1
390	RESTD GND FT1 Element OP	1
391	RESTD GND FT2 Element OP	1
392	RESTD GND FT3 Element OP	1
393	RESTD GND FT4 Element OP	1
394	RESTD GND FT5 Element OP	1
395	RESTD GND FT6 Element OP	1
396	Not Used	---
397	Not Used	---

Table E–3: BINARY INPUTS (Sheet 10 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
398	Not Used	---
399	Not Used	---
400	NEG SEQ IOC1 Element OP	1
401	NEG SEQ IOC2 Element OP	1
402	Not Used	---
↓	↓	↓
415	Not Used	---
416	NEG SEQ TOC1 Element OP	1
417	NEG SEQ TOC2 Element OP	1
418	Not Used	---
↓	↓	↓
423	Not Used	---
424	NEG SEQ OV Element OP	1
425	Not Used	---
↓	↓	↓
431	Not Used	---
432	HI-Z Element OP	1
433	BUS 1 Element OP	1
434	BUS 2 Element OP	1
435	Not Used	---
↓	↓	↓
447	Not Used	---
448	PHASE UV1 Element OP	1
449	PHASE UV2 Element OP	1
450	Not Used	---
↓	↓	↓
455	Not Used	---
456	PHASE OV1 Element OP	1
457	Not Used	---
↓	↓	↓
463	Not Used	---
464	PH DIST Z1 Element OP	1
465	PH DIST Z2 Element OP	1
466	PH DIST Z3 Element OP	1
467	PH DIST Z4 Element OP	1
468	Not Used	---
469	Not Used	---
470	Not Used	---
471	Not Used	---
472	LINE PICKUP Element OP	1
473	Not Used	---
↓	↓	↓
479	Not Used	---
480	GND DIST Z1 Element OP	1
481	GND DIST Z2 Element OP	1
482	GND DIST Z3 Element OP	1
483	GND DIST Z4 Element OP	1

Table E-3: BINARY INPUTS (Sheet 11 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
484	Not Used	---
485	Not Used	---
486	Not Used	---
487	Not Used	---
488	DUTT Element OP	1
489	PUTT Element OP	1
490	POTT Element OP	1
491	HYBRID POTT Element OP	1
492	BLOCK SCHEME Element OP	1
493	Not Used	---
494	POWER SWING Element OP	1
495	Not Used	---
496	DATA TRIG 1 Element OP	1
497	DATA TRIG 2 Element OP	1
498	DATA TRIG 3 Element OP	1
499	DATA TRIG 4 Element OP	1
500	Not Used	---
↓	↓	↓
511	Not Used	---
512	XFRMR INST DIFF Elemnt OP	1
513	XFRMR PCNT DIFF Elemnt OP	1
514	VOLTS PER HERTZ Elem. OP	1
515	STATOR DIFF Element OP	1
516	Not Used	---
↓	↓	↓
527	Not Used	---
528	SRC1 VT FUSE FAIL Elem OP	1
529	SRC2 VT FUSE FAIL Elem OP	1
530	SRC3 VT FUSE FAIL Elem OP	1
531	SRC4 VT FUSE FAIL Elem OP	1
532	SRC5 VT FUSE FAIL Elem OP	1
533	SRC6 VT FUSE FAIL Elem OP	1
534	Not Used	---
535	Not Used	---
536	SRC1 50DD Element OP	1
537	SRC2 50DD Element OP	1
538	SRC3 50DD Element OP	1
539	SRC4 50DD Element OP	1
540	SRC5 50DD Element OP	1
541	SRC6 50DD Element OP	1
542	Not Used	---
543	Not Used	---
544	87L DIFF Element OP	1
545	Not Used	---
546	OPEN POLE Element OP	1
547	Not Used	1
548	50DD Element OP	1

Table E-3: BINARY INPUTS (Sheet 12 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
549	CONT MONITOR Element OP	1
550	CT FAIL Element OP	1
551	CT Trouble 1	1
552	CT Trouble 2	1
553	87I TRIP Element OP	1
554	STUB BUS Element OP	1
555	Not Used	---
↓	↓	↓
559	Not Used	---
560	87PC Element OP	1
561	Not Used	---
562	Not Used	---
563	Not Used	---
564	MOTOR Element OP	1
565	Not Used	---
↓	↓	↓
575	Not Used	---
576	BREAKER 1 Element OP	1
577	BREAKER 2 Element OP	1
578	Not Used	---
↓	↓	↓
583	Not Used	---
584	BKR FAIL 1 Element OP	1
585	BKR FAIL 2 Element OP	1
586	Not Used	---
↓	↓	↓
591	Not Used	---
592	BKR ARC 1 Element OP	1
593	BKR ARC 2 Element OP	1
594	Not Used	---
↓	↓	↓
607	Not Used	---
608	AR 1 Element OP	1
609	AR 2 Element OP	1
610	AR 3 Element OP	1
611	AR 4 Element OP	1
612	AR 5 Element OP	1
613	AR 6 Element OP	1
614	Not Used	---
615	Not Used	---
616	SYNC 1 Element OP	1
617	SYNC 2 Element OP	1
618	Not Used	---
↓	↓	↓
623	Not Used	---
624	COLD LOAD 1 Element OP	1
625	COLD LOAD 2 Element OP	1

Table E-3: BINARY INPUTS (Sheet 13 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
626	Not Used	---
627	Not Used	---
628	AMP UNBALANCE 1 Elem. OP	1
629	AMP UNBALANCE 2 Elem. OP	1
630	Not Used	---
↓	↓	↓
639	Not Used	---
640	SETTING GROUP Element OP	1
641	RESET Element OP	1
642	Not Used	---
↓	↓	↓
654	Not Used	---
655	OVERFREQ Element OP	1
656	UNDERFREQ 1 Element OP	1
657	UNDERFREQ 2 Element OP	1
658	UNDERFREQ 3 Element OP	1
659	UNDERFREQ 4 Element OP	1
660	UNDERFREQ 5 Element OP	1
661	UNDERFREQ 6 Element OP	1
662	Not Used	---
↓	↓	↓
815	Not Used	---
816	DIG ELEM 1 Element OP	1
817	DIG ELEM 2 Element OP	1
818	DIG ELEM 3 Element OP	1
819	DIG ELEM 4 Element OP	1
820	DIG ELEM 5 Element OP	1
821	DIG ELEM 6 Element OP	1
822	DIG ELEM 7 Element OP	1
823	DIG ELEM 8 Element OP	1
824	DIG ELEM 9 Element OP	1
825	DIG ELEM 10 Element OP	1
826	DIG ELEM 11 Element OP	1
827	DIG ELEM 12 Element OP	1
828	DIG ELEM 13 Element OP	1
829	DIG ELEM 14 Element OP	1
830	DIG ELEM 15 Element OP	1
831	DIG ELEM 16 Element OP	1
832	Not Used	---
↓	↓	↓
847	Not Used	---
848	COUNTER 1 Element OP	1
849	COUNTER 2 Element OP	1
850	COUNTER 3 Element OP	1
851	COUNTER 4 Element OP	1
852	COUNTER 5 Element OP	1
853	COUNTER 6 Element OP	1

Table E-3: BINARY INPUTS (Sheet 14 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
854	COUNTER 7 Element OP	1
855	COUNTER 8 Element OP	1
856	Not Used	---
↓	↓	↓
863	Not Used	---
864	LED State 1 (IN SERVICE)	1
865	LED State 2 (TROUBLE)	1
866	LED State 3 (TEST MODE)	1
867	LED State 4 (TRIP)	1
868	LED State 5 (ALARM)	1
869	LED State 6 (PICKUP)	1
870	Not Used	---
↓	↓	↓
879	Not Used	---
880	LED State 9 (VOLTAGE)	1
881	LED State 10 (CURRENT)	1
882	LED State 11 (FREQUENCY)	1
883	LED State 12 (OTHER)	1
884	LED State 13 (PHASE A)	1
885	LED State 14 (PHASE B)	1
886	LED State 15 (PHASE C)	1
887	LED State 16 (NTL/GROUND)	1
888	Not Used	---
↓	↓	↓
895	Not Used	---
896	CHANNEL 1 FAILED	1
897	CHANNEL 2 FAILED	1
898	FLASH PROGRAMMING	1
899	BATTERY FAIL	1
900	PRI ETHERNET FAIL	1
901	SEC ETHERNET FAIL	1
902	EPROM DATA ERROR	1
903	SRAM DATA ERROR	1
904	PROGRAM MEMORY	1
905	WATCHDOG ERROR	1
906	LOW ON MEMORY	1
907	REMOTE DEVICE OFF	1
908	Not Used	----
909	Not Used	----
910	Any Major Error	1
911	Any Minor Error	1
912	Any Self-Tests	1
913	IRIG-B FAILURE	1
914	DSP ERROR	1
915	Not Used	
916	NO DSP INTERRUPTS	1
917	UNIT NOT CALIBRATED	1

Table E-3: BINARY INPUTS (Sheet 15 of 15)

POINT INDEX	NAME/DESCRIPTION	CHANGE EVENT CLASS (1/2/3/none)
918	Not Used	---
919	CLOCK NOT SET	1
920	FACTORY SERVICE MODE	1
921	PROTOTYPE FIRMWARE	1
922	FLEXLOGIC ERR TOKEN	1
923	EQUIPMENT MISMATCH	1
924	RAM CODE FAILURE	1
925	UNIT NOT PROGRAMMED	1
926	SYSTEM EXCEPTION	1
927	SYNCHRONIZING	1

E.3.2 BINARY OUTPUT AND CONTROL RELAY OUTPUT

Supported Control Relay Output Block fields: Pulse On, Pulse Off, Latch On, Latch Off, Paired Trip, Paired Close.

BINARY OUTPUT STATUS POINTS

Object Number: **10**

Request Function Codes supported: **1 (read)**

Default Variation reported when variation 0 requested: **2 (Binary Output Status)**

CONTROL RELAY OUTPUT BLOCKS

Object Number: **12**

Request Function Codes supported: **3 (select), 4 (operate), 5 (direct operate), 6 (direct operate, noack)**

Table E-4: BINARY/CONTROL OUTPUT POINT LIST

POINT INDEX	NAME/DESCRIPTION
0	Virtual Input 1
1	Virtual Input 2
2	Virtual Input 3
3	Virtual Input 4
4	Virtual Input 5
5	Virtual Input 6
6	Virtual Input 7
7	Virtual Input 8
8	Virtual Input 9
9	Virtual Input 10
10	Virtual Input 11
11	Virtual Input 12
12	Virtual Input 13
13	Virtual Input 14
14	Virtual Input 15
15	Virtual Input 16

Table E-4: BINARY/CONTROL OUTPUT POINT LIST

POINT INDEX	NAME/DESCRIPTION
16	Virtual Input 17
17	Virtual Input 18
18	Virtual Input 19
19	Virtual Input 20
20	Virtual Input 21
21	Virtual Input 22
22	Virtual Input 23
23	Virtual Input 24
24	Virtual Input 25
25	Virtual Input 26
26	Virtual Input 27
27	Virtual Input 28
28	Virtual Input 29
29	Virtual Input 30
30	Virtual Input 31
31	Virtual Input 32

E.3.3 COUNTERS

The following table lists both Binary Counters (Object 20) and Frozen Counters (Object 21). When a freeze function is performed on a Binary Counter point, the frozen value is available in the corresponding Frozen Counter point.

BINARY COUNTERS

Static (Steady-State) Object Number: **20**

Change Event Object Number: **22**

Request Function Codes supported: **1 (read), 7 (freeze), 8 (freeze noack), 9 (freeze and clear), 10 (freeze and clear, noack), 22 (assign class)**

Static Variation reported when variation 0 requested: **1 (32-Bit Binary Counter with Flag)**

Change Event Variation reported when variation 0 requested: **1 (32-Bit Counter Change Event without time)**

FROZEN COUNTERS

Static (Steady-State) Object Number: **21**

Change Event Object Number: **23**

Request Function Codes supported: **1 (read)**

Static Variation reported when variation 0 requested: **1 (32-Bit Frozen Counter with Flag)**

Change Event Variation reported when variation 0 requested: **1 (32-Bit Frozen Counter Event without time)**

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Table E-5: BINARY and FROZEN COUNTERS

POINT INDEX	NAME/DESCRIPTION
0	Digital Counter 1
1	Digital Counter 2
2	Digital Counter 3
3	Digital Counter 4
4	Digital Counter 5
5	Digital Counter 6
6	Digital Counter 7
7	Digital Counter 8
8	Oscillography Trigger Count
9	Events Since Last Clear

Note that a counter freeze command has no meaning for counters 8 and 9.

E.3.4 ANALOG INPUTS

The following table lists Analog Inputs (Object 30). It is important to note that 16-bit and 32-bit variations of Analog Inputs are transmitted through DNP as signed numbers. Even for analog input points that are not valid as negative values, the maximum positive representation is 32767. This is a requirement of DNP.

The deadbands for all Analog Input points are in the same units as the Analog Input quantity. For example, an Analog Input quantity measured in volts has a corresponding deadband in units of volts. This is in conformance with DNP Technical Bulletin 9809-001 Analog Input Reporting Deadband. Default deadbands are set to relatively high values to prevent the generation of unexpected change events. Deadbands can be changed using DNP Object 34.

When using the UR in DNP systems with limited memory, the long ANALOG INPUT POINTS LIST below may be replaced with a user-definable list. This user-definable list uses the same settings as the Modbus User Map and can be configured with the MODBUS USER MAP settings. When used with DNP, each entry in the Modbus User Map represents the starting Modbus address of a data item available as a DNP Analog Input point. To enable use of the Modbus User Map for DNP Analog Input points, set the USER MAP FOR DNP ANALOGS setting to Enabled (this setting is in the PRODUCT SETUP \ COMMUNICATIONS \ DNP PROTOCOL menu). The new DNP Analog points list can be checked via the "DNP Analog Input Points List" webpage, accessible from the "Device Information menu" webpage.



NOTE

After changing the USER MAP FOR DNP ANALOGS setting, the relay must be powered off and then back on for the setting to take effect.

In the following table, only applicable Source data values are included in class 0 polls. The product order code is used to determine the maximum number of AC Signal Sources and this information is used to determine which Source values are included in class 0 polls.

Units for Analog Input points are as follows:

- | | | | |
|-------------------|-----|--------------|-----------|
| • Current: | A | • Energy | Wh, varh |
| • Voltage: | V | • Frequency: | Hz |
| • Real Power: | W | • Angle: | degrees |
| • Reactive Power: | var | • Ohm Input: | Ohms |
| • Apparent Power: | VA | • RTD Input: | degrees C |

Static (Steady-State) Object Number: **30**

Change Event Object Number: **32**

Request Function Codes supported: **1 (read), 2 (write, deadbands only), 22 (assign class)**

Static Variation reported when variation 0 requested: **1 (32-Bit Analog Input)**

Change Event Variation reported when variation 0 requested: **1 (Analog Change Event w/o Time)**

Change Event Scan Rate: Defaults to 500 ms.

Table E-6: ANALOG INPUT POINTS (Sheet 1 of 10)

POINT	DESCRIPTION
0	SRC 1 Phase A Current RMS
1	SRC 1 Phase B Current RMS
2	SRC 1 Phase C Current RMS
3	SRC 1 Neutral Current RMS
4	SRC 1 Phase A Current Magnitude
5	SRC 1 Phase A Current Angle
6	SRC 1 Phase B Current Magnitude
7	SRC 1 Phase B Current Angle
8	SRC 1 Phase C Current Magnitude
9	SRC 1 Phase C Current Angle
10	SRC 1 Neutral Current Magnitude
11	SRC 1 Neutral Current Angle
12	SRC 1 Ground Current RMS
13	SRC 1 Ground Current Magnitude
14	SRC 1 Ground Current Angle
15	SRC 1 Zero Sequence Current Magnitude
16	SRC 1 Zero Sequence Current Angle
17	SRC 1 Positive Sequence Current Magnitude
18	SRC 1 Positive Sequence Current Angle
19	SRC 1 Negative Sequence Current Magnitude
20	SRC 1 Negative Sequence Current Angle
21	SRC 1 Differential Ground Current Magnitude
22	SRC 1 Differential Ground Current Angle
23	SRC 2 Phase A Current RMS
24	SRC 2 Phase B Current RMS
25	SRC 2 Phase C Current RMS
26	SRC 2 Neutral Current RMS
27	SRC 2 Phase A Current Magnitude
28	SRC 2 Phase A Current Angle
29	SRC 2 Phase B Current Magnitude
30	SRC 2 Phase B Current Angle
31	SRC 2 Phase C Current Magnitude
32	SRC 2 Phase C Current Angle
33	SRC 2 Neutral Current Magnitude
34	SRC 2 Neutral Current Angle
35	SRC 2 Ground Current RMS
36	SRC 2 Ground Current Magnitude
37	SRC 2 Ground Current Angle
38	SRC 2 Zero Sequence Current Magnitude
39	SRC 2 Zero Sequence Current Angle
40	SRC 2 Positive Sequence Current Magnitude
41	SRC 2 Positive Sequence Current Angle
42	SRC 2 Negative Sequence Current Magnitude
43	SRC 2 Negative Sequence Current Angle
44	SRC 2 Differential Ground Current Magnitude
45	SRC 2 Differential Ground Current Angle

Table E-6: ANALOG INPUT POINTS (Sheet 2 of 10)

POINT	DESCRIPTION
46	SRC 3 Phase A Current RMS
47	SRC 3 Phase B Current RMS
48	SRC 3 Phase C Current RMS
49	SRC 3 Neutral Current RMS
50	SRC 3 Phase A Current Magnitude
51	SRC 3 Phase A Current Angle
52	SRC 3 Phase B Current Magnitude
53	SRC 3 Phase B Current Angle
54	SRC 3 Phase C Current Magnitude
55	SRC 3 Phase C Current Angle
56	SRC 3 Neutral Current Magnitude
57	SRC 3 Neutral Current Angle
58	SRC 3 Ground Current RMS
59	SRC 3 Ground Current Magnitude
60	SRC 3 Ground Current Angle
61	SRC 3 Zero Sequence Current Magnitude
62	SRC 3 Zero Sequence Current Angle
63	SRC 3 Positive Sequence Current Magnitude
64	SRC 3 Positive Sequence Current Angle
65	SRC 3 Negative Sequence Current Magnitude
66	SRC 3 Negative Sequence Current Angle
67	SRC 3 Differential Ground Current Magnitude
68	SRC 3 Differential Ground Current Angle
69	SRC 4 Phase A Current RMS
70	SRC 4 Phase B Current RMS
71	SRC 4 Phase C Current RMS
72	SRC 4 Neutral Current RMS
73	SRC 4 Phase A Current Magnitude
74	SRC 4 Phase A Current Angle
75	SRC 4 Phase B Current Magnitude
76	SRC 4 Phase B Current Angle
77	SRC 4 Phase C Current Magnitude
78	SRC 4 Phase C Current Angle
79	SRC 4 Neutral Current Magnitude
80	SRC 4 Neutral Current Angle
81	SRC 4 Ground Current RMS
82	SRC 4 Ground Current Magnitude
83	SRC 4 Ground Current Angle
84	SRC 4 Zero Sequence Current Magnitude
85	SRC 4 Zero Sequence Current Angle
86	SRC 4 Positive Sequence Current Magnitude
87	SRC 4 Positive Sequence Current Angle
88	SRC 4 Negative Sequence Current Magnitude
89	SRC 4 Negative Sequence Current Angle
90	SRC 4 Differential Ground Current Magnitude
91	SRC 4 Differential Ground Current Angle

Table E-6: ANALOG INPUT POINTS (Sheet 3 of 10)

POINT	DESCRIPTION
92	SRC 5 Phase A Current RMS
93	SRC 5 Phase B Current RMS
94	SRC 5 Phase C Current RMS
95	SRC 5 Neutral Current RMS
96	SRC 5 Phase A Current Magnitude
97	SRC 5 Phase A Current Angle
98	SRC 5 Phase B Current Magnitude
99	SRC 5 Phase B Current Angle
100	SRC 5 Phase C Current Magnitude
101	SRC 5 Phase C Current Angle
102	SRC 5 Neutral Current Magnitude
103	SRC 5 Neutral Current Angle
104	SRC 5 Ground Current RMS
105	SRC 5 Ground Current Magnitude
106	SRC 5 Ground Current Angle
107	SRC 5 Zero Sequence Current Magnitude
108	SRC 5 Zero Sequence Current Angle
109	SRC 5 Positive Sequence Current Magnitude
110	SRC 5 Positive Sequence Current Angle
111	SRC 5 Negative Sequence Current Magnitude
112	SRC 5 Negative Sequence Current Angle
113	SRC 5 Differential Ground Current Magnitude
114	SRC 5 Differential Ground Current Angle
115	SRC 6 Phase A Current RMS
116	SRC 6 Phase B Current RMS
117	SRC 6 Phase C Current RMS
118	SRC 6 Neutral Current RMS
119	SRC 6 Phase A Current Magnitude
120	SRC 6 Phase A Current Angle
121	SRC 6 Phase B Current Magnitude
122	SRC 6 Phase B Current Angle
123	SRC 6 Phase C Current Magnitude
124	SRC 6 Phase C Current Angle
125	SRC 6 Neutral Current Magnitude
126	SRC 6 Neutral Current Angle
127	SRC 6 Ground Current RMS
128	SRC 6 Ground Current Magnitude
129	SRC 6 Ground Current Angle
130	SRC 6 Zero Sequence Current Magnitude
131	SRC 6 Zero Sequence Current Angle
132	SRC 6 Positive Sequence Current Magnitude
133	SRC 6 Positive Sequence Current Angle
134	SRC 6 Negative Sequence Current Magnitude
135	SRC 6 Negative Sequence Current Angle
136	SRC 6 Differential Ground Current Magnitude
137	SRC 6 Differential Ground Current Angle

Table E-6: ANALOG INPUT POINTS (Sheet 4 of 10)

POINT	DESCRIPTION
138	SRC 1 Phase AG Voltage RMS
139	SRC 1 Phase BG Voltage RMS
140	SRC 1 Phase CG Voltage RMS
141	SRC 1 Phase AG Voltage Magnitude
142	SRC 1 Phase AG Voltage Angle
143	SRC 1 Phase BG Voltage Magnitude
144	SRC 1 Phase BG Voltage Angle
145	SRC 1 Phase CG Voltage Magnitude
146	SRC 1 Phase CG Voltage Angle
147	SRC 1 Phase AB Voltage RMS
148	SRC 1 Phase BC Voltage RMS
149	SRC 1 Phase CA Voltage RMS
150	SRC 1 Phase AB Voltage Magnitude
151	SRC 1 Phase AB Voltage Angle
152	SRC 1 Phase BC Voltage Magnitude
153	SRC 1 Phase BC Voltage Angle
154	SRC 1 Phase CA Voltage Magnitude
155	SRC 1 Phase CA Voltage Angle
156	SRC 1 Auxiliary Voltage RMS
157	SRC 1 Auxiliary Voltage Magnitude
158	SRC 1 Auxiliary Voltage Angle
159	SRC 1 Zero Sequence Voltage Magnitude
160	SRC 1 Zero Sequence Voltage Angle
161	SRC 1 Positive Sequence Voltage Magnitude
162	SRC 1 Positive Sequence Voltage Angle
163	SRC 1 Negative Sequence Voltage Magnitude
164	SRC 1 Negative Sequence Voltage Angle
165	SRC 2 Phase AG Voltage RMS
166	SRC 2 Phase BG Voltage RMS
167	SRC 2 Phase CG Voltage RMS
168	SRC 2 Phase AG Voltage Magnitude
169	SRC 2 Phase AG Voltage Angle
170	SRC 2 Phase BG Voltage Magnitude
171	SRC 2 Phase BG Voltage Angle
172	SRC 2 Phase CG Voltage Magnitude
173	SRC 2 Phase CG Voltage Angle
174	SRC 2 Phase AB Voltage RMS
175	SRC 2 Phase BC Voltage RMS
176	SRC 2 Phase CA Voltage RMS
177	SRC 2 Phase AB Voltage Magnitude
178	SRC 2 Phase AB Voltage Angle
179	SRC 2 Phase BC Voltage Magnitude
180	SRC 2 Phase BC Voltage Angle
181	SRC 2 Phase CA Voltage Magnitude
182	SRC 2 Phase CA Voltage Angle
183	SRC 2 Auxiliary Voltage RMS

Table E-6: ANALOG INPUT POINTS (Sheet 5 of 10)

POINT	DESCRIPTION
184	SRC 2 Auxiliary Voltage Magnitude
185	SRC 2 Auxiliary Voltage Angle
186	SRC 2 Zero Sequence Voltage Magnitude
187	SRC 2 Zero Sequence Voltage Angle
188	SRC 2 Positive Sequence Voltage Magnitude
189	SRC 2 Positive Sequence Voltage Angle
190	SRC 2 Negative Sequence Voltage Magnitude
191	SRC 2 Negative Sequence Voltage Angle
192	SRC 3 Phase AG Voltage RMS
193	SRC 3 Phase BG Voltage RMS
194	SRC 3 Phase CG Voltage RMS
195	SRC 3 Phase AG Voltage Magnitude
196	SRC 3 Phase AG Voltage Angle
197	SRC 3 Phase BG Voltage Magnitude
198	SRC 3 Phase BG Voltage Angle
199	SRC 3 Phase CG Voltage Magnitude
200	SRC 3 Phase CG Voltage Angle
201	SRC 3 Phase AB Voltage RMS
202	SRC 3 Phase BC Voltage RMS
203	SRC 3 Phase CA Voltage RMS
204	SRC 3 Phase AB Voltage Magnitude
205	SRC 3 Phase AB Voltage Angle
206	SRC 3 Phase BC Voltage Magnitude
207	SRC 3 Phase BC Voltage Angle
208	SRC 3 Phase CA Voltage Magnitude
209	SRC 3 Phase CA Voltage Angle
210	SRC 3 Auxiliary Voltage RMS
211	SRC 3 Auxiliary Voltage Magnitude
212	SRC 3 Auxiliary Voltage Angle
213	SRC 3 Zero Sequence Voltage Magnitude
214	SRC 3 Zero Sequence Voltage Angle
215	SRC 3 Positive Sequence Voltage Magnitude
216	SRC 3 Positive Sequence Voltage Angle
217	SRC 3 Negative Sequence Voltage Magnitude
218	SRC 3 Negative Sequence Voltage Angle
219	SRC 4 Phase AG Voltage RMS
220	SRC 4 Phase BG Voltage RMS
221	SRC 4 Phase CG Voltage RMS
222	SRC 4 Phase AG Voltage Magnitude
223	SRC 4 Phase AG Voltage Angle
224	SRC 4 Phase BG Voltage Magnitude
225	SRC 4 Phase BG Voltage Angle
226	SRC 4 Phase CG Voltage Magnitude
227	SRC 4 Phase CG Voltage Angle
228	SRC 4 Phase AB Voltage RMS
229	SRC 4 Phase BC Voltage RMS

Table E-6: ANALOG INPUT POINTS (Sheet 6 of 10)

POINT	DESCRIPTION
230	SRC 4 Phase CA Voltage RMS
231	SRC 4 Phase AB Voltage Magnitude
232	SRC 4 Phase AB Voltage Angle
233	SRC 4 Phase BC Voltage Magnitude
234	SRC 4 Phase BC Voltage Angle
235	SRC 4 Phase CA Voltage Magnitude
236	SRC 4 Phase CA Voltage Angle
237	SRC 4 Auxiliary Voltage RMS
238	SRC 4 Auxiliary Voltage Magnitude
239	SRC 4 Auxiliary Voltage Angle
240	SRC 4 Zero Sequence Voltage Magnitude
241	SRC 4 Zero Sequence Voltage Angle
242	SRC 4 Positive Sequence Voltage Magnitude
243	SRC 4 Positive Sequence Voltage Angle
244	SRC 4 Negative Sequence Voltage Magnitude
245	SRC 4 Negative Sequence Voltage Angle
246	SRC 5 Phase AG Voltage RMS
247	SRC 5 Phase BG Voltage RMS
248	SRC 5 Phase CG Voltage RMS
249	SRC 5 Phase AG Voltage Magnitude
250	SRC 5 Phase AG Voltage Angle
251	SRC 5 Phase BG Voltage Magnitude
252	SRC 5 Phase BG Voltage Angle
253	SRC 5 Phase CG Voltage Magnitude
254	SRC 5 Phase CG Voltage Angle
255	SRC 5 Phase AB Voltage RMS
256	SRC 5 Phase BC Voltage RMS
257	SRC 5 Phase CA Voltage RMS
258	SRC 5 Phase AB Voltage Magnitude
259	SRC 5 Phase AB Voltage Angle
260	SRC 5 Phase BC Voltage Magnitude
261	SRC 5 Phase BC Voltage Angle
262	SRC 5 Phase CA Voltage Magnitude
263	SRC 5 Phase CA Voltage Angle
264	SRC 5 Auxiliary Voltage RMS
265	SRC 5 Auxiliary Voltage Magnitude
266	SRC 5 Auxiliary Voltage Angle
267	SRC 5 Zero Sequence Voltage Magnitude
268	SRC 5 Zero Sequence Voltage Angle
269	SRC 5 Positive Sequence Voltage Magnitude
270	SRC 5 Positive Sequence Voltage Angle
271	SRC 5 Negative Sequence Voltage Magnitude
272	SRC 5 Negative Sequence Voltage Angle
273	SRC 6 Phase AG Voltage RMS
274	SRC 6 Phase BG Voltage RMS
275	SRC 6 Phase CG Voltage RMS

Table E-6: ANALOG INPUT POINTS (Sheet 7 of 10)

POINT	DESCRIPTION
276	SRC 6 Phase AG Voltage Magnitude
277	SRC 6 Phase AG Voltage Angle
278	SRC 6 Phase BG Voltage Magnitude
279	SRC 6 Phase BG Voltage Angle
280	SRC 6 Phase CG Voltage Magnitude
281	SRC 6 Phase CG Voltage Angle
282	SRC 6 Phase AB Voltage RMS
283	SRC 6 Phase BC Voltage RMS
284	SRC 6 Phase CA Voltage RMS
285	SRC 6 Phase AB Voltage Magnitude
286	SRC 6 Phase AB Voltage Angle
287	SRC 6 Phase BC Voltage Magnitude
288	SRC 6 Phase BC Voltage Angle
289	SRC 6 Phase CA Voltage Magnitude
290	SRC 6 Phase CA Voltage Angle
291	SRC 6 Auxiliary Voltage RMS
292	SRC 6 Auxiliary Voltage Magnitude
293	SRC 6 Auxiliary Voltage Angle
294	SRC 6 Zero Sequence Voltage Magnitude
295	SRC 6 Zero Sequence Voltage Angle
296	SRC 6 Positive Sequence Voltage Magnitude
297	SRC 6 Positive Sequence Voltage Angle
298	SRC 6 Negative Sequence Voltage Magnitude
299	SRC 6 Negative Sequence Voltage Angle
300	SRC 1 Three Phase Real Power
301	SRC 1 Phase A Real Power
302	SRC 1 Phase B Real Power
303	SRC 1 Phase C Real Power
304	SRC 1 Three Phase Reactive Power
305	SRC 1 Phase A Reactive Power
306	SRC 1 Phase B Reactive Power
307	SRC 1 Phase C Reactive Power
308	SRC 1 Three Phase Apparent Power
309	SRC 1 Phase A Apparent Power
310	SRC 1 Phase B Apparent Power
311	SRC 1 Phase C Apparent Power
312	SRC 1 Three Phase Power Factor
313	SRC 1 Phase A Power Factor
314	SRC 1 Phase B Power Factor
315	SRC 1 Phase C Power Factor
316	SRC 2 Three Phase Real Power
317	SRC 2 Phase A Real Power
318	SRC 2 Phase B Real Power
319	SRC 2 Phase C Real Power
320	SRC 2 Three Phase Reactive Power
321	SRC 2 Phase A Reactive Power

Table E-6: ANALOG INPUT POINTS (Sheet 8 of 10)

POINT	DESCRIPTION
322	SRC 2 Phase B Reactive Power
323	SRC 2 Phase C Reactive Power
324	SRC 2 Three Phase Apparent Power
325	SRC 2 Phase A Apparent Power
326	SRC 2 Phase B Apparent Power
327	SRC 2 Phase C Apparent Power
328	SRC 2 Three Phase Power Factor
329	SRC 2 Phase A Power Factor
330	SRC 2 Phase B Power Factor
331	SRC 2 Phase C Power Factor
332	SRC 3 Three Phase Real Power
333	SRC 3 Phase A Real Power
334	SRC 3 Phase B Real Power
335	SRC 3 Phase C Real Power
336	SRC 3 Three Phase Reactive Power
337	SRC 3 Phase A Reactive Power
338	SRC 3 Phase B Reactive Power
339	SRC 3 Phase C Reactive Power
340	SRC 3 Three Phase Apparent Power
341	SRC 3 Phase A Apparent Power
342	SRC 3 Phase B Apparent Power
343	SRC 3 Phase C Apparent Power
344	SRC 3 Three Phase Power Factor
345	SRC 3 Phase A Power Factor
346	SRC 3 Phase B Power Factor
347	SRC 3 Phase C Power Factor
348	SRC 4 Three Phase Real Power
349	SRC 4 Phase A Real Power
350	SRC 4 Phase B Real Power
351	SRC 4 Phase C Real Power
352	SRC 4 Three Phase Reactive Power
353	SRC 4 Phase A Reactive Power
354	SRC 4 Phase B Reactive Power
355	SRC 4 Phase C Reactive Power
356	SRC 4 Three Phase Apparent Power
357	SRC 4 Phase A Apparent Power
358	SRC 4 Phase B Apparent Power
359	SRC 4 Phase C Apparent Power
360	SRC 4 Three Phase Power Factor
361	SRC 4 Phase A Power Factor
362	SRC 4 Phase B Power Factor
363	SRC 4 Phase C Power Factor
364	SRC 5 Three Phase Real Power
365	SRC 5 Phase A Real Power
366	SRC 5 Phase B Real Power
367	SRC 5 Phase C Real Power

Table E-6: ANALOG INPUT POINTS (Sheet 9 of 10)

POINT	DESCRIPTION
368	SRC 5 Three Phase Reactive Power
369	SRC 5 Phase A Reactive Power
370	SRC 5 Phase B Reactive Power
371	SRC 5 Phase C Reactive Power
372	SRC 5 Three Phase Apparent Power
373	SRC 5 Phase A Apparent Power
374	SRC 5 Phase B Apparent Power
375	SRC 5 Phase C Apparent Power
376	SRC 5 Three Phase Power Factor
377	SRC 5 Phase A Power Factor
378	SRC 5 Phase B Power Factor
379	SRC 5 Phase C Power Factor
380	SRC 6 Three Phase Real Power
381	SRC 6 Phase A Real Power
382	SRC 6 Phase B Real Power
383	SRC 6 Phase C Real Power
384	SRC 6 Three Phase Reactive Power
385	SRC 6 Phase A Reactive Power
386	SRC 6 Phase B Reactive Power
387	SRC 6 Phase C Reactive Power
388	SRC 6 Three Phase Apparent Power
389	SRC 6 Phase A Apparent Power
390	SRC 6 Phase B Apparent Power
391	SRC 6 Phase C Apparent Power
392	SRC 6 Three Phase Power Factor
393	SRC 6 Phase A Power Factor
394	SRC 6 Phase B Power Factor
395	SRC 6 Phase C Power Factor
396	SRC 1 Frequency
397	SRC 2 Frequency
398	SRC 3 Frequency
399	SRC 4 Frequency
400	SRC 5 Frequency
401	SRC 6 Frequency
402	Breaker 1 Arcing Amp Phase A
403	Breaker 1 Arcing Amp Phase B
404	Breaker 1 Arcing Amp Phase C
405	Breaker 2 Arcing Amp Phase A
406	Breaker 2 Arcing Amp Phase B
407	Breaker 2 Arcing Amp Phase C
408	Synchrocheck 1 Delta Voltage
409	Synchrocheck 1 Delta Frequency
410	Synchrocheck 1 Delta Phase
411	Synchrocheck 2 Delta Voltage
412	Synchrocheck 2 Delta Frequency
413	Synchrocheck 2 Delta Phase

Table E-6: ANALOG INPUT POINTS (Sheet 10 of 10)

POINT	DESCRIPTION
414	Power Swing S1 S2 Angle
415	Tracking Frequency
416	Communications Group
417	Current Setting Group

F.1.1 REVISION HISTORY

Table F–1: REVISION HISTORY

MANUAL P/N	L60 REVISION	RELEASE DATE	ECO
1601-0082-A1	1.5X	04 November 1998	N/A
1601-0082-A2	1.5X	25 June 1999	URL-054
1601-0082-A3	1.5X	19 August 1999	URL-056
1601-0082-A4	2.0X	26 January 2000	URL-062
1601-0082-A5	2.2X	12 May 2000	URL-066
1601-0082-A6	2.2X	14 June 2000	URL-069
1601-0082-A6a	2.2X	28 June 2000	URL-069a
1601-0082-B1	2.4X	08 September 2000	URL-074
1601-0082-B2	2.4X	03 November 2000	URL-076
1601-0082-B3	2.6X	09 March 2000	URL-080

F.1.2 CHANGES TO L60 MANUAL

Table F–2: MAJOR UPDATES FOR L60 MANUAL-B3 (Sheet 1 of 2)

PAGE (B2)	CHANGE	DESCRIPTION
Title	Update	Manual part number from B2 to B3
1-7	Add	Added section for connecting URPC with the L60.
2-	Update	Numerous specifications have been updated
2-2	Update	Updated SINGLE LINE DIAGRAM from 831707AN to 831707AP
2-2	Update	Updated DEVICE NUMBERS AND FUNCTIONS and OTHER DEVICE FUNCTIONS tables.
2-3	Update	Updated ORDER CODES table to include additional Transducer I/O and additional CT/VT DSP options.
2-6	Add	Added specifications for POWER SWING DETECT element.
3-12, 3-13	Update	Updated Section 3.2.6: CONTACT INPUTS/OUTPUTS Updated FORM-A CONTACT FUNCTIONS diagram from 827821A2 to 827821A4
3-24	Update	Updated L60 7Z MODULE WIRING diagram from L60W7Z to 831739A1
5-12	Add	Added DNP unsolicited response settings to the SETTINGS \ PRODUCT SETUP \ COMMUNICATIONS \ DNP PROTOCOL menu
5-17	Update	Updated the DIGITAL CHANNELS settings to range from 2 to 63.
5-30	Add	Added DISTURBANCE DETECTOR LOGIC DIAGRAM and DISTURBANCE DETECTORS (INTERNAL) description
5-41	Add	Added SELF-DIAGNOSTIC and POWER SWING DETECT Flexlogic operands to FLEXLOGIC OPERANDS table.
5-63	Add	Added COMMON DISTANCE SETTINGS sub-section

Table F-2: MAJOR UPDATES FOR L60 MANUAL-B3 (Sheet 2 of 2)

PAGE (B2)	CHANGE	DESCRIPTION
5-63	Add	Added MEMORY VOLTAGE LOGIC diagram
5-64	Update	Updated description for PHASE DISTANCE Z2 sub-section
5-64	Update	Updated PHASE DISTANCE Z2 OP diagram from 837020A1 to 837020A3
5-65	Update	Updated PHASE DISTANCE MHO LOGIC diagram from 837002A5 to 837002A7
5-66	Update	Updated description for GROUND DISTANCE Z2 sub-section
5-68	Update	Updated GROUND DISTANCE MHO LOGIC diagram from 837007A6 to 837007A7
5-69	Add	Added POWER SWING DETECT section
5-97	Update	Updated description for NEUTRAL DIRECTIONAL OC1/OC2 sub-section
5-136	Update	Updated CT FAILURE logic diagram from 827048A5 to 827048A6
5-140	Update	Updated 87PC SCHEME setpoints and description section
5-143	Update	Updated SINGLE PHASE COMPARISON LOGIC diagram from 831017A7 to 831017A8
5-144	Update	Updated DUAL PHASE COMPARISON LOGIC diagram from 831018A5 to 831018A6
5-145	Add	Added DUAL PHASE COMPARISON LOGIC WITH 2 FREQUENCY FSK PLC logic diagram (rev. 831021A2)
5-161	Update	Updated CHANNEL TESTS section
6-8	Add	Added UR CONVENTION FOR MEASURING PHASE ANGLES and UR CONVENTION FOR MEASURING SYMMETRICAL COMPONENTS sub-sections to the METERING CONVENTIONS section.
6-14	Remove	Deleted FAULT COMPONENT PHASORS diagram
9-	Move	Chapter 9: COMMISSIONING is now Chapter 10: COMMISSIONING
9-	Add	Added POWER SWING DETECT settings tables
9-53	Move	Section 9.8.2: PHASE COMPARISON ELEMENT 87PC is now Chapter 9: APPLICATION OF SETTINGS
B-33	Update	MODBUS MEMORY MAP updated for version 2.6X firmware
C-1	Update	Appendix C: UCA/MMS updated
E-1	Update	Updated DNP DEVICE PROFILE DOCUMENT for Counter 9, Analog Deadbands (Object 34), Sends Unsolicited Response values, and additional timeouts.
E-5	Update	Added Object 34 and Function Code 22 to DNP IMPLEMENTATION TABLE.
E-9	Updated	Updated BINARY INPUTS table.
E-17	Update	Updated BINARY AND FROZEN COUNTERS table for Index 9, Events Since Last Clear.

Table F–3: MAJOR UPDATES FOR L60 MANUAL-B2

PAGE (OLD)	CHANGE	FROM	TO (NEW PAGE)
Title	Updated	P/N ...B1	P/N ...B2
Addendum	Updated		L60 Communications modules
2-	Updated		INPUTS: AC Current conversion Range Specifications (page 2-9)
2-	Updated		METERING Frequency Accuracy Specifications (page 2-8)
3-	Updated		Form-A Contact Functions Wiring diagram (page 3-13)
E-	Updated		<i>DNP Implementation Table</i>

Table F–4: MAJOR UPDATES FOR L60 MANUAL-B1 (Sheet 1 of 2)

PAGE (OLD)	CHANGE	FROM	TO (NEW PAGE)
Title	Modified	L60 Revision: 2.2X	L60 Revision: 2.4X
Title	Modified	P/N ...A6a	P/N ...B1
Title	Updated		ISO references
Addendum	Updated		
1-	Added		Battery Tab information (page 1-11)
2-	Added		Order Codes for new Digital I/O modules (page 2-3,4)
2-9	Updated		ISO reference
4-	Added		UR Vertical Faceplate drawing (page 4-6)
4-11,12	Updated		Custom Labeling of LEDs (page 4-12,13)
5-12	Updated		Settings>Product Setup> Communications
5-18	Updated		Settings>Product Setup> User Programmable LEDs (page 5-)
5-21	Replaced	Settings>Product Setup>Message Scratchpad	Settings>Product Setup> User-Definable Displays (page 5-)
5-24	Updated		Settings>System Setup> Power System (page 5-)
5-36	Updated		FlexLogic Operands (page 5-)
5-	Added		FlexLogic Operators (One Shots) (page 5-)
5-	Added		Settings>Grouped Elements> Setting Group 1(8) (page 5-)
5-100	Updated		Settings>...> Phase Undervoltage (page 5-)

Table F-4: MAJOR UPDATES FOR L60 MANUAL-B1 (Sheet 2 of 2)

PAGE (OLD)	CHANGE	FROM	TO (NEW PAGE)
5-103	Updated		Settings>Control Elements > Setting Groups (page 5-)
5-109	Updated		Settings>Control Elements > AutoReclose (page 5-)
5-144	Updated		Settings>Inputs/Outputs > Virtual Inputs (page 5-)
5-146	Updated		Settings>Inputs/Outputs > Contact Outputs (page 5-)
6-12	Removed	Actual Values>Metering>AC Inputs> Current Banks & Voltage Banks	
6-20	Updated		Actual Values> Product Info (page 6-)
7-2	Updated		Commands Clear Records
C-1	Updated		UCA/MMS

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GE POWER MANAGEMENT RELAY WARRANTY

General Electric Power Management Inc. (GE Power Management) warrants each relay it manufactures to be free from defects in material and workmanship under normal use and service for a period of 24 months from date of shipment from factory.

In the event of a failure covered by warranty, GE Power Management will undertake to repair or replace the relay providing the warrantor determined that it is defective and it is returned with all transportation charges prepaid to an authorized service centre or the factory. Repairs or replacement under warranty will be made without charge.

Warranty shall not apply to any relay which has been subject to misuse, negligence, accident, incorrect installation or use not in accordance with instructions nor any unit that has been altered outside a GE Power Management authorized factory outlet.

GE Power Management is not liable for special, indirect or consequential damages or for loss of profit or for expenses sustained as a result of a relay malfunction, incorrect application or adjustment.

For complete text of Warranty (including limitations and disclaimers), refer to GE Power Management Standard Conditions of Sale.

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