

Design of Flip-Flops Using ABB 2000R Series Intelligent Electronic Devices

Introduction

The ABB 2000R series of relays are designed to provide advanced protective elements as well as flexible control functions. This flexibility is often accomplished by the use of internal logic functions. The internal logic functions allow for the creation of virtually any desired logic scheme. This application note describes the design of S-R Flip Flops in the DPU2000R relay and includes a typical application.

Latch Design

The overall circuit for the design of an S-R latch is shown below:



By utilizing the advantages of the 2000R series relays, the latch design can be accomplished with no additional wiring. For our purposes, the SET and RESET inputs to the latch are momentary pushbuttons hard wired to physical inputs IN1 and IN2 respectively. When the SET pushbutton is pressed, the physical output OUT1 will close and the physical output OUT2 will open. When the RESET pushbutton is pressed, OUT1 will open and OUT2 will close.

When the SET pushbutton is pressed, IN1 will go High and will set ULI1. ULI1 is *internally* fed forward to ULO1. ULO1 is mapped to OUT1 and FBO5. OUT1 will close and FBO5 becomes High. The negated FBO5 is *internally* fed back to FB5 and resets ULI5 and ULO5 to a Low state. This will cause FB6 and hence FBO6 to become Low as well. This will cause OUT2 to open. The negated FBO6 seals in FB5 and keeps OUT1 closed.

When the RESET pushbutton is pressed, IN2 will go High and will set UL11. UL12 is fed forward to ULO2. ULO2 is mapped to OUT2 and FBO6. OUT2 will close and FBO6 becomes High. The negated FBO6 is fed back to FB6 and reset UL16 and ULO6 to a Low state. This will cause FB5 and hence FBO5 to become Low. This will cause OUT1 to open. The negated FBO5 seals in FB6 and keeps OUT2 closed.

In this logic, a problem arises during the start up of the relay where the flip flop will go to a undetermined state. The logic in the dotted box will alleviate this problem. During startup, all Feedbacks are in a Low state by default. Therefore a Low FB3 is negated and fed into the RESET circuit via ULI/ULO8. This will cause the relay to automatically go to a RESET state during startup. When the IN1 pushbutton is pressed to SET the circuit, FB3 becomes High, and remains High through a seal-in via ULI/ULO7. This will then effectively take FB3 out of the circuit.

Application

It is desired that a utility would like to have the control to remotely enable or disable the reclosing function on the DPU2000R relay. However, the SCADA signals being sent to the existing RTU are momentary signals. The solution in the past was to purchase and install an external latching relay to the existing control scheme to attain the desired seal-in necessary to either enable or disable reclosing. The utility also has additional logic required at the substation. A local 43A (reclose cut off) switch is located at the substation. When this switch is off, reclosing is disabled. When this switch is on, and SCADA enables reclosing, then reclosing is enabled. Additionally, a LOCAL/SUPERVISORY switch is located at the substation. When this switch is in the LOCAL position, the control scheme is to ignore all SCADA signals. When this switch is in the SUPV position, the control scheme can act on any signals.

All of the above logic can be accomplished internally to the DPU2000R relay. The backbone to the control scheme is the S-R Flip Flop. This will accomplish the required latching from the SCADA momentary signals. The only wiring required to the DPU2000R is SCADA Enable, SCADA disable, 43A status, and LOCAL/SUPV status.

The following page shows the logic gates necessary as well as the relay programming required to accomplish the scheme.

Logic Description

The logic description for the above application is as follows. The upper left "AND" gate is accomplished simply by anding together IN6 (SCADA Enable) and NOT IN3 (LOCAL/SUPV). The NOT IN3 is accomplished by simply putting an "O" in the IN3 column. This forms the logical input ULI1. ULI1 is *internally* transferred to User Logical Output 1 (ULO1). This is the input to the top portion on the S-R Flip Flop. The logic for the lower left "AND" gate is accomplished exactly as above except IN5 (SCADA Disable) is anded with NOT IN3 thus forming ULI2 and ULO2. This is the input to the bottom portion of the Flip Flop.



	FBOI	FBOZ	FBO3	FBU4	FBOD	FBOC
	OR	OR	OR	OR	OR	OR
				:	1	:
ULO1			· · · X- ·	+	×	
ULO2						X
ULO3				· X	1	
ULO4				· X	1	
ULO5						X
ULO6			4		X	
ULO7			X			
ULO8						X

3

In our case, the Output of the entire Flip Flop is FB6. The logical "AND" of FB6 and IN4 (43A) is mapped to ULI3. The logical "AND" of IN3 (LOCAL/SUPV) and IN4(43A) is mapped to ULI4. ULI3 and ULI4 are *internally* transferred to ULO3 and ULO4 respectively. The logical "OR" of ULO3 and ULO4 is mapped to FBO4 which is *internally* transferred to FB4. FB4 is consequently the output of the entire system and is therefore mapped to the 43A logical input. Hence, whenever FB4 is true, reclosing is in service.

Conclusion

The use of the above logic for remote reclosing control is only one example of the many uses of Flip Flops in the 2000R relay. We at ABB Power T&D hope that this note will encourage you to investigate the advanced logic capabilities of the relay. If there are any questions regarding this or any other application you are considering, please contact ABB technical support at 1-800-634-6005.

Submitted by: Jim Hubertus

> ABB Power T&D Company Inc. Power Automation and Protection Division 7036 Snowdrift Road Allentown PA 18106 Telephone 610-395-7333

Revision 0 April 1997